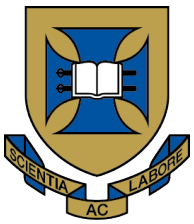

THE UNIVERSITY OF QUEENSLAND

AUSTRALIA

Image Detection with RISC-V Processor on FPGA

Draft Project Proposal

Joshua Wallace

45809978

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The University of Queensland

School of Information Technology and Electrical Engineering

List of Abbreviations

Abbreviations	
FPGA	Field Programmable Gate Array
ASIC	Application Specific Integrated Circuit
CPU	Central Processing Unit
GPU	Graphical Processing Unit
SoC	System on Chip
ISA	Instruction Set Architecture
RISC	Reduced Instruction Set Computer
CISC	Complex Instruction Set Computer
IO	Input Output
RTOS	Real Time Operating System
CNN	Convolutional Neural Network
YOLO	You Only Look Once
VGA	Video Graphics Array

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Chapter 1

Introduction

1.1 Motivation

In recent years, the demand for efficient and versatile image processing systems has surged across various domains, including surveillance, medical imaging, autonomous vehicles, and more. Field Programmable Gate Arrays (FPGAs) have emerged as a prominent solution due to their reconfigurability, parallel processing capabilities, and low power consumption. Hence, image processing is a good candidate for the application of parallel processing due to the algorithm complexity and large volume of data. [3]

One significant aspect of image processing systems is the choice of the underlying processor architecture. Traditional approaches often rely on general-purpose CPUs or GPUs to execute image processing tasks. However, these architectures may not always offer the best balance of performance, power efficiency, and flexibility for image processing applications. In recent years, the RISC-V instruction set architecture (ISA) has gained traction as an open, customizable, and energy-efficient alternative to proprietary processor designs. These soft processors can be implemented on FPGAs, providing a flexible and scalable platform for image processing tasks.

This thesis focuses on the exploration and implementation of image detection algorithms using a RISC-V processor architecture deployed on an FPGA platform. By leveraging the configurability of FPGAs and the energy efficiency of the RISC-V ISA, this research aims to develop a scalable and adaptable solution for real-time image detection tasks. The data processing capacity is large that the processing speed must be strict to meet the demands of real-time time image transmission [4].

Chapter 2

Background

2.1 Background

A review of existing literature relevant to the topic has been conducted to provide a basis for the work. The related works to the research were selected: Field-Programmable Gate Arrays (FPGAs), RISC-V processors, image detection methods, and convolutional neural networks (CNNs). These are broadly discussed below, with a focus on the application of these technologies to image detection and hardware implementations.

2.1.1 Image Detection and Analysis

Image analysis is the process of extracting features from an image, to simplify it into a form that is more easily interpreted [5]. This often includes edge detection, object recognition, and image classification as subset actions. Edge detection forms the basis of many image analysis techniques, as it is used to localize the variations in the image and to identify the physical phenomena which produce them [2]. These are generally classed as gradient-based or Laplacian based, though gradient-based algorithms are dominant for the task [2].

The Robert, Prewitt and Sobel techniques are the most prominent of the gradient-based algorithms, applying kernels to the image to detect edges [6]. [4, 7–10] all provide a hardware implementation of the these filters, utilising the parallel processing capabilities of FPGAs to accelerate the gradient operations. These designs realized improve efficiency in performance, per the throughput, and resource utilisation. Hence, FPGAs are providing a platform for processing real time algorithms on application-specific hardware with substantially higher performance than programmable digital signal processors (DSPs) [1]. This strongly indicates that FPGA-based implementations of image detection algorithms can offer significant improvements in running time for a range of digital signal processing methods.

The general pipeline for image detection and analysis is shown in Figure 2.1. This covers the available techniques which can be abstracted into hardware, to provide a high-speed, real-time image detection system.

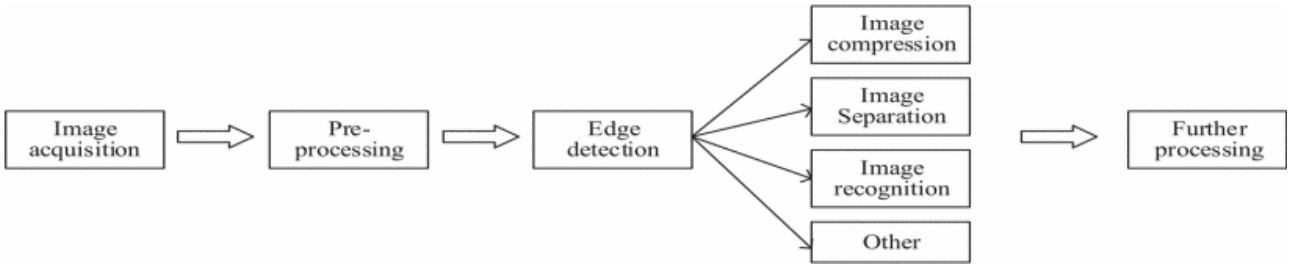

Figure 2.1: Pipeline for image analysis techniques [1]

[10, 11] follow a similar pipeline to Figure 2.1, with the image being captured by a camera module, and then processed by an FPGA though using differing image techniques. The FPGA platform is optimal for any image detection tasks, as it can accelerate the required multiplication and addition operators separately - required for classical, and deep learning, based techniques [12]

2.1.2 Convolutional Neural Networks and Deep Learning

Convolutional neural networks (CNNs) are a type of artificial neural network that is primarily used for image detection. Due to the lack of memory in low-end FPGA models, the CNN is optimal for an image processing task on SoC, as it has a low number of weights and biases relative to other neural networks [13] The convolution operation requires a large number of multiply-accumulate (MAC) operations, and is the primary bottleneck in the performance of CNNs. The operation must window over the entire image, and the number of MAC operations is proportional to the size of the image and the number of filters in the layer. Hence, the CNN is computationally intensive, demanding a significant quantity of operations for high accuracy [14]. However, the proceeding [13] article found that the use of an embedded makes the implementation CNN less challenging on the FPGA platform, as the network can be designed in a systems language such as C. This can then be compiled and translated into machine code, as there exists a toolchain for RISC-V.

Similar works for image-analysis using different neural network architectures have also been implemented using FPGA hardware. [15, 16] demonstratesa hardware implementation of the You Only Look Once (YOLO) algorithm using a Xilinx Virtex-7 FPGA. Like the CNN hardware implementations, the architecture is focused on accelerating the convolution operation - and is a common denominator in the performance neural networks in hardware. This acceleration is not specific to the convolution operator, and can be applied to any intensive operation in the network as the FPGA has little overhead on each operator when compared to traditional platforms [17]. This is corroborated by [18], which found that the implementation of hybrid neural networks on a Xilinix Virtex-7 690T FPGA achieved 4.13 times higher throughput than state of the accelerators in 2019.

2.1.3 RISC-V

Instruction set architectures (ISAs) define the operations a processor can execute, but the majority of ISAs are proprietary. Reduced Instruction Set Computing (RISC) is a form of ISA which offers a simpler, more efficient design than the traditional Complex Instruction Set Computing (CISC) ISAs - such as the prevalent x86 instruction set [19]. Arm and RISC-V are the two most prominent RISC ISAs, with Arm being the most widely used in embedded systems but with RISC-V offering royalty-free licensing and an open-source nature. The lack of licensing fees and the open-source nature of RISC-V has led to its increasing popularity in the embedded systems domain [20]. It is estimated that the number of chips utilising RISC-V technology "will grow 73.6 percent per year to 2027, when there will be some 25 billion AI chips produced, accounting for US $291 billion in revenue" [13].

There exists a number of FPGA implementations to create softcore processors using the RISC-V ISA [21]. The 2023 paper [20] demonstrates a RISC-V implementation of the NEORV32 core, using a Wishbone bus interface. The authors selected the NEORV32 core due to the vendor-agnostic and platform independency, and the project being highly documented. The softcore nature allows for the implementation details to be customised to the specific application, such that the core can be adapted to the specific use case [22]. The NEORV32 processors offers a system-on-chip (SoC) Harvard architecture, with a 32-bit RISC-V processor, and a range of peripherals. It supports UART, SPI, standard GPIO and the Wishbone b4 external bus interface for SoC connectivity [23].

As it is an open-source ISA, RISC-V has the added benefit of being extensible and modular [24], allowing for instructions to be added to the processor. [25] utilises this to create custom instructions within the RISC-V ISA to accelerate the expensive convolution operation for a CNN.

2.1.4 Field-Programmable Gate Arrays

Field Programmable gate arrays (FPGAs) provide flexible compute resources that can be reconfigured to suit a wide range of applications. Similar to graphics processing units (GPUs), FPGAs offer parallel processing capabilities, but with the added benefit of reconfigurability [26]. The ability to develop custom logic designs is not unique to FPGAs, as application-specific integrated circuits (ASICs) also offer this capability, but FPGAs offer a faster development cycle and lower cost for low-volume production. Hence, FPGA technology is optimal for edge applications on images due to the parallelised pipeline structure, which enables high-speed processing of large amounts of image data, and it's high processing speed ensures real-time image data processing [4].

FPGAs have been studied extensively in the field of image detection, as replacements to existing hardware infrastructures. The most common application is to accelerate the convolution operation using the parallel processing capabilities of FPGAs. This is the most computationally intensive operation in CNNs, and is the primary bottleneck in the performance of CNNs REF.

Figure 2.2 shows an implemention of a hardware-accelerated edge-detection algorithm for video images, using the Intel Cyclone IV FPGA platform direct from a camera module. This requires a

camera module, FPGA and uses a VGA monitor to display the output - but does not use a softcore processor.

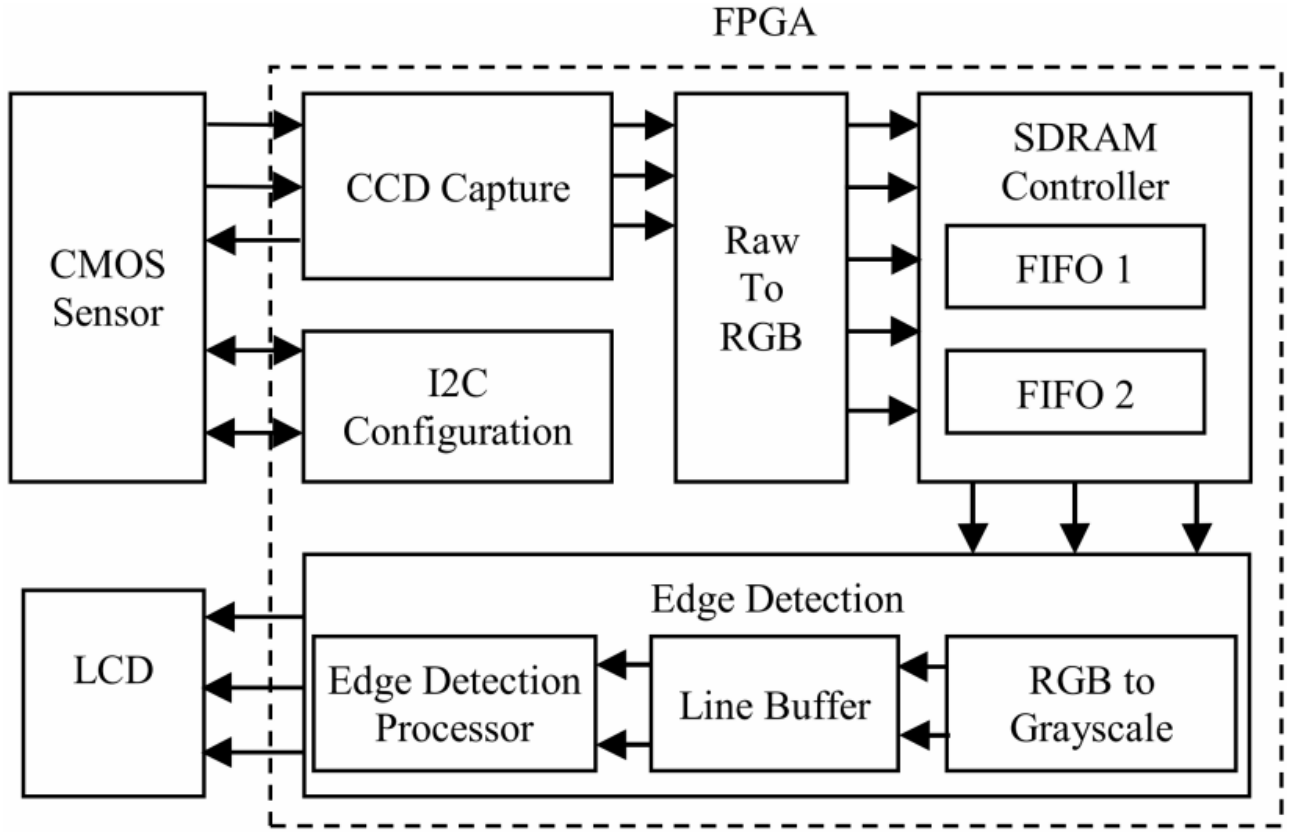

Figure 2.2: Video detection FPGA pipeline [2]

This pipeline has the core advantage over traditional CPU architectures which are serially structured, as it can perform the operations in hardware and in parallel. Hence, an image processing system employing an FPGA as the primary control chip is better suited to the low-latency and high speed demands of real-time image processing [1].

Chapter 3

Topic

3.1 Topic

Image detection, a critical task in computer vision, involves identifying and locating objects within images. Traditional software-based approaches for image detection often face challenges related to processing speed and resource utilization, particularly when dealing with large datasets or real-time applications. In response to these challenges, I propose leveraging Field-Programmable Gate Arrays (FPGAs) to accelerate image detection algorithms in hardware. By offloading computationally intensive tasks to FPGA-based hardware accelerators, we aim to significantly enhance the performance and efficiency of image detection systems.

The integration of FPGA-based hardware acceleration offers several compelling advantages. Firstly, FPGAs provide inherent parallelism and customizable hardware architectures, enabling efficient execution of image processing algorithms. This parallelism can lead to substantial improvements in processing speed, making real-time image detection feasible for applications such as surveillance, autonomous vehicles, and industrial automation. Additionally, FPGA-based solutions offer flexibility and scalability, allowing for the optimization of hardware resources to suit specific image detection requirements. This adaptability is particularly advantageous in scenarios where the detection algorithms need to be customized or updated frequently.

Furthermore, hardware-accelerated image detection using FPGAs can lead to significant reductions in power consumption compared to traditional CPU-based approaches, making it suitable for resource-constrained environments and embedded systems. By harnessing the computational efficiency of FPGA-based acceleration, we can achieve higher throughput and lower latency, thereby improving the responsiveness and effectiveness of image detection systems. Overall, this research aims to demonstrate the practical significance and utility of FPGA-based hardware acceleration in advancing the capabilities of image detection technology, paving the way for more efficient and scalable solutions in various domains.

Hence, this projects aim to:

- Demonstrate the feasibility and benefits of FPGA-based hardware acceleration for image detection algorithms.
- Demonstrate the control of the image detection algorithm using a RISC-V softcore processor.
- Evaluate the performance, efficiency, and scalability of the FPGA-based image detection system.

It will not include the development of a new image detection algorithm or method, but rather the implementation of the algorithm in hardware, and the control of the algorithm using a RISC-V softcore processor.

3.2 Overview

The work can be divided into subcomponents to provide a timeline and structure to the project, as dependencies on previous work are required to progress.

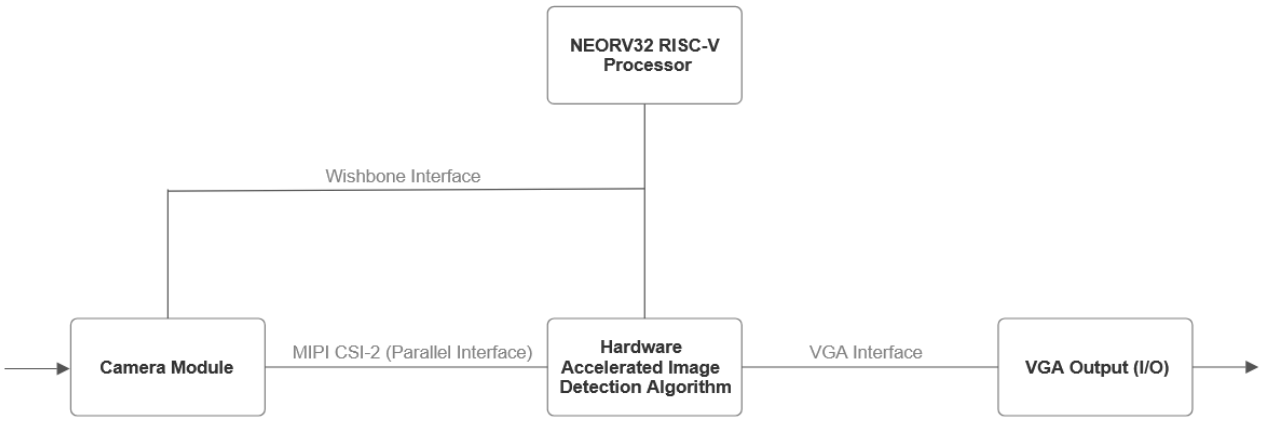

Figure 3.1: Overview of proposed FPGA-based system.

3.2.1 Hardware

The work will require the Xilinx Artix 7 XC7A100T FPGA, and a corresponding board to access I/O. A Digilent Basys 3 board is available initially for development, however, a Digilent Nexys A7-100T board may be required depending on resource limits. Both these boards use the Artix 7 XC7A100T FPGA, and have VGA outputs to allow for images to be displayed. Figure REF below designates a high-level overview of the proposed system.

The camera module will be connected to the FPGA, and the NEORV32 processor will be used to control the image detection algorithm.

3.2.2 Softcore Processor

The NEORV32 RISC-V softcore processor has been selected due familiarity with it, and a highly documented ecosystem surrounding it. This processor will be implemented on the FPGA, and will be used to control the image detection algorithm, and display the processed image on a VGA monitor.

3.2.3 Image Detection Algorithm

The image detection algorithm has not yet been selected, and it is dependent on the resources available, and complexity desired. The current options being considered are a convolutional neural network, such as in REF, or implementing classical imaging techniques via hardware such as that proposed in REF. It is desired to implement a convolutional neural network, as image analysis is moving in the direction of deep learning algorithms [27]

3.3 Performance Indicators

The performance of the system to establish the success of the project are provided in Table 3.1 below.

Table 3.1: Table of performance indicators.

Indicator	Description
Algorithm accuracy	The ability of the system to correctly detect features in an image.
Scalability	A measure of the limits of the system in terms of image size, image complexity and algorithm complexity
Throughput	Measured as the number of images processed per time unit
Latency	The time delay between acquisition of image and output of results relative to the clock-speed of the Xilinx Artix 7 XC7A100T FPGA
Resource Utilization	The amount of FPGA resources used to implement the system specified by number of LUTs and BRAM required for implementation

3.4 Required Resources

The hardware will be designed using both a Digilent Basys 3 development board for initial prototyping, before being migrated to a Digilent Nexys A7-100T development board, to access more I/O and resources. Both boards have a VGA output, which will be used to display the processed image directly from the FPGA board. The specific camera module to be used has not yet been selected, however, a VGA OV7670 camera module which uses an I2C communication protocol is being considered for initial trials. A VGA monitor will also be required to display the output of the processed image.

Benchmarking materials are dependent on the image detection algorithm selected, and cannot be provided at this time. Thus, the following resources are required for the project at this stage:

- Xilinx Artix 7 XC7A100T FPGA
- Digilent Basys 3 FPGA Board
- Digilent Nexys A7 100T FPGA Board
- Camera Module
- VGA OV7670 Camera Module I2C
- VGA Monitor
- USB Power Supply
- VGA to VGA Cable

Chapter 4

Research Plan

4.1 Milestones

To track the development of the project, a set of milestones have been established with consideration of assessable dates. Table 4.1 below outlines the milestones for the work and what is required for each phase. Emboldened text indicates an assessable milestone.

Table 4.1: Timeline of milestones.

Milestone	Description	Date
Project Proposal	Complete the project proposal and literature review.	23/4
Configure hardware	Implement NEORV32 processor on FPGA, connect to external components through wishbone interface.	23/4
Seminar	Present the current project status.	23/4
Image detection algorithm	Select and implement image detection algorithm in hardware.	23/4
VGA driver	Develop driver and interface to display processed image on VGA monitor.	23/4
Benchmark	Benchmark system performance against related works.	23/4
Demo	Demonstrate the complete project.	23/4
Thesis	Document and write project results.	23/4

4.2 Risk Assessment

This project is conducted in the low-risk laboratory covered by general OHS laboratory rules.

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