CSCE 611
Lab 2
ALU Testbench Design
Due Date: 9/30 (by midnight)

Objective

In this lab you will design a self-checking testbench for your MIPS ALU. Create a hexadecimal test vector file containing the inputs and expected outputs for your testbench. For each test vector, you can add a comment that describes its intended behavior.

Your testbench should test each of the cases described in the table below. Make sure the test cases appear in the same order as shown in the table.

Example test vector:
// vector format:
// a_b_shamt(zero-padded to 8 bits)_op_hi_lo_zero(padded to 4 bits)
// test bitwise AND
0F0F0F0F_FFFFFFFF_00_0_00000000_0F0F0F0F_0

Maintain a 32-bit error counter.

ALU Operation	Test Case	Inputs	Expected Outputs
bitwise AND	non-zero output	a=0F0F0F0F b=FFFFFFFF shamt=don't care	lo=0F0F0F0F hi=00000000 zero=0
	all zero output	a=0F0F0F0F b=F0F0F0F0 shamt=don't care	lo=00000000 hi=00000000 zero=1
	all one output	a=FFFFFFFF b=FFFFFFFF shamt=don't care	
bitwise OR	all one output	a=0F0F0F0F b=F0F0F0F0 shamt=don't care	
	non-zero output	a=0F0F0F0F b=00000000 shamt=don't care	
	all zero output		
bitwise XOR	invert bits of a by setting b to all ones, non-zero output		
	all one output		
	all zero output		
bitwise NOR	invert bits of a by setting b to all		

	zeros, non-zero output		
	all one output		
	all zero output		
Shift left logical	shift by non-zero number of bits		
	shift by zero bits		
Shift right logical	shift by non-zero number of bits		
	shift by zero bits		
Shift right arithmetic	shift positive value by non-zero number of bits		
	shift negative value by non-zero number of bits		
Set on less than	$a < b$	a, b positive	lo = 00000001
	$a = b$	a, b positive	lo = 00000000
	$a > b$	a, b positive	
	$a < b$	a, b negative	
	$a > b$	a, b negative	
	$a < b$	a negative, b positive	
	$a > b$	a positive, b negative	
Set on less than unsigned	$a = b$		
	$a < b$	a[31] = 0, b[31] = 0	
	$a < b$	a[31] = 0, b[31] = 1	
	$a > b$	a[31] = 0, b[31] = 0	
	$a > b$	a[31] = 1, b[31] = 0	
add	$0 < a + b \leq 2^{31}-1$ $a > 0$ $b > 0$		zero = 0 lo = sum of a and b
	$a + b = 0$		
	$-2^{31} \leq a + b < 0$		
	$a + b < -2^{31}$		
	$a + b > 2^{31}-1$		
Subtract	$0 < a - b \leq 2^{31}-1$ $a > 0$ $b > 0$		
	$a - b = 0$		
	$-2^{31} \leq a - b < 0$		
	$a - b < -2^{31}$		
	$a - b > 2^{31}-1$		
Multiply	$a * b < 2^{32}$	a, b positive	
	$a * b = 2^{32}$	a, b positive	
	$a * b > 2^{32}$	a, b positive	

		a positive, b negative	
		a, b negative	
Multiply unsigned		a is non-zero, a[31] = 0, b is non-zero, b[31] = 0	
		a[31] = 1, b is non-zero, b[31] = 0	
		a is non-zero, a[31] = 0, b[31] = 1	
		a[31] = 1, b[31] = 1	

Submit your projects through the course Moodle site [http://dropbox.cse.sc.edu]. Upload your Verilog test bench design and your test vector file.

Demo Requirements

Demo your project running on the FPGA to the TA within a week of submission.

For the demo, make the following changes:

- Replace the testbench clock with the onboard 50 MHz clock.
- Add SignalTap probes to all the ALU inputs and outputs.
- Connect your error counter to all eight 7-segment displays (allowing for the display of an error counter up to FFFF $FFFF_{16}$.
- Remove the calls to $display() and any other non-synthesizable code.
- The TA will ask you to trigger on specific tests to show the operation of the ALU on the FPGA.