CSCE 611
MIPS Register File

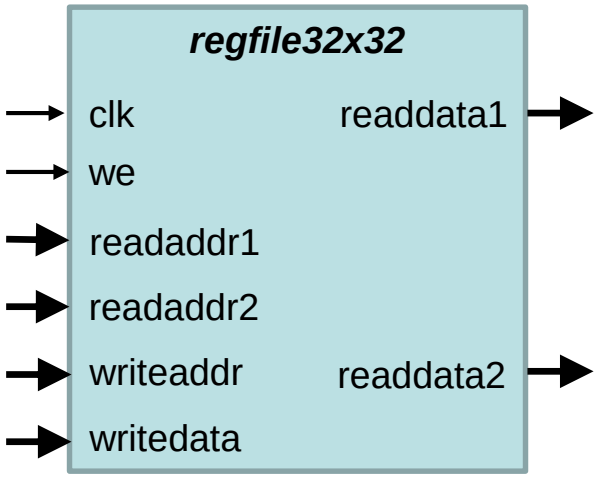
Instructor: Jason D. Bakos

UNIVERSITY OF SOUTH CAROLINA

RegFile32x32

- The MIPS ISA has 32 x 32-bit general-purpose registers
  - Allows for two reads and one write per cycle
  - Register 0 is always 0
  - Register 31 is written in bltzal, bgezal, and jal instructions ("link address")
  - jalr allows you to specify the link register in rd field

- Single-cycle and pipelined MIPS processors take advantage of *bypassed* writes:
  - When the same register is written and read at the same time, the read port should reflect the write data



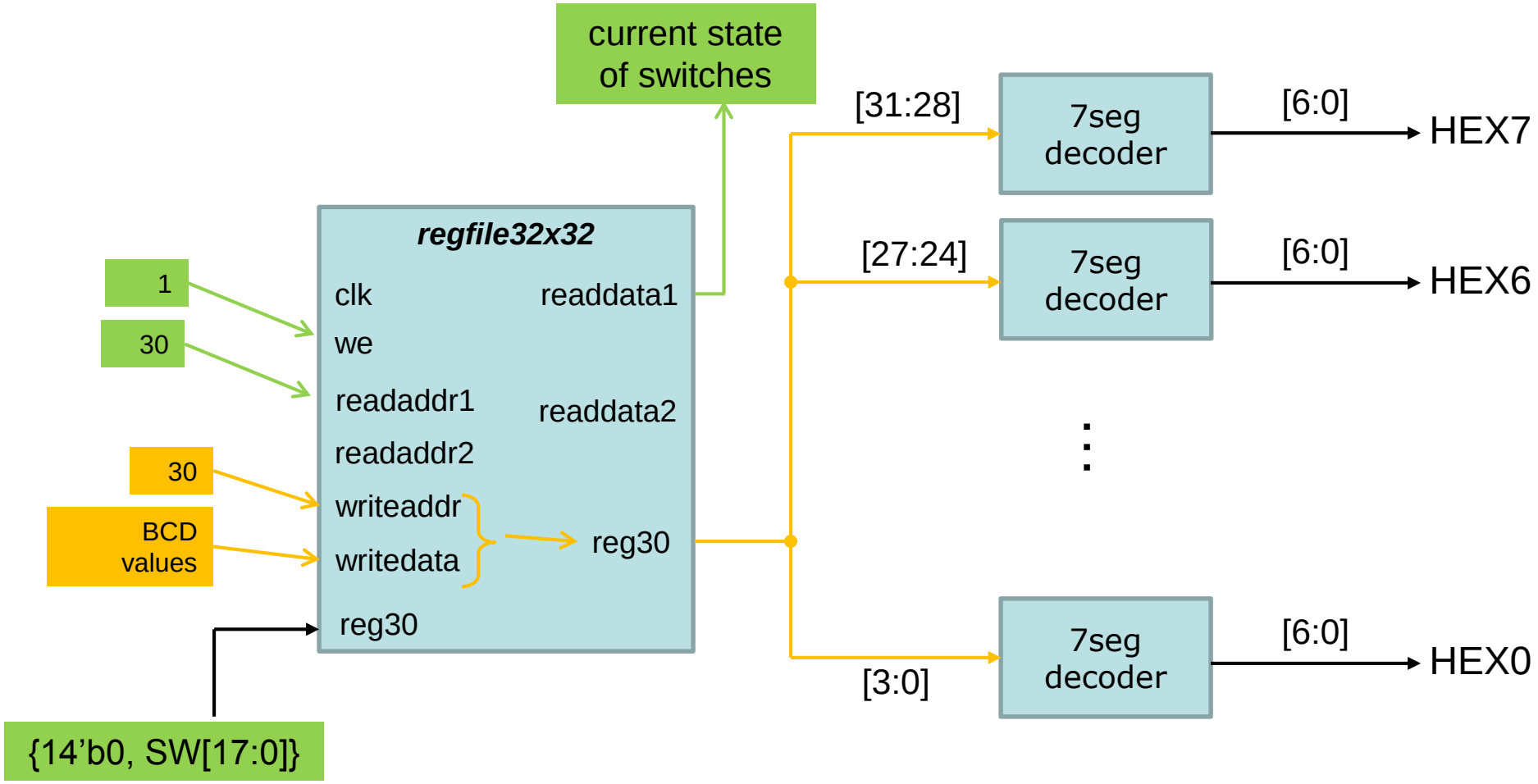
RegFile32x32

- In our design, we'd also like to map register 30 to a peripheral
  - When READING from register 30, the register file will return the value from a special input called "reg30_in"
    - For our CPU: register 30 maps to the DE2 switches (when read)
    - Connect reg30_in to SW[17:0] (zero pad top 14 bits)
  - When WRITING to register 30, the register file will assign the written data to be the value assigned to a special output called "reg30_out"
    - In other words, the "reg30_out" output will always be driven to the most recent value written to register 30
    - For our CPU: register 30 maps to the value displayed on the DE2 7-segment LEDs (when written)
    - Connect reg30_out to HEX7:HEX0 using decoders
    - You must maintain reg30_out as a separate register (not part of RAM)

HEX Digits

- DE2 offers:
  - Eight 7-segment LEDs
    - Signals HEX0[6:0], HEX1[6:0], …, HEX7[6:0]
  - 18 switches
    - Signals SW[17:0]
  - 4 buttons
    - KEY[3:0]

Proposed Design



Lab 2

- Design regfile32x32 with specifications:
  - Write bypass
  - 2 asynchronous read ports, one synchronous (rising edge) write port
  - Register 0 is always 0, register 30 (write) goes to HEXs, register 30 (read) comes from SWITCHES
- Write self-checking testbench:
  - Generates clk
  - Write testvectors to test:
    - Write-then-reads on different cycles for 3 different registers
    - Write-and-read on same cycle for a 4th register
- Test on DE2 board
  - Connect readdata2 to writedata
  - Hardwire writeaddr to 30
  - Hardwire readaddr2 to 30
  - Hardwire write enable to 1

DE2 Test Design