

How Miruvor’s Spiking Neural Network (SNN) Works

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Abstract

Miruvor is a neuromorphic memory system that uses spiking neural networks (SNNs) to provide efficient, continual, and associative memory across diverse data types. Unlike conventional vector-based memory systems that rely on dense computations and similarity searches, Miruvor encodes input data as temporally sparse spike trains and uses a large, sparsely connected recurrent reservoir with axonal delays. This design enables content-addressable recall through synaptic activation and polychronous dynamics, similar to biological neural mechanisms. The system combines an offline phase for Hebbian structure formation and Spike-Timing-Dependent Plasticity (STDP) refinement with an online phase for continual adaptation. Miruvor works across textual, visual, and sensory signals, providing robust memory for applications like brain-computer interfaces, humanoid robotics, and autonomous vehicles. It achieves ultra-low energy consumption and real-time operation on neuromorphic hardware, surpassing traditional memory models in pattern completion, continual learning, and efficiency. This paper describes Miruvor’s architecture, learning algorithms, hardware mapping, and experimental results within the context of contemporary SNN and neuromorphic computing research.

Keywords: Spiking Neural Networks, Associative Memory, Neuromorphic Computing, Latency Coding, STDP, Polychronous Groups, Multimodal Signal Processing

1 Introduction

The evolution of artificial intelligence (AI) systems has shown the critical need for efficient, context-sensitive, and adaptive memory architectures that can support long-term, associative recall across multiple modalities. Traditional AI memory solutions, such as vector databases and knowledge graphs, rely heavily on dense embedding spaces and computationally expensive similarity searches [1]. While these approaches work well to some extent, they face significant challenges when scaling: high latency, energy consumption, and an inability to naturally support pattern completion or continual learning without catastrophic forgetting.

Biological memory offers a fundamentally different approach: event-driven, highly sparse, and inherently adaptive. Spiking neural networks (SNNs), where information is communicated and computed via discrete spikes, capture these principles and promise orders-of-magnitude improvements in efficiency and adaptability when mapped to neuromorphic hardware [2, 3]. However, realizing general-purpose associative memory with SNNs that can handle heterogeneous data in

real time remains an open research challenge.

Miruvor addresses this gap by presenting a unified, neuromorphic memory system based on SNN principles. At its core is a large, recurrent reservoir of leaky integrate-and-fire (LIF) or adaptive LIF neurons, with sparse connectivity and axonal delays. Input data, regardless of modality, is encoded as temporally precise spike trains using latency coding. Memory storage and retrieval emerge from the dynamic interplay of Hebbian plasticity, STDP, and the formation of polychronous neuronal groups. The result is a system that can perform content-addressable recall, continual adaptation, and efficient operation on neuromorphic platforms. This paper details how Miruvor’s SNN works, including its learning dynamics, hardware mapping strategies, and empirical performance, positioning it within the broader landscape of neuromorphic and SNN-based memory architectures.

2 Related Work

2.1 SNN Associative Memory

The idea that recurrent SNNs with axonal delays can support distributed, content-addressable memory dates back to the work of Izhikevich, who introduced the concept of polychronous groups - dynamically formed assemblies of neurons firing in precise temporal patterns that can encode and recall complex spatiotemporal memories [4]. Later studies extended these ideas, showing that Hebbian mechanisms and STDP can reliably form and refine such groups, creating robust attractor dynamics for pattern completion [5].

Hybrid models have also emerged, combining SNNs with probabilistic frameworks such as hidden Markov models (HMMs), where STDP-trained SNNs encode emission probabilities, allowing for Bayesian inference on sequential data. Tavanaei and Maida, for instance, proposed a hybrid HMM-SNN system in which each HMM state is associated with an SNN trained via STDP to model emission distributions, enabling biologically plausible, unsupervised learning and classification of sequential patterns [6]. While these approaches demonstrate the power of SNNs for associative memory, they often focus on either symbolic or sequential data and do not generalize easily to high-dimensional, multimodal signals or real-time edge applications.

2.2 Neuromorphic Hardware and Efficiency

Recent years have seen significant advances in neuromorphic hardware designed specifically for SNN execution. Platforms such as Intel’s Loihi 2, BrainChip’s Akida, and BrainScaleS-2 implement event-driven, parallel computation with on-chip

plasticity and support for axonal delays [1, 7]. These architectures enable ultra-low power consumption and real-time performance, especially when compared to software simulation of SNNs on conventional CPUs or GPUs. For instance, Arnold et al. demonstrated that SNNs implemented on BrainScaleS-2 could outperform traditional digital signal processing (DSP) systems in both power efficiency and bit error rate for optical communication equalization tasks [7].

While mapping large-scale SNNs to resource-constrained neuromorphic chips is challenging - requiring partitioning, clustering, and careful handling of crossbar resource limits [8, 9] - the payoff is substantial. Compiling and optimizing SNNs for such hardware can yield 10-1000× energy savings and orders-of-magnitude reduction in latency, making them ideal for edge computing and embedded AI.

2.3 Memory for AI Systems

Mainstream AI memory systems, such as vector stores (Mem0, Zep) and graph-based retrieval-augmented generation (GraphRAG), are fundamentally built around dense vector spaces and require explicit similarity search or graph traversal for recall [1]. While effective for certain applications, these methods suffer from scalability issues, high latency, and an inability to naturally support pattern completion or lifelong learning. In contrast, SNN-based associative memory architectures - where recall emerges from synaptic activation and attractor dynamics - offer a more brain-like, adaptive, and efficient alternative.

2.4 Multimodal SNNs and Generalization

Efforts to extend SNNs beyond symbolic or sequential domains have yielded promising results in vision, robotics, and signal processing [7, 10]. Event-based vision sensors (e.g., dynamic vision sensors, DVS) generate spike-like outputs natively, and SNNs can process such streams with high temporal fidelity. However, most existing systems lack a unified approach to memory across disparate modalities or fail to address the challenges of continual adaptation and associative recall in embodied agents.

Miruvor advances the state of the art by providing a unified, latency-coded SNN reservoir architecture that generalizes across text, image, audio, and sensor data, and by demonstrating hardware-native efficiency and adaptability.

3 Method

3.1 Spike Encoding: Latency Coding (Time-To-First-Spike)

The first step in Miruvor’s memory pipeline is converting input data into spike-based representations. Whether the data consists of text embeddings, images, audio, or sensor readings, each feature dimension is converted into a spike train using latency coding, also known as time-to-first-spike (TTFS) [4, 5]. In this scheme, the magnitude of a feature is mapped to spike

latency within a fixed temporal window: stronger features fire earlier, while weaker features fire later or not at all.

This encoding strategy preserves the semantic or perceptual structure of the input while producing highly sparse, temporally precise spike trains - typically one spike per feature dimension. Positive and negative values can be handled via separate channels, ensuring bidirectional representation. The result is a deterministic, sparse event stream that is well-suited for downstream synaptic learning and temporal pattern matching.

3.2 Reservoir Architecture: Sparse Recurrent SNN with Axonal Delays

At the heart of Miruvor is a large, sparsely connected recurrent reservoir of adaptive leaky integrate-and-fire (ALIF) neurons. The network typically scales from 10,000 to 500,000 neurons, with random, sparse connectivity (1-5%) and axonal delays ranging from 1 to 16 timesteps [4]. Each neuron integrates incoming spikes according to its membrane dynamics and fires when a threshold is crossed, after which the membrane potential resets.

The incorporation of heterogeneous axonal delays is critical: it enables the formation of polychronous groups - neuronal assemblies that fire in precisely timed chains. These groups encode complex spatiotemporal patterns and provide the substrate for distributed, overlapping memory traces. Theoretical analyses reveal that such SNNs possess exponential memory capacity, as the number of possible polychronous groups grows combinatorially with network size and delay diversity [4].

3.3 Offline Imprinting: Hebbian Structure Formation and STDP Refinement

Miruvor uses a hybrid learning approach, separating memory formation into offline (imprinting) and online (adaptation) phases. In the offline phase, historical data representing the desired memory corpus is repeatedly presented to the reservoir as spike trains. During each presentation, local Hebbian plasticity mechanisms strengthen or grow synaptic connections between co-active neurons, laying down the structural backbone for memory [5, 6].

Once the basic structure is established, synaptic weights are refined via spike-timing-dependent plasticity (STDP). STDP adjusts synaptic efficacy based on the precise temporal relationship of pre- and post-synaptic spikes: if a presynaptic neuron fires shortly before its postsynaptic target, the synapse is potentiated; if the order is reversed, the synapse is depressed [5, 6]. Over successive presentations, this process sharpens the memory attractors, ensuring that partial or noisy inputs converge reliably to stored patterns and supporting robust pattern completion and recall.

3.4 Online Adaptation and Lifelong Learning

To support continual learning and adaptation, Miruvor incorporates online plasticity mechanisms. During deployment, new inputs are injected as spike trains into the reservoir. Brief, local STDP updates allow the network to refine or extend its memory traces in response to novel stimuli or changing environments. To prevent catastrophic forgetting and maintain core memories, consolidation schemes inspired by elastic weight consolidation (EWC) or synaptic tagging are employed, selectively protecting the weights most critical to existing attractor basins [5].

The combination of offline imprinting and online adaptation mirrors biological memory processes, enabling Miruvor to maintain a stable knowledge base while flexibly incorporating new experiences.

3.5 Associative Retrieval: Content-Addressable Recall via Synaptic Activation

Perhaps the most distinctive aspect of Miruvor is its approach to memory retrieval. Rather than relying on explicit similarity computation or index-based search, Miruvor exploits the physical structure of its synaptic pathways. A query is encoded as a spike train and injected into the reservoir, where the network evolves dynamically. Only those synapses that were strengthened during the encoding of related memories will activate strongly, triggering the corresponding polychronous group [4, 5].

Recurrent dynamics and axonal delays ensure that even partial or noisy queries can propagate through the appropriate chains, completing the pattern via attractor dynamics. The most active neuronal assembly, identified through integrated spike counts or a lightweight winner-take-all (WTA) layer, corresponds directly to the recalled memory. This process is inherently content-addressable: recall emerges naturally from the network’s synaptic topology, without the need for global search or dense computation.

3.6 Neuromorphic Hardware Mapping

While SNNs can, in principle, be simulated on conventional CPUs or GPUs, such software emulation is inefficient, requiring every neuron and timestep to be processed, even when most neurons are silent [1, 2, 8]. Neuromorphic chips, by contrast, are designed for asynchronous, event-driven operation: circuits activate only in response to spikes, with no global clock. Hardware primitives naturally support sparse connectivity, local plasticity, and axonal delays, matching Miruvor’s architectural requirements [1, 7].

Platforms such as Loihi 2, Akida, and BrainScaleS-2 implement on-chip STDP, programmable delays, and real-time parallel synaptic integration, enabling Miruvor to achieve microsecond-level recall and milliwatt-level power consumption [1, 7]. Mapping large SNNs to such hardware requires partitioning the network into clusters or tiles, optimizing crossbar utilization, and minimizing inter-cluster communication

[8, 9]. Recent techniques, such as greedy clustering, spatial decomposition, and swarm-based placement, address these constraints while preserving model fidelity [8, 9].

3.7 Applications in Humanoids, Drones, and Multimodal AI

The versatility of Miruvor’s SNN core supports a range of demanding AI applications:

Humanoid Robots: By fusing vision, proprioception, and audio streams into multimodal spike trains, the reservoir forms long-term associations, such as mapping verbal commands (“grasp red cup”) to motor sequences. Online STDP enables real-time adaptation to new objects or user preferences, while neuromorphic efficiency supports all-day operation on battery power [10].

Drones and Autonomous Vehicles: Event-camera outputs (from dynamic vision sensors) are directly compatible with spike-based processing. The reservoir stores navigation patterns, obstacle associations, and mission context as polychronous groups. Split-second content-addressable recall enables fast, robust navigation, while continual learning allows adaptation to new environments without cloud retraining [7, 10].

Signal Processing and Brain-Computer Interfaces: Miruvor’s architecture generalizes to signal domains, supporting robust, low-power processing of high-bandwidth data streams [7].

4 Key Algorithms for Retrieval and Pattern Completion

4.1 Content-Addressable Recall via Polychronous Activation

Central to Miruvor’s memory function is the content-addressable recall mechanism. When a query is presented as a spike train, it activates those polychronous groups whose synaptic chains closely match the temporal structure of the input [4, 5]. Axonal delays and recurrent connectivity ensure that even partial activation can recruit the entire assembly, completing the pattern through dynamic propagation.

This process parallels the brain’s associative recall, allowing the system to retrieve memories based on cues, partial patterns, or noisy inputs - a property that traditional vector-based systems cannot achieve.

4.2 Assembly Scoring and Winner-Take-All (WTA) Selection

To identify the most relevant memory in response to a query, Miruvor employs simple, biologically plausible scoring mechanisms. The integrated spike count of each assembly (or the membrane potential of readout neurons) is monitored over a retrieval window. A lightweight WTA circuit selects the assembly with maximal activation, corresponding to the recalled

memory ID. This process avoids global search, relying instead on local competition and temporal integration [4, 5].

4.3 Pattern Completion via Attractor Dynamics

STDP-trained weights in the reservoir create basins of attraction - regions of synaptic state space where partial or degraded cues converge to full stored patterns through iterative network dynamics [5]. As shown by Yoon and Kim, such attractor dynamics can be harnessed for robust pattern completion and memory retrieval, outperforming vector or graph-based baselines in recall accuracy and noise tolerance [5].

5 Experimental Results

5.1 Textual Recall and Pattern Completion

Miruvor was evaluated on synthetic textual datasets and agent interaction logs, using both vector search and graph-based retrieval-augmented generation (RAG) as baselines. Inputs were encoded as spike trains via TTFS latency coding and injected into the reservoir. Recall accuracy, pattern completion rate, and energy consumption were measured.

Results showed that Miruvor achieved superior pattern completion compared to baselines, reliably recalling full memory traces from partial or noisy queries. On neuromorphic hardware, energy consumption was reduced by $10\text{-}1000\times$ relative to GPU-based vector search, and recall latency was reduced to microseconds [1, 7].

5.2 Signal Data: Image and Sensor Processing

Miruvor was also tested on image datasets such as MNIST and CIFAR, as well as event-based sensor data. Spike-encoded images were used to imprint memory traces in the reservoir. During recall, the system demonstrated robust classification and associative retrieval, even under significant input corruption.

Compared to SNNs mapped via conventional approaches, Miruvor’s event-driven design and optimized hardware mapping yielded higher throughput, lower energy consumption, and improved model quality [7–9]. The system maintained high accuracy while supporting real-time, continual learning.

5.3 Hardware Mapping and Scalability

Mapping large SNNs to resource-constrained neuromorphic chips was addressed using greedy clustering, partitioning, and placement algorithms [8, 9]. These methods maximized crossbar utilization, minimized inter-cluster communication, and preserved synaptic structure. Experimental results on platforms such as BrainScaleS-2 and DYNAP-SE demonstrated high scalability and efficient hardware utilization, with minimal loss in model fidelity.

6 Discussion

6.1 Advantages over Traditional Memory Architectures

Miruvor’s SNN-based memory system offers several key advantages:

Content-Addressable Recall: Unlike vector stores or graph RAG, recall is achieved via synaptic activation, not similarity search. This supports true associative memory and pattern completion [4, 5].

Extreme Sparsity and Efficiency: The event-driven nature of SNNs ensures that computation and energy are expended only when spikes occur. On neuromorphic hardware, this translates to orders-of-magnitude improvements in energy efficiency and latency [1, 7].

Biological Plausibility and Adaptability: Hebbian learning, STDP, and polychronous groups mirror biological mechanisms of memory formation and recall, supporting continual learning and resilience to forgetting [4–6].

Multimodal Generalization: Latency coding and reservoir dynamics enable seamless handling of diverse input modalities, from text to vision to sensor data [10].

6.2 Challenges and Limitations

Hardware Constraints: Mapping very large SNNs to neuromorphic chips requires sophisticated partitioning and clustering to address crossbar resource limitations [8, 9].

Training Complexity: While local, unsupervised learning rules are efficient, tuning the reservoir for optimal attractor dynamics and memory capacity can be challenging.

Interfacing with Conventional Systems: Integrating spike-based memory architectures with mainstream AI pipelines (e.g., transformer models, non-spiking controllers) requires careful co-design.

7 Conclusion

Miruvor demonstrates that brain-inspired, SNN-based memory architectures can deliver efficient, robust, and adaptive associative memory for a broad range of AI applications. By leveraging sparse, event-driven computation, local plasticity, and polychronous group dynamics, Miruvor achieves content-addressable recall, continual adaptation, and ultra-low power operation on neuromorphic hardware.

Experimental results validate its superiority over conventional vector and graph-based memory systems in pattern completion, recall accuracy, and energy efficiency. Hardware mapping strategies ensure scalability and efficient deployment on state-of-the-art neuromorphic platforms.

With applications spanning textual AI, embodied robotics, signal processing, and edge intelligence, Miruvor provides a versatile, brain-inspired foundation for next-generation AI memory systems.

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