Odin_II Status & Roadmap

FPGA2020

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Goal

- Improve test coverage
- Bring up to Verilog 2005
- Add some basic System Verilog support (macros, file, io)
- Improve Hard-Block/Soft-logic heterogenous mapping
- Superficial Statistic to Improve Placement

Synthesis goals and todo's

- <Q2> *70%* coverage with the micro-benchmarks, hoping for *~80%* with micro alone
- <Q1> improve odin test framework to test for expected failures.
- <Q1> Add QoR to Odin (see WIP #1167)
- <Q3> Major keyword left: inout, assign, deassign.
- <Q3> Todo: finish task and scoping.
- <Q2> Syntax support is tricky to document (Generate support status via Travis weekly?)
- <Q2> Adding some (VERY) basic system verilog support OOG withing Odin.

```
`__FILE__, `__LINE__, etc
```

Netlist improvements

- <Q1> Odin map all hard-logic to .subckt logic, the goal is to build heterogenous circuitry when advantageous (size vs speed tradeoffs).
- <Q1> Improving and adding ability to tweak soft-logic implementation of composite and hard-block logic.
- <experimental Q1> Use HB adder (when and if available) to build soft multipliers.
- <experimental Q3> Improve Custom Hard-Block interface.

Contact Information

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