Thermal equivalent circuit of advanced SiGe HBT

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# I. INTRODUCTION

Hetero-junction Bipolar Transistor (HBT) implements two semiconductor material types between the two junctions, Emitter-Base and Base-Collector, allowing higher frequency and higher output power than the classic bipolar transistor. The HBT is mainly used in modern RF circuits.

With the increase of the power performance at high frequency required for 5G and the development of the 6G, the HBT technologies upgrade at each generation. ST Microelectronics develops an HBT technology called B55, with higher perfomance in frequency than precedent 55nm device, as can be seen in Fig.1. However, to face the 6G technological developments, today technology has been improved and called B55x [1].

### II. THERMAL CHARACTERIZATION

The main challenge for an HBT is to correctly manage the heat dissipation within the device to avoid thermal instability and potential destruction of the device. To understand the thermal behavior of the device, a thermal characterization need to be achieved. Firstly, an extraction of the thermal resistance is performed [2]. By comparing the thermal resistance of the two devices at the same emitter area, the B55x shows a reduction of around 40% compared to the B55.

The next step is the extraction of the thermal impedance  $(Z_{TH})$  representing the diffusion of the temperature through the device [3]. To extract  $Z_{TH}$ , the S-Parameters need to be measured. These measurements were achieved between 30kHz and 3GHz, caracteristic of the thermal response.

$$Z_{TH}(\omega) = R_{TH} \frac{Y_{22}(\omega) - Y_{22}^{AC}}{Y_{22}^{DC} - Y_{22}^{AC}} \frac{I_C + V_{BE} Y_{12}^{DC} + V_{CE} Y_{22}^{DC}}{I_C + V_{BE} Y_{12}(\omega) + V_{CE} Y_{22}(\omega)}$$
(1)

The equation (2) is used with  $Y_{ij}^{DC}$ , the value for  $\omega$  close to 0 and  $Y_{ij}^{AC}$ , the Y-parameters associated to isothermal conditions.

The next step is to simulate the thermal equivalent circuit and extrapolate for different dimensions. The simulation is achieved, considering only a thermal network with a single RC cell. Afterwards, the modified model implementing the 3-cell thermal network is implemented and the parameters extracted according to measurements.

# III. PULSED MEASUREMENTS AND STRESS

Pulsed measurements allow to observe transient effects which are not observable on I-V measurements. The main objective is to observe the impact of the  $C_{TH}$ .

The pulse is sent to the base and its response is observed on the collector current [4]. The aim of these measurements is to compared the different model versions. Two models are compared and the modified model featuring 3-cell network represent better the measurement in particular the rise of the pulse, as illustrated by Fig.2.

# IV. CONCLUSION

To conclude, the thermal characterization proves that the B55x performs better in terms of self-heating management than the B55. The extraction of thermal resistance shows a decrease compared to B55 showing a better heat dissipation. The thermal impedance shows better dissipative behavior for the B55x. The modified model including 3-cell thermal network does not change in I-V characteristics but performs better in transient simulations like S-Parameters. The next steps will be to simulate the transistor as a function of its various dimensions, and then to do pulsed stresses to check that the degradation and compared it with a DC stress.

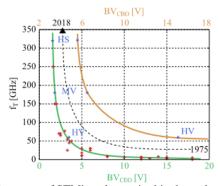


Fig. 1: Performance of STMicroelectronics bipolar technologies along

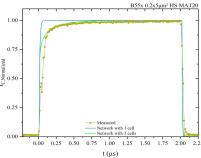


Fig. 2:  $I_C$  response in function of time comparing measurement and simulation for pulse width of  $2\mu s$ 

#### REFERENCES

- [1] E. Brezza, "Development and evaluation of a new heterojunction bipolar transistor architecture for high-performance and low-cost 55 nm BiC-MOS technology", These de doctorat, Université de Lille (2022-....),
- [2] M. Couret, "Failure mechanisms implementation into SiGe HBT compact model operating close to safe operating area edges", Université de Bordeaux, 2020.
- A. K. Sahoo et al., "Thermal Impedance Modeling of Si–Ge HBTs From Low-Frequency Small-Signal Measurements", IEEE Electron Device Lett., vol. 32, n 2, p. 119-121, févr. 2011.

  M. Couret et al., "Physical, small-signal and pulsed thermal impedance characterization of multi-finger SiGe HBTs close to the SOA edges",
- in 2019 IEEE 32nd International Conference on Microelectronic Test Structures (ICMTS), mars 2019, p. 154-159.