Compact Modelling of Reconfigurable Field Effect Transistors Towards Smart Sensing Applications

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***Abstract*—In this paper, we present a physics-based compact model for double-gate Reconfigurable Field-Effect Transistors (RFET). By solving the current continuity equation and corresponding charge calculations, we derive the expression of the surface potential, effective Schottky barrier and the total drain current.**

***Index Terms*—Reconfigurable field effect transistor, compact modelling, Schottky barrier, drift-diffusion and drain current.**

I. Introduction

Reconfigurable Field Effect Transistors (RFETs) are a potential key-enabling technology that can be directly co-integrated into the front-end-of-line (FEOL) of a standard CMOS process offering a number of interesting applications including analog smart sensor design. Specifically, we have chosen a 22nm FDSOI Technology for the co-integration of our RFETs.

II. Device Structure

Figure 1 schematically illustrates the structure of the double-gate RFET under test [2]. The device under test in this study was fabricated using modified I/O n-FETs from the 22 nm FDSOI technology reported in [3] [1].

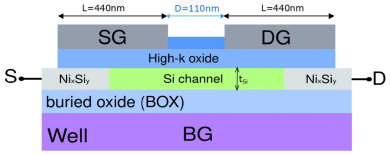

Fig. 1. Schematic of a Reconfigurable FET (RFET).

III. Device Modelling

In this section, we introduce the organisation of our compact model. Compared to a previous compact modelling approach, our model derives the net drain current based on surface potential and charge calculations and the consideration of an effective Schottky barrier height. The total device current is obtained by solving the current continuity equations, which solves for the resultant current between the current through the Schottky-barrier contacts and the drift-diffusion current of both carriers in the channel.

IV. Results and Discussion

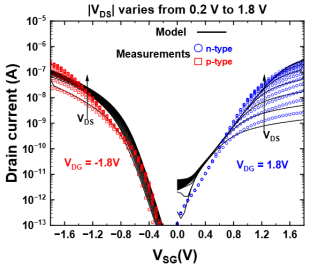

Fig. 2. Transfer characteristics (I_D–V_G) at different V_{DS} for $n-type$ and $p-type$.

Figure 3 illustrates the device transfer characteristics, comparing experimental data [2] with the compact model simulations on a semi-logarithmic scale. The figure presents the n-mode, where the drain-gate voltage (DG) acts as the polarity gate, is set to $1.8V$, while the drain voltage V_{DS} varies from 0.2V to 1.8V. The same figure also depicts the p-mode, with $V_{\mathrm{DG}} = -1.8V$ and V_{DS} ranging between $-0.2V$ and $-1.8V$. The model exhibits partial agreement with experimental data but does not achieve a perfect fit.

V. Conclusion

The model shows fair agreement with experimental data for different bias configurations. Further model improvement will be followed including additional effects, such as trapping.

References

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