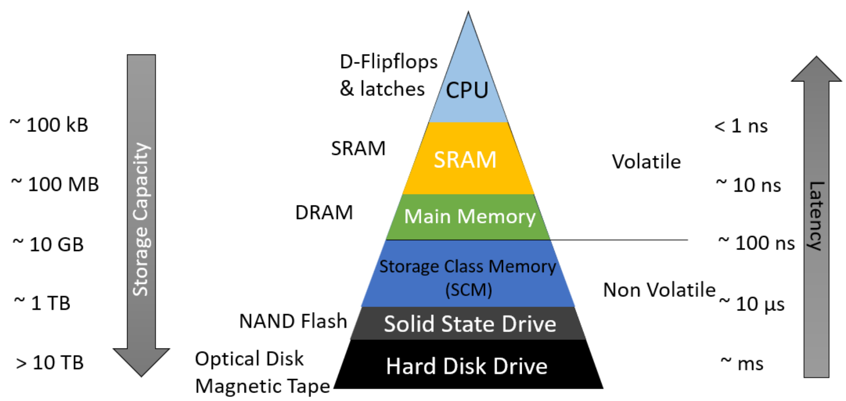
VERILOG-A COMPACT MODEL OF FERROELECTRIC MEMORY DEVICES FOR BRAIN INSPIRED COMPUTE-IN-PLACE APPLICATIONS

Poovendran Muthusamy, Chhandak Mukherjee, Marina Deng, Cristell Maneux, Francois Marc.
IMS Laboratory, University of Bordeaux, CNRS UMR 5218, 33405 Talence, France

In the rapidly evolving field of nanoelectronics, HfO_2-based ferroelectric components, with distinct characteristics such as nonlinearity and hysteresis, hold the potential to be used in advanced memory devices. By integrating ferroelectric capacitors on top of MOSFETs to form Ferroelectric Memory FETs (FeMFET), we can leverage their unique properties to create memory architectures with enhanced performance. Additionally, this integration significantly enhances retention capabilities, paving the way for more efficient and reliable memory systems. This integration holds great promise for advancements in Compute-In-Place applications, offering a pathway to more advanced and high-performing computing systems.



Storage Class Memory (SCM)

Candidates	CMOS Integration
Phase Change Memory (PCM)	Partial
Magnetic Random Access Memory (M-RAM)	Partial
Resistive Random Access Memory (ReRAM)	Partial
HfO_2 based Ferroelectric Memory Devices	**Native CMOS Integration**

The current research focuses on developing a compact, current-based model for ferroelectric memory devices, accurately characterizing their complex behaviour. The proposed model will be validated and optimized through extensive simulations against experimental data, showcasing its potential for performance enhancement and energy efficiency of next-generation computing systems. By incorporating this compact model written in Verilog-A into tools like CADENCE, designers can optimize memory architectures for improved computational efficiency.

In its current state, our current-based model captures the essential dynamics of ferroelectric capacitance, providing detailed insights into its impact on overall device performance. This study also explores the scalability of ferroelectric memory devices, highlighting their potential for integration into large-scale computing systems. This research not only demonstrates the feasibility of integrating ferroelectric components into advanced memory architectures but also underscores the impact of such integration on enhancing computational efficiency and reliability of ferroelectric devices.

Acknowledgement:
This work has received state aid managed by the Agence Nationale de la Recherche (ANR) under France 2030, referring to ANR-23-PEEL-0003.