



Poovendran Muthusamy

pooovendran.km@gmail.com

PROFILE

Curiosity driven engineer with strong aptitude for problem solving and collaborating with multidisciplinary teams to achieve project objectives. Proficient in utilizing various software tools and simulation equipment to analyse advanced devices. Dedicated to staying aware of industry trends and advancements to deliver innovative solutions.

RESEARCH INTERESTS

- Ferroelectric and other emerging Memory devices
- Compact modelling (Verilog-A)
- Compute-in-place / in-memory architectures
- TCAD / SPICE Simulation

EDUCATION

- **Ph.D. (Electronics Engineering) – Student**

Thesis Title- Electrical And Reliability Characterization And Modelling Of Ferroelectric Memory Devices
(Oct 2024 – present) - IMS Laboratory University of Bordeaux, France.

Presented a poster in CNANO 2025

Presented a poster in GDR SOC2 2025

- **Master of Technology (Micro-Electronics and VLSI Systems)**

2024 - IIITDM Kancheepuram, India.

Presented a poster in IWPSD workshop by IIT Madras & SSD

Project - Hybrid FET for Memory and Neuromorphic Application – (Synopsys Sentaurus TCAD)

- **Bachelor of Engineering (Electronics and Communication Engineering)**

2013 - ANNA UNIVERSITY, India.

Participated in TECHKRITI, autonomous robotics workshop by IIT Kanpur

Project - Automated Military Robot using LabVIEW

RELEVANT TECHNICAL SKILLS

Modelling & Simulation

: Verilog-A (ICCAP & ADS)

VLSI Design

: Cadence Virtuoso

(Schematic, layout, DRC & LVS check, RC extraction and post layout simulation)

TCAD Simulation

: Synopsys Sentaurus TCAD workbench

Other Spice Tools

: LT-Spice, NG-Spice, H-Spice & MAGIC layout to NG-Spice simulation

PREVIOUS CAREER

Diraa HR & Financial Services - HR Trainee → Talent Acquisition Specialist

Mahindra & Mahindra Financial Services – NPA Specialist → Customer Relationship Manager