

# Benefits of On-wafer Calibration for RF Characterization of Indium Phosphide Double Heterojunction Bipolar Transistor Devices

Moussa Cissé<sup>1</sup>, Nil Davy<sup>2</sup>, Virginie Nodjiadjim<sup>2</sup>, Bertrand Ardouin<sup>2</sup>, Colin Mismer<sup>2</sup>, Magali De Matos<sup>1</sup>, Cristell Maneux<sup>1</sup>, Valentin Thary<sup>1</sup>, François Marc<sup>1</sup>, Chhandak Mukherjee<sup>1</sup>, Marina Deng<sup>1</sup>

<sup>1</sup> IMS Laboratory, University of Bordeaux, CNRS UMR 5218, Bordeaux INP, Talence, France.

<sup>2</sup> III-V Lab, joint lab between Nokia Bell Labs, Thales and CEA Leti, Palaiseau, France.

**Abstract**—In this study, calibration methods are performed on passive structures up to 220 GHz using off-wafer standards and on-wafer standards. The open and short transistor interconnect measurements are analyzed through a comparison with the electromagnetic (EM) predictive simulation. The results clearly demonstrate the benefits of utilizing on-wafer calibration methods compared to off-wafer ones to improve measurement accuracy by significantly reducing the parasitic effects due to the transistor's interconnects.

**Keywords**—RF on-wafer characterization, calibration, open-short de-embedding, EM simulation, indium phosphide (InP).

## I. INTRODUCTION

Accurate on-wafer RF characterization is essential to fully exploit Indium Phosphide Bipolar Transistors. As highlighted in [1], high-frequency measurements face challenges due to parasitic effects from interconnects and test structures, which hinder precise extraction of key metrics such as cut-off frequency ( $f_T$ ) and ( $f_{MAX}$ ). Conventional approaches consisting of off-wafer SOLT calibration followed by Open-Short de-embedding [2] have shown good accuracy up to 110 GHz using optimized pads [3], but extending measurements toward 220 GHz remains limited. As predicted by interconnect modelling in [1], reducing parasitics in de-embedding structures is crucial for improving accuracy beyond 110 GHz. This work therefore relies on electromagnetic (EM) simulations of test structures identical to those in [3], using detailed material stacks, substrate, dielectrics, and metal layers. The resulting predictive EM data serve as the physical reference for validating high-frequency on-wafer measurements.

## II. METHODOLOGY

Several samples with passive devices were fabricated at III-V Lab using the InP DHBT baseline. Various de-embedding structures (OPEN circuits, SHORT circuits) and transmission lines were included to benchmark calibration methods and assess parasitic-extraction accuracy through on-wafer measurements. Each passive layout was simulated in the ADS EM simulator Momentum. EM simulation results for structures such as OPEN and SHORT were then validated against measurements from 1 to 110 GHz and 140 to 220 GHz using two reference planes, as shown in Fig.1.

## III. RESULTS AND DISCUSSION

The passive structures OPEN and SHORT transistors are measured using both off-wafer SOLT and on-wafer TRL calibration methods. As a result, an excellent agreement between calibrated measurements and EM simulation of the structures

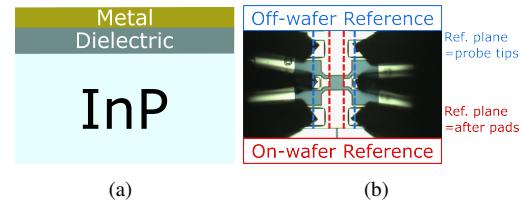


Fig. 1. Material stack used for EM simulation of the structures: a) stack cross section view, b) both ref. plane of the Pad-Open structure

was achieved until 220 GHz, as it can be observed in Fig.2 through OPEN and SHORT.

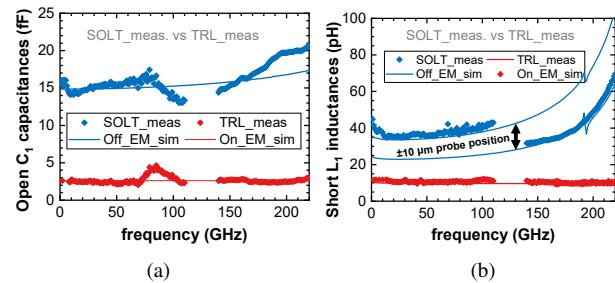


Fig. 2. Comparison between off-wafer SOLT and on-wafer TRL calibrated measurements up to 220 GHz: a) Open C1 structure, b) Short L1 structure

On-wafer TRL calibration significantly outperformed off-wafer SOLT by moving the calibration reference plane closer to the actual device terminals. This technique reduced parasitic capacitance by 80% and inductive effects by 72%, which can offer more reliable extraction of intrinsic device metrics.

## CONCLUSION

This research successfully demonstrated that on-wafer TRL calibration can drastically improve the accuracy of RF characterization in Indium Phosphide Double Heterojunction Bipolar Transistor Devices beyond 110 GHz. This finding constitutes an important part of the PhD progression, which fixes the foundation of the necessary next steps.

## REFERENCES

- [1] N. Davy et al., in *2023 EuMiC*, Sep. 2023, pp. 101–104. doi: [10.23919/EuMIC58042.2023.10288849](https://doi.org/10.23919/EuMIC58042.2023.10288849).
- [2] M.C.A.M. Koolen et al., in *1991 BCTM*, Sep. 1991, pp. 188–191. doi: [10.1109/BIPOL.1991.160985](https://doi.org/10.1109/BIPOL.1991.160985).
- [3] N. Davy et al., in *2022 ESSDERC*, Sep. 2022, pp. 320–323. doi: [10.1109/ESSDERC55479.2022.9947170](https://doi.org/10.1109/ESSDERC55479.2022.9947170).