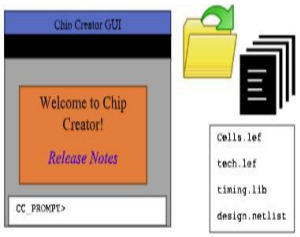
Create Chip Designs Using the Chip Creator™ Tool

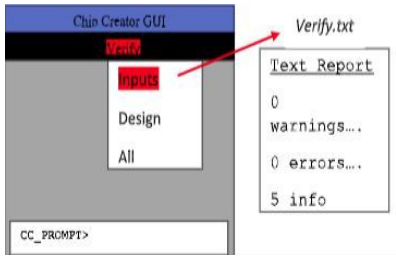
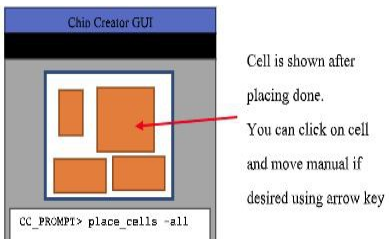
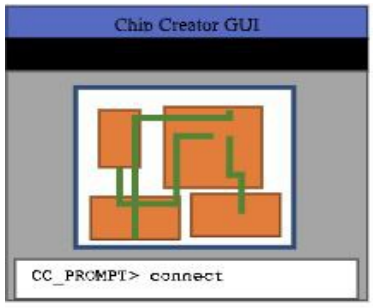
The Chip Creator™ tool is a software application that processes stored technical design information and manual input to produce chip images utilizing multiple wire connections. A simplistic GUI interface, flexible management control capabilities, collaborative opportunities, batch scalability options, and updated performance enhancements provide a seamless experience. Previews during the process, optional third-party verification tools, and the ability to re-run the application ensure designers create reliable chip design templates.

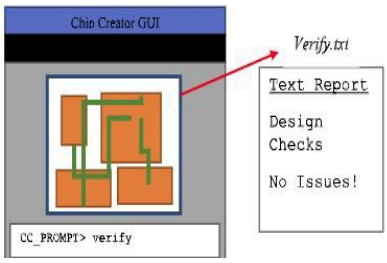
Prerequisites:

- a valid license to use the application
- access to a command prompt to launch the application

Procedures:

Step 1		**Start the Chip Creator™ tool:** From a command prompt, execute the following commands to start the tool: *% setenv TOOL_HOME <path_to_Chip_Creator>* *% $TOOL_HOME/bin/chip_creator_app* *CC_PROMPT> start_gui*
Step 2		**Import the design files:** • From the GUI menu, select **File > Open Design** or • Enter *read_file* at the CC_PROMPT (GUI prompt). design files: tech.lef Note: *tech.lef* must be the first file imported cells.lef timing.lib design.netlist A text report (*verify.txt*) details warning errors and information regarding the import process. The tool supports using older project files.

Step 3		**Verify the imports:** Select **Check > Inputs** to verify all files processed correctly allowing the tool to proceed to the next step. INFO may message during this step to confirm it read each file correctly.
Step 4		**Create the chip outline:** • Select **Run > Create Auto Outline** to create an automatic chip outline or • Select **Edit > Draw Outline** to draw a manual outline or • Enter *create_outline* with applicable parameters to create the outline using the GUI prompt.
Step 5		**Place the cells into the chip design:** • Select **Run -> Place All Cells** or • Enter *place_cells -all* at the GUI prompt. Cells can be manually adjusted using the arrow keys.
Step 6		**Connect the wires:** • Select **Run > Connect Wires** or • Enter *connect* at the GUI prompt. Wires connect with different layers based on the *tech.lef* file; add custom layers by entering ***set_layers*** at the GUI prompt. Reconnect the wires if they do not properly connect; the *place_cells -all* command contains a random algorithm that sometimes results in bad wiring connections.

Step 7		**Verify the design integrity:** • Select **Verify > All Design** or • Enter *verify* at the GUI prompt. Once the verification completes, the process generates a text report (*Verify.txt*) noting any issues. Using third-party tools for further validation enhances the design. The GUI is capable of multiple re-runs if there are issues.

Results:

The process produces an accurate chip image based on technical design information and manual input. Manufacturers use the resulting chip image to create the chips in integrated circuit packages for cellular phones or computers.