Jianing Yang

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EDUCATION:

Georgia Institute of Technology, Atlanta, GA **August 2015 – Present**

- Candidate for Bachelor of Science in Computer Science Expected Graduation: Fall 2018
- Concentration: Artificial Intelligence, System Architecture
- GPA: 4.0/4.0, Faculty Honors

WORK EXPERIENCE:

Georgia Institute of Technology, Atlanta, GA **August 2017 – Present**

Research Assistant, SunLab.org

- Submitted as a co-author a health informatics paper to AMIA
- Implemented 3 machine learning projects in the lab using Jupyter/Google Colab notebook

Amazon Web Services, Seattle, WA **May 2017 (2018) – July 2017 (2018)**

SDE Intern, AWS Directory Service

- Designed and implemented a better back-up mechanism to enhance system reliability (2017 project)
- Extended existing system to increase service availability for customers (2018 project)

Nead Werx, Inc., Atlanta, GA **August 2016 – December 2016**

Middleware Co-op

- Familiarized with MerchLogix, an enterprise resource planning software used by 2000+ stores in 3 countries
- Enhanced system configurability by eliminating customer-specific constants and hard-coded business logic
- Improved middleware robustness by converting legacy Ajax calls to RESTful API calls

PROJECTS:

Part-of-Speech Sequence Labeling (NLP class project) **February 2018**

- Built a Viterbi tagger with Hidden Markov Model as a baseline
- Implemented a Bi-LSTM with conditional random field in PyTorch to further improve performance

Scene Recognition using Deep Learning (Computer Vision class project) **November 2017**

- Built deep learning architecture with MatLab to improve scene recognition performance to 87.3% accuracy
- Optimized model by using jittering, regularization and normalization

Distributed Key-value Store System (Advanced OS class project) **April 2018**

- Designed a simplified key-value store system by using ideas from Amazon Dynamo
- Improved availability and scalability by implementing replication, eventual consistency and fault-tolerance

FPGA 5-Stage Pipeline Processor (Processor Design class project) **April 2017**

- Designed and implemented a 5-stage pipeline processor using Verilog and FPGA
- Improved throughput by adding branch prediction and data forwarding

Flappy Bird GBA (github.com/jedyang97/flappy-bird-gba) **April 2016**

- Rewrote the popular iPhone game in C to provide a GBA version
- Optimized with DMA hardware acceleration to render high-resolution graphics

SKILLS:

Programming Languages:
Java, Python, C, PHP, HTML, JavaScript/JQuery, Android, SQL, JSP
Frameworks/Libraries: PyTorch, Jupyter, OpenCV, Spring, Struts2, Hibernate, Maven, QT
Systems: Linux/Unix, MacOS, Windows
Languages: English, Chinese (Mandarin)