# CHRIST UNIVERSITY, BANGALORE-560029

**End Semester Examination Sept / Oct - 2014**
**Bachelor of Computer Applications**

**Code : BCA134** **Max. Marks : 100**
**Sub : DIGITAL COMPUTER FUNDAMENTALS** **Duration : 3Hrs**

## SECTION A

**Answer All Queations** **10 X 2 = 20**

1 Perform the following conversion $(69)_{10} = ( ? )_2$.
2 What do you mean by sign-magnitude representation of a number?
3 Simplify the expression A+A'B using boolean laws.
4 What is an inverter? What is the purpose of using it in circuits?
5 Define multiplexer.
6 Draw the half subtractor circuit using logic gates.
7 Arrange two half adders to form a full adder.
8 What do you mean by 'toggle'? Which flip flop gives a toggle output and when?
9 How does PROM differ from ROM?
10 A shift register has eight flipflop. What is the largest decimal number that can be stored in it.

## SECTION B

**Answer any FIVE Questions** **5 X 6 = 30**

11 Convert $(369)_{10}$ to binary and octal.
12 Define EBCDIC. Explain its features.
13 State and prove distributive laws using truth table.
14 Simplify using K-Map.

$F(X,Y,Z) = \Sigma m(3,4,6,7)$

15 Explain with example the rules to simplify the SOP expression by using K- Map.
16 Explain the Decimal-to-BCD encoder.
17 Define counter. How does a synchronous counter differ from an asynchronous counter?

## SECTION C

**Answer any FIVE Questions.** **5 X 10 = 50**

18 Perform the following using Binary system.

(a). $4C_{16} + 3A_{16}$ (b). $BCD_{16} + 173_{16}$

19 (a). Demorganise the following expression and draw the logic diagram for the simplified expression (X(Y'Z'+YZ)) + X'Z'. (b). Simplify the expression by using boolean laws: AB+A(B+C)+B(B+C).
20 Realise AND, OR, NOT, NAND,XOR and XNOR using only NOR gate.
21 Explain in detail 1-line-to-4-line Demultiplexer.
22 Explain with circuit diagram and truth table about an active HIGH input S-R Latch and active LOW input S-R Latch.
23 Explain the working principle of J-K master slave Flip-Flop with a timing diagram.
24 Explain in detail Serial In Serial Out mode of operation of shift register.