Suraj Vijay Shetty

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Objective

Seeking a Summer 2025 internship in Hardware Design and Verification roles

Education

M.S in Electrical and Computer Engineering Sept 2024-Present
Portland State University, Portland Oregon
Courses:(By January 2025) System Verilog, Pre-Silicon Functional Validation, Microprocessor System Design, Formal Verification of HW/SW, ASIC Modeling and Synthesis, Computer Architecture

B.E in Electronics and Telecommunication Aug 2016 – Nov 2020
University Of Mumbai, Mumbai Maharashtra

Technical Skills

- Programming Languages and Protocols: SystemVerilog, Python, C, MIPI MPHY, AMBA(APB, AHB, AXI), MESI
- Verification Methodologies: UVM, Assertion-Based Verification (SystemVerilog Assertions)
- Tools and Operating Systems: Cadence(Xcelium, VManager, IMC, Simvision, Indago), Synopsys (Verdi, Design Compiler), ModelSim, Questasim, JIRA, Git, Windows, Linux
- Technical Abilities: UVM testbench development, Functional and Code Coverage closure, Digital logic verification, Waveform Debugging, Formal verification, Gate-Level Simulation, Formal Verification, Scripting

Experience

Samsung Semiconductor India Research (SSIR) – Banglore, India Aug 2021 – Aug 2024
Senior Engineer:

- Coordinated and supervised a team in verifying MIPI MPHY (v4.0, v5.0) PCS/PMA Verilog models and SerDes designs, overseeing test plan development and achieving full functional and code coverage
- Verified receiver DFE operation, validated BIST paths, PMA sub-blocks (CDR, PLL), and interface noise tolerance, while enhancing testbench components and collaborating with VIP vendors for improvements
- Developed assertion-based checkers for analog/digital interfaces in MPHY sublayer, improving bug detection by 40%, managed regression tests, ensured protocol compliance, and achieved 100% code and functional coverage

Maven Silicon – Banglore, India Nov 2020 – July 2021
Apprenticeship:

- Developed and verified RTL designs in Verilog HDL, implementing block-level structures and validating modules

Technical Projects

System Verilog Design for Last Level Cache in a shared memory configuration December 2023

- Simulated a Last Level Cache with a shared memory configuration using the MESI protocol for cache coherence across processors. Reported statistics on cache performance and validated behavior through compiled trace files

Python-Based Implementation of LFSR Modeling Using Pyrtl December 2023

- Hardware modeling using Python and PyRTL, specifically implementing a 4-bit Linear Feedback Shift Register (LFSR) with configurable feedback paths by use of PyRTL's simulation framework

Publications

An Enhanced DV approach for effectively verifying High Speed Low Power MIPI MPHY5.0 Designs- ***Achieved 2nd place in the Best Poster Presentation category*** March 2023

Published in DVCON US, Link/DVconUS/Doc/mipimphy

Advancements in UVM TestBench Architecture for Verifying High Speed MIPI MPHY 5.0 IP Sept 2022

Published in DVCON INDIA, Link/DVconIndia/Doc/mipimphy