TAPPITA JEEVAN PRASAD

+91-8074585019 jeevanprasadtappita@gmail.com LinkedIn GitHub

PROFILE SUMMARY

Enthusiastic Electronics and Communication Engineering student specializing in VLSI design and FPGA design development. Proficient in Verilog, System Verilog, Java and C-programming with practical experience in physical design and digital system projects.

EDUCATION

GMR Institute of Technology, Rajam, India
B.Tech ECE; GPA: 9.02 June 2022 – April 2026

Narayana Junior College, Bobbili, India
Senior Secondary; State Board; Percentage: 93.8 June 2020–May 2022

SKILLS

Languages: Java, C-programming
Tools: Cadence Virtuoso, Xilinx/Vivado, Matlab, Eclipse, VS-Code, Anaconda, Capture
Soft Skills: People Management, Leadership, Communication, Team Work, Adaptability, Puzzle solving

EXPERIENCE

VLSI-Physical design Intern, Abhyasa Semicon Technologies Jun 2024 – Jul 2024

- Completed a one-month VLSI Physical Design internship at Abhyasa Semicon Technologies, Vizag.
- Worked on Floor planning, placement, and clock tree synthesis using industrial EDA tools.
- Trained under Dr. S. Visweswara rao, gaining practical exposure to backend VLSI design flow.

VLSI design Intern, Cranes Varsity Jul 2025 – Present

- Pursuing an Advanced Diploma in VLSI Design & Verification at Cranes Varsity with Hands-on RTL and FPGA Design experience
- Implementing digital systems using Verilog, SystemVerilog, and FPGA boards like Artix-7 and Zynq
- Engaged in Verification of on-chip protocols including UART, SPI, I2C, and AXI4 using SystemVerilog
- Strengthening core skills in digital electronics, C/C++ Programming, and hardware debugging
- Working with industry-grade tools such as Xilinx Vivado and EDA playground for real time project development

PROJECTS

4-bit Low Voltage Comparator

- Designed a 4-bit CMOS low-voltage comparator achieving fast, accurate voltage comparison with minimal power consumption
- Optimized circuit performance for low-power digital Systems while maintaining reliability and speed
- **Technologies Used:** Verilog Programming, Circuit connection in Cadence Virtuoso

Bidirectional Parallel-Serial Data Transfer Unit

- Designed and implemented a digital System enabling conversion between parallel and serial data with bidirectional transfer capability
- Verified functionality using Verilog on EDA Playground through simulation and testbench validation
- **Tools used:** EDA Playground

Attendance Management System (Java)

- Built a Java-based system to record, track, and manage student attendance efficiently
- Implemented automated reporting and secure data handling, reducing manual effort and errors
- **Tools used:** Java (JDK)

CERTIFICATIONS

- VLSI-Physical design– Abhyasa Semicon Technologies (2024)
- Introduction to programming with Matlab (2024)
- Coursera c for everyone (2024)
- Foundation-Physical design (2025)

ACHIEVEMENTS

- Solved **50+ problems on Code chef**
- **IEI COORDINATOR:** Worked as a [IEI] Institute of Engineers (India) coordinator conducted events by engaging nearly 40-50 students in each event