ML507 BSB PPC440 Design

Adding Standard IP

May 2009

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ML507 Standard IP Design Overview

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  - Software Requirements
  - ML507 Setup
  - Using the Pre-Built Design
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  - Add Standard IP
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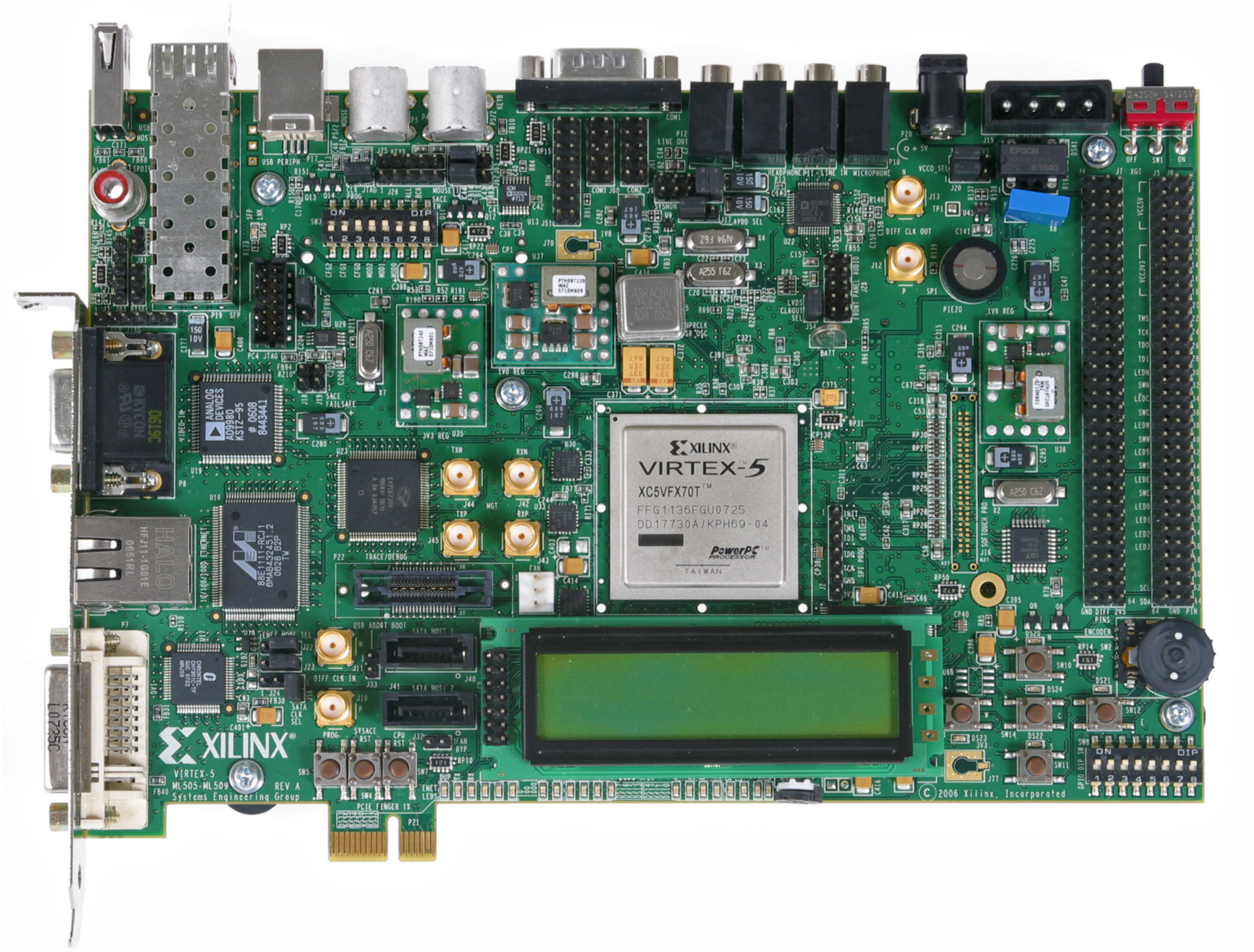
- **Create MFS Image**
- **Compile Standard IP Design**
  - Generate the ELF Files
  - Generate the Bitstream
- **Loading a Bootloop ELF into the Block RAM**
  - Running the Lwipdemo Application
- **Create an ACE File**
- **References**

Note: This Presentation applies to the ML507

ML507 Standard IP Design Overview

- **Standard IP Added:**
  - TFT – xps_tft
  - PS/2 – xps_ps2
  - General Purpose IO – xps_gpio
  - IIC Interface – xps_iic
  - Second PLB v46 bus – plb_v46
  - PLB to PLB Bridge – plbv46_plbv46_bridge
- **Standard IP Modified:**
  - SRAM Interface – xps_mch_emc

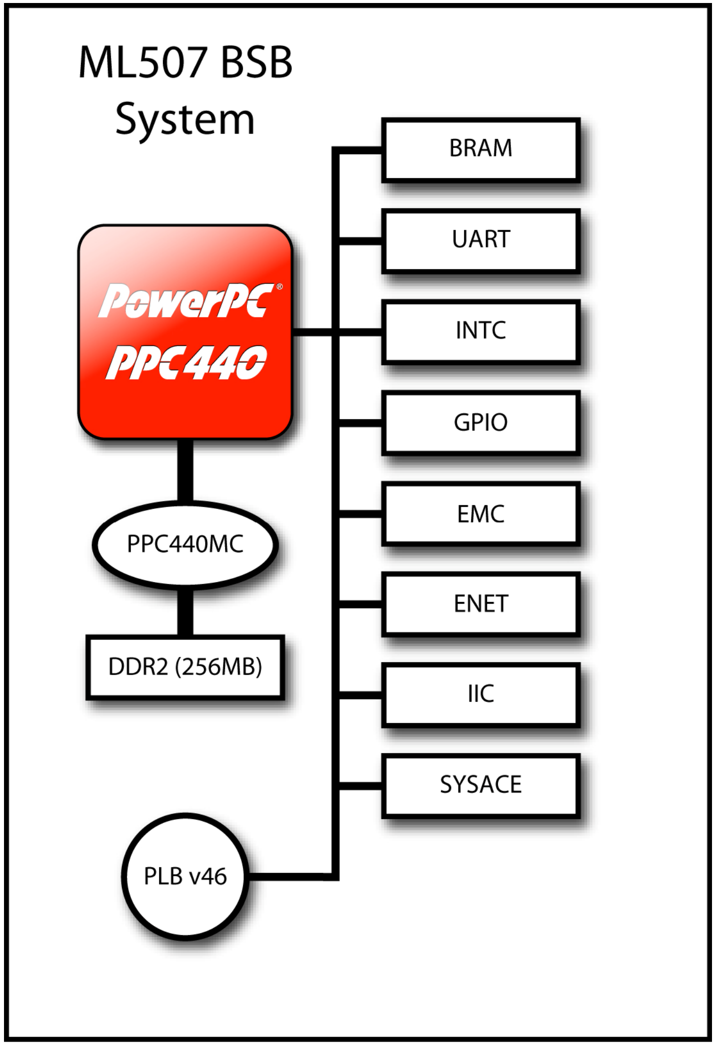
Xilinx ML507 Board



Note: Presentation applies to the ML507

ML507 Base System Builder Hardware

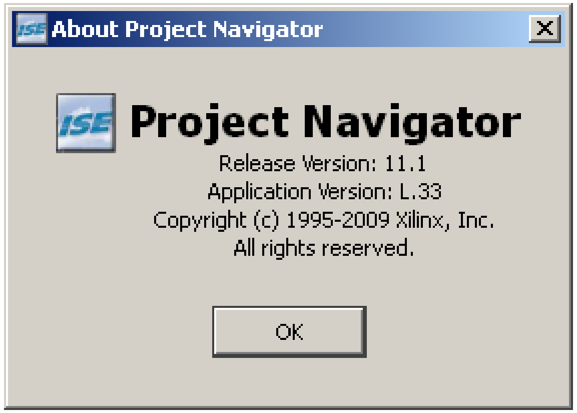
- **The ML507 PPC440 Design Hardware includes:**
  - PPC440MC DDR2 Interface
  - BRAM
  - External Memory Controller (EMC)
    - ZBT SRAM
  - Networking
  - UART
  - Interrupt Controller
  - System ACE CF Interface
  - GPIO (IIC, LEDs and LCD)
  - PLB Arbiter



Note: Presentation applies to the ML507

ISE Software Requirement

- **Xilinx ISE 11.1 software**



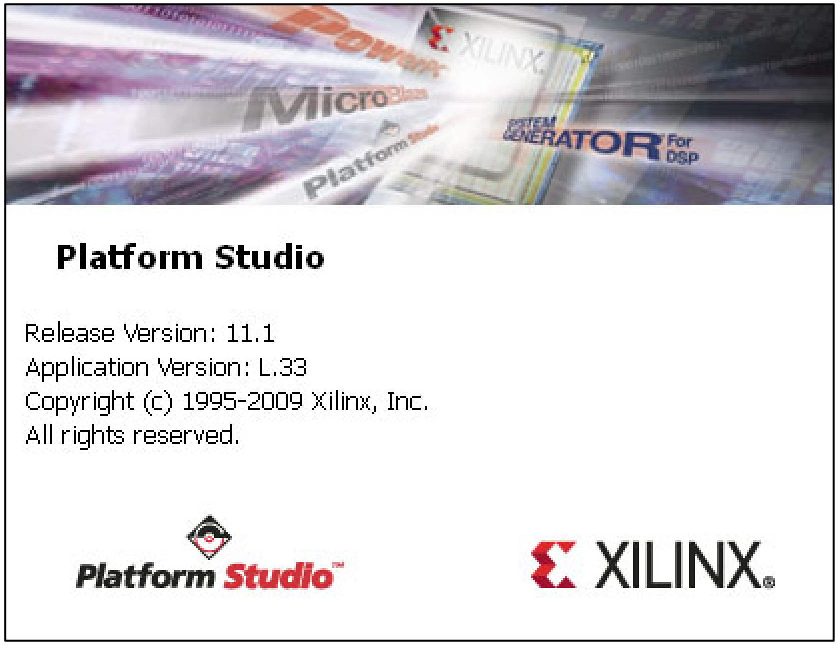
About Project Navigator

Project Navigator

Release Version: 11.1
Application Version: L.33
Copyright (c) 1995-2009 Xilinx, Inc.
All rights reserved.

EDK Software Requirement

- **Xilinx EDK 11.1 software**



Platform Studio

Release Version: 11.1
Application Version: L.33
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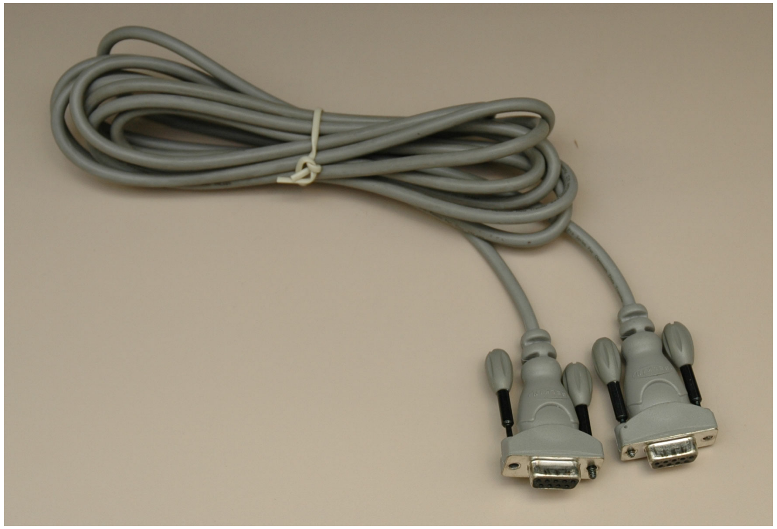
All rights reserved.

Note: Presentation applies to the ML507

ML507 Setup

- Connect the Xilinx Platform Cable USB to the ML507 board

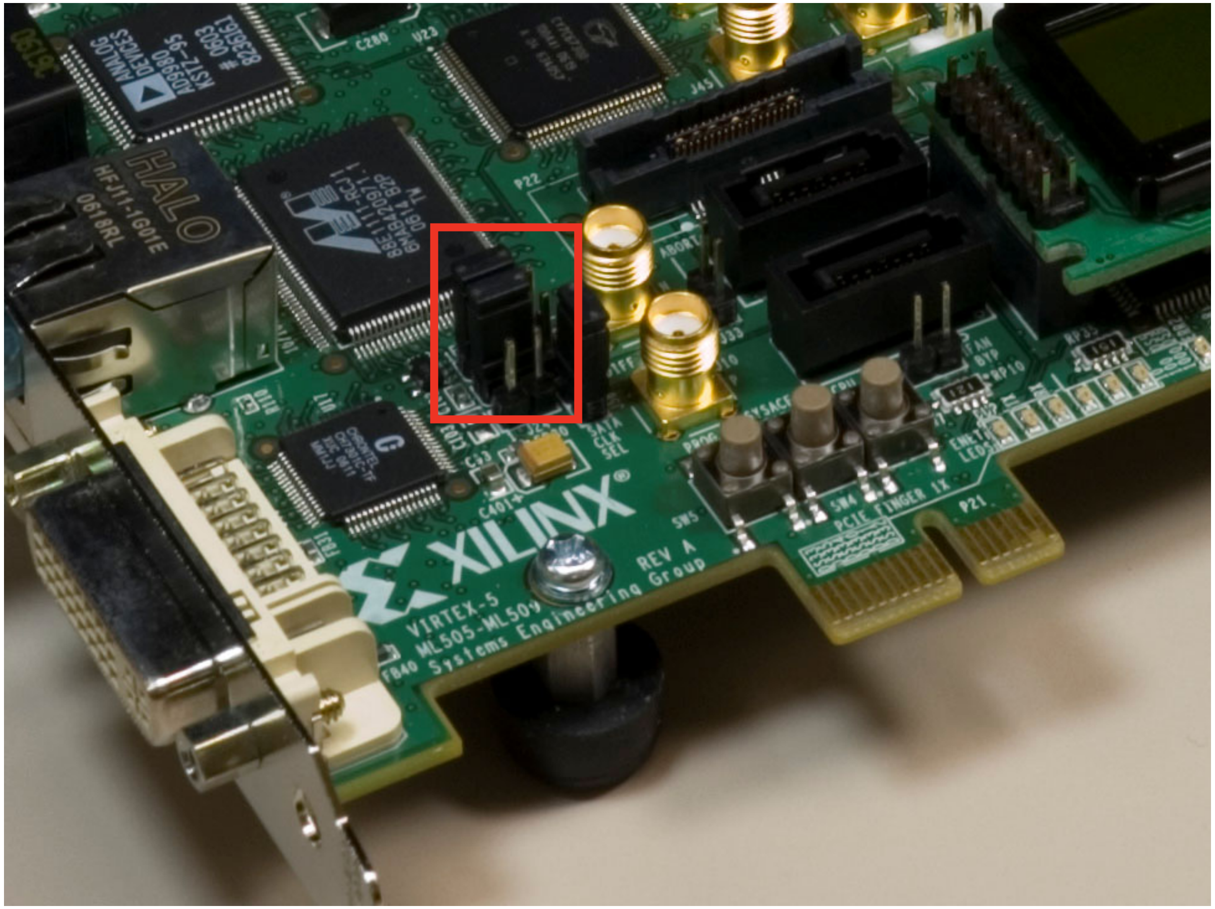
- Connect the RS232 null modem cable to the ML507 board



Note: Presentation applies to the ML507

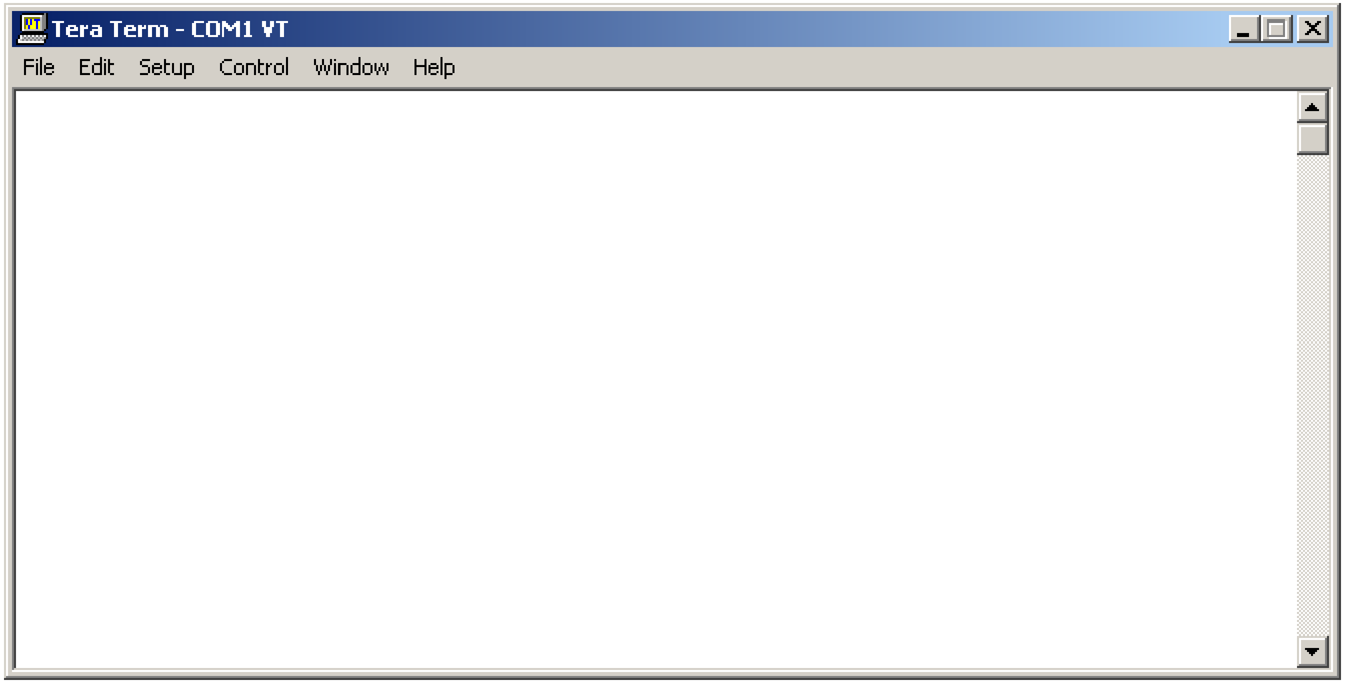
ML507 Setup

- **Set ML507 Jumpers for GMII**
  - Set both J22 and J23 to positions 1-2 (as shown)



ML507 Setup

- **Start the Terminal Program:**



Note: Presentation applies to the ML507

Additional ML507 Setup Details

- **Refer to ml505_overview_setup.ppt for details on:**
  - Software Requirements
  - ML507 Board Setup
  - Equipment and Cables
  - Software
  - Network
- **Terminal Programs**
  - This presentation requires the 9600-8-N-1 Baud terminal setup

ML505/506/507 Overview and Setup

Overview of the Hardware Designs and Software Applications

How to set up the equipment, software, CompactFlash, network, and terminal programs

Note: Presentation applies to the ML507

Using the Pre-Built Design

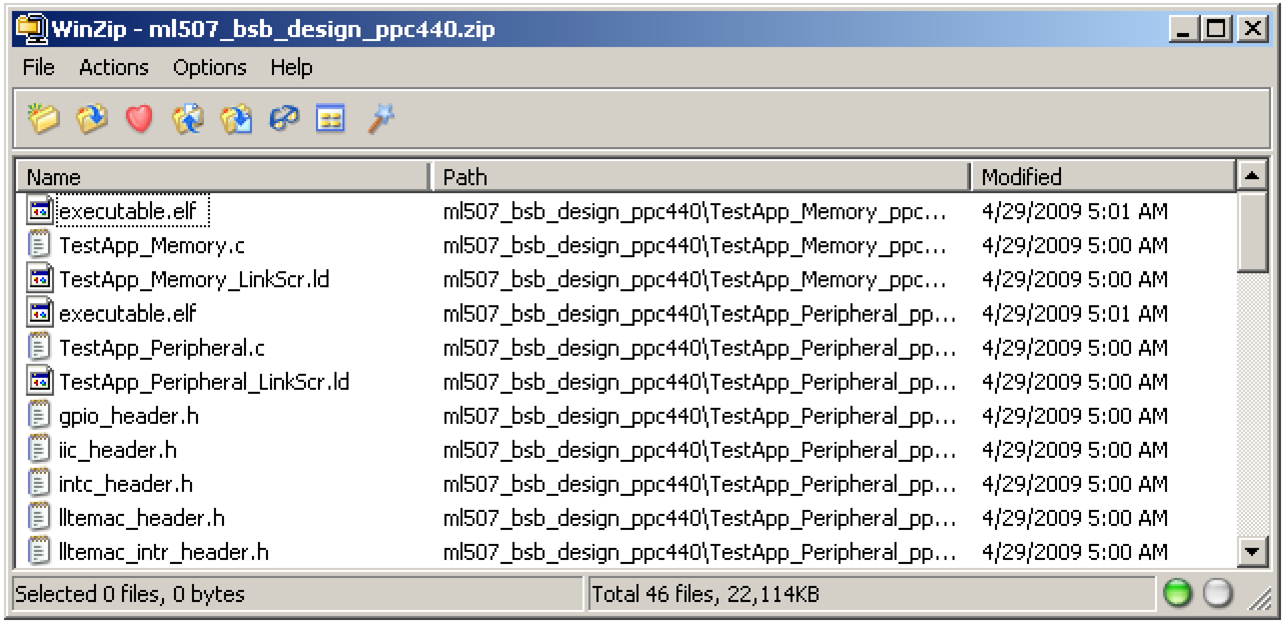
- **Unzip ml507_bsb_std_ip_ppc440.zip and locate pre-built bitstream and executable software files:**
  - ml507_bsb_std_ip_ppc440/implementation/download.bit
  - ml507_bsb_std_ip_ppc440/ppc440_0/code/*.elf
- **Configure FPGA**
  - Launch XPS project, ml507_bsb_system.xmp
  - From the menu, select Project → Launch EDK Shell and type:

    impact -batch etc/download.cmd
  - Go to Slide 92, to run the software application
- **For a tutorial on how to create the contents of the ml507_bsb_std_ip_ppc440.zip continue to the next slide**

Add Standard IP to BSB Design

Extracting the Design

- **Unzip the ml507_bsb_design_ppc440.zip file**
  - This creates ISE and EDK project directories



Name	Path	Modified
executable.elf	ml507_bsb_design_ppc440\TestApp_Memory_ppc...	4/29/2009 5:01 AM
TestApp_Memory.c	ml507_bsb_design_ppc440\TestApp_Memory_ppc...	4/29/2009 5:00 AM
TestApp_Memory_LinkScr.ld	ml507_bsb_design_ppc440\TestApp_Memory_ppc...	4/29/2009 5:00 AM
executable.elf	ml507_bsb_design_ppc440\TestApp_Peripheral_pp...	4/29/2009 5:01 AM
TestApp_Peripheral.c	ml507_bsb_design_ppc440\TestApp_Peripheral_pp...	4/29/2009 5:00 AM
TestApp_Peripheral_LinkScr.ld	ml507_bsb_design_ppc440\TestApp_Peripheral_pp...	4/29/2009 5:00 AM
gpio_header.h	ml507_bsb_design_ppc440\TestApp_Peripheral_pp...	4/29/2009 5:00 AM
iic_header.h	ml507_bsb_design_ppc440\TestApp_Peripheral_pp...	4/29/2009 5:00 AM
intc_header.h	ml507_bsb_design_ppc440\TestApp_Peripheral_pp...	4/29/2009 5:00 AM
lltemac_header.h	ml507_bsb_design_ppc440\TestApp_Peripheral_pp...	4/29/2009 5:00 AM
lltemac_intr_header.h	ml507_bsb_design_ppc440\TestApp_Peripheral_pp...	4/29/2009 5:00 AM

Selected 0 files, 0 bytes

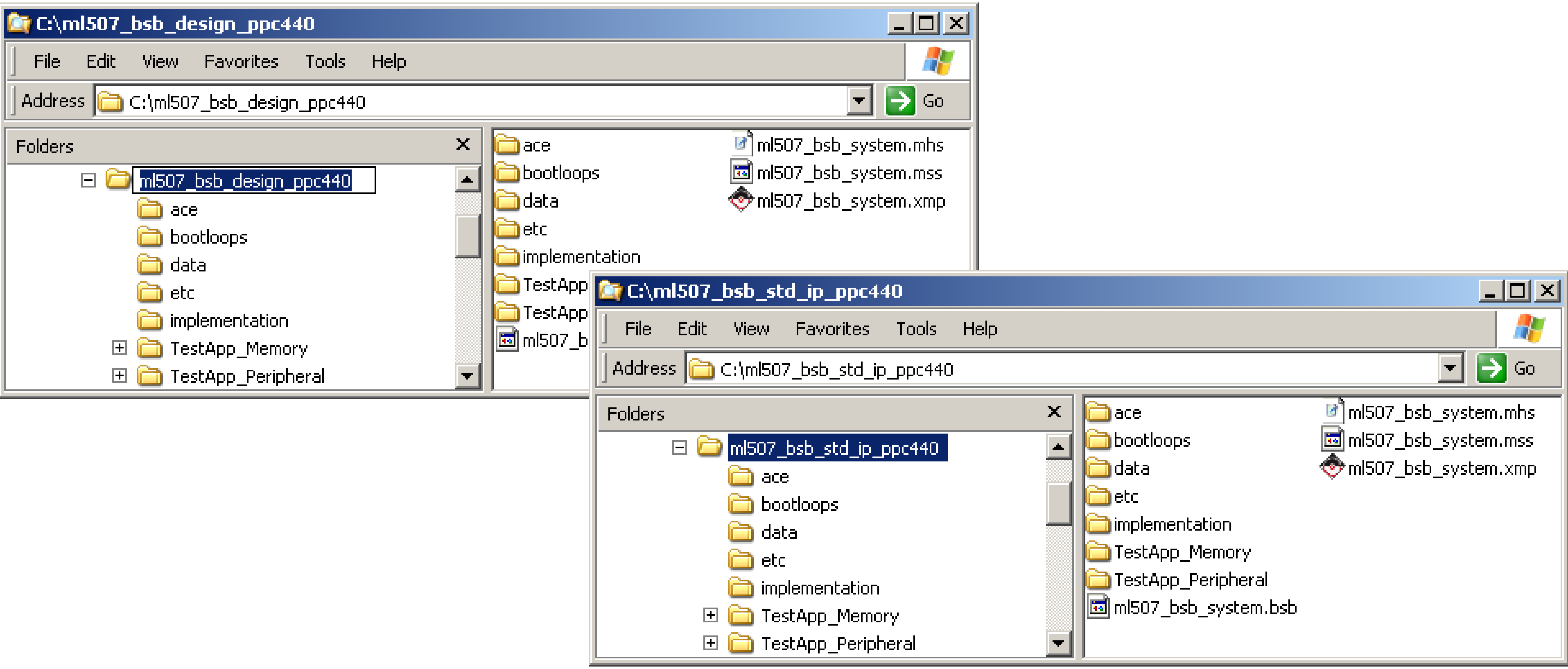
Total 46 files, 22,114KB

Note: Presentation applies to the ML507

Extracting the Design

- **Rename the project directory to**

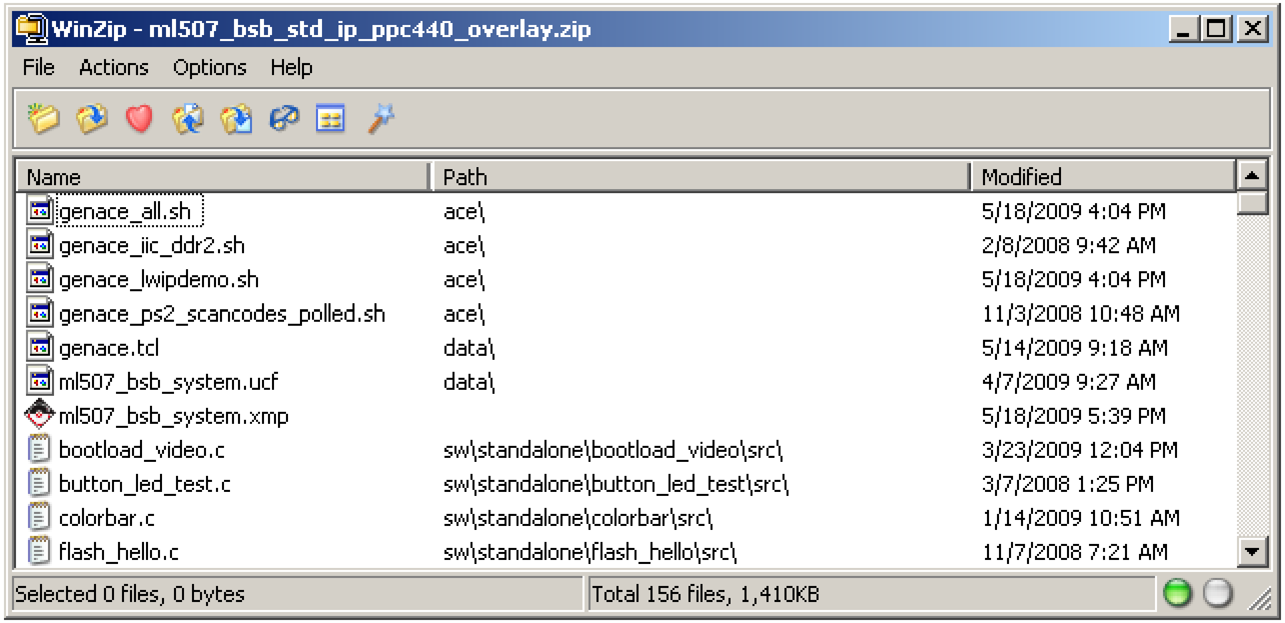
  ml507_bsb_std_ip_ppc440



Note: Presentation applies to the ML507

Extracting the Design

- **Unzip the ml507_bsb_std_ip_ppc440_overlay.zip file**
  - Unzip to the ml507_bsb_std_ip_ppc440 directory
  - This adds the Standard IP UCF and software to the design directory



Name	Path	Modified
genace_all.sh	ace\	5/18/2009 4:04 PM
genace_iic_ddr2.sh	ace\	2/8/2008 9:42 AM
genace_lwipdemo.sh	ace\	5/18/2009 4:04 PM
genace_ps2_scancodes_polled.sh	ace\	11/3/2008 10:48 AM
genace.tcl	data\	5/14/2009 9:18 AM
ml507_bsb_system.ucf	data\	4/7/2009 9:27 AM
ml507_bsb_system.xmp		5/18/2009 5:39 PM
bootload_video.c	sw\standalone\bootload_video\src\	3/23/2009 12:04 PM
button_led_test.c	sw\standalone\button_led_test\src\	3/7/2008 1:25 PM
colorbar.c	sw\standalone\colorbar\src\	1/14/2009 10:51 AM
flash_hello.c	sw\standalone\flash_hello\src\	11/7/2008 7:21 AM

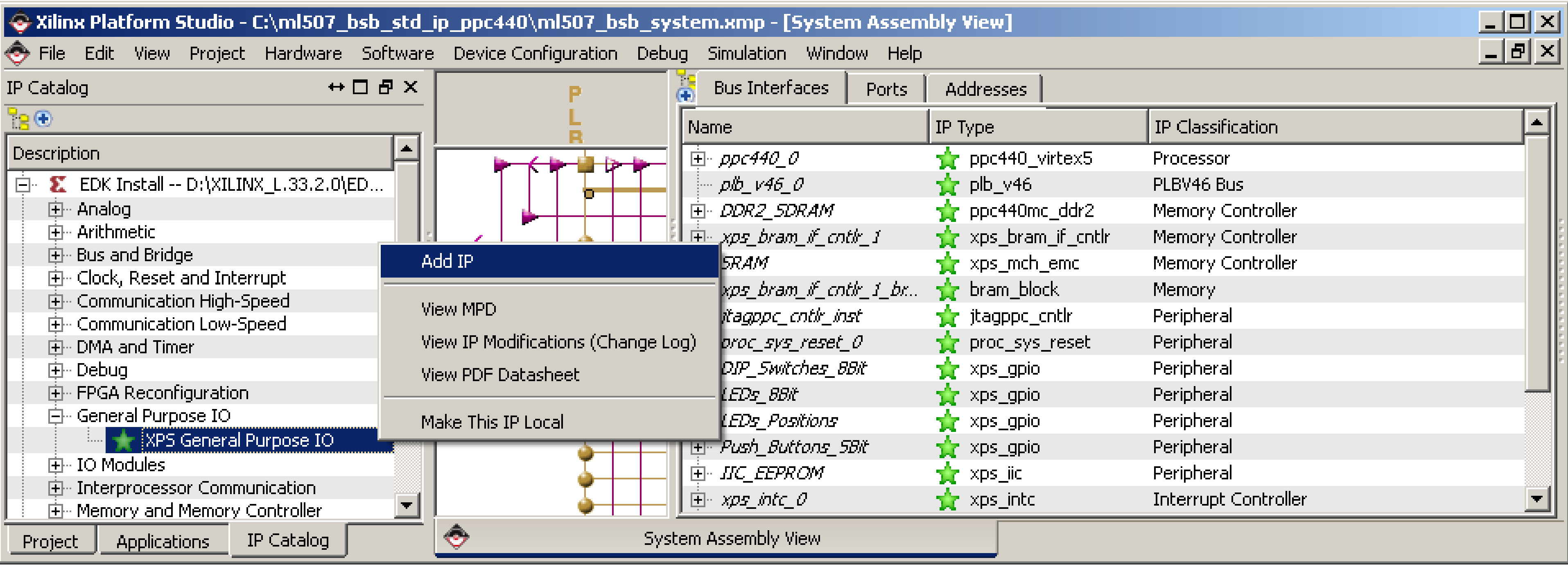
Selected 0 files, 0 bytes

Total 156 files, 1,410KB

Note: Presentation applies to the ML507

Add Standard IP

- **Open XPS project <design path>\ml507_bsb_system.xmp**
- **Add General Purpose IO**
  - Right-click on the **XPS General Purpose IO**
  - Select **Add IP …**

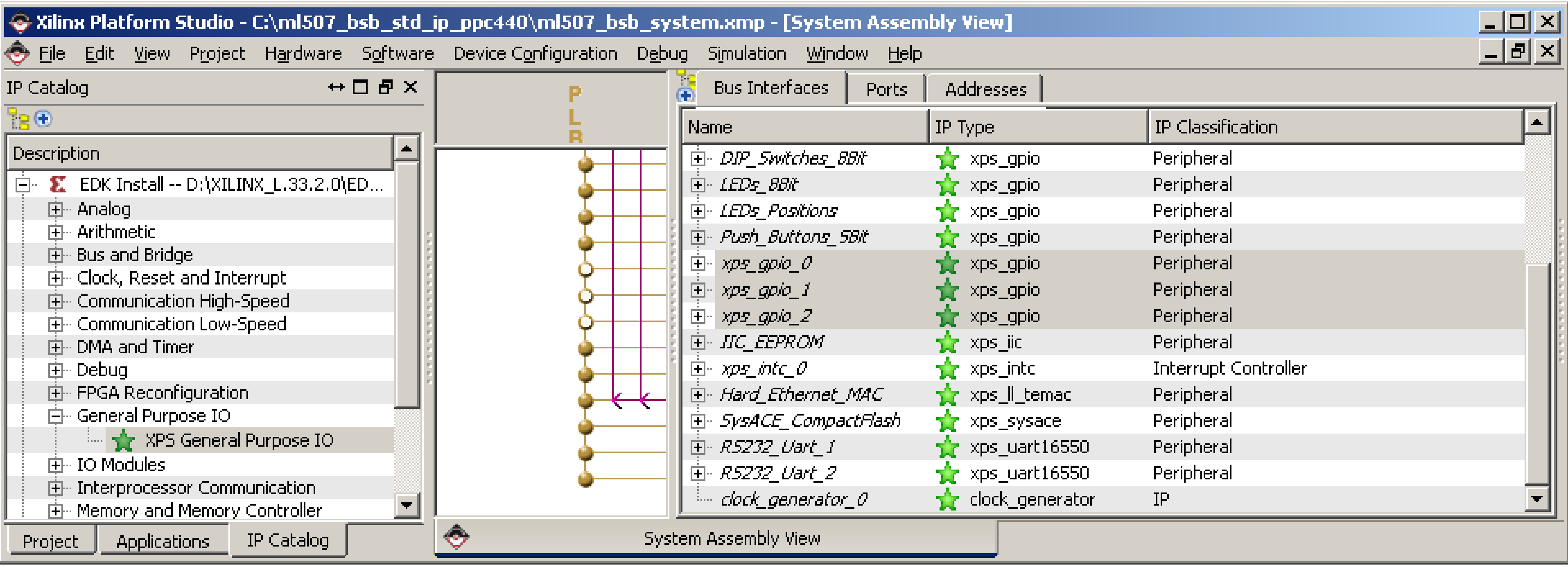


Name	IP Type	IP Classification
ppc440_0	ppc440_virtex5	Processor
plb_v46_0	plb_v46	PLBV46 Bus
DDR2_SDRAM	ppc440mc_ddr2	Memory Controller
xps_bram_if_cntlr_1	xps_bram_if_cntlr	Memory Controller
SRAM	xps_mch_emc	Memory Controller
xps_bram_if_cntlr_1_br..	bram_block	Memory
jtagppc_cntlr_inst	jtagppc_cntlr	Peripheral
proc_sys_reset_0	proc_sys_reset	Peripheral
DIP_Switches_8Bit	xps_gpio	Peripheral
LEDs_8Bit	xps_gpio	Peripheral
LEDs_Positions	xps_gpio	Peripheral
Push_Buttons_5Bit	xps_gpio	Peripheral
IIC_EEPROM	xps_iic	Peripheral
xps_intc_0	xps_intc	Interrupt Controller

Note: Presentation applies to the ML507

Add Standard IP

- **Add General Purpose IO**
  - Add 2 more instances of the XPS General Purpose IO IP



Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp - [System Assembly View]
File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help
IP Catalog
Bus Interfaces
Ports
Addresses
PLB
Project
Applications
IP Catalog
System Assembly View

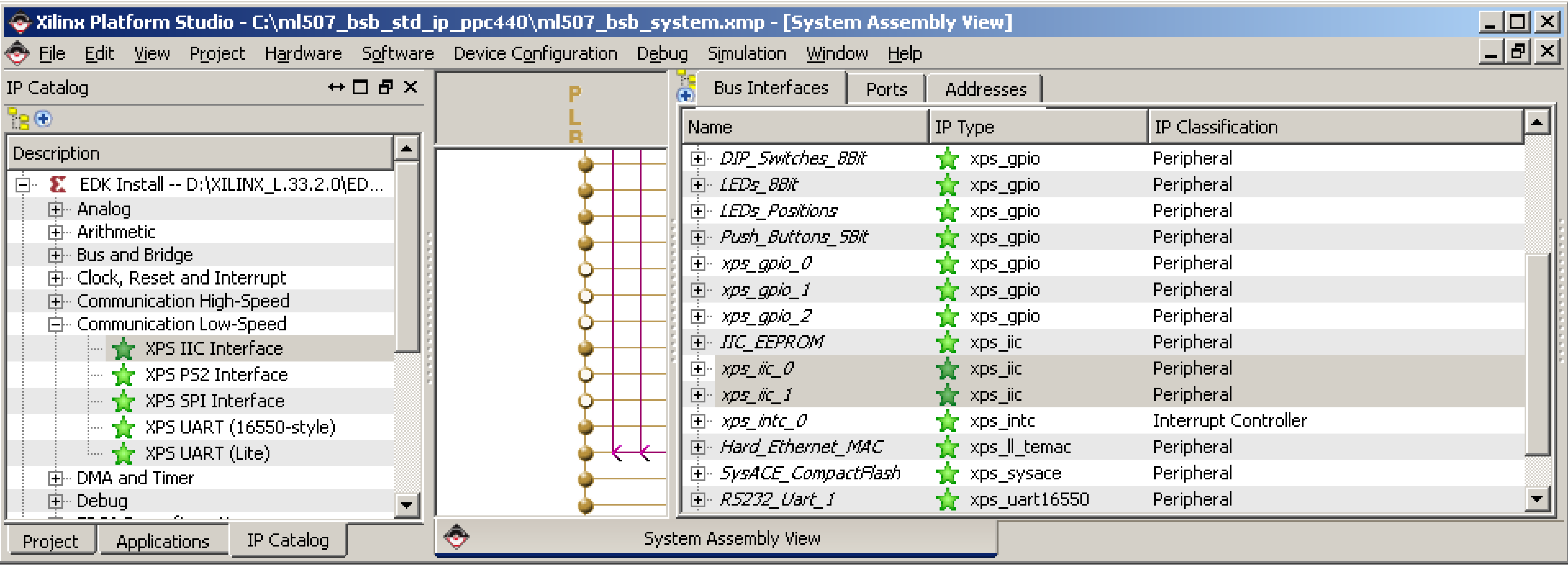
Description
- EDK Install -- D:\XILINX_L.33.2.0\ED...
  - Analog
  - Arithmetic
  - Bus and Bridge
  - Clock, Reset and Interrupt
  - Communication High-Speed
  - Communication Low-Speed
  - DMA and Timer
  - Debug
  - FPGA Reconfiguration
  - General Purpose IO
    - XPS General Purpose IO
  - IO Modules
  - Interprocessor Communication
  - Memory and Memory Controller

Name	IP Type	IP Classification
DIP_Switches_8Bit	xps_gpio	Peripheral
LEDs_8Bit	xps_gpio	Peripheral
LEDs_Positions	xps_gpio	Peripheral
Push_Buttons_5Bit	xps_gpio	Peripheral
xps_gpio_0	xps_gpio	Peripheral
xps_gpio_1	xps_gpio	Peripheral
xps_gpio_2	xps_gpio	Peripheral
IIC_EEPROM	xps_iic	Peripheral
xps_intc_0	xps_intc	Interrupt Controller
Hard_Ethernet_MAC	xps_ll_temac	Peripheral
SysACE_CompactFlash	xps_sysace	Peripheral
RS232_Uart_1	xps_uart16550	Peripheral
RS232_Uart_2	xps_uart16550	Peripheral
clock_generator_0	clock_generator	IP

Note: Presentation applies to the ML507

Add Standard IP

- **Add two instances of the XPS IIC Interface**
  - – Right-click on XPS IIC Interface
  - – Select **Add IP…**
  - – Repeat for second instance



Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp - [System Assembly View]
File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help
IP Catalog
Description
Bus Interfaces
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Addresses
PLB
Project
Applications
IP Catalog
System Assembly View

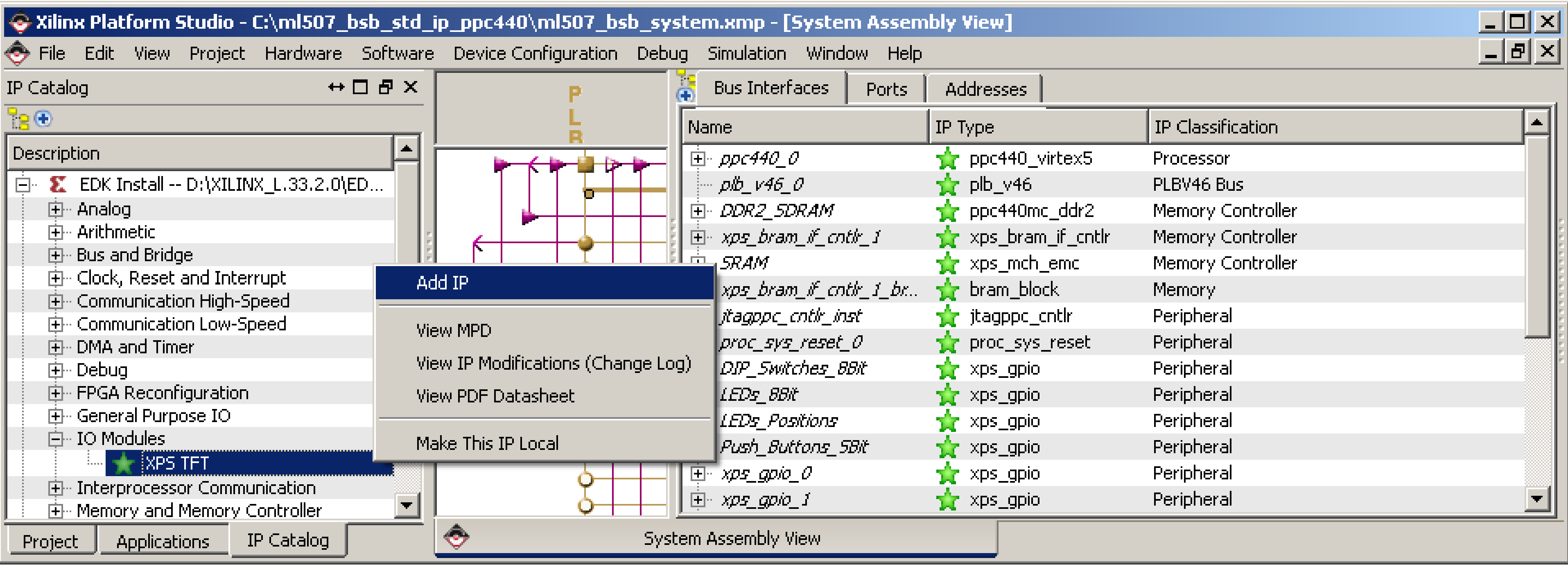
- EDK Install -- D:\XILINX_L.33.2.0\ED...
  - Analog
  - Arithmetic
  - Bus and Bridge
  - Clock, Reset and Interrupt
  - Communication High-Speed
  - Communication Low-Speed
    - XPS IIC Interface
    - XPS PS2 Interface
    - XPS SPI Interface
    - XPS UART (16550-style)
    - XPS UART (Lite)
  - DMA and Timer
  - Debug

Name	IP Type	IP Classification
DIP_Switches_8Bit	xps_gpio	Peripheral
LEDs_8Bit	xps_gpio	Peripheral
LEDs_Positions	xps_gpio	Peripheral
Push_Buttons_5Bit	xps_gpio	Peripheral
xps_gpio_0	xps_gpio	Peripheral
xps_gpio_1	xps_gpio	Peripheral
xps_gpio_2	xps_gpio	Peripheral
IIC_EEPROM	xps_iic	Peripheral
xps_iic_0	xps_iic	Peripheral
xps_iic_1	xps_iic	Peripheral
xps_intc_0	xps_intc	Interrupt Controller
Hard_Ethernet_MAC	xps_ll_temac	Peripheral
SysACE_CompactFlash	xps_sysace	Peripheral
RS232_Uart_1	xps_uart16550	Peripheral

Note: Presentation applies to the ML507

Add Standard IP

- **Add Video Controller**
  - – Right-click on **XPS TFT**
  - – Select **Add IP…**

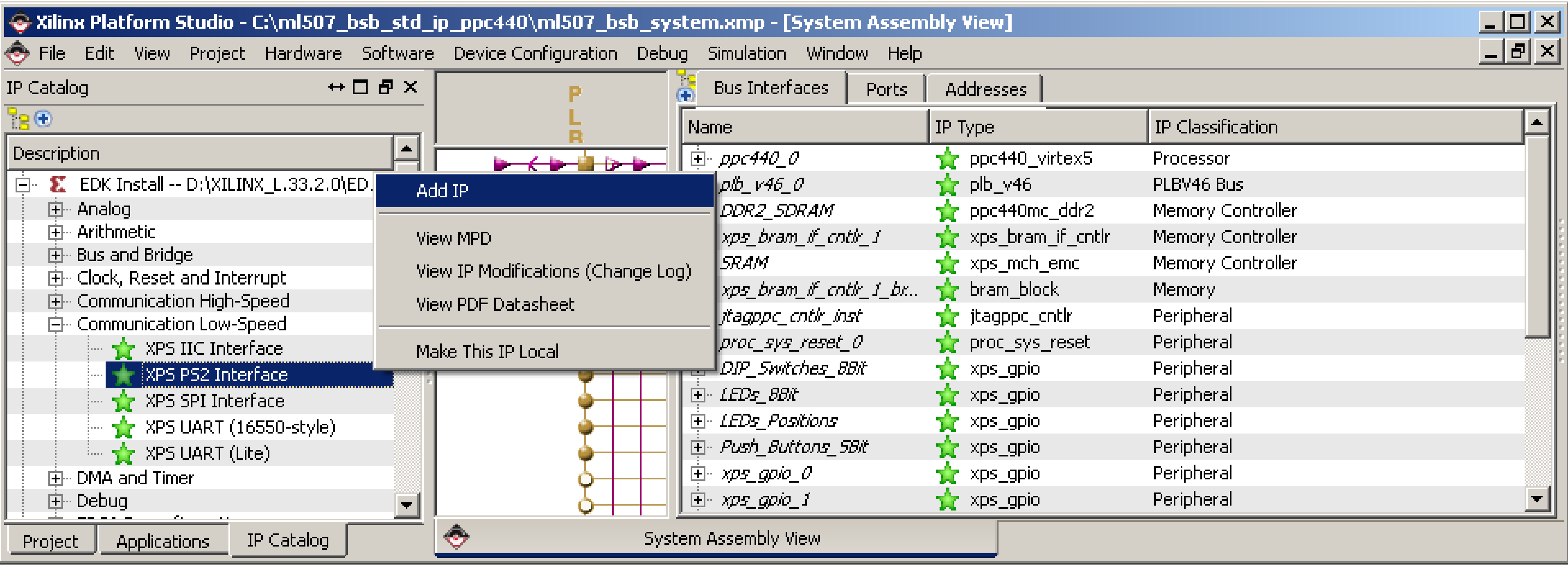


Name	IP Type	IP Classification
ppc440_0	ppc440_virtex5	Processor
plb_v46_0	plb_v46	PLBV46 Bus
DDR2_SDRAM	ppc440mc_ddr2	Memory Controller
xps_bram_if_cntlr_1	xps_bram_if_cntlr	Memory Controller
SRAM	xps_mch_emc	Memory Controller
xps_bram_if_cntlr_1_br..	bram_block	Memory
jtagppc_cntlr_inst	jtagppc_cntlr	Peripheral
proc_sys_reset_0	proc_sys_reset	Peripheral
DIP_Switches_8Bit	xps_gpio	Peripheral
LEDs_8Bit	xps_gpio	Peripheral
LEDs_Positions	xps_gpio	Peripheral
Push_Buttons_5Bit	xps_gpio	Peripheral
xps_gpio_0	xps_gpio	Peripheral
xps_gpio_1	xps_gpio	Peripheral

Note: Presentation applies to the ML507

Add Standard IP

- **Add PS/2 Interface**
  - Right-click on **XPS PS2 Interface**
  - Select **Add IP…**

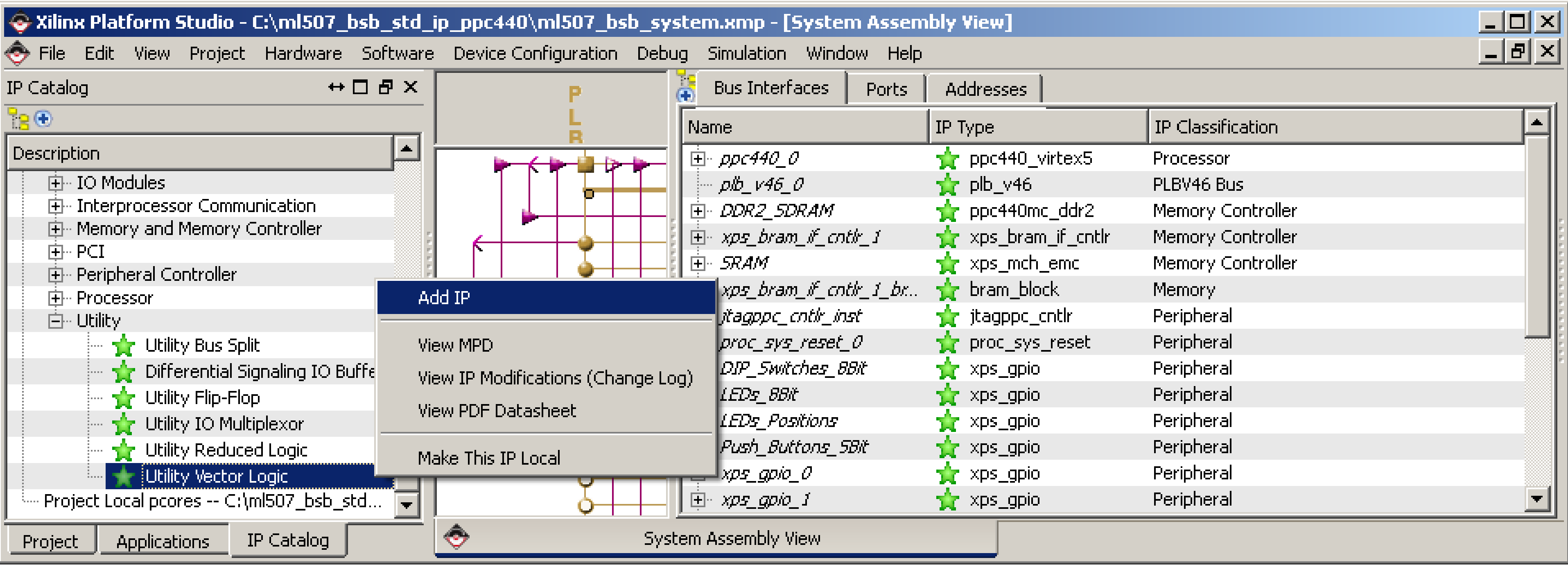


Name	IP Type	IP Classification
ppc440_0	ppc440_virtex5	Processor
plb_v46_0	plb_v46	PLBV46 Bus
DDR2_SDRAM	ppc440mc_ddr2	Memory Controller
xps_bram_if_cntlr_1	xps_bram_if_cntlr	Memory Controller
SRAM	xps_mch_emc	Memory Controller
xps_bram_if_cntlr_1_br...	bram_block	Memory
jtagppc_cntlr_inst	jtagppc_cntlr	Peripheral
proc_sys_reset_0	proc_sys_reset	Peripheral
DIP_Switches_8Bit	xps_gpio	Peripheral
LEDs_8Bit	xps_gpio	Peripheral
LEDs_Positions	xps_gpio	Peripheral
Push_Buttons_5Bit	xps_gpio	Peripheral
xps_gpio_0	xps_gpio	Peripheral
xps_gpio_1	xps_gpio	Peripheral

Note: Presentation applies to the ML507

Add Standard IP

- **Add an Inverter**
  - Right-click on **Utility Vector Logic**
  - Select **Add IP…**

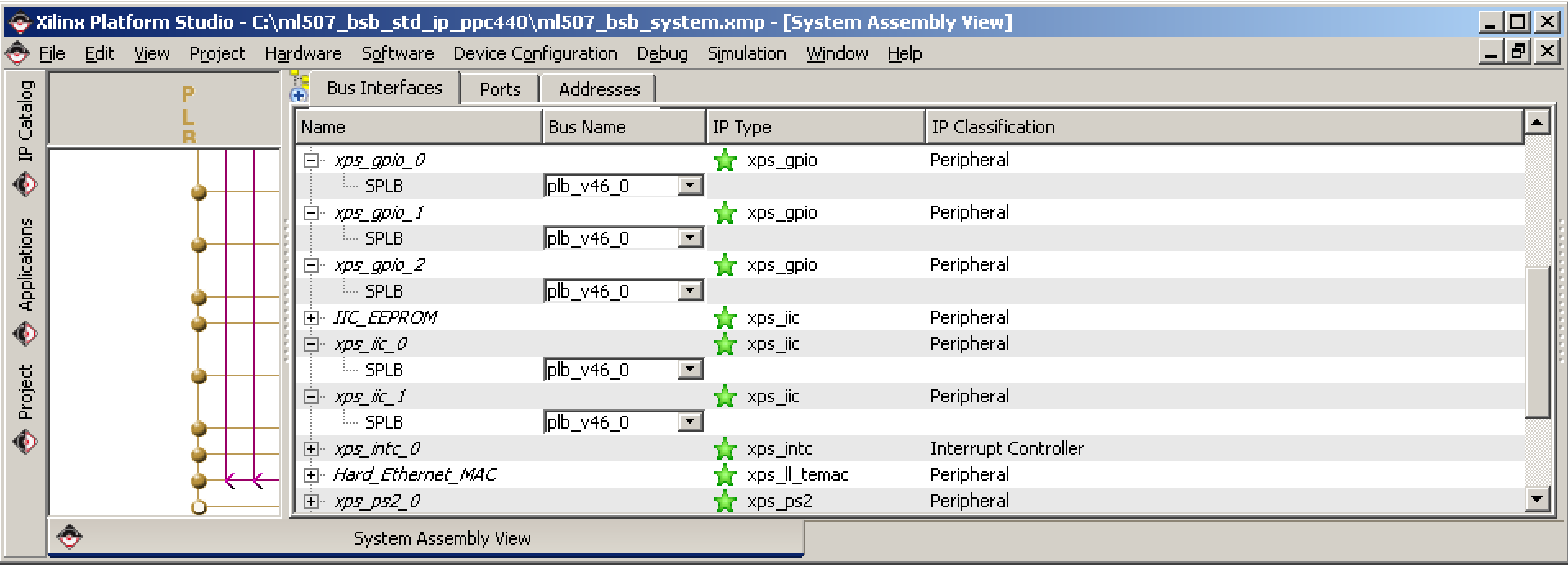

Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp - [System Assembly View]
File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help
IP Catalog
Description
IO Modules
Interprocessor Communication
Memory and Memory Controller
PCI
Peripheral Controller
Processor
Utility
Utility Bus Split
Differential Signaling IO Buffe
Utility Flip-Flop
Utility IO Multiplexor
Utility Reduced Logic
Utility Vector Logic
Project Local pcores -- C:\ml507_bsb_std...
Add IP
View MPD
View IP Modifications (Change Log)
View PDF Datasheet
Make This IP Local
Project
Applications
IP Catalog
PLB
System Assembly View
Bus Interfaces
Ports
Addresses

Name	IP Type	IP Classification
ppc440_0	ppc440_virtex5	Processor
plb_v46_0	plb_v46	PLBV46 Bus
DDR2_SDRAM	ppc440mc_ddr2	Memory Controller
xps_bram_if_cntlr_1	xps_bram_if_cntlr	Memory Controller
SRAM	xps_mch_emc	Memory Controller
xps_bram_if_cntlr_1_br..	bram_block	Memory
jtagppc_cntlr_inst	jtagppc_cntlr	Peripheral
proc_sys_reset_0	proc_sys_reset	Peripheral
DIP_Switches_8Bit	xps_gpio	Peripheral
LEDs_8Bit	xps_gpio	Peripheral
LEDs_Positions	xps_gpio	Peripheral
Push_Buttons_5Bit	xps_gpio	Peripheral
xps_gpio_0	xps_gpio	Peripheral
xps_gpio_1	xps_gpio	Peripheral

Note: Presentation applies to the ML507

Connect Buses

- **Expand these instances:**
  - **xps_gpio_0, xps_gpio_1, xps_gpio_3, xps_iic_0,** and **xps_iic_1**
  - Connect them to **plb_v46_0**

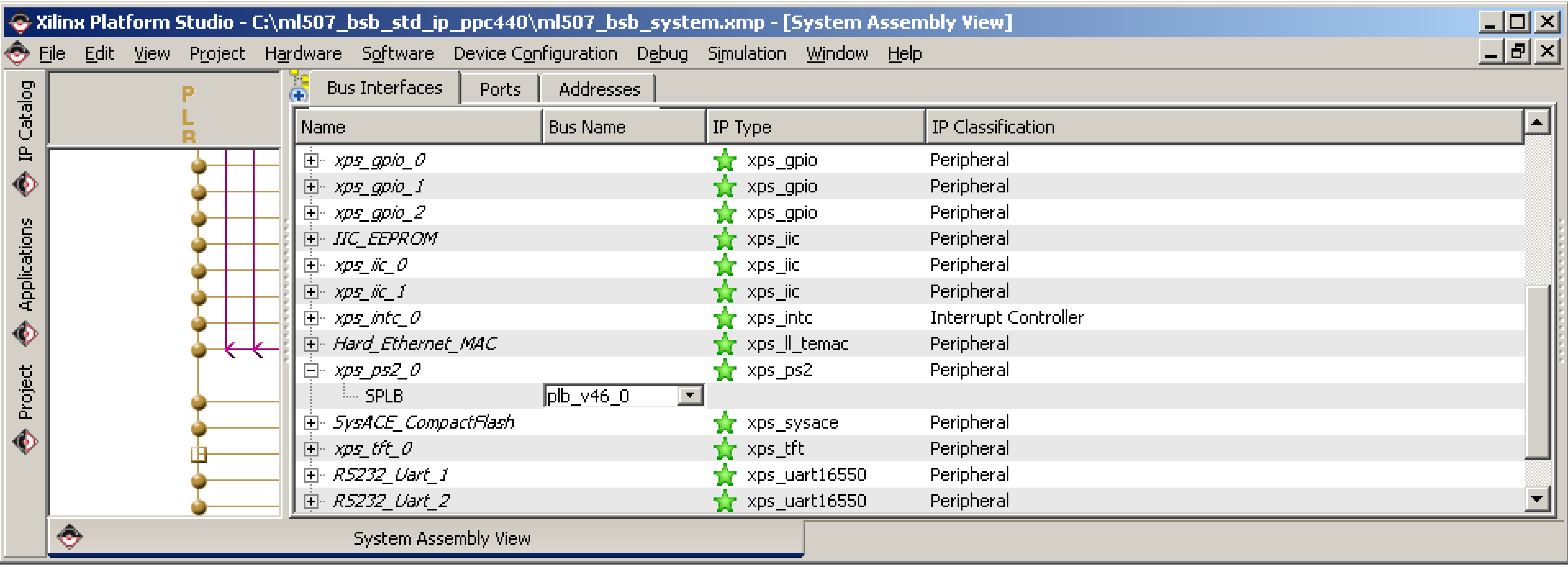


Name	Bus Name	IP Type	IP Classification
⊟ *xps_gpio_0*		xps_gpio	Peripheral
SPLB	plb_v46_0		
⊟ *xps_gpio_1*		xps_gpio	Peripheral
SPLB	plb_v46_0		
⊟ *xps_gpio_2*		xps_gpio	Peripheral
SPLB	plb_v46_0		
⊞ *IIC_EEPROM*		xps_iic	Peripheral
⊟ *xps_iic_0*		xps_iic	Peripheral
SPLB	plb_v46_0		
⊟ *xps_iic_1*		xps_iic	Peripheral
SPLB	plb_v46_0		
⊞ *xps_intc_0*		xps_intc	Interrupt Controller
⊞ *Hard_Ethernet_MAC*		xps_ll_temac	Peripheral
⊞ *xps_ps2_0*		xps_ps2	Peripheral

Note: Presentation applies to the ML507

Connect Buses

- **Expand this instance:**
  - **xps_ps2_0**
  - Connect it to **plb_v46_0**



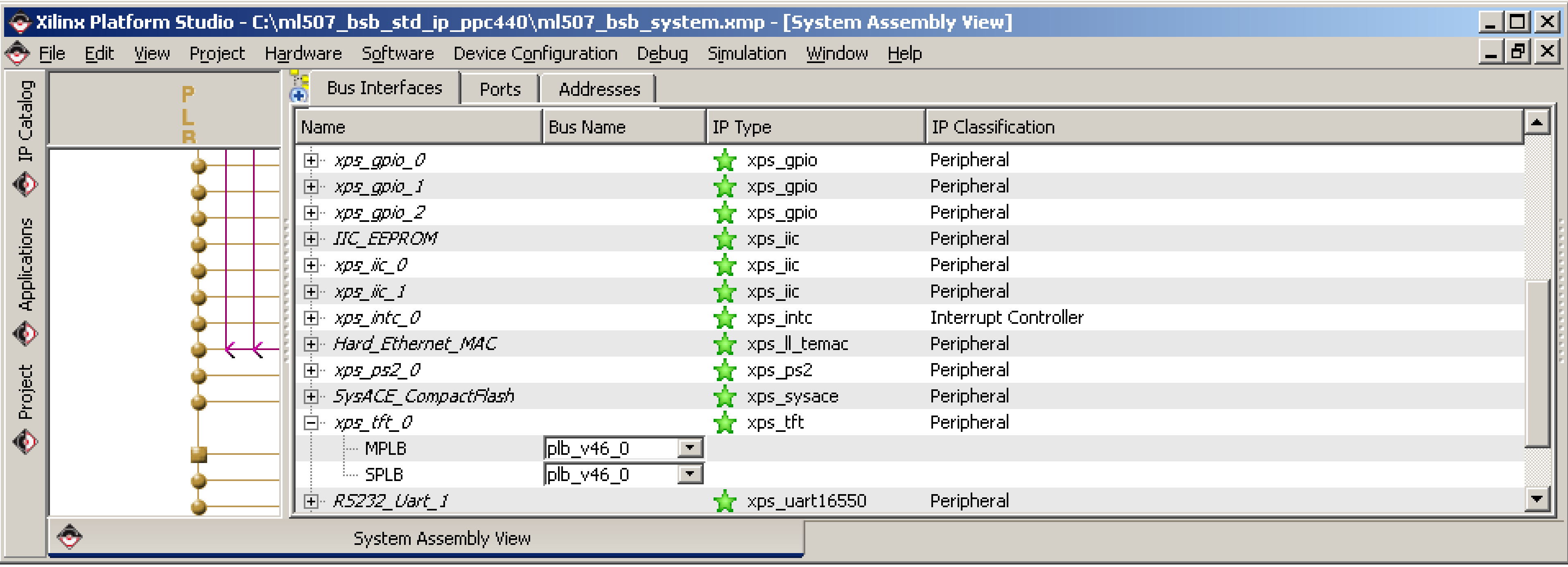
Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp - [System Assembly View]

Name	Bus Name	IP Type	IP Classification
⊞ *xps_gpio_0*		xps_gpio	Peripheral
⊞ *xps_gpio_1*		xps_gpio	Peripheral
⊞ *xps_gpio_2*		xps_gpio	Peripheral
⊞ *IIC_EEPROM*		xps_iic	Peripheral
⊞ *xps_iic_0*		xps_iic	Peripheral
⊞ *xps_iic_1*		xps_iic	Peripheral
⊞ *xps_intc_0*		xps_intc	Interrupt Controller
⊞ *Hard_Ethernet_MAC*		xps_ll_temac	Peripheral
⊟ *xps_ps2_0*		xps_ps2	Peripheral
SPLB	plb_v46_0		
⊞ *SysACE_CompactFlash*		xps_sysace	Peripheral
⊞ *xps_tft_0*		xps_tft	Peripheral
⊞ *RS232_Uart_1*		xps_uart16550	Peripheral
⊞ *RS232_Uart_2*		xps_uart16550	Peripheral

Note: Presentation applies to the ML507

Connect Buses

- **Expand this instance:**
  - **xps_tft_0**
  - Connect both the **MPLB** and the **SPLB** to **plb_v46_0**



Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp - [System Assembly View]
File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help
IP Catalog
Applications
Project
PLB
Bus Interfaces
Ports
Addresses
System Assembly View

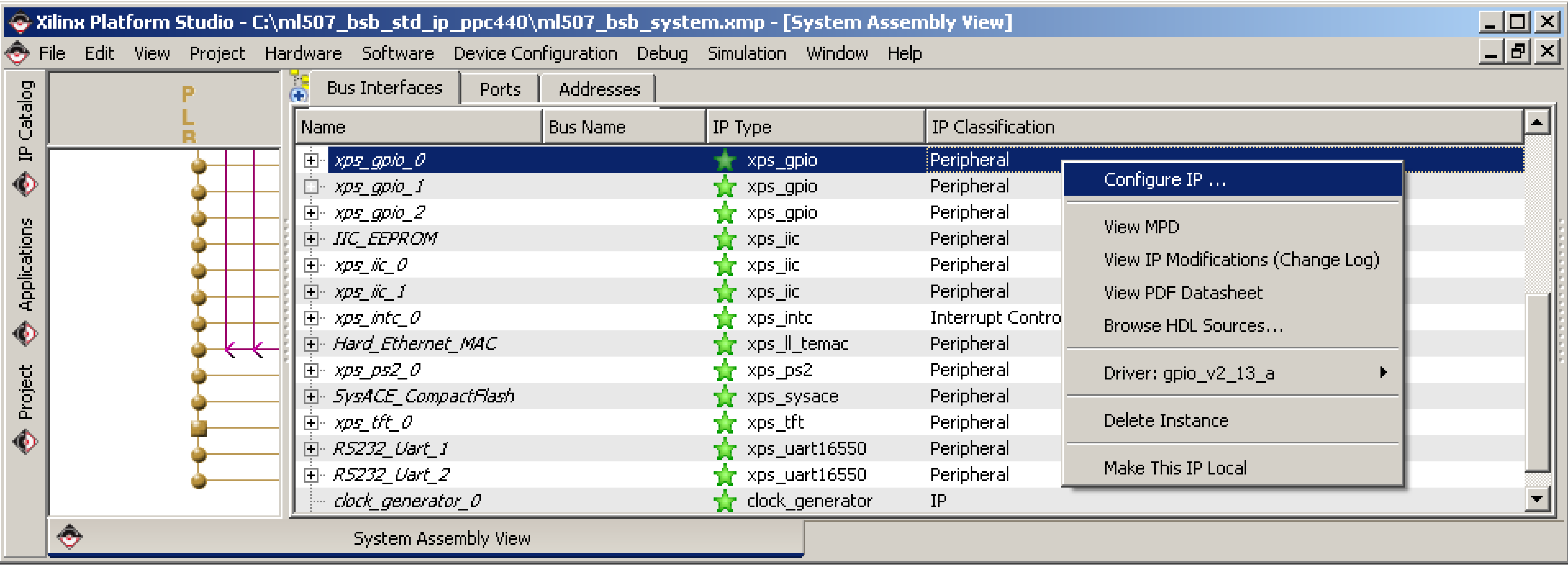
Name	Bus Name	IP Type	IP Classification
xps_gpio_0		xps_gpio	Peripheral
xps_gpio_1		xps_gpio	Peripheral
xps_gpio_2		xps_gpio	Peripheral
IIC_EEPROM		xps_iic	Peripheral
xps_iic_0		xps_iic	Peripheral
xps_iic_1		xps_iic	Peripheral
xps_intc_0		xps_intc	Interrupt Controller
Hard_Ethernet_MAC		xps_ll_temac	Peripheral
xps_ps2_0		xps_ps2	Peripheral
SysACE_CompactFlash		xps_sysace	Peripheral
xps_tft_0		xps_tft	Peripheral
MPLB	plb_v46_0		
SPLB	plb_v46_0		
RS232_Uart_1		xps_uart16550	Peripheral

Note: Presentation applies to the ML507

IP Configuration

Configure IP

- **Configure the GPIO IP**
  - Right-click on the **xps_gpio_0**
  - Select **Configure IP…**

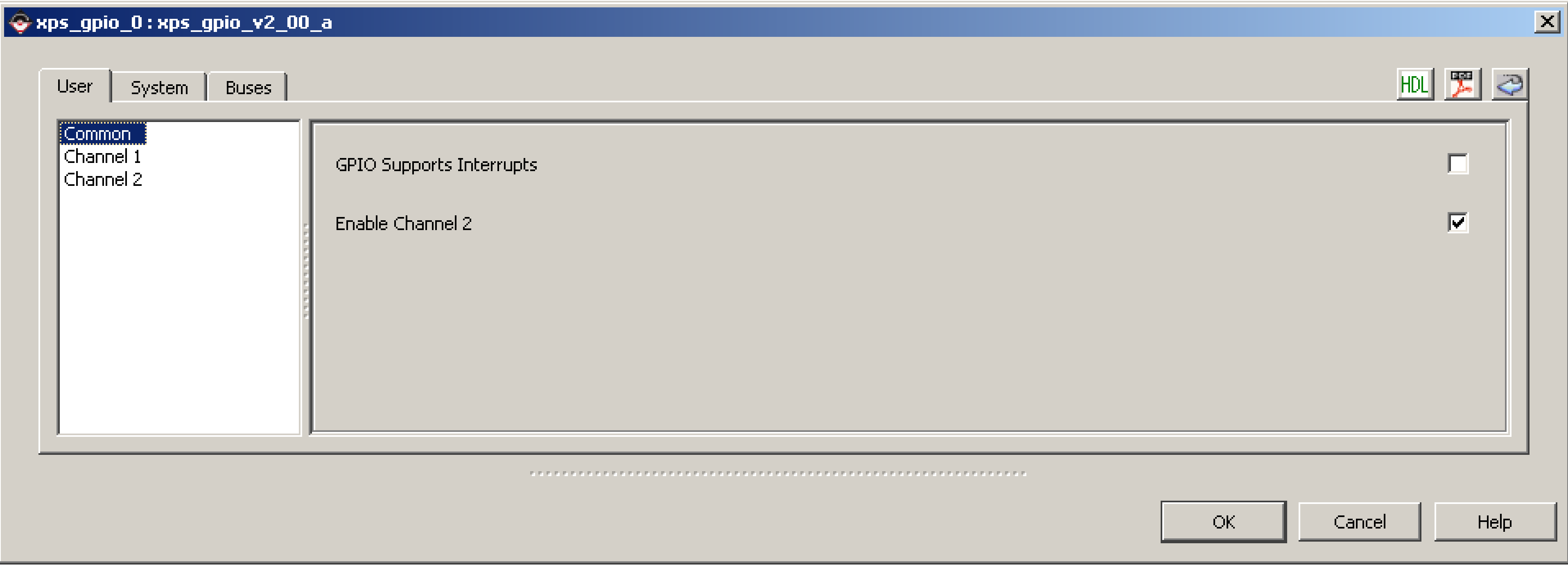


Name	Bus Name	IP Type	IP Classification
xps_gpio_0		xps_gpio	Peripheral
xps_gpio_1		xps_gpio	Peripheral
xps_gpio_2		xps_gpio	Peripheral
IIC_EEPROM		xps_iic	Peripheral
xps_iic_0		xps_iic	Peripheral
xps_iic_1		xps_iic	Peripheral
xps_intc_0		xps_intc	Interrupt Contro
Hard_Ethernet_MAC		xps_ll_temac	Peripheral
xps_ps2_0		xps_ps2	Peripheral
SysACE_CompactFlash		xps_sysace	Peripheral
xps_tft_0		xps_tft	Peripheral
RS232_Uart_1		xps_uart16550	Peripheral
RS232_Uart_2		xps_uart16550	Peripheral
clock_generator_0		clock_generator	IP

Note: Presentation applies to the ML507

Configure IP

- **Under the User tab:**
  - Select **Common**
  - Check **Enable Channel 2**



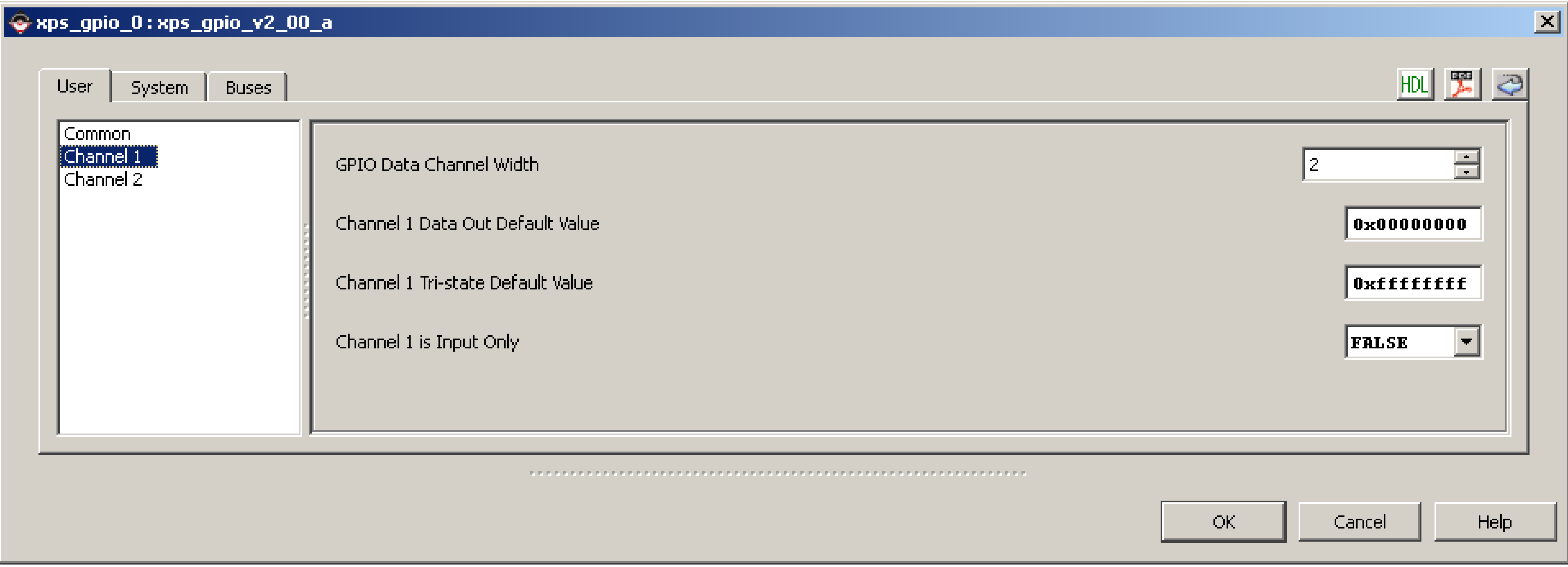
GPIO Supports Interrupts □

Enable Channel 2 ☑

Note: Presentation applies to the ML507

Configure IP

- **Under the User tab:**
  - Select **Channel 1**
  - Set GPIO2 Data Channel Width to **2** (Error LEDs)



xps_gpio_0 : xps_gpio_v2_00_a

GPIO Data Channel Width: 2

Channel 1 Data Out Default Value: 0x00000000

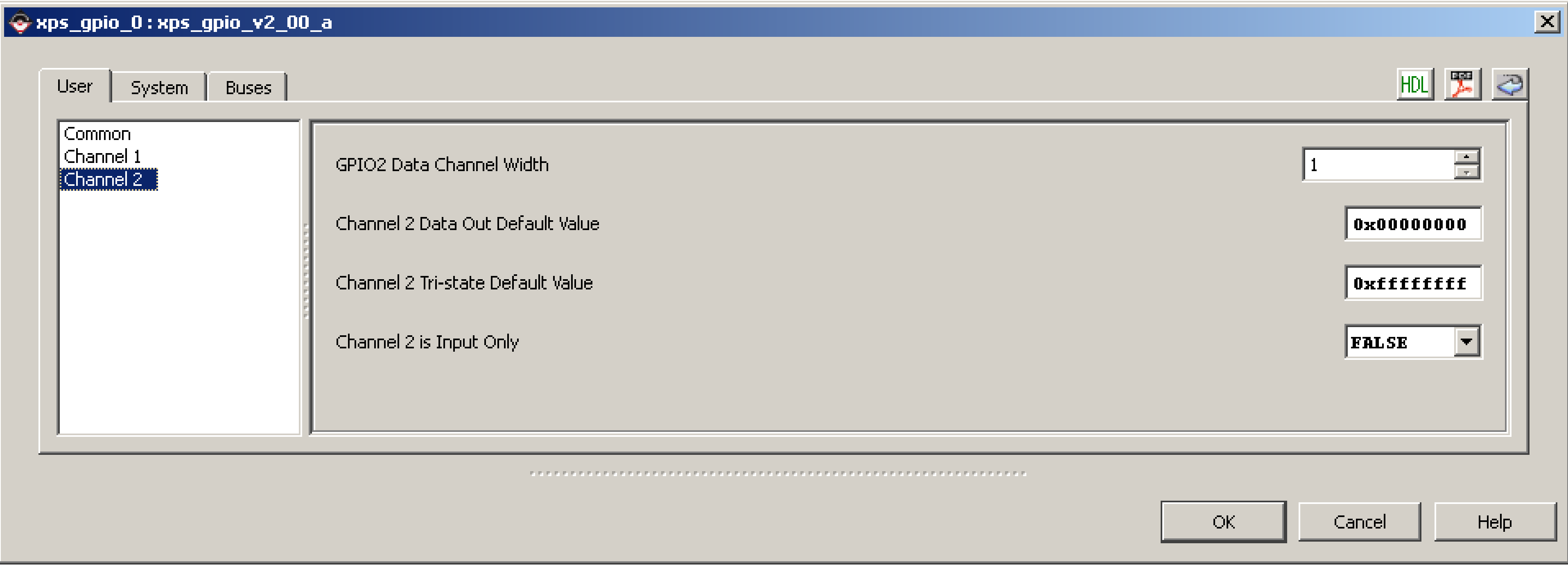
Channel 1 Tri-state Default Value: 0xffffffff

Channel 1 is Input Only: FALSE

Note: Presentation applies to the ML507

Configure IP

- **Under the User tab:**
  - Select **Channel 2**
  - Set GPIO2 Data Channel Width to **1** (Piezo transducer)



GPIO2 Data Channel Width: 1

Channel 2 Data Out Default Value: 0x00000000

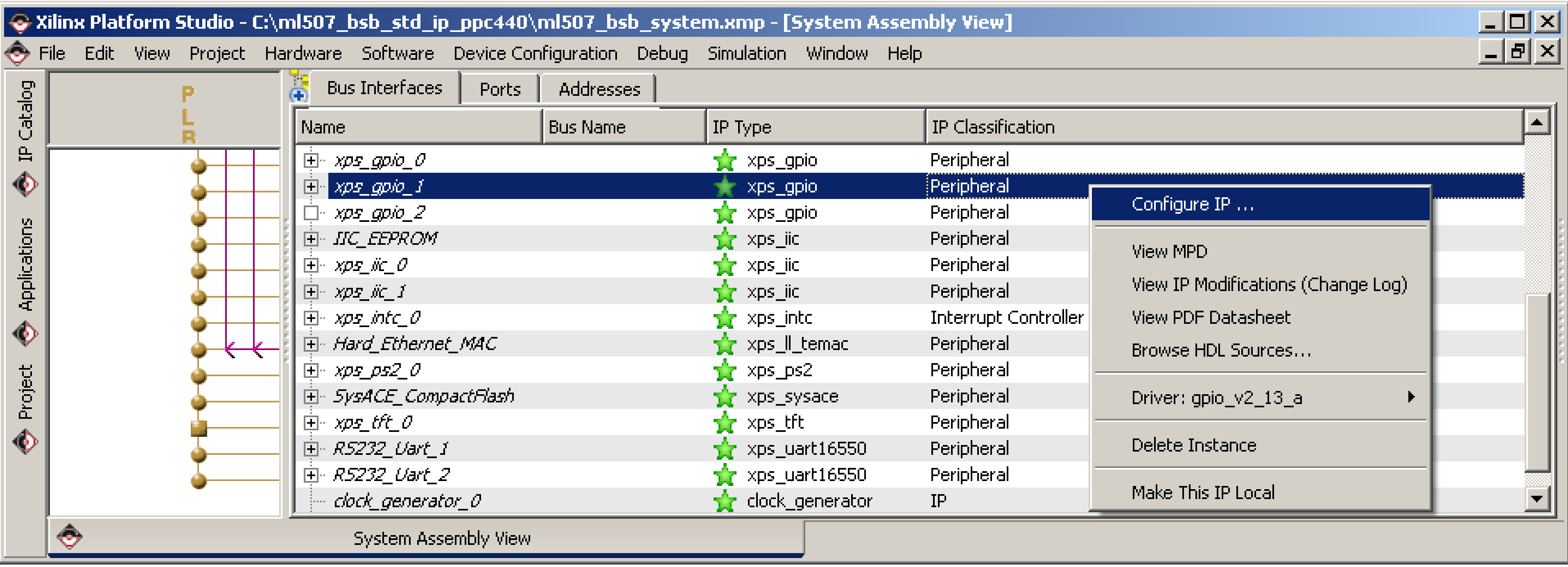
Channel 2 Tri-state Default Value: 0xffffffff

Channel 2 is Input Only: FALSE

Note: Presentation applies to the ML507

Configure IP

- **Configure the GPIO IP**
  - Right-click on the **xps_gpio_1**
  - Select **Configure IP…**



Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp - [System Assembly View]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

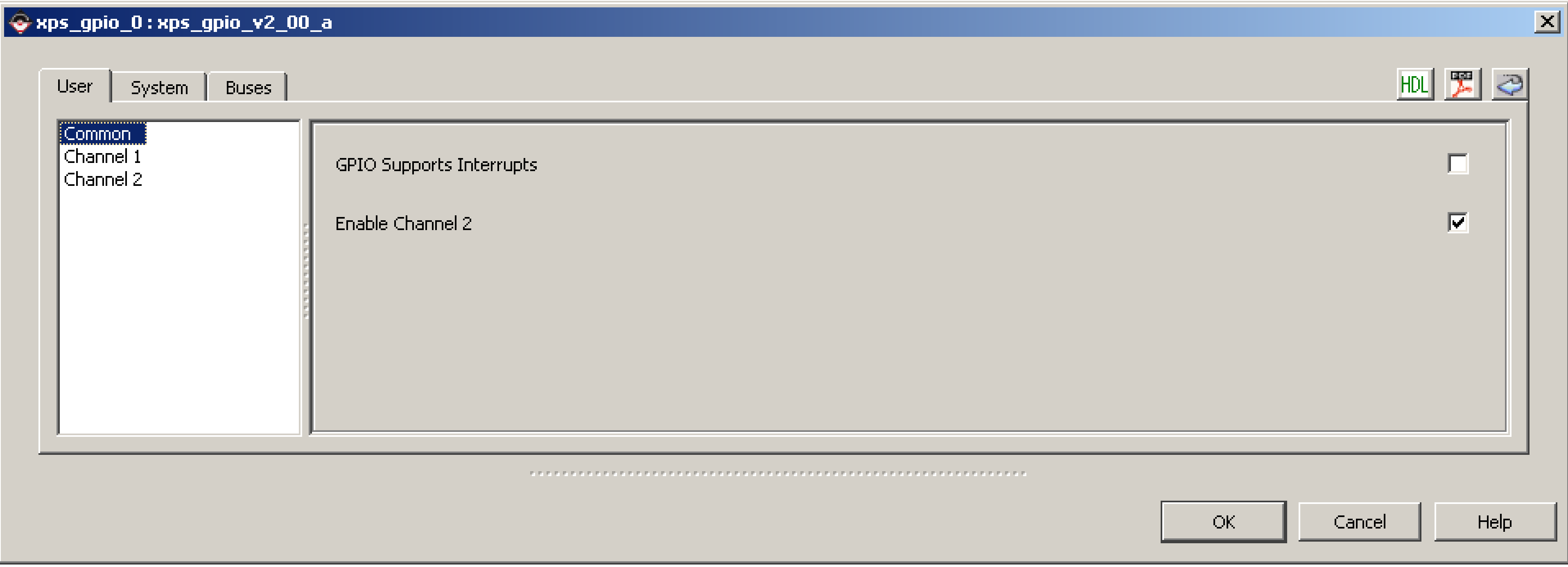
Bus Interfaces | Ports | Addresses

Name	Bus Name	IP Type	IP Classification
xps_gpio_0		xps_gpio	Peripheral
xps_gpio_1		xps_gpio	Peripheral
xps_gpio_2		xps_gpio	Peripheral
IIC_EEPROM		xps_iic	Peripheral
xps_iic_0		xps_iic	Peripheral
xps_iic_1		xps_iic	Peripheral
xps_intc_0		xps_intc	Interrupt Controller
Hard_Ethernet_MAC		xps_ll_temac	Peripheral
xps_ps2_0		xps_ps2	Peripheral
SysACE_CompactFlash		xps_sysace	Peripheral
xps_tft_0		xps_tft	Peripheral
RS232_Uart_1		xps_uart16550	Peripheral
RS232_Uart_2		xps_uart16550	Peripheral
clock_generator_0		clock_generator	IP

Note: Presentation applies to the ML507

Configure IP

- **Under the User tab:**
  - Select **Common**
  - Check **Enable Channel 2**



xps_gpio_0 : xps_gpio_v2_00_a

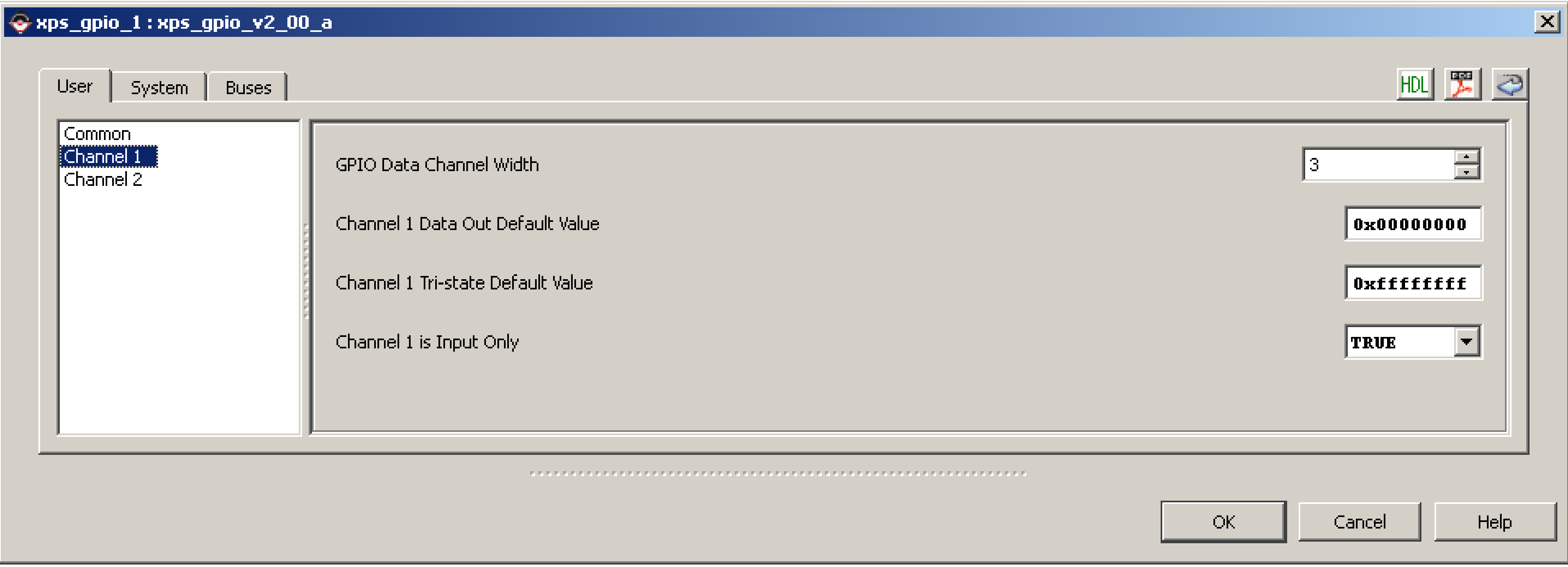
GPIO Supports Interrupts □

Enable Channel 2 ☑

Note: Presentation applies to the ML507

Configure IP

- **Under the User tab:**
  - Select **Channel 1**
  - Set GPIO2 Data Channel Width to **3** (Rotary Encoder/Push Button)
  - Set Channel 1 is Input Only to **TRUE**



xps_gpio_1 : xps_gpio_v2_00_a

GPIO Data Channel Width: 3

Channel 1 Data Out Default Value: 0x00000000

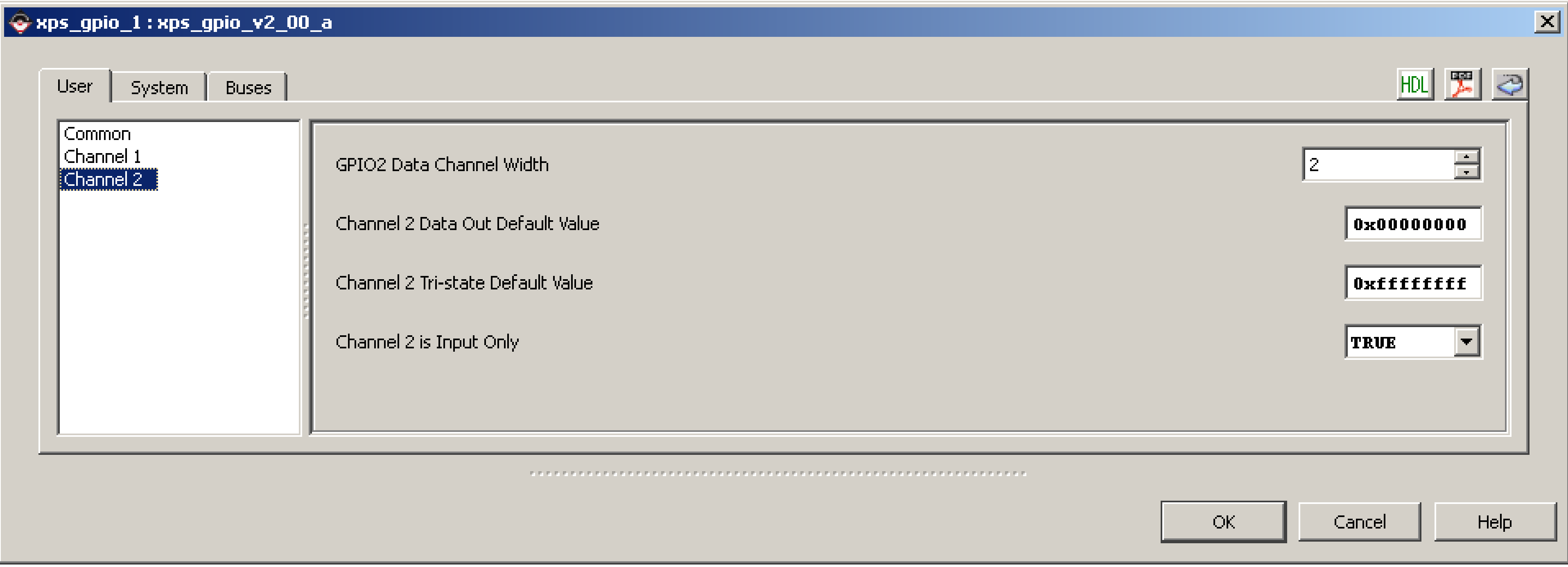
Channel 1 Tri-state Default Value: 0xffffffff

Channel 1 is Input Only: TRUE

Note: Presentation applies to the ML507

Configure IP

- **Under the User tab:**
  - Select **Channel 2**
  - Set GPIO2 Data Channel Width to **2** (SMA Diff CLK In)
  - Set Channel 2 is Input Only to **TRUE**



xps_gpio_1 : xps_gpio_v2_00_a

GPIO2 Data Channel Width: 2

Channel 2 Data Out Default Value: 0x00000000

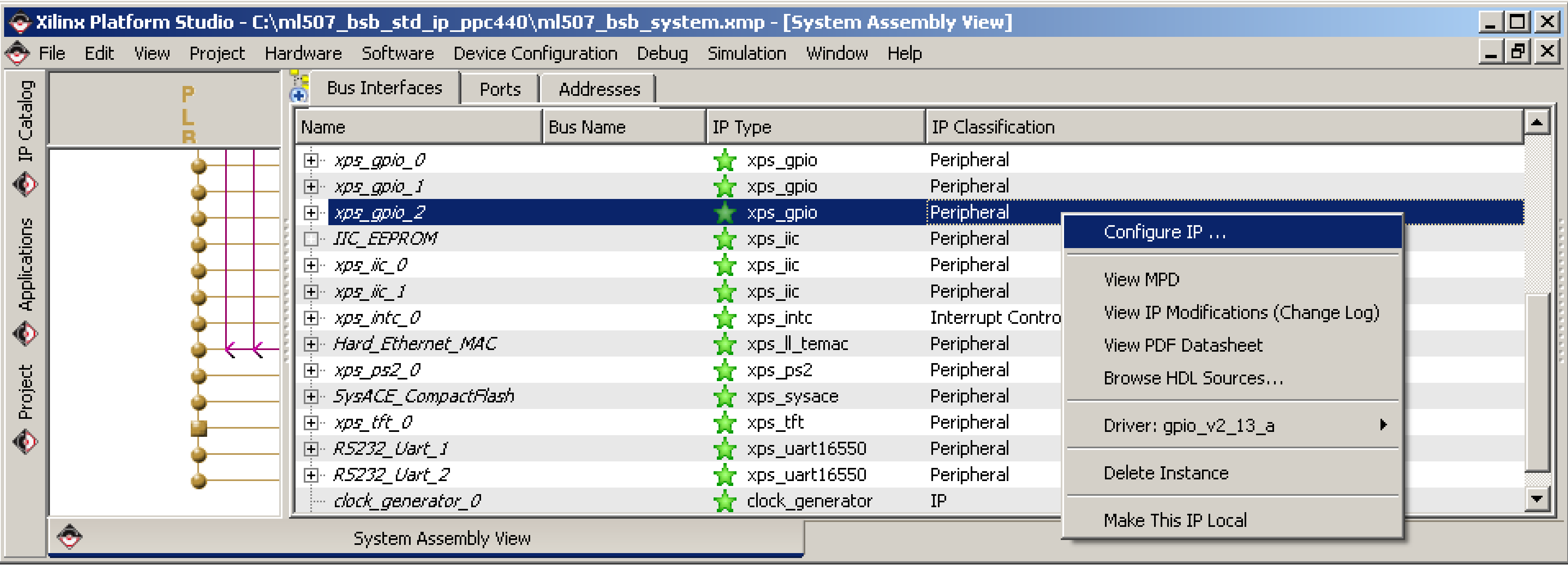
Channel 2 Tri-state Default Value: 0xffffffff

Channel 2 is Input Only: TRUE

Note: Presentation applies to the ML507

Configure IP

- **Configure the GPIO IP**
  - Right-click on the **xps_gpio_2**
  - Select **Configure IP…**

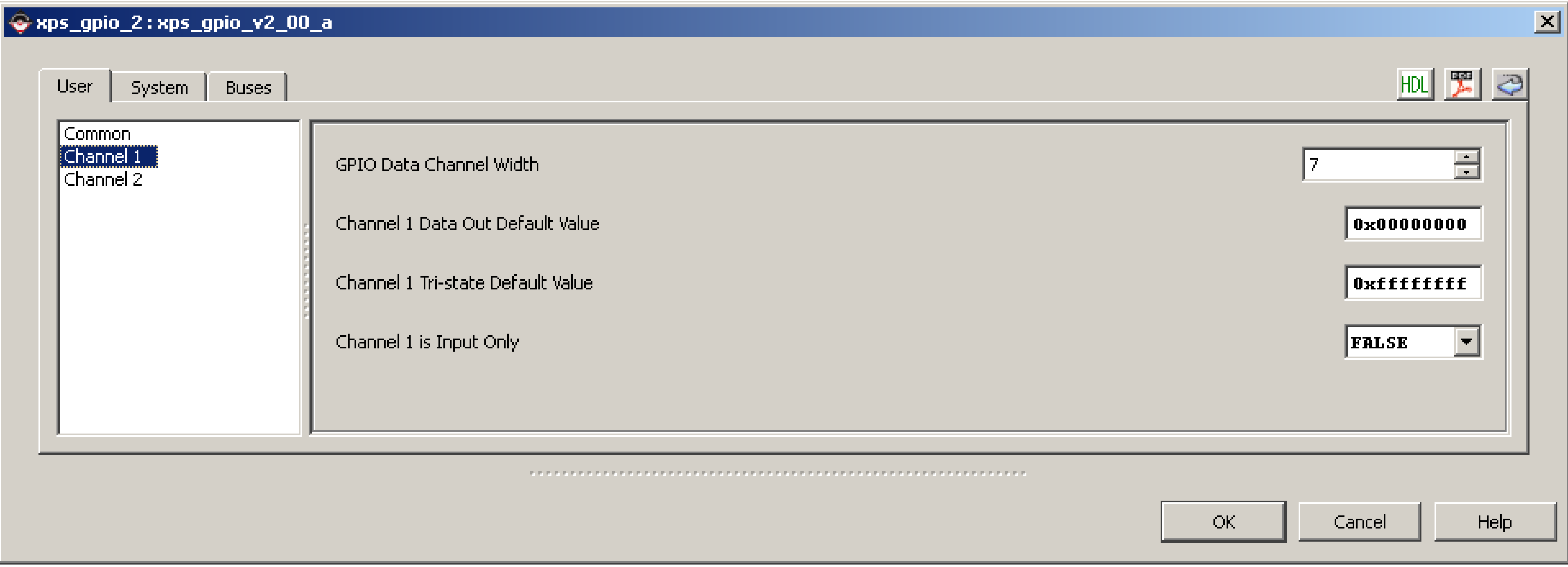


Name	Bus Name	IP Type	IP Classification
xps_gpio_0		xps_gpio	Peripheral
xps_gpio_1		xps_gpio	Peripheral
xps_gpio_2		xps_gpio	Peripheral
IIC_EEPROM		xps_iic	Peripheral
xps_iic_0		xps_iic	Peripheral
xps_iic_1		xps_iic	Peripheral
xps_intc_0		xps_intc	Interrupt Contro
Hard_Ethernet_MAC		xps_ll_temac	Peripheral
xps_ps2_0		xps_ps2	Peripheral
SysACE_CompactFlash		xps_sysace	Peripheral
xps_tft_0		xps_tft	Peripheral
RS232_Uart_1		xps_uart16550	Peripheral
RS232_Uart_2		xps_uart16550	Peripheral
clock_generator_0		clock_generator	IP

Note: Presentation applies to the ML507

Configure IP

- **Under the User tab:**
  - Select **Channel 1**
  - Set GPIO2 Data Channel Width to **7** (LCD Display)



GPIO Data Channel Width: 7

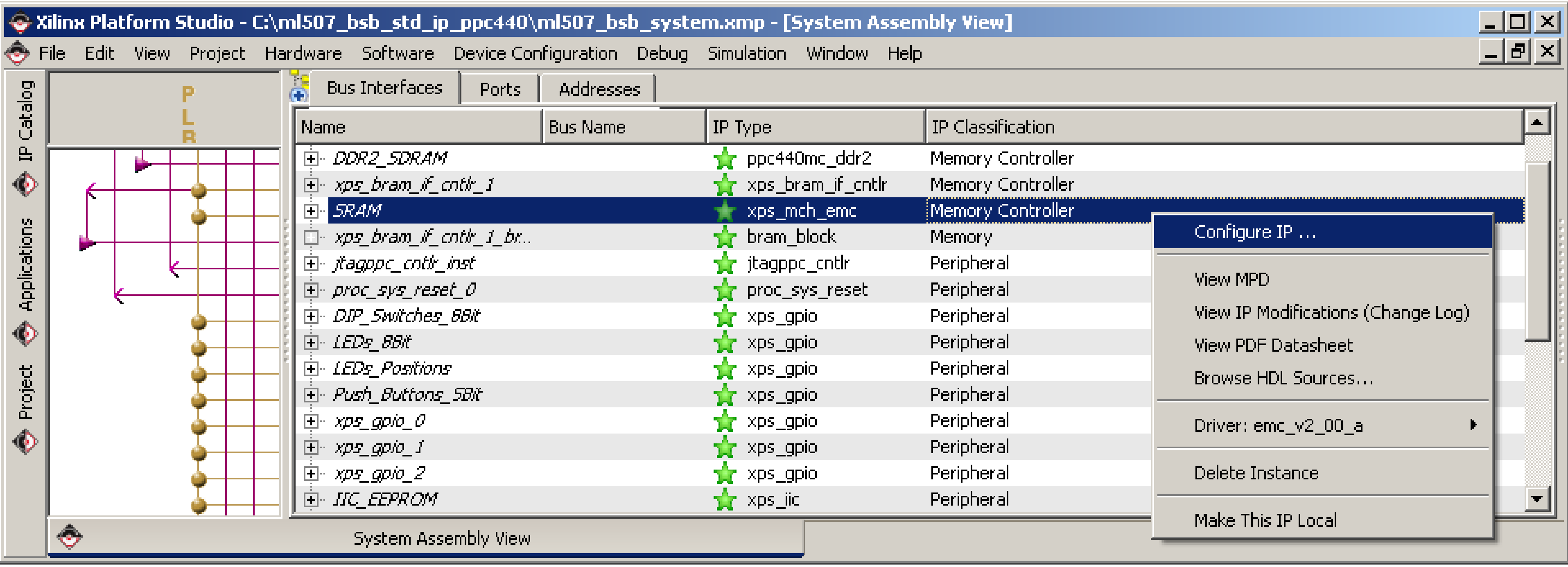
Channel 1 Data Out Default Value: 0x00000000

Channel 1 Tri-state Default Value: 0xffffffff

Channel 1 is Input Only: FALSE

Configure IP

- **Configure the SRAM**
  - Right-click on the **SRAM**
  - Select **Configure IP…**

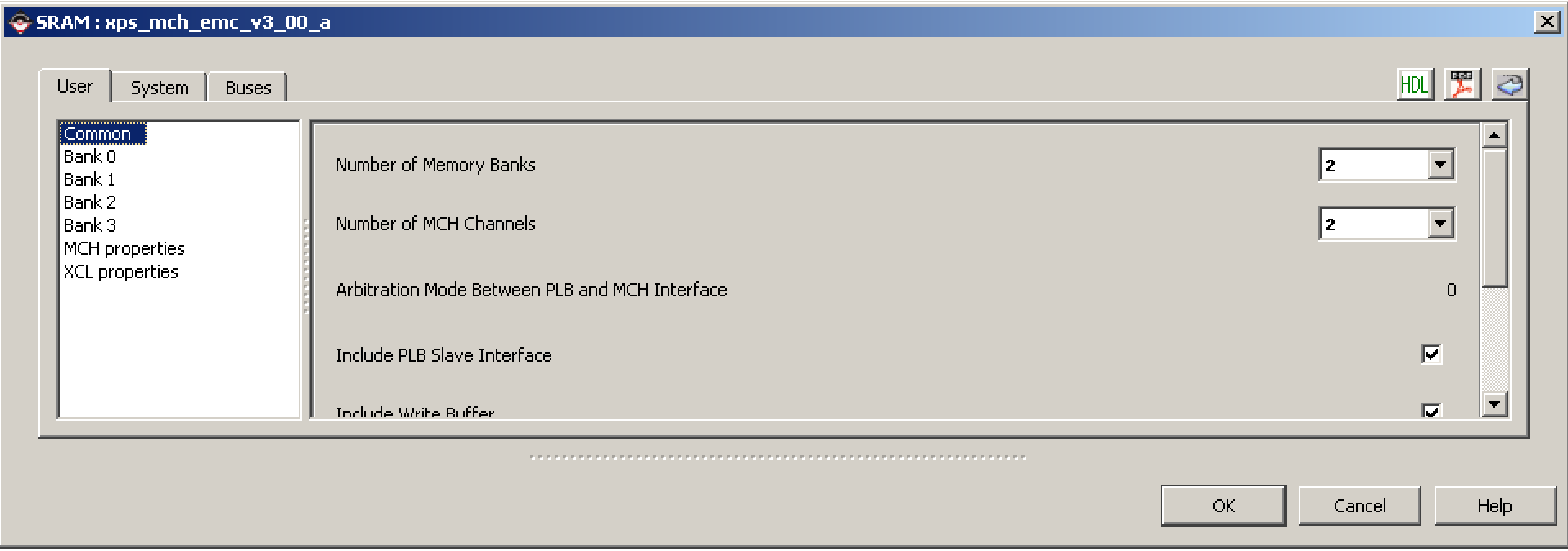


Name	Bus Name	IP Type	IP Classification
DDR2_SDRAM		ppc440mc_ddr2	Memory Controller
xps_bram_if_cntlr_1		xps_bram_if_cntlr	Memory Controller
SRAM		xps_mch_emc	Memory Controller
xps_bram_if_cntlr_1_br..		bram_block	Memory
jtagppc_cntlr_inst		jtagppc_cntlr	Peripheral
proc_sys_reset_0		proc_sys_reset	Peripheral
DIP_Switches_8Bit		xps_gpio	Peripheral
LEDs_8Bit		xps_gpio	Peripheral
LEDs_Positions		xps_gpio	Peripheral
Push_Buttons_5Bit		xps_gpio	Peripheral
xps_gpio_0		xps_gpio	Peripheral
xps_gpio_1		xps_gpio	Peripheral
xps_gpio_2		xps_gpio	Peripheral
IIC_EEPROM		xps_iic	Peripheral

Note: Presentation applies to the ML507

Configure IP

- **Under the User tab:**
  - Select **Common**
  - Set Number of Memory Banks to **2**
  - Set number of MCH Channels to **2**



SRAM : xps_mch_emc_v3_00_a

Number of Memory Banks: 2

Number of MCH Channels: 2

Arbitration Mode Between PLB and MCH Interface: 0

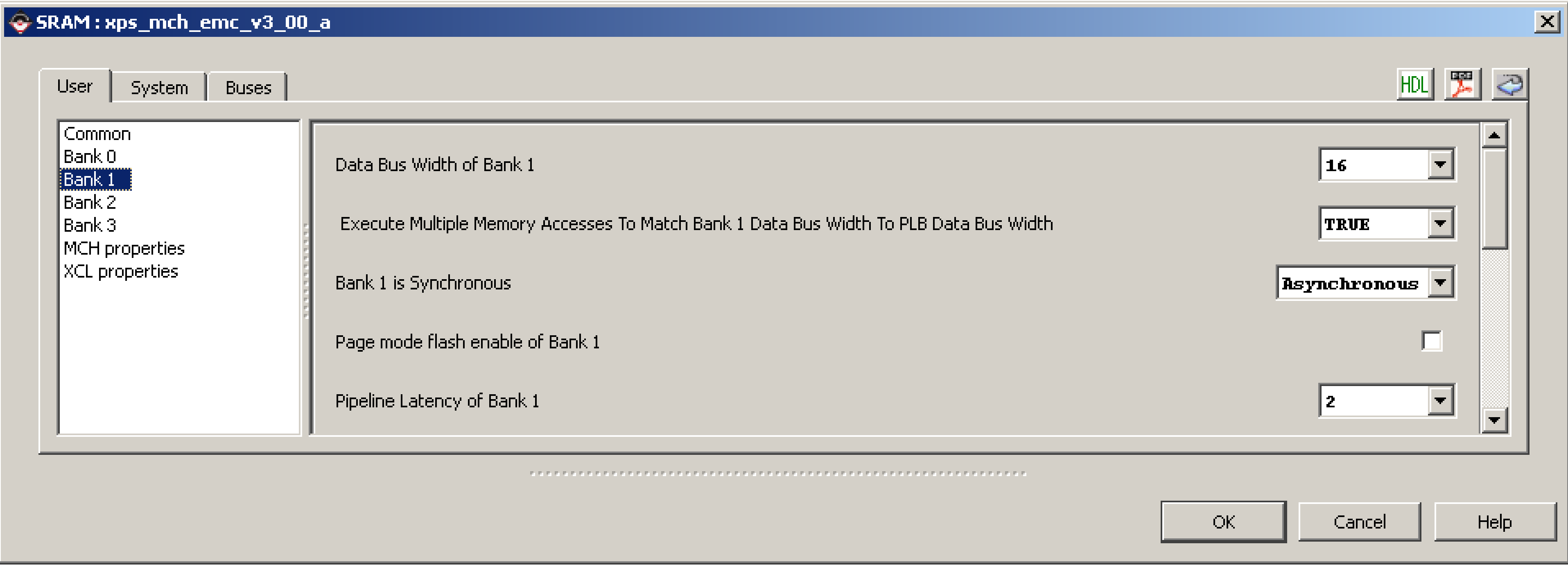
Include PLB Slave Interface ☑

Include Write Buffer ☑

Note: Presentation applies to the ML507

Configure IP

- **Under the User tab:**
  - Select **Bank 1**
  - Set Data Bus Width of Bank 1 to **16**
  - Set Data Width Matching to **True**



SRAM : xps_mch_emc_v3_00_a

Data Bus Width of Bank 1: 16

Execute Multiple Memory Accesses To Match Bank 1 Data Bus Width To PLB Data Bus Width: TRUE

Bank 1 is Synchronous: Asynchronous

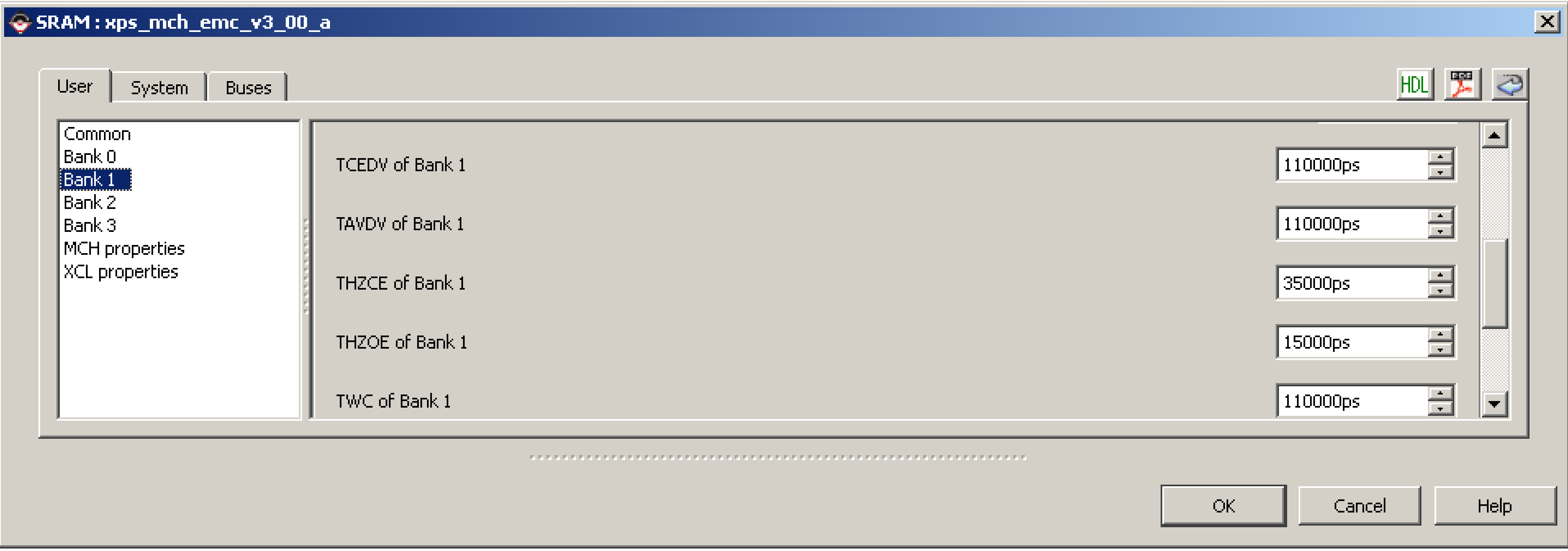
Page mode flash enable of Bank 1: □

Pipeline Latency of Bank 1: 2

Note: Presentation applies to the ML507

Configure IP

- **Under the User tab, Bank 1:**
  - Set TCEDV and TAVDV to: **110000**
  - Set THZCE to: **35000**
  - Set THZOE to: **15000**
  - Set TWC to: **110000**



SRAM : xps_mch_emc_v3_00_a

TCEDV of Bank 1: 110000ps

TAVDV of Bank 1: 110000ps

THZCE of Bank 1: 35000ps

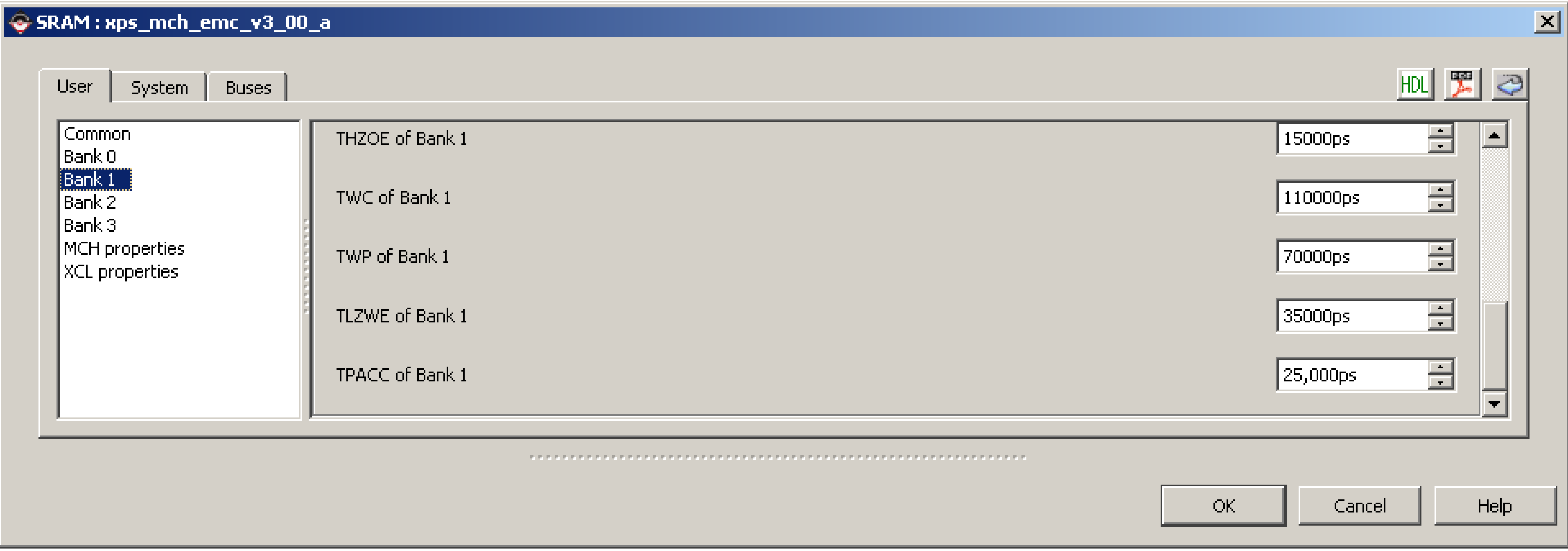
THZOE of Bank 1: 15000ps

TWC of Bank 1: 110000ps

Note: Presentation applies to the ML507

Configure IP

- **Under the User tab, Bank 1:**
  - Set TWP to: **70000**
  - Set TLZWE to: **35000**



SRAM : xps_mch_emc_v3_00_a

THZOE of Bank 1 15000ps

TWC of Bank 1 110000ps

TWP of Bank 1 70000ps

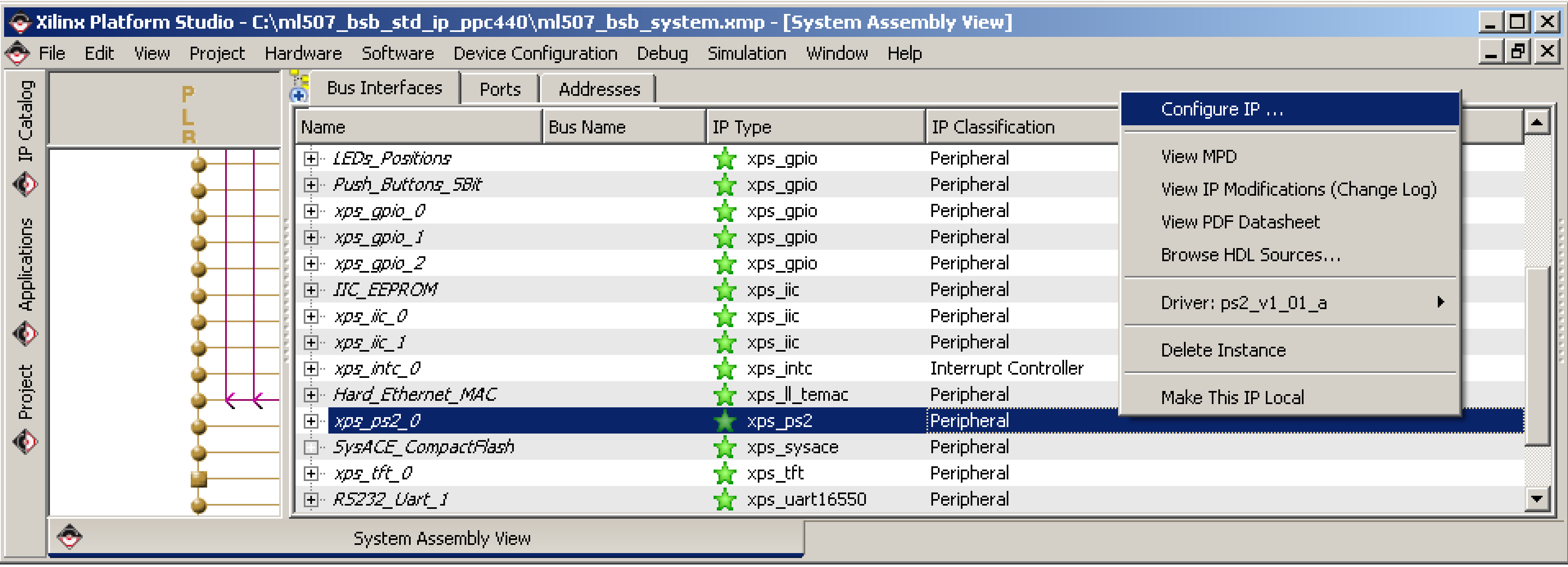
TLZWE of Bank 1 35000ps

TPACC of Bank 1 25,000ps

Note: Presentation applies to the ML507

Configure IP

- **Configure the PS/2 Interface**
  - Right-click on the **xps_ps2_0**
  - Select **Configure IP…**

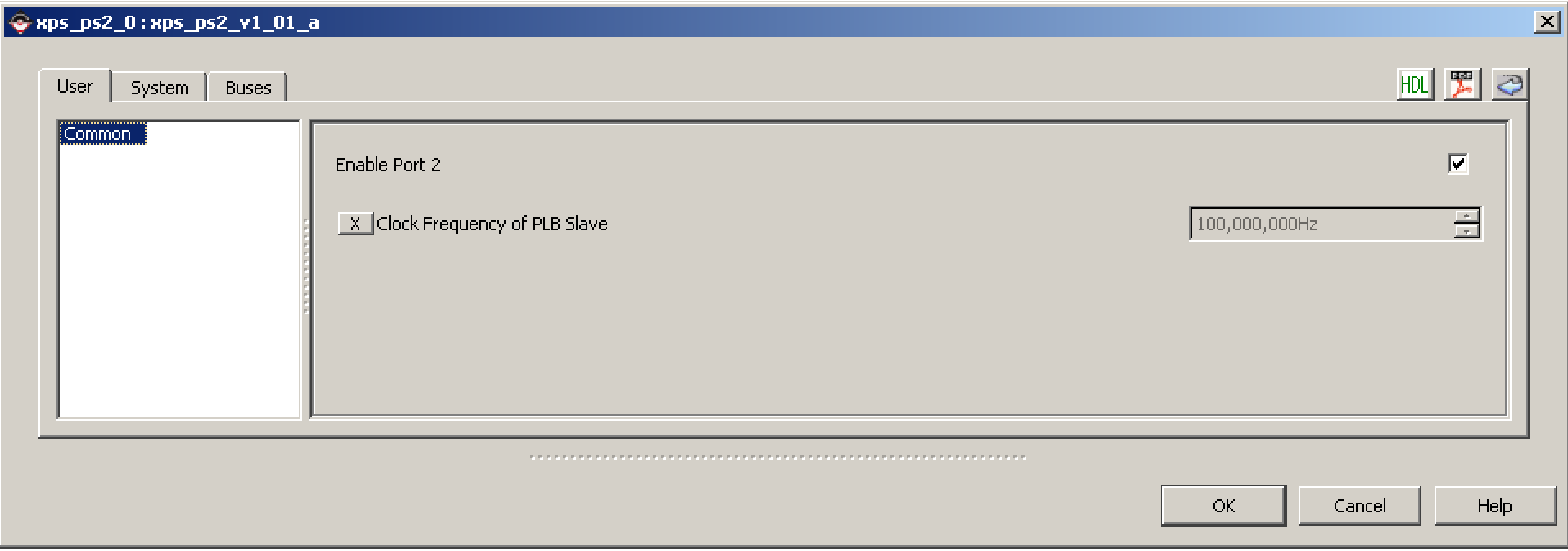


Name	Bus Name	IP Type	IP Classification
LEDs_Positions		xps_gpio	Peripheral
Push_Buttons_5Bit		xps_gpio	Peripheral
xps_gpio_0		xps_gpio	Peripheral
xps_gpio_1		xps_gpio	Peripheral
xps_gpio_2		xps_gpio	Peripheral
IIC_EEPROM		xps_iic	Peripheral
xps_iic_0		xps_iic	Peripheral
xps_iic_1		xps_iic	Peripheral
xps_intc_0		xps_intc	Interrupt Controller
Hard_Ethernet_MAC		xps_ll_temac	Peripheral
xps_ps2_0		xps_ps2	Peripheral
SysACE_CompactFlash		xps_sysace	Peripheral
xps_tft_0		xps_tft	Peripheral
RS232_Uart_1		xps_uart16550	Peripheral

Note: Presentation applies to the ML507

Configure IP

- **Under the User tab:**
  - Select **Common**
  - Check **Enable Port 2**



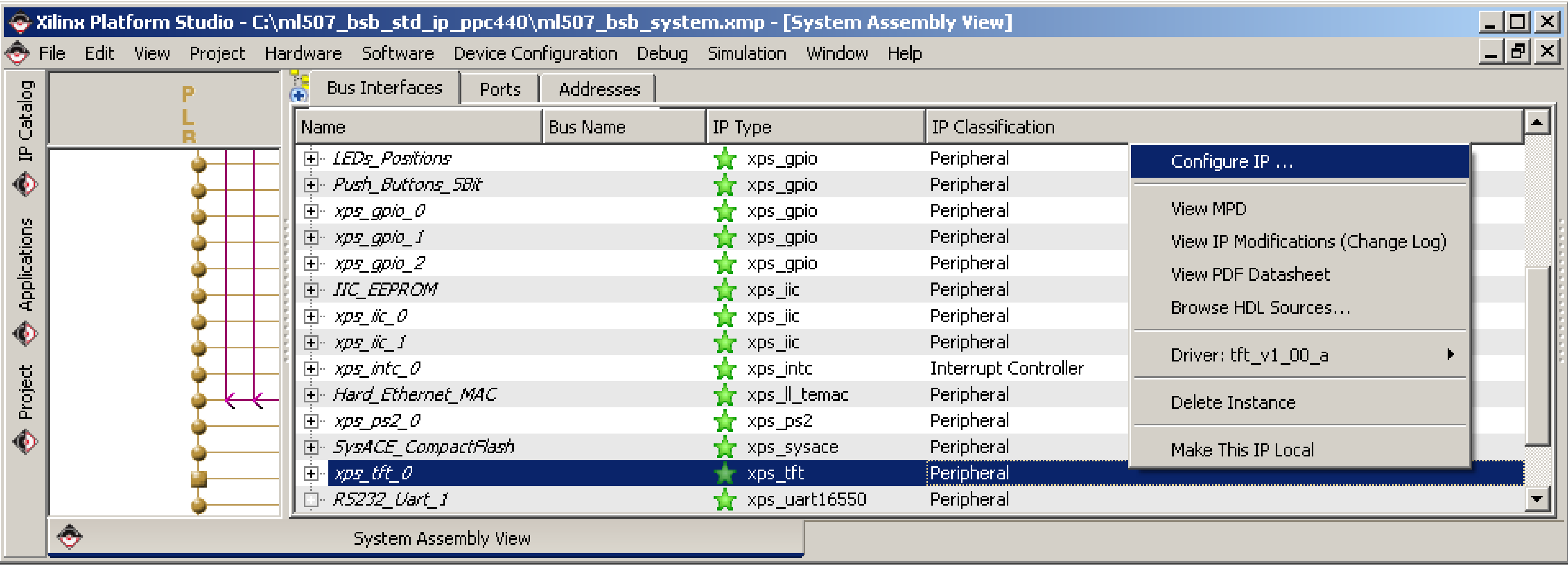
Enable Port 2 ☑

X Clock Frequency of PLB Slave 100,000,000Hz

Note: Presentation applies to the ML507

Configure IP

- **Configure the DVI Interface**
  - Right-click on the **xps_tft_0**
  - Select **Configure IP…**

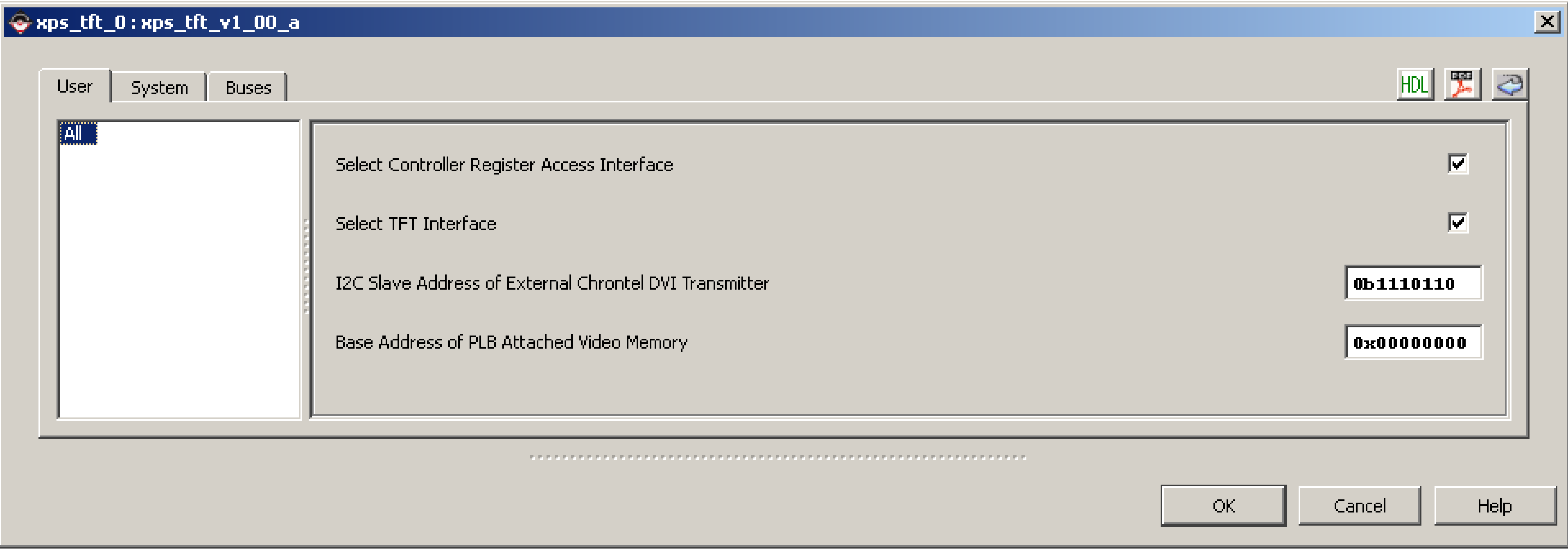


Name	Bus Name	IP Type	IP Classification
LEDs_Positions		xps_gpio	Peripheral
Push_Buttons_5Bit		xps_gpio	Peripheral
xps_gpio_0		xps_gpio	Peripheral
xps_gpio_1		xps_gpio	Peripheral
xps_gpio_2		xps_gpio	Peripheral
IIC_EEPROM		xps_iic	Peripheral
xps_iic_0		xps_iic	Peripheral
xps_iic_1		xps_iic	Peripheral
xps_intc_0		xps_intc	Interrupt Controller
Hard_Ethernet_MAC		xps_ll_temac	Peripheral
xps_ps2_0		xps_ps2	Peripheral
SysACE_CompactFlash		xps_sysace	Peripheral
xps_tft_0		xps_tft	Peripheral
RS232_Uart_1		xps_uart16550	Peripheral

Note: Presentation applies to the ML507

Configure IP

- **Under the User tab:**
  - Select **All**
  - Set Base Address of PLB Attached Video Memory to **0x00000000**



Select Controller Register Access Interface ☑

Select TFT Interface ☑

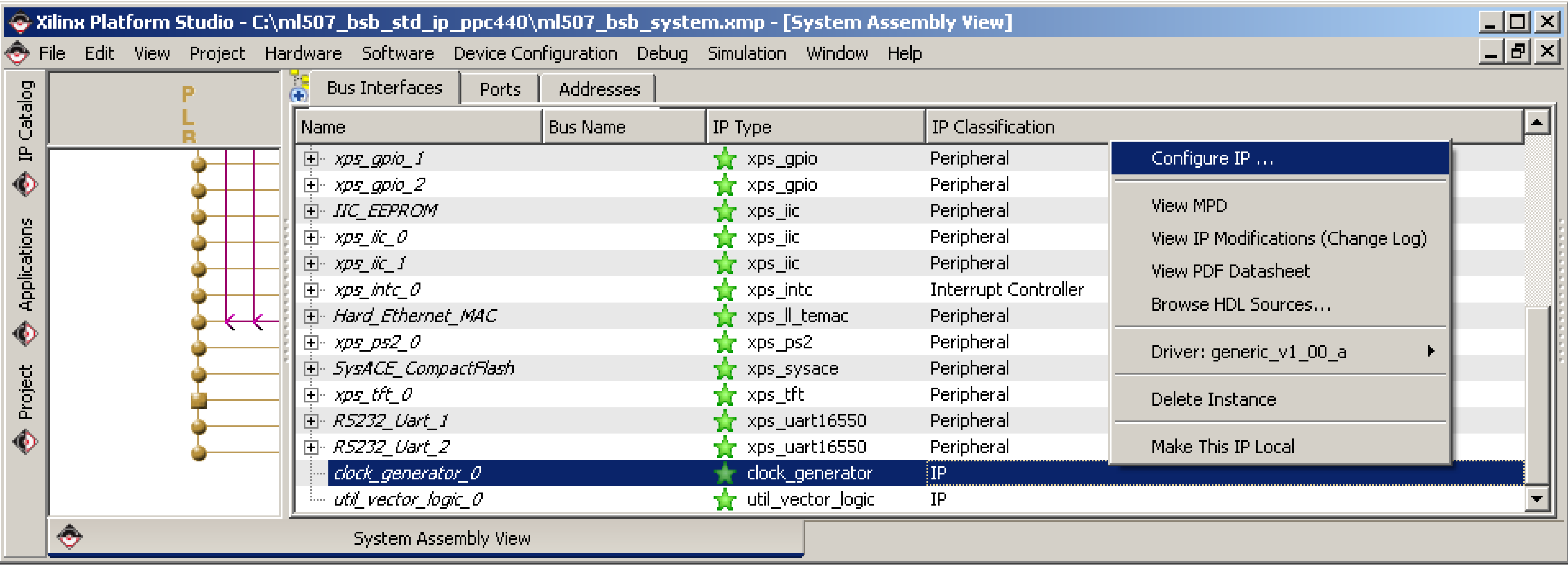
I2C Slave Address of External Chrontel DVI Transmitter 0b1110110

Base Address of PLB Attached Video Memory 0x00000000

Note: Presentation applies to the ML507

Configure IP

- **Configure the Clock Generator**
  - Select the Bus Interfaces Tab
  - Right-click on the **clock_generator**
  - Select **Configure IP…**

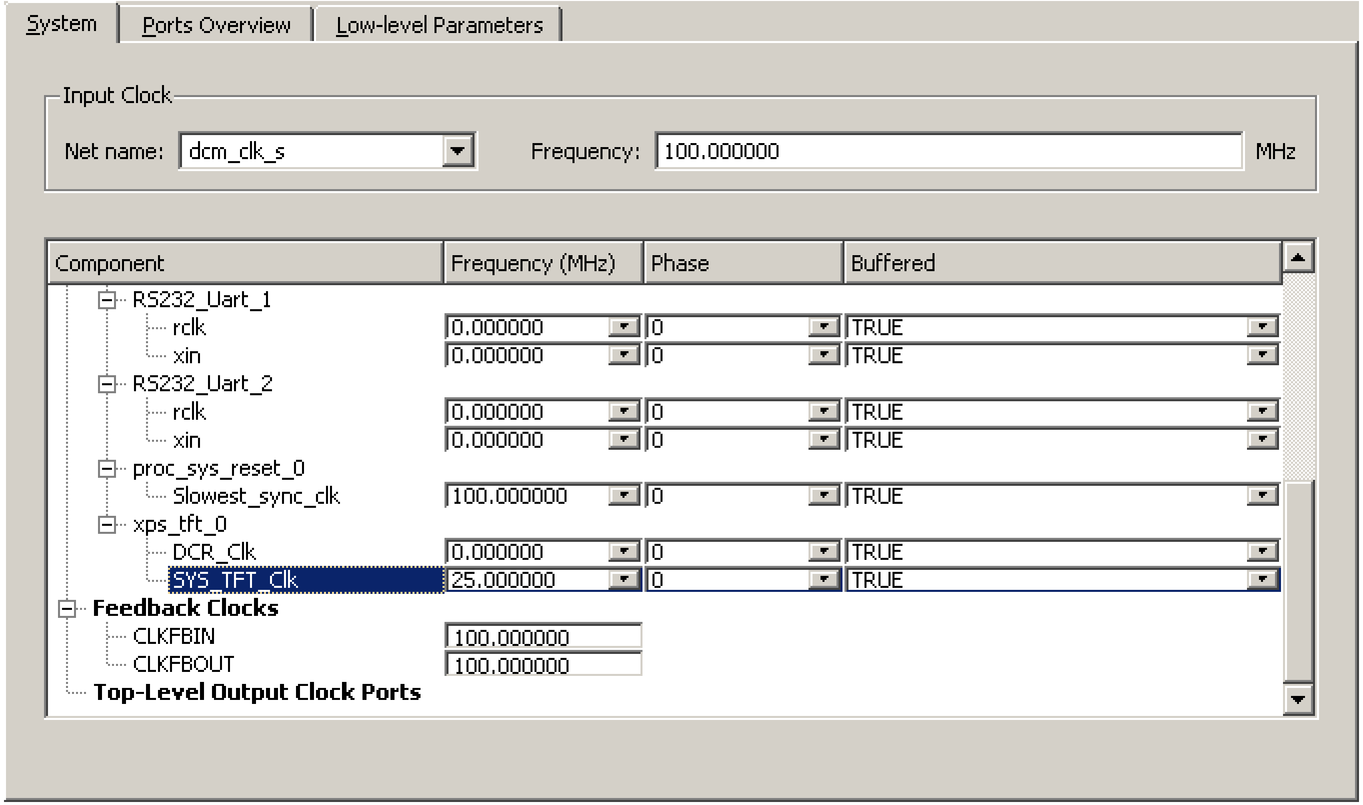

Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp - [System Assembly View]
File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help
IP Catalog
Applications
Project
Bus Interfaces
Ports
Addresses
Configure IP ...
View MPD
View IP Modifications (Change Log)
View PDF Datasheet
Browse HDL Sources...
Driver: generic_v1_00_a
Delete Instance
Make This IP Local
System Assembly View

Name	Bus Name	IP Type	IP Classification
xps_gpio_1		xps_gpio	Peripheral
xps_gpio_2		xps_gpio	Peripheral
IIC_EEPROM		xps_iic	Peripheral
xps_iic_0		xps_iic	Peripheral
xps_iic_1		xps_iic	Peripheral
xps_intc_0		xps_intc	Interrupt Controller
Hard_Ethernet_MAC		xps_ll_temac	Peripheral
xps_ps2_0		xps_ps2	Peripheral
SysACE_CompactFlash		xps_sysace	Peripheral
xps_tft_0		xps_tft	Peripheral
RS232_Uart_1		xps_uart16550	Peripheral
RS232_Uart_2		xps_uart16550	Peripheral
clock_generator_0		clock_generator	IP
util_vector_logic_0		util_vector_logic	IP

Note: Presentation applies to the ML507

Configure IP

- **Under the System tab:**
  - Select **xps_tft_0 → SYS_TFT_Clk**
  - Set the frequency to **25 MHz**



Input Clock

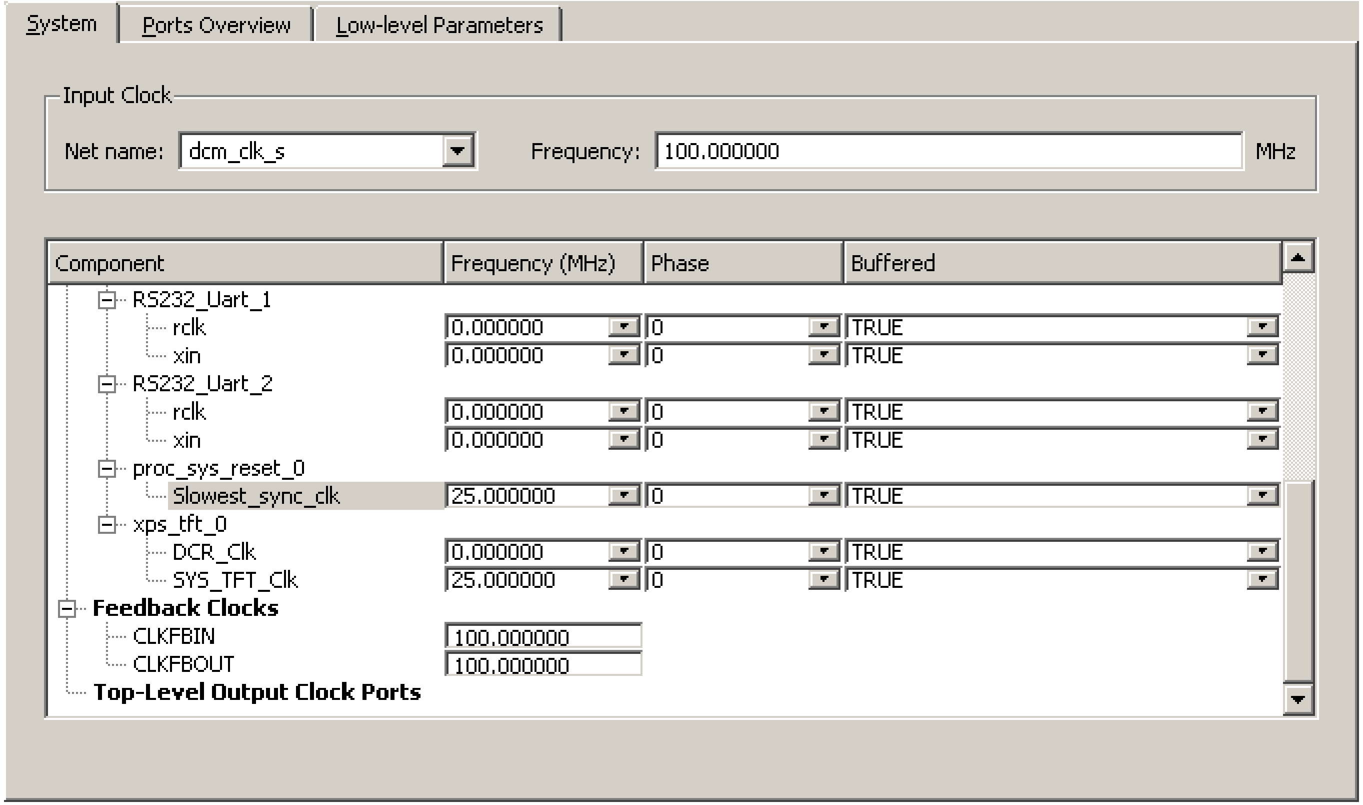
Net name: dcm_clk_s   Frequency: 100.000000 MHz

Component	Frequency (MHz)	Phase	Buffered
RS232_Uart_1			
rclk	0.000000	0	TRUE
xin	0.000000	0	TRUE
RS232_Uart_2			
rclk	0.000000	0	TRUE
xin	0.000000	0	TRUE
proc_sys_reset_0			
Slowest_sync_clk	100.000000	0	TRUE
xps_tft_0			
DCR_Clk	0.000000	0	TRUE
SYS_TFT_Clk	25.000000	0	TRUE
Feedback Clocks			
CLKFBIN	100.000000		
CLKFBOUT	100.000000		
Top-Level Output Clock Ports			

Note: Presentation applies to the ML507

Configure IP

- **Under the System tab:**
  - Select **proc_sys_reset_0 → Slowest_sync_clk**
  - Set the frequency to **25 MHz**



Input Clock

Net name: dcm_clk_s

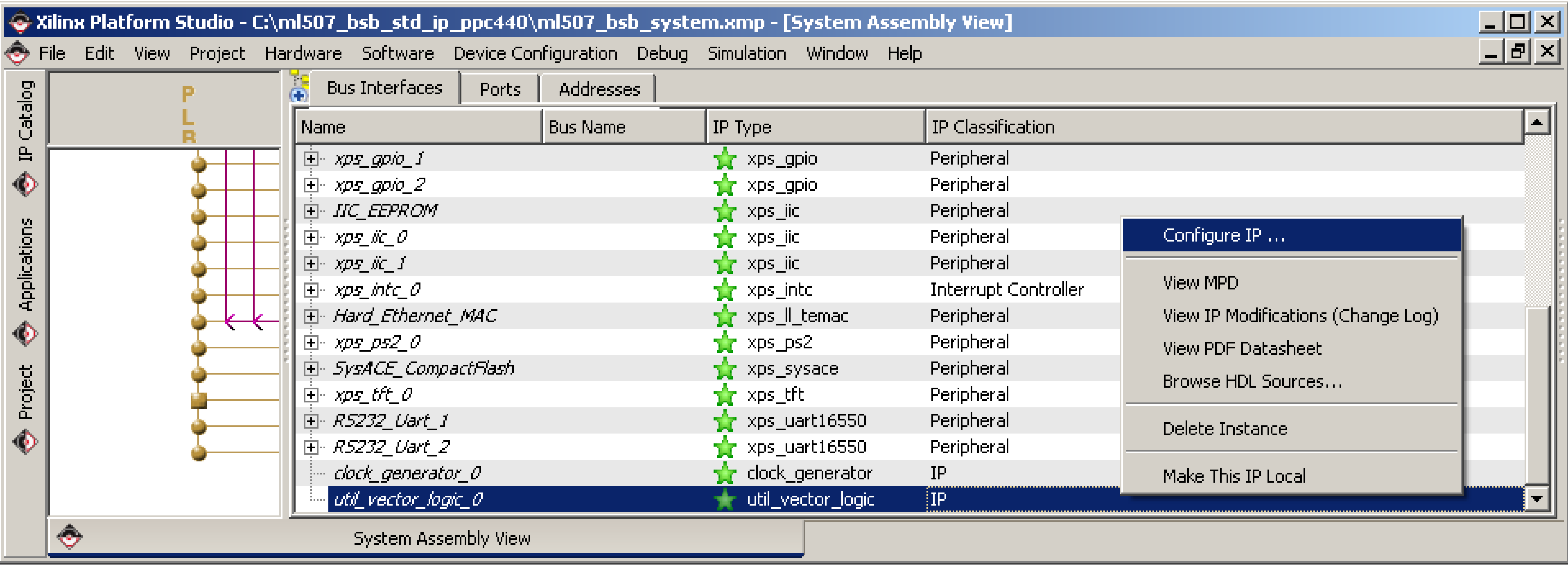
Frequency: 100.000000 MHz

Component	Frequency (MHz)	Phase	Buffered
RS232_Uart_1			
rclk	0.000000	0	TRUE
xin	0.000000	0	TRUE
RS232_Uart_2			
rclk	0.000000	0	TRUE
xin	0.000000	0	TRUE
proc_sys_reset_0			
Slowest_sync_clk	25.000000	0	TRUE
xps_tft_0			
DCR_Clk	0.000000	0	TRUE
SYS_TFT_Clk	25.000000	0	TRUE
Feedback Clocks			
CLKFBIN	100.000000		
CLKFBOUT	100.000000		
Top-Level Output Clock Ports			

Note: Presentation applies to the ML507

Configure IP

- **Configure the Utility Vector Logic**
  - Right-click on the **util_vector_logic_0**
  - Select **Configure IP…**



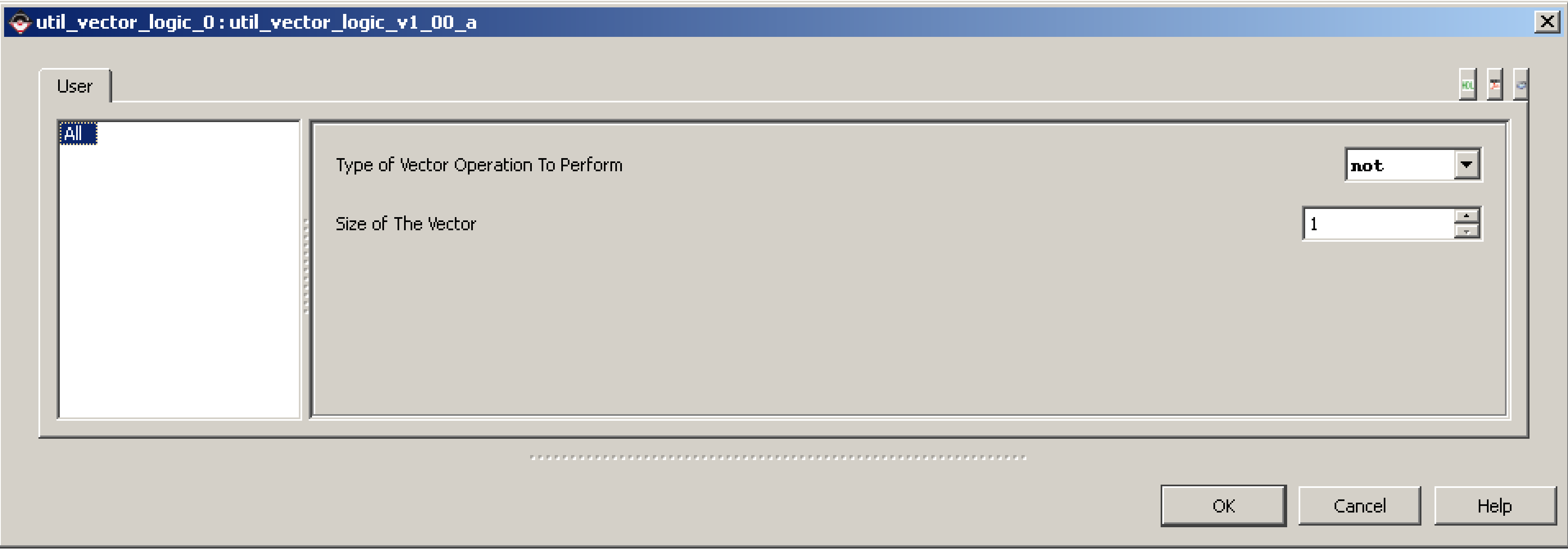
Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp - [System Assembly View]

Name	Bus Name	IP Type	IP Classification
xps_gpio_1		xps_gpio	Peripheral
xps_gpio_2		xps_gpio	Peripheral
IIC_EEPROM		xps_iic	Peripheral
xps_iic_0		xps_iic	Peripheral
xps_iic_1		xps_iic	Peripheral
xps_intc_0		xps_intc	Interrupt Controller
Hard_Ethernet_MAC		xps_ll_temac	Peripheral
xps_ps2_0		xps_ps2	Peripheral
SysACE_CompactFlash		xps_sysace	Peripheral
xps_tft_0		xps_tft	Peripheral
RS232_Uart_1		xps_uart16550	Peripheral
RS232_Uart_2		xps_uart16550	Peripheral
clock_generator_0		clock_generator	IP
util_vector_logic_0		util_vector_logic	IP

Note: Presentation applies to the ML507

Configure IP

- **Under the User tab:**
  - Select **All**
  - Set Type of Vector Operation To Perform to **not**
  - Set Size of The Vector to **1**



util_vector_logic_0 : util_vector_logic_v1_00_a

User

All

Type of Vector Operation To Perform: not

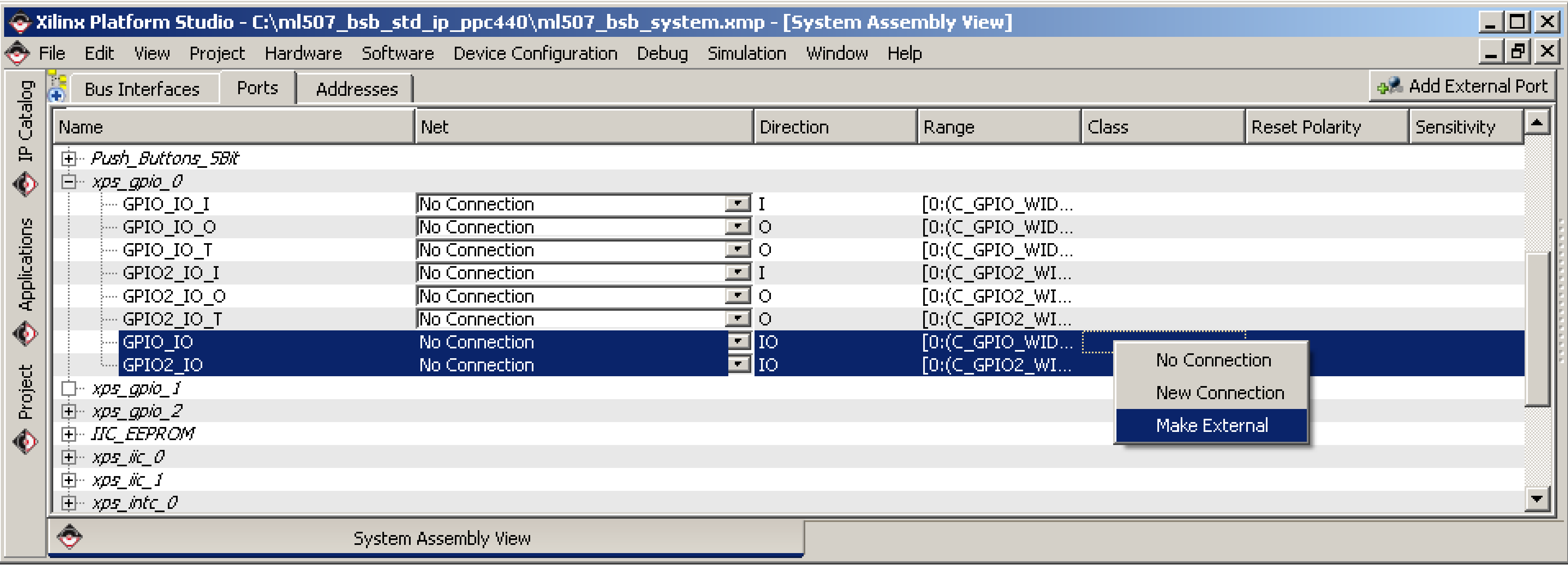
Size of The Vector: 1

Note: Presentation applies to the ML507

Connect IP Ports

Connect Ports

- **Select the Ports tab**
- **Expand this instance:**
  - **xps_gpio_0**
  - Select **Make External** for the **GPIO_IO** and **GPIO2_IO** ports

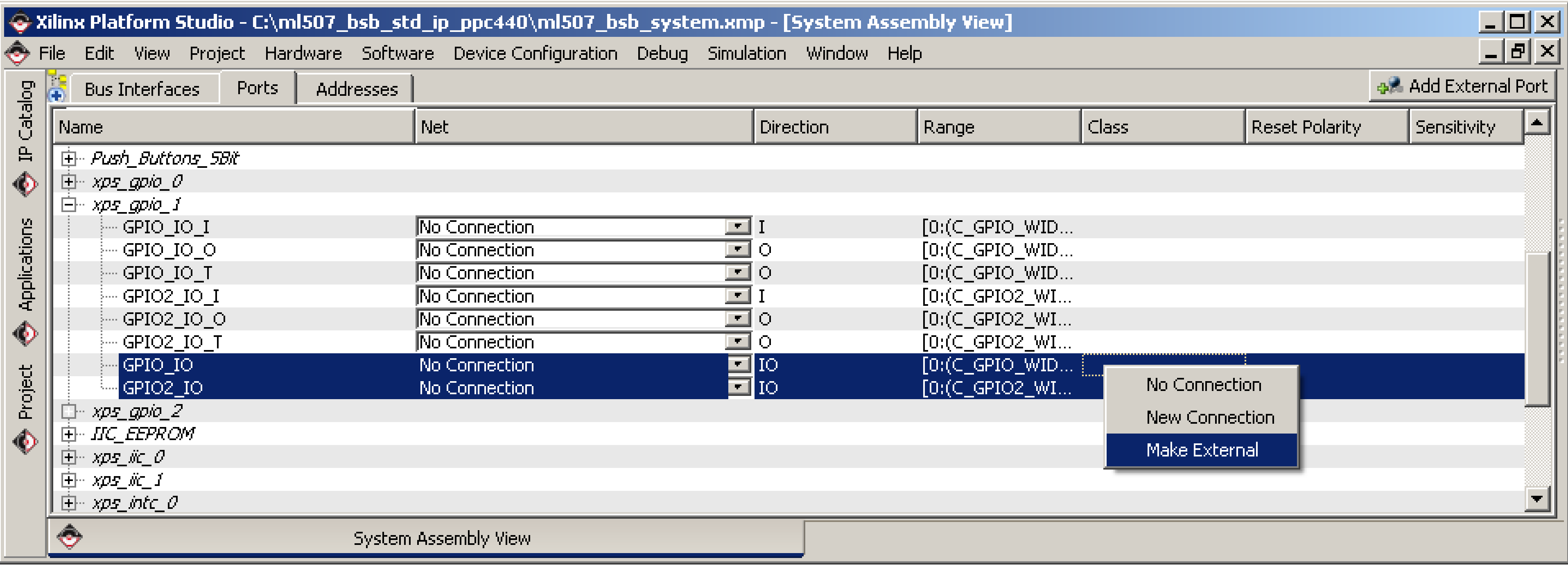


Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
Push_Buttons_5Bit						
xps_gpio_0						
GPIO_IO_I	No Connection	I	[0:(C_GPIO_WID...			
GPIO_IO_O	No Connection	O	[0:(C_GPIO_WID...			
GPIO_IO_T	No Connection	O	[0:(C_GPIO_WID...			
GPIO2_IO_I	No Connection	I	[0:(C_GPIO2_WI...			
GPIO2_IO_O	No Connection	O	[0:(C_GPIO2_WI...			
GPIO2_IO_T	No Connection	O	[0:(C_GPIO2_WI...			
GPIO_IO	No Connection	IO	[0:(C_GPIO_WID...			
GPIO2_IO	No Connection	IO	[0:(C_GPIO2_WI...			
xps_gpio_1						
xps_gpio_2						
IIC_EEPROM						
xps_iic_0						
xps_iic_1						
xps_intc_0						

Note: Presentation applies to the ML507

Connect Ports

- **Expand this instance:**
  - **xps_gpio_1**
  - Select **Make External** for the **GPIO_IO** and **GPIO2_IO** ports

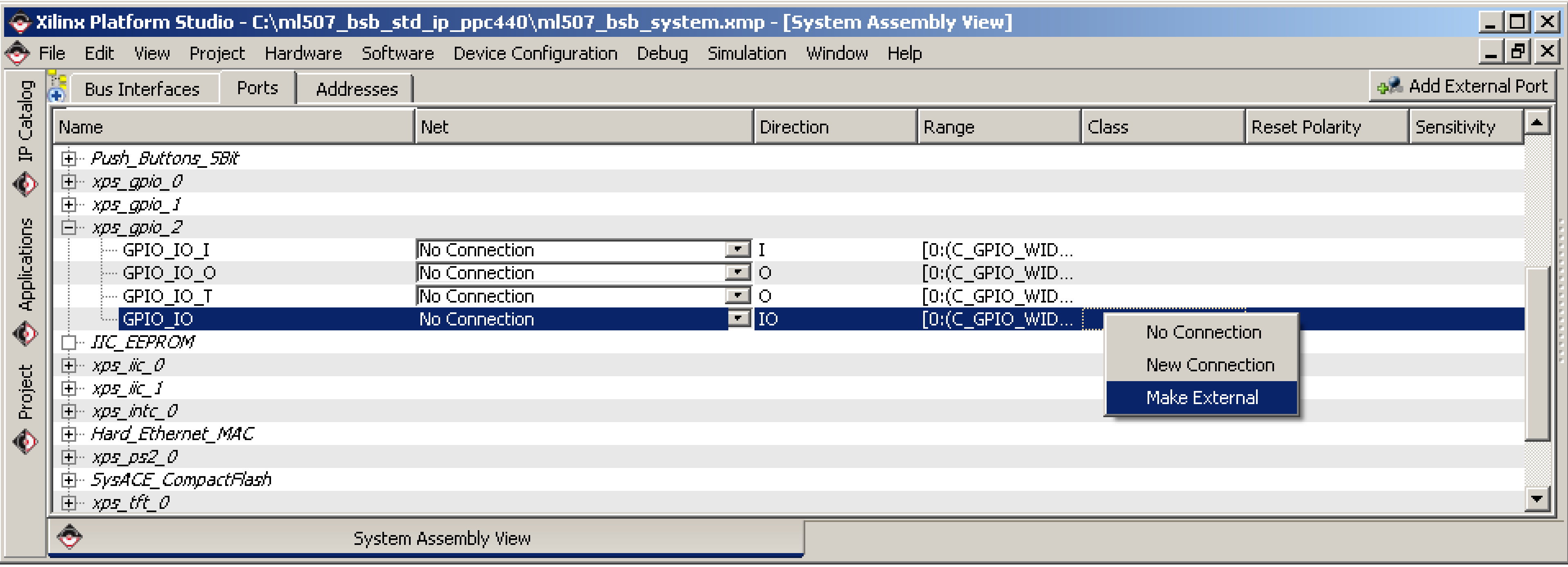


Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
Push_Buttons_5Bit						
xps_gpio_0						
xps_gpio_1						
GPIO_IO_I	No Connection	I	[0:(C_GPIO_WID...			
GPIO_IO_O	No Connection	O	[0:(C_GPIO_WID...			
GPIO_IO_T	No Connection	O	[0:(C_GPIO_WID...			
GPIO2_IO_I	No Connection	I	[0:(C_GPIO2_WI...			
GPIO2_IO_O	No Connection	O	[0:(C_GPIO2_WI...			
GPIO2_IO_T	No Connection	O	[0:(C_GPIO2_WI...			
GPIO_IO	No Connection	IO	[0:(C_GPIO_WID...			
GPIO2_IO	No Connection	IO	[0:(C_GPIO2_WI...			
xps_gpio_2						
IIC_EEPROM						
xps_iic_0						
xps_iic_1						
xps_intc_0						

Note: Presentation applies to the ML507

Connect Ports

- **Expand this instance:**
  - **xps_gpio_2**
  - Select **Make External** for the **GPIO_IO** port



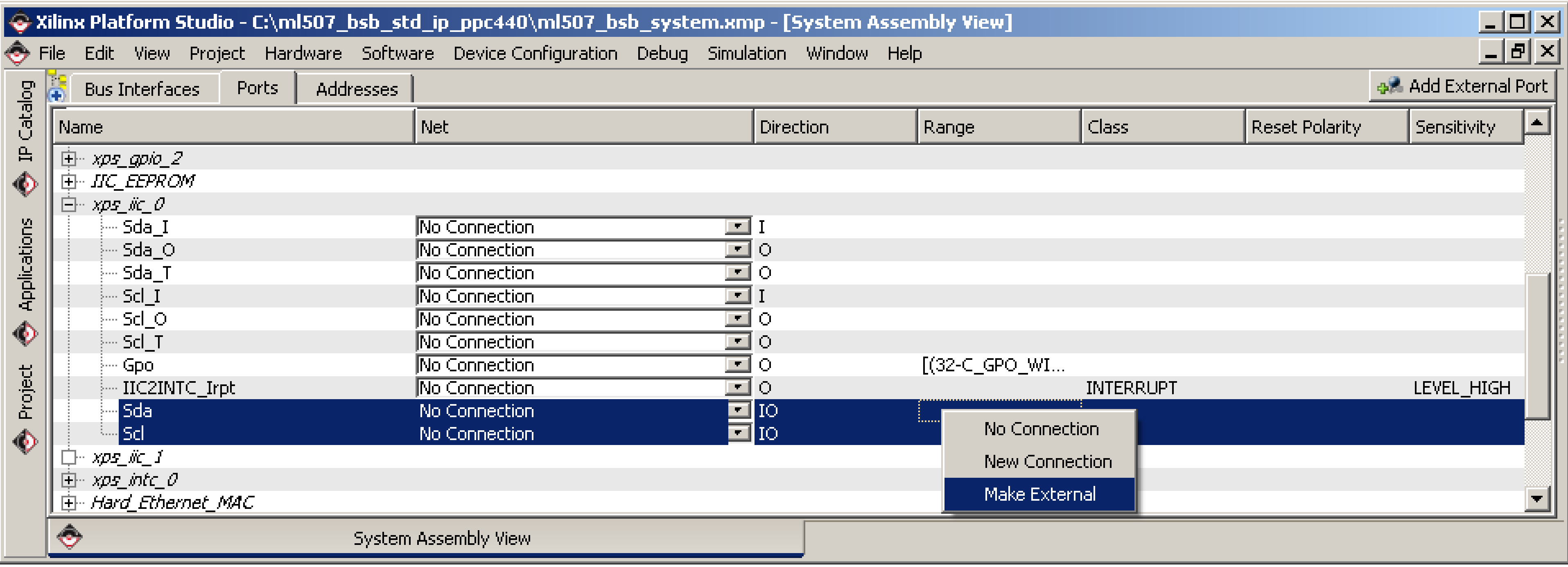
Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp - [System Assembly View]

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
⊞ *Push_Buttons_5Bit*						
⊞ *xps_gpio_0*						
⊞ *xps_gpio_1*						
⊟ *xps_gpio_2*						
GPIO_IO_I	No Connection	I	[0:(C_GPIO_WID...			
GPIO_IO_O	No Connection	O	[0:(C_GPIO_WID...			
GPIO_IO_T	No Connection	O	[0:(C_GPIO_WID...			
GPIO_IO	No Connection	IO	[0:(C_GPIO_WID...			
□ *IIC_EEPROM*						
⊞ *xps_iic_0*						
⊞ *xps_iic_1*						
⊞ *xps_intc_0*						
⊞ *Hard_Ethernet_MAC*						
⊞ *xps_ps2_0*						
⊞ *SysACE_CompactFlash*						
⊞ *xps_tft_0*						

Note: Presentation applies to the ML507

Connect Ports

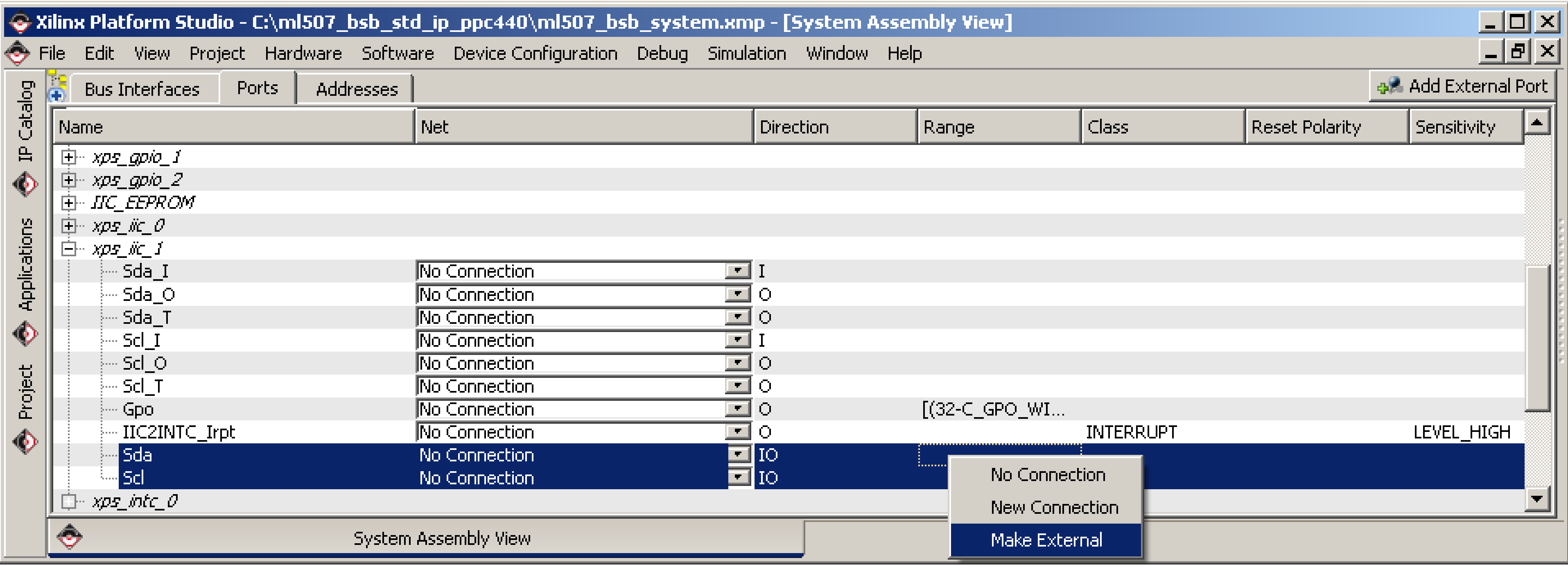
- **Expand this instance:**
  - **xps_iic_0**
  - Select **Make External** for the **Sda** and **Scl** ports



Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
xps_gpio_2						
IIC_EEPROM						
xps_iic_0						
Sda_I	No Connection	I				
Sda_O	No Connection	O				
Sda_T	No Connection	O				
Scl_I	No Connection	I				
Scl_O	No Connection	O				
Scl_T	No Connection	O				
Gpo	No Connection	O	[(32-C_GPO_WI...			
IIC2INTC_Irpt	No Connection	O		INTERRUPT		LEVEL_HIGH
Sda	No Connection	IO				
Scl	No Connection	IO				
xps_iic_1						
xps_intc_0						
Hard_Ethernet_MAC						

Connect Ports

- **Expand this instance:**
  - **xps_iic_1**
  - Select **Make External** for the **Sda** and **Scl** ports



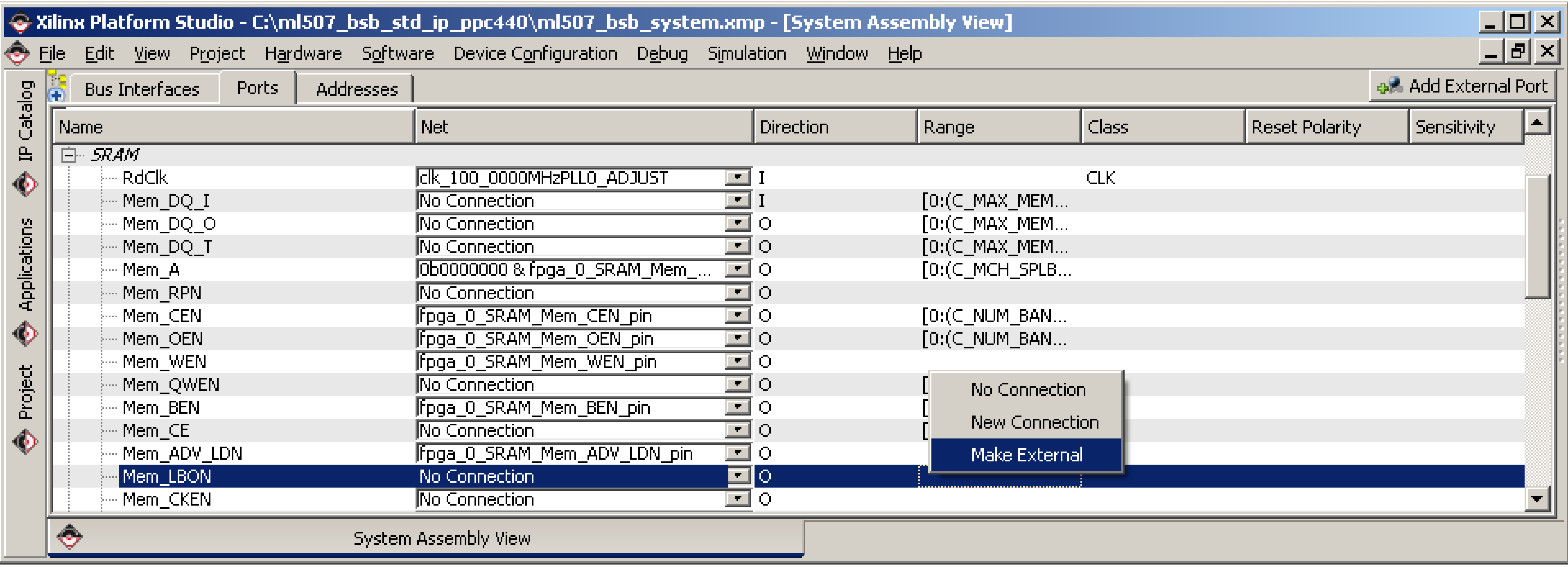
Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp - [System Assembly View]

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
⊞ *xps_gpio_1*						
⊞ *xps_gpio_2*						
⊞ *IIC_EEPROM*						
⊞ *xps_iic_0*						
⊟ *xps_iic_1*						
Sda_I	No Connection	I				
Sda_O	No Connection	O				
Sda_T	No Connection	O				
Scl_I	No Connection	I				
Scl_O	No Connection	O				
Scl_T	No Connection	O				
Gpo	No Connection	O	[(32-C_GPO_WI...			
IIC2INTC_Irpt	No Connection	O		INTERRUPT		LEVEL_HIGH
Sda	No Connection	IO				
Scl	No Connection	IO				
⊞ *xps_intc_0*						

Note: Presentation applies to the ML507

Connect Ports

- **Expand this instance:**
  - **SRAM**
  - Select **Make External** for the **Mem_LBON** port


Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp - [System Assembly View]
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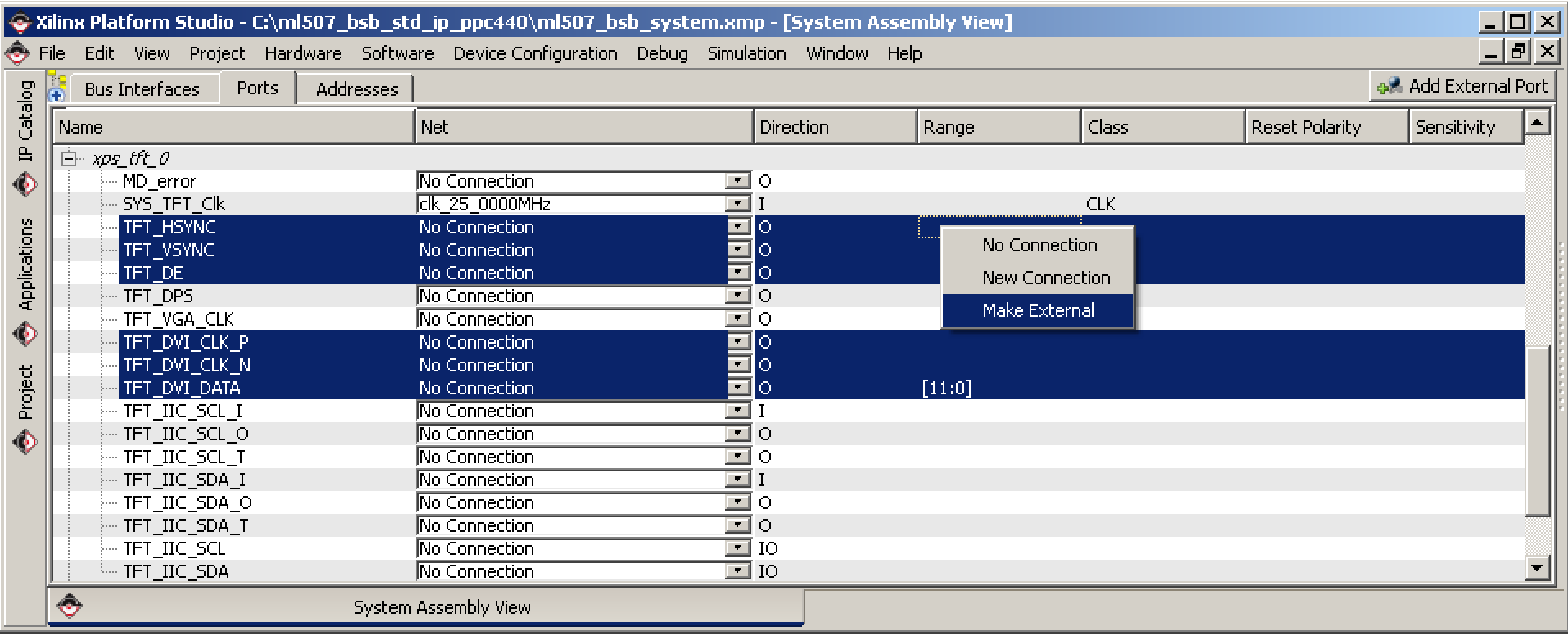
No Connection
New Connection
Make External
System Assembly View

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
SRAM						
RdClk	clk_100_0000MHzPLL0_ADJUST	I		CLK		
Mem_DQ_I	No Connection	I	[0:(C_MAX_MEM...			
Mem_DQ_O	No Connection	O	[0:(C_MAX_MEM...			
Mem_DQ_T	No Connection	O	[0:(C_MAX_MEM...			
Mem_A	0b0000000 & fpga_0_SRAM_Mem_...	O	[0:(C_MCH_SPLB...			
Mem_RPN	No Connection	O				
Mem_CEN	fpga_0_SRAM_Mem_CEN_pin	O	[0:(C_NUM_BAN...			
Mem_OEN	fpga_0_SRAM_Mem_OEN_pin	O	[0:(C_NUM_BAN...			
Mem_WEN	fpga_0_SRAM_Mem_WEN_pin	O				
Mem_QWEN	No Connection	O	[			
Mem_BEN	fpga_0_SRAM_Mem_BEN_pin	O	[			
Mem_CE	No Connection	O	[			
Mem_ADV_LDN	fpga_0_SRAM_Mem_ADV_LDN_pin	O				
Mem_LBON	No Connection	O				
Mem_CKEN	No Connection	O				

Note: Presentation applies to the ML507

Connect Ports

- **Expand this instance:**
  - **xps_tft_0**
  - Select **Make External** for **TFT_HSYNC**, **TFT_VSYNC**, **TFT_DE**, **TFT_DVI_CLK_P**, **TFT_DVI_CLK_N**, and **TFT_DVI_DATA**

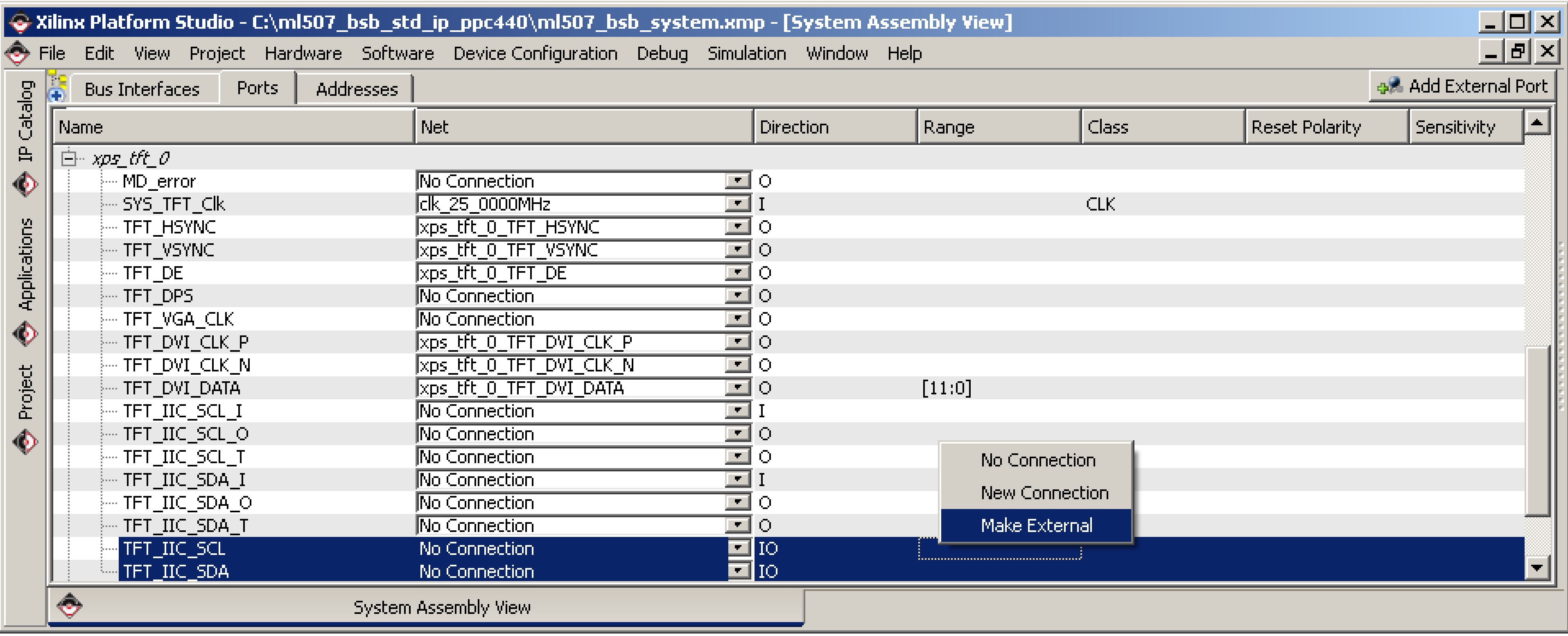


Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
xps_tft_0						
MD_error	No Connection	O				
SYS_TFT_Clk	clk_25_0000MHz	I		CLK		
TFT_HSYNC	No Connection	O				
TFT_VSYNC	No Connection	O				
TFT_DE	No Connection	O				
TFT_DPS	No Connection	O				
TFT_VGA_CLK	No Connection	O				
TFT_DVI_CLK_P	No Connection	O				
TFT_DVI_CLK_N	No Connection	O				
TFT_DVI_DATA	No Connection	O	[11:0]			
TFT_IIC_SCL_I	No Connection	I				
TFT_IIC_SCL_O	No Connection	O				
TFT_IIC_SCL_T	No Connection	O				
TFT_IIC_SDA_I	No Connection	I				
TFT_IIC_SDA_O	No Connection	O				
TFT_IIC_SDA_T	No Connection	O				
TFT_IIC_SCL	No Connection	IO				
TFT_IIC_SDA	No Connection	IO				

Note: Presentation applies to the ML507

Connect Ports

- **For instance xps_tft_0:**
  - Select **Make External** for **TFT_IIC_SCL** and **TFT_IIC_SDA** ports


Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp - [System Assembly View]
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No Connection
New Connection
Make External
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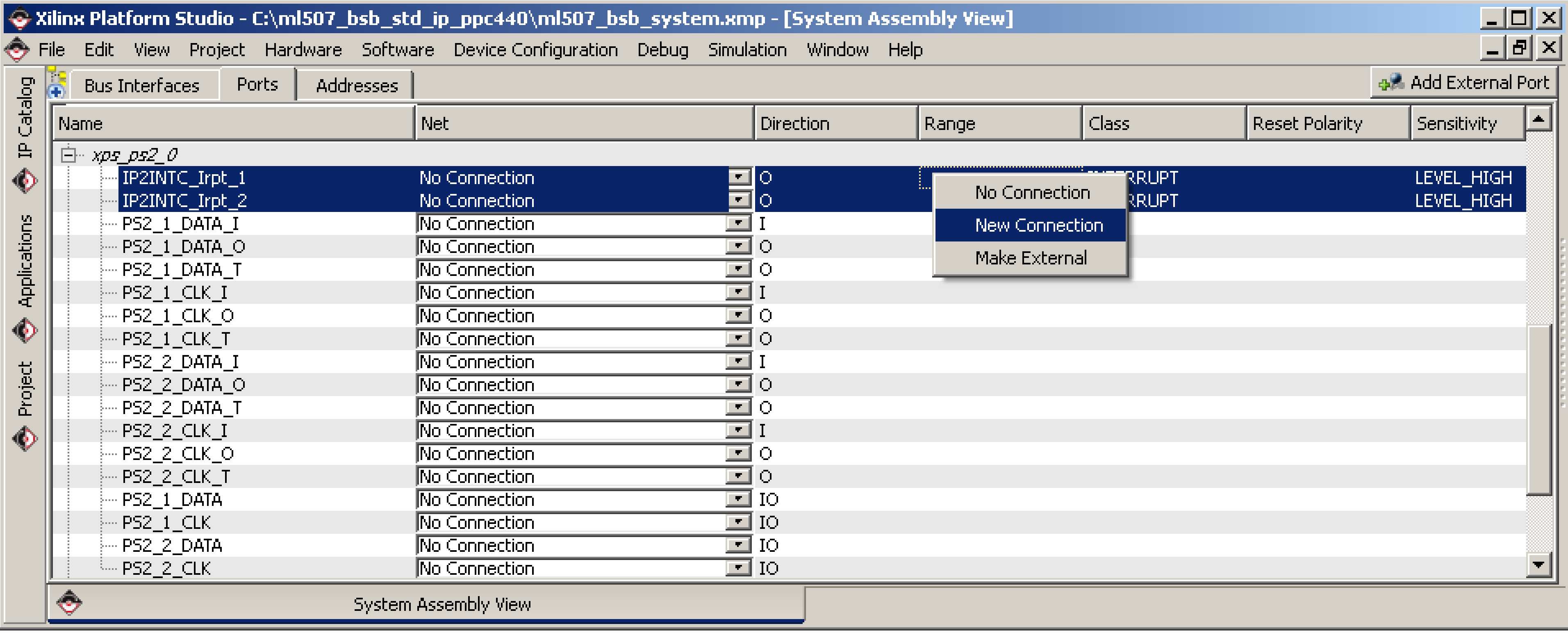
Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
xps_tft_0						
MD_error	No Connection	O				
SYS_TFT_Clk	clk_25_0000MHz	I		CLK		
TFT_HSYNC	xps_tft_0_TFT_HSYNC	O				
TFT_VSYNC	xps_tft_0_TFT_VSYNC	O				
TFT_DE	xps_tft_0_TFT_DE	O				
TFT_DPS	No Connection	O				
TFT_VGA_CLK	No Connection	O				
TFT_DVI_CLK_P	xps_tft_0_TFT_DVI_CLK_P	O				
TFT_DVI_CLK_N	xps_tft_0_TFT_DVI_CLK_N	O				
TFT_DVI_DATA	xps_tft_0_TFT_DVI_DATA	O	[11:0]			
TFT_IIC_SCL_I	No Connection	I				
TFT_IIC_SCL_O	No Connection	O				
TFT_IIC_SCL_T	No Connection	O				
TFT_IIC_SDA_I	No Connection	I				
TFT_IIC_SDA_O	No Connection	O				
TFT_IIC_SDA_T	No Connection	O				
TFT_IIC_SCL	No Connection	IO				
TFT_IIC_SDA	No Connection	IO				

Note: Presentation applies to the ML507

Connect Ports

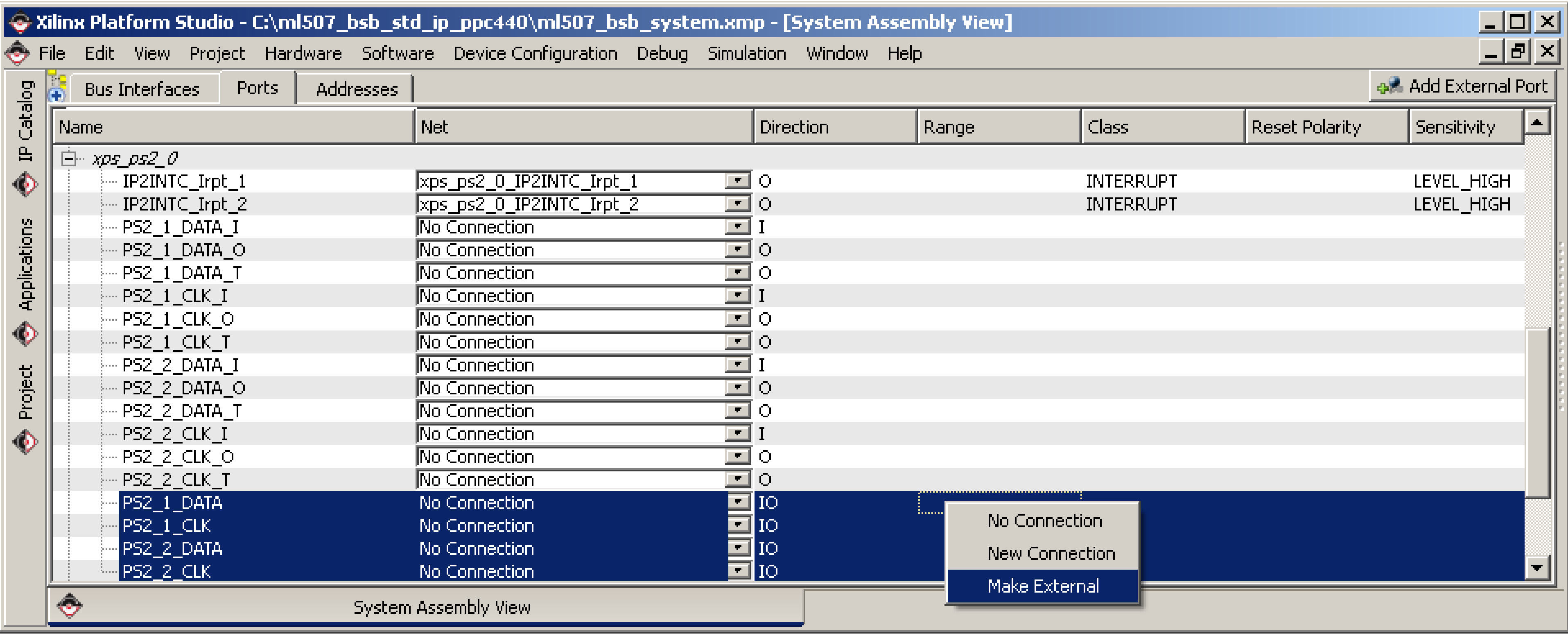
- **Expand this instance:**
  - **xps_ps2_0**
  - Select **New Connection** for **IP2INTC_Irpt_1** and **IP2INTC_Irpt_2** ports



Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
xps_ps2_0						
IP2INTC_Irpt_1	No Connection	O		RRUPT		LEVEL_HIGH
IP2INTC_Irpt_2	No Connection	O		RRUPT		LEVEL_HIGH
PS2_1_DATA_I	No Connection	I				
PS2_1_DATA_O	No Connection	O				
PS2_1_DATA_T	No Connection	O				
PS2_1_CLK_I	No Connection	I				
PS2_1_CLK_O	No Connection	O				
PS2_1_CLK_T	No Connection	O				
PS2_2_DATA_I	No Connection	I				
PS2_2_DATA_O	No Connection	O				
PS2_2_DATA_T	No Connection	O				
PS2_2_CLK_I	No Connection	I				
PS2_2_CLK_O	No Connection	O				
PS2_2_CLK_T	No Connection	O				
PS2_1_DATA	No Connection	IO				
PS2_1_CLK	No Connection	IO				
PS2_2_DATA	No Connection	IO				
PS2_2_CLK	No Connection	IO				

Connect Ports

- **For instance xps_ps2_0:**
  - Select **Make External** for **PS2_1_DATA**, **PS2_1_CLK**, **PS2_2_DATA**, and **PS2_2_CLK** ports

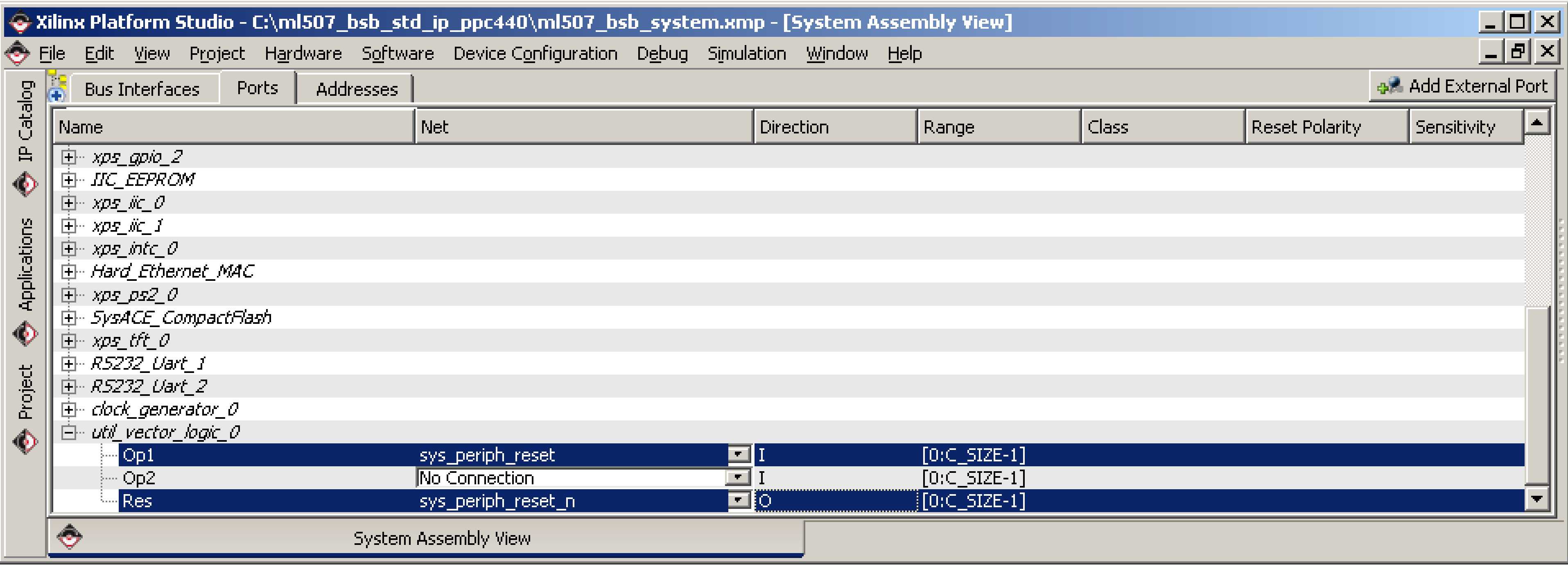


Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
xps_ps2_0						
IP2INTC_Irpt_1	xps_ps2_0_IP2INTC_Irpt_1	O		INTERRUPT		LEVEL_HIGH
IP2INTC_Irpt_2	xps_ps2_0_IP2INTC_Irpt_2	O		INTERRUPT		LEVEL_HIGH
PS2_1_DATA_I	No Connection	I				
PS2_1_DATA_O	No Connection	O				
PS2_1_DATA_T	No Connection	O				
PS2_1_CLK_I	No Connection	I				
PS2_1_CLK_O	No Connection	O				
PS2_1_CLK_T	No Connection	O				
PS2_2_DATA_I	No Connection	I				
PS2_2_DATA_O	No Connection	O				
PS2_2_DATA_T	No Connection	O				
PS2_2_CLK_I	No Connection	I				
PS2_2_CLK_O	No Connection	O				
PS2_2_CLK_T	No Connection	O				
PS2_1_DATA	No Connection	IO				
PS2_1_CLK	No Connection	IO				
PS2_2_DATA	No Connection	IO				
PS2_2_CLK	No Connection	IO				

Note: Presentation applies to the ML507

Connect Ports

- **Expand this instance:**
  - **util_vector_logic_0**
  - Connect **Op1** to **sys_periph_reset**
  - Connect **Res** to **sys_periph_reset_n**



Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp - [System Assembly View]
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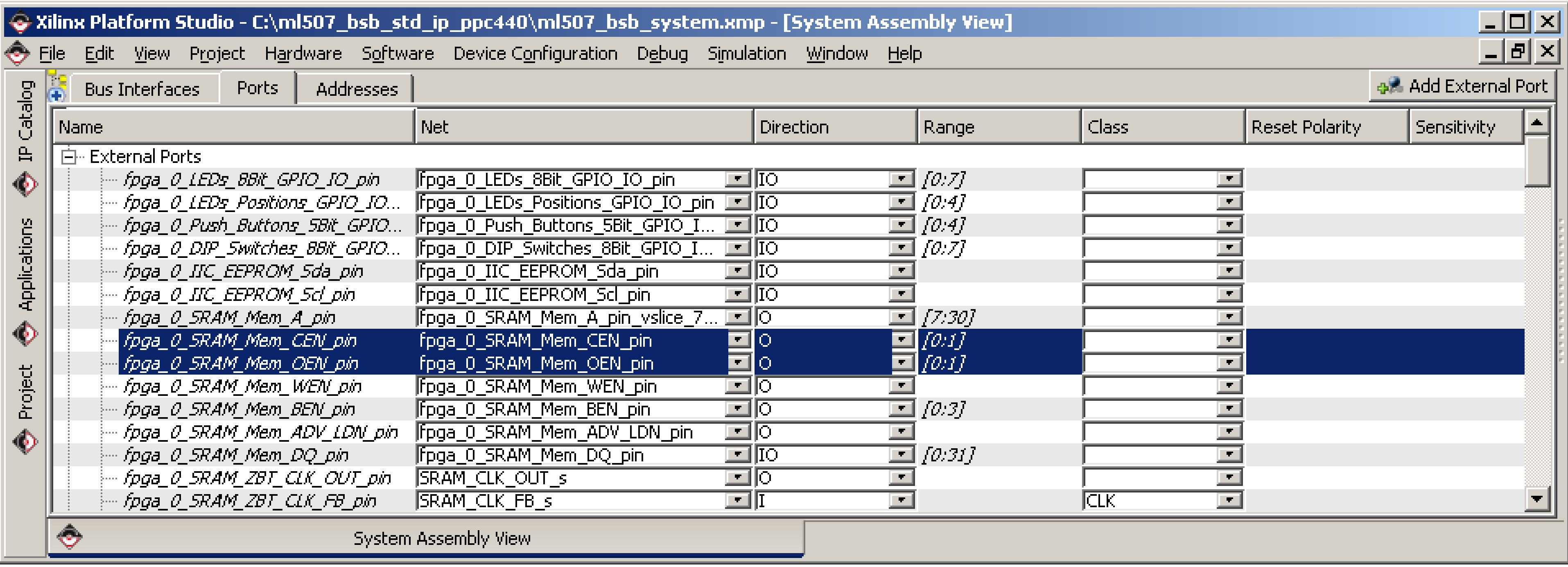
Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
xps_gpio_2						
IIC_EEPROM						
xps_iic_0						
xps_iic_1						
xps_intc_0						
Hard_Ethernet_MAC						
xps_ps2_0						
SysACE_CompactFlash						
xps_tft_0						
RS232_Uart_1						
RS232_Uart_2						
clock_generator_0						
util_vector_logic_0						
Op1	sys_periph_reset	I	[0:C_SIZE-1]			
Op2	No Connection	I	[0:C_SIZE-1]			
Res	sys_periph_reset_n	O	[0:C_SIZE-1]			

Note: Presentation applies to the ML507

Connect Ports

- **Expand External Ports**
  - Set **fpga_0_SRAM_Mem_CEN_pin** and **fpga_0_SRAM_Mem_OEN_pin** to a range of **[0:1]**



Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp - [System Assembly View]
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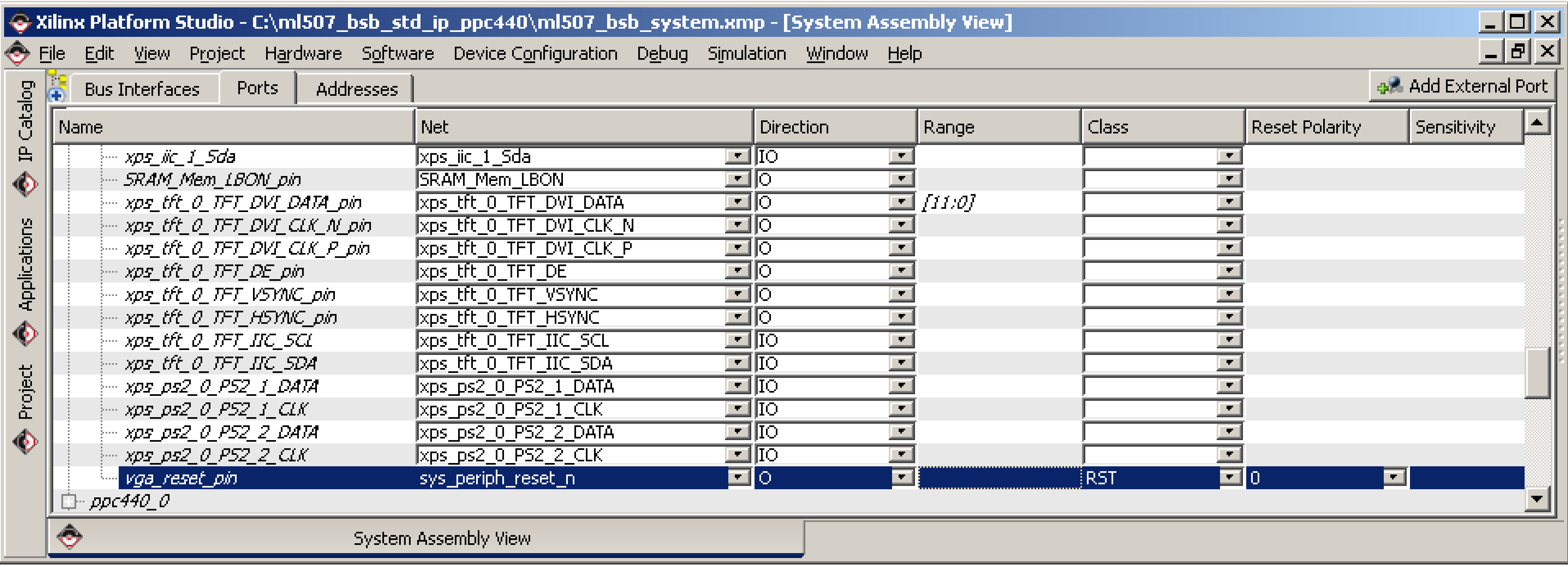
Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
External Ports						
fpga_0_LEDs_8Bit_GPIO_IO_pin	fpga_0_LEDs_8Bit_GPIO_IO_pin	IO	*[0:7]*			
fpga_0_LEDs_Positions_GPIO_IO...	fpga_0_LEDs_Positions_GPIO_IO_pin	IO	*[0:4]*			
fpga_0_Push_Buttons_5Bit_GPIO...	fpga_0_Push_Buttons_5Bit_GPIO_I...	IO	*[0:4]*			
fpga_0_DIP_Switches_8Bit_GPIO...	fpga_0_DIP_Switches_8Bit_GPIO_I...	IO	*[0:7]*			
fpga_0_IIC_EEPROM_Sda_pin	fpga_0_IIC_EEPROM_Sda_pin	IO				
fpga_0_IIC_EEPROM_Scl_pin	fpga_0_IIC_EEPROM_Scl_pin	IO				
fpga_0_SRAM_Mem_A_pin	fpga_0_SRAM_Mem_A_pin_vslice_7...	O	*[7:30]*			
fpga_0_SRAM_Mem_CEN_pin	fpga_0_SRAM_Mem_CEN_pin	O	*[0:1]*			
fpga_0_SRAM_Mem_OEN_pin	fpga_0_SRAM_Mem_OEN_pin	O	*[0:1]*			
fpga_0_SRAM_Mem_WEN_pin	fpga_0_SRAM_Mem_WEN_pin	O				
fpga_0_SRAM_Mem_BEN_pin	fpga_0_SRAM_Mem_BEN_pin	O	*[0:3]*			
fpga_0_SRAM_Mem_ADV_LDN_pin	fpga_0_SRAM_Mem_ADV_LDN_pin	O				
fpga_0_SRAM_Mem_DQ_pin	fpga_0_SRAM_Mem_DQ_pin	IO	*[0:31]*			
fpga_0_SRAM_ZBT_CLK_OUT_pin	SRAM_CLK_OUT_s	O				
fpga_0_SRAM_ZBT_CLK_FB_pin	SRAM_CLK_FB_s	I		CLK		

Note: Presentation applies to the ML507

Connect Ports

- **Add an External Port**
  - Click **Add External Port**
  - Pin name: **vga_reset_pin**
  - Net name: **sys_periph_reset_n**, Dir: **O**, Class: **RST**, Reset Polarity: **0**



Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp - [System Assembly View]
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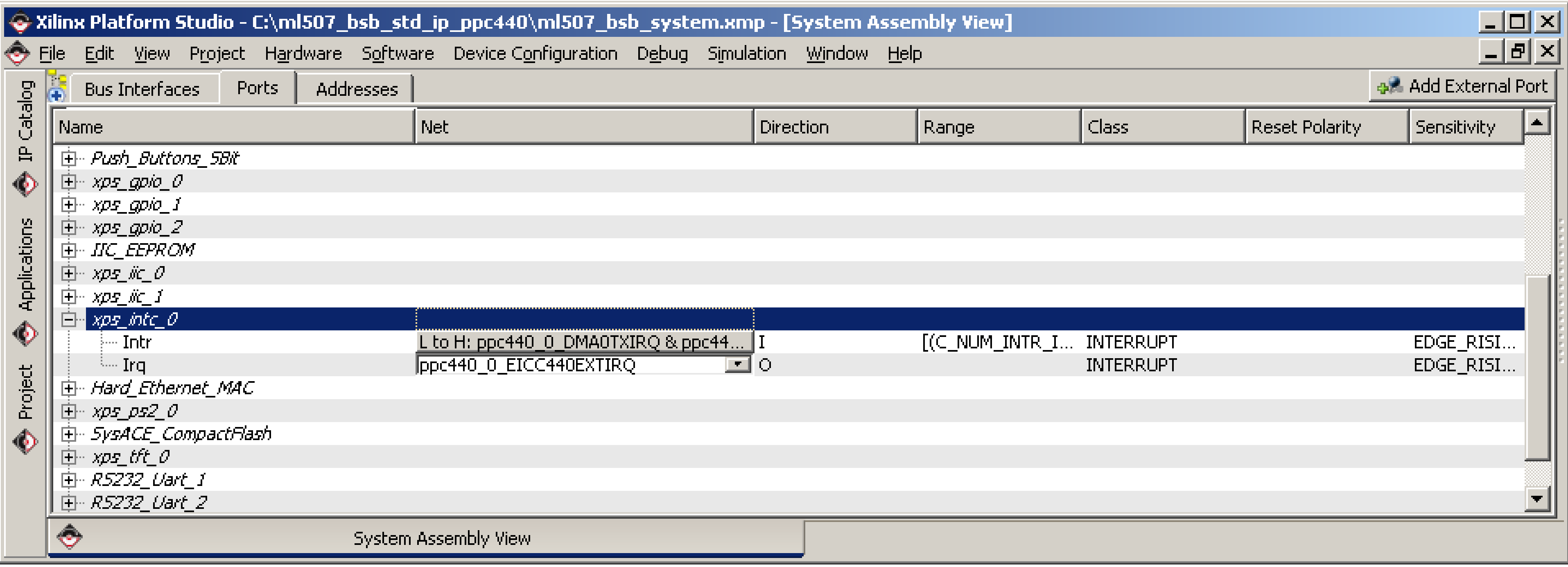
Add External Port
System Assembly View

Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
xps_iic_1_Sda	xps_iic_1_Sda	IO				
SRAM_Mem_LBON_pin	SRAM_Mem_LBON	O				
xps_tft_0_TFT_DVI_DATA_pin	xps_tft_0_TFT_DVI_DATA	O	*[11:0]*			
xps_tft_0_TFT_DVI_CLK_N_pin	xps_tft_0_TFT_DVI_CLK_N	O				
xps_tft_0_TFT_DVI_CLK_P_pin	xps_tft_0_TFT_DVI_CLK_P	O				
xps_tft_0_TFT_DE_pin	xps_tft_0_TFT_DE	O				
xps_tft_0_TFT_VSYNC_pin	xps_tft_0_TFT_VSYNC	O				
xps_tft_0_TFT_HSYNC_pin	xps_tft_0_TFT_HSYNC	O				
xps_tft_0_TFT_IIC_SCL	xps_tft_0_TFT_IIC_SCL	IO				
xps_tft_0_TFT_IIC_SDA	xps_tft_0_TFT_IIC_SDA	IO				
xps_ps2_0_PS2_1_DATA	xps_ps2_0_PS2_1_DATA	IO				
xps_ps2_0_PS2_1_CLK	xps_ps2_0_PS2_1_CLK	IO				
xps_ps2_0_PS2_2_DATA	xps_ps2_0_PS2_2_DATA	IO				
xps_ps2_0_PS2_2_CLK	xps_ps2_0_PS2_2_CLK	IO				
vga_reset_pin	sys_periph_reset_n	O		RST	0	
ppc440_0						

Note: Presentation applies to the ML507

Connect Ports

- **Expand this instance:**
  - **xps_intc_0**
  - Click on the gray Intr area to open the Interrupts dialog



Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp - [System Assembly View]
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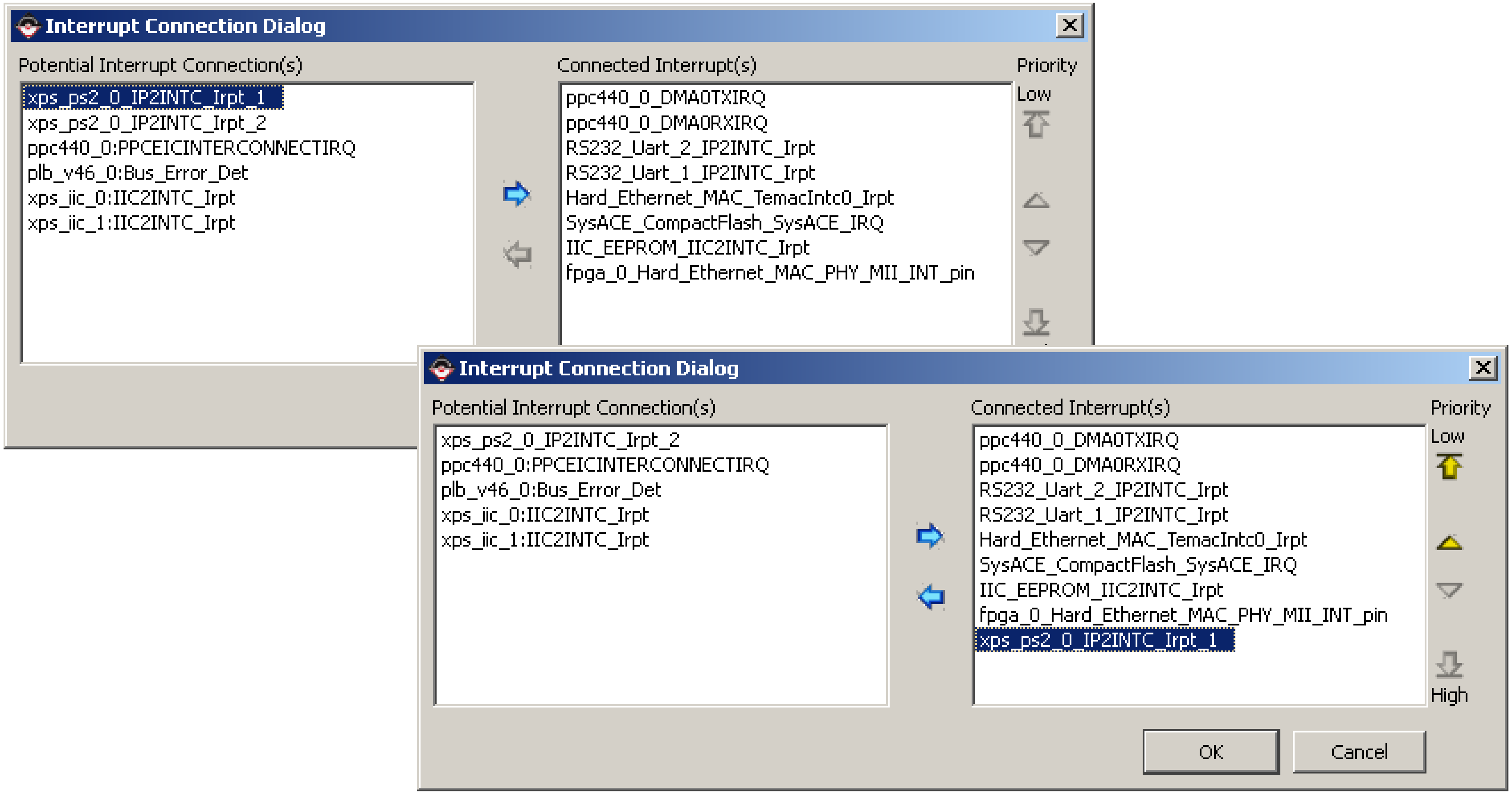
Name	Net	Direction	Range	Class	Reset Polarity	Sensitivity
Push_Buttons_5Bit						
xps_gpio_0						
xps_gpio_1						
xps_gpio_2						
IIC_EEPROM						
xps_iic_0						
xps_iic_1						
xps_intc_0						
Intr	L to H: ppc440_0_DMA0TXIRQ & ppc44...	I	[(C_NUM_INTR_I...	INTERRUPT		EDGE_RISI...
Irq	ppc440_0_EICC440EXTIRQ	O		INTERRUPT		EDGE_RISI...
Hard_Ethernet_MAC						
xps_ps2_0						
SysACE_CompactFlash						
xps_tft_0						
RS232_Uart_1						
RS232_Uart_2						

Note: Presentation applies to the ML507

Connect Ports

- **Add this interrupt:**
  - **xps_ps2_0_IP2INTC_Irpt_1**



Interrupt Connection Dialog
Potential Interrupt Connection(s)
Connected Interrupt(s)
Priority
Low
High
OK
Cancel

Interrupt Connection Dialog (before)

Potential Interrupt Connection(s):
- xps_ps2_0_IP2INTC_Irpt_1
- xps_ps2_0_IP2INTC_Irpt_2
- ppc440_0:PPCEICINTERCONNECTIRQ
- plb_v46_0:Bus_Error_Det
- xps_iic_0:IIC2INTC_Irpt
- xps_iic_1:IIC2INTC_Irpt

Connected Interrupt(s):
- ppc440_0_DMA0TXIRQ
- ppc440_0_DMA0RXIRQ
- RS232_Uart_2_IP2INTC_Irpt
- RS232_Uart_1_IP2INTC_Irpt
- Hard_Ethernet_MAC_TemacIntc0_Irpt
- SysACE_CompactFlash_SysACE_IRQ
- IIC_EEPROM_IIC2INTC_Irpt
- fpga_0_Hard_Ethernet_MAC_PHY_MII_INT_pin

Interrupt Connection Dialog (after)

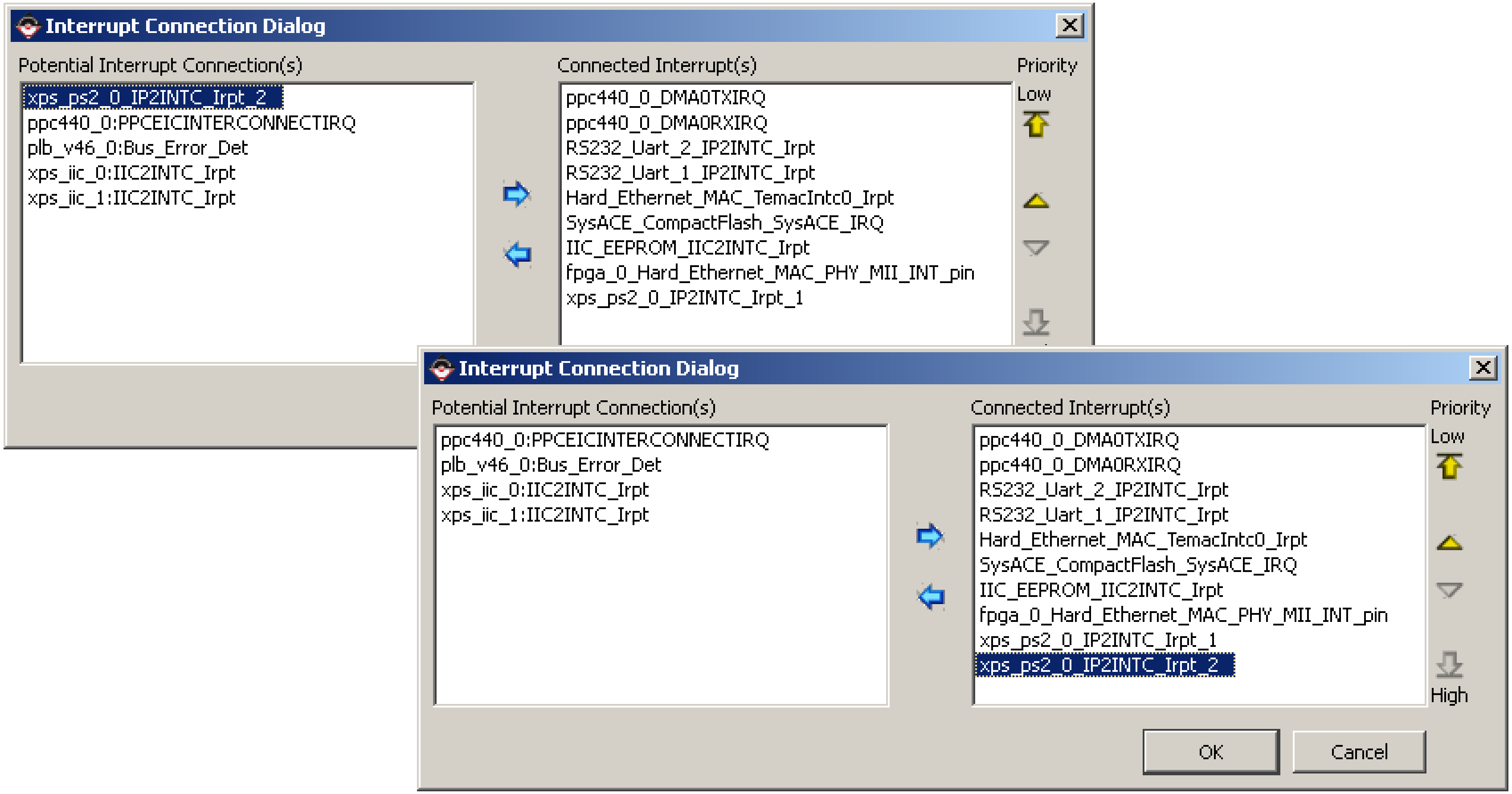
Potential Interrupt Connection(s):
- xps_ps2_0_IP2INTC_Irpt_2
- ppc440_0:PPCEICINTERCONNECTIRQ
- plb_v46_0:Bus_Error_Det
- xps_iic_0:IIC2INTC_Irpt
- xps_iic_1:IIC2INTC_Irpt

Connected Interrupt(s):
- ppc440_0_DMA0TXIRQ
- ppc440_0_DMA0RXIRQ
- RS232_Uart_2_IP2INTC_Irpt
- RS232_Uart_1_IP2INTC_Irpt
- Hard_Ethernet_MAC_TemacIntc0_Irpt
- SysACE_CompactFlash_SysACE_IRQ
- IIC_EEPROM_IIC2INTC_Irpt
- fpga_0_Hard_Ethernet_MAC_PHY_MII_INT_pin
- xps_ps2_0_IP2INTC_Irpt_1

Note: Presentation applies to the ML507

Connect Ports

- **Add this interrupt:**
  - **xps_ps2_0_IP2INTC_Irpt_2**



Interrupt Connection Dialog

Potential Interrupt Connection(s)

- xps_ps2_0_IP2INTC_Irpt_2
- ppc440_0:PPCEICINTERCONNECTIRQ
- plb_v46_0:Bus_Error_Det
- xps_iic_0:IIC2INTC_Irpt
- xps_iic_1:IIC2INTC_Irpt

Connected Interrupt(s)

- ppc440_0_DMA0TXIRQ
- ppc440_0_DMA0RXIRQ
- RS232_Uart_2_IP2INTC_Irpt
- RS232_Uart_1_IP2INTC_Irpt
- Hard_Ethernet_MAC_TemacIntc0_Irpt
- SysACE_CompactFlash_SysACE_IRQ
- IIC_EEPROM_IIC2INTC_Irpt
- fpga_0_Hard_Ethernet_MAC_PHY_MII_INT_pin
- xps_ps2_0_IP2INTC_Irpt_1

Interrupt Connection Dialog

Potential Interrupt Connection(s)

- ppc440_0:PPCEICINTERCONNECTIRQ
- plb_v46_0:Bus_Error_Det
- xps_iic_0:IIC2INTC_Irpt
- xps_iic_1:IIC2INTC_Irpt

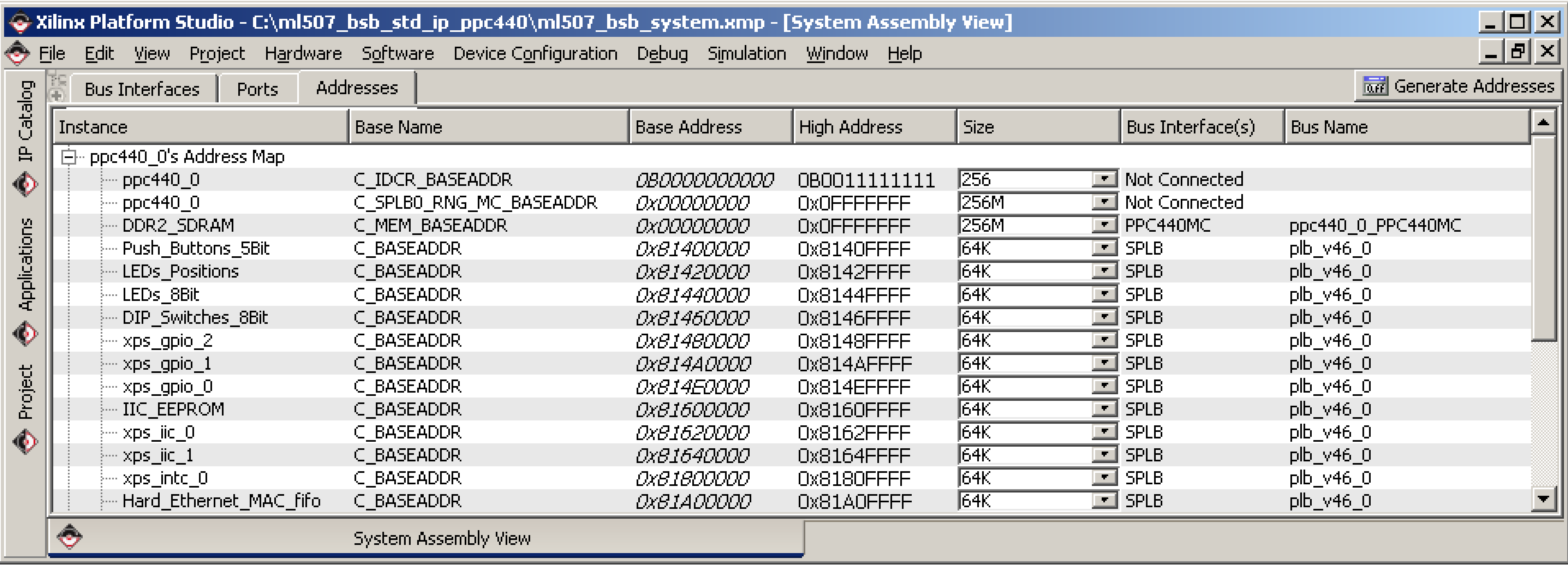
Connected Interrupt(s)

- ppc440_0_DMA0TXIRQ
- ppc440_0_DMA0RXIRQ
- RS232_Uart_2_IP2INTC_Irpt
- RS232_Uart_1_IP2INTC_Irpt
- Hard_Ethernet_MAC_TemacIntc0_Irpt
- SysACE_CompactFlash_SysACE_IRQ
- IIC_EEPROM_IIC2INTC_Irpt
- fpga_0_Hard_Ethernet_MAC_PHY_MII_INT_pin
- xps_ps2_0_IP2INTC_Irpt_1
- xps_ps2_0_IP2INTC_Irpt_2

Generate Addresses

Generate Addresses

- **Select the Addresses tab**
  - Click the **Generate Addresses** Button



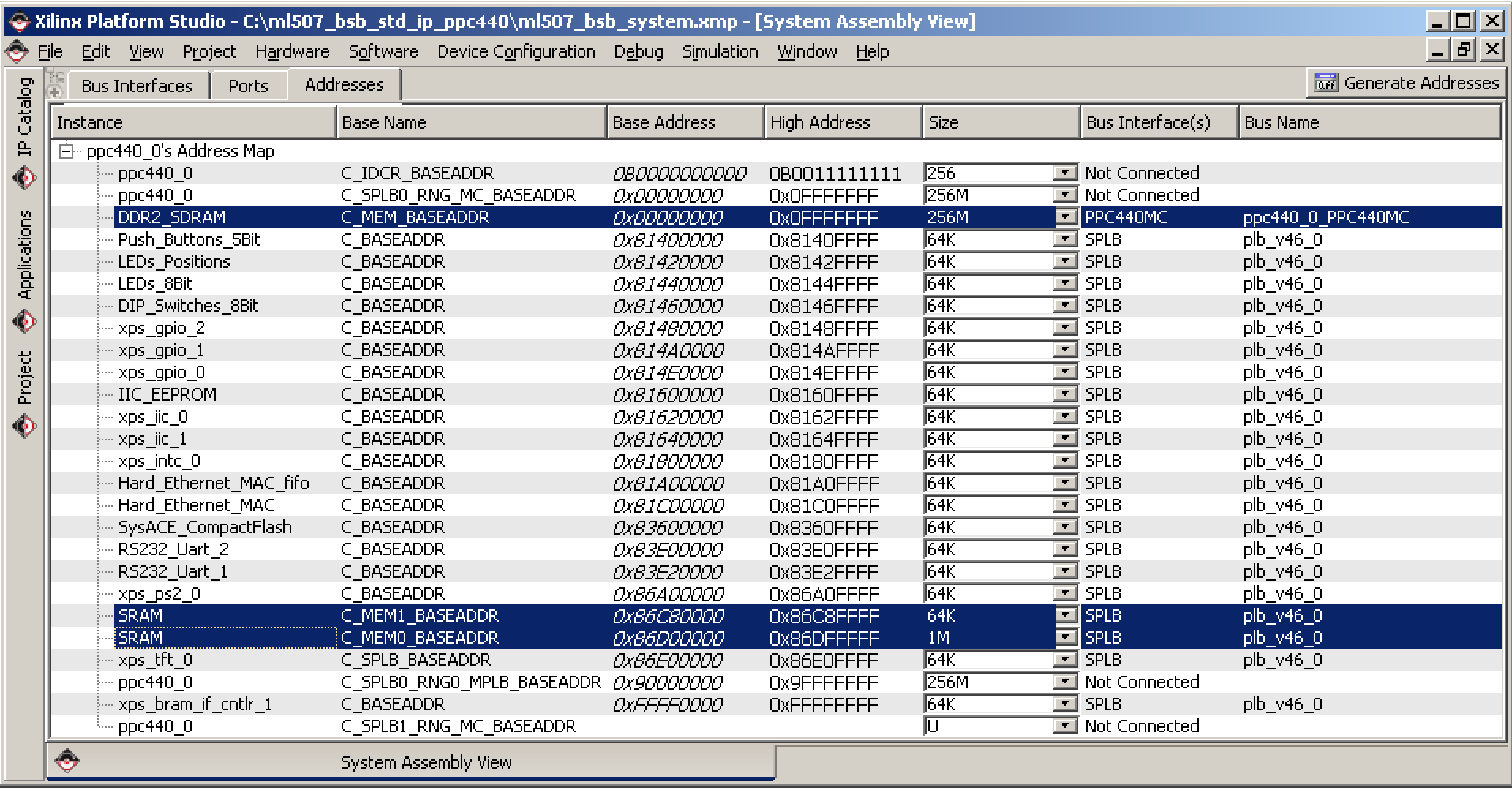
Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp - [System Assembly View]
File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help
IP Catalog
Applications
Project
Bus Interfaces
Ports
Addresses
Generate Addresses
System Assembly View

Instance	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name
ppc440_0's Address Map						
ppc440_0	C_IDCR_BASEADDR	0B0000000000	0B0011111111	256	Not Connected	
ppc440_0	C_SPLB0_RNG_MC_BASEADDR	0x00000000	0x0FFFFFFF	256M	Not Connected	
DDR2_SDRAM	C_MEM_BASEADDR	0x00000000	0x0FFFFFFF	256M	PPC440MC	ppc440_0_PPC440MC
Push_Buttons_5Bit	C_BASEADDR	0x81400000	0x8140FFFF	64K	SPLB	plb_v46_0
LEDs_Positions	C_BASEADDR	0x81420000	0x8142FFFF	64K	SPLB	plb_v46_0
LEDs_8Bit	C_BASEADDR	0x81440000	0x8144FFFF	64K	SPLB	plb_v46_0
DIP_Switches_8Bit	C_BASEADDR	0x81460000	0x8146FFFF	64K	SPLB	plb_v46_0
xps_gpio_2	C_BASEADDR	0x81480000	0x8148FFFF	64K	SPLB	plb_v46_0
xps_gpio_1	C_BASEADDR	0x814A0000	0x814AFFFF	64K	SPLB	plb_v46_0
xps_gpio_0	C_BASEADDR	0x814E0000	0x814EFFFF	64K	SPLB	plb_v46_0
IIC_EEPROM	C_BASEADDR	0x81600000	0x8160FFFF	64K	SPLB	plb_v46_0
xps_iic_0	C_BASEADDR	0x81620000	0x8162FFFF	64K	SPLB	plb_v46_0
xps_iic_1	C_BASEADDR	0x81640000	0x8164FFFF	64K	SPLB	plb_v46_0
xps_intc_0	C_BASEADDR	0x81800000	0x8180FFFF	64K	SPLB	plb_v46_0
Hard_Ethernet_MAC_fifo	C_BASEADDR	0x81A00000	0x81A0FFFF	64K	SPLB	plb_v46_0

Note: Presentation applies to the ML507

Generate Addresses

- **The new addresses appear**

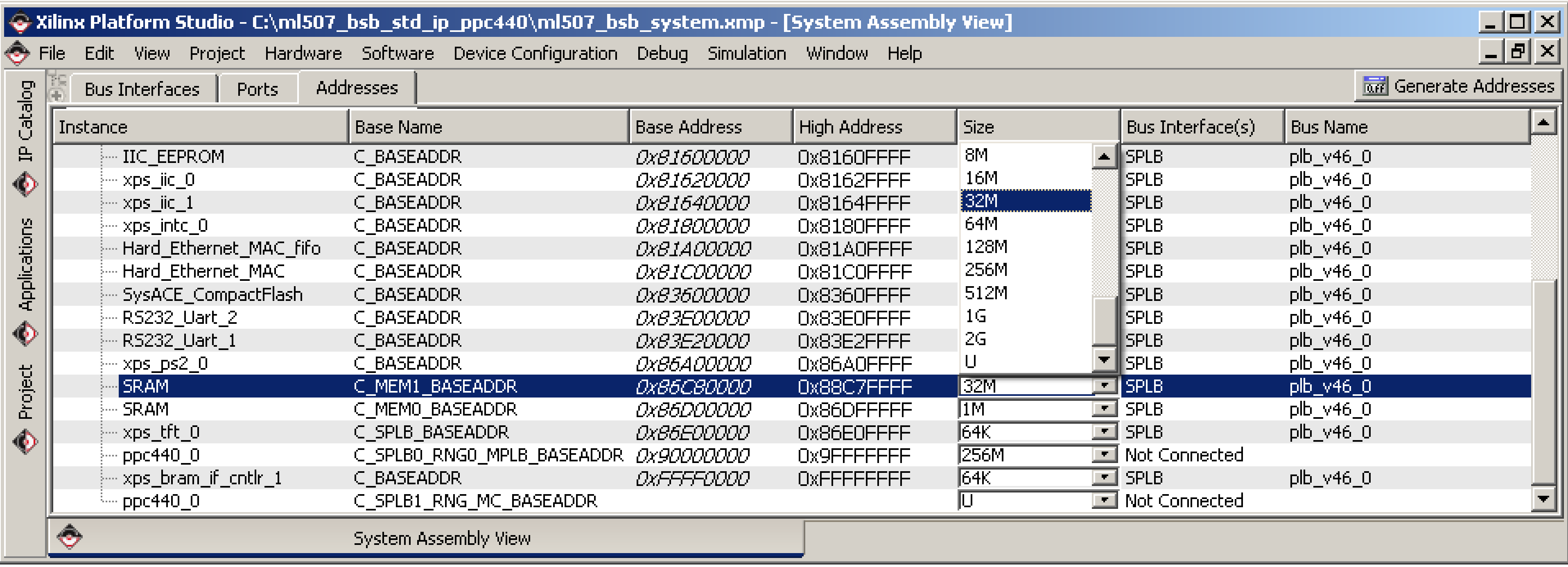


Instance	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name
ppc440_0's Address Map						
ppc440_0	C_IDCR_BASEADDR	0B0000000000	0B0011111111	256	Not Connected	
ppc440_0	C_SPLB0_RNG_MC_BASEADDR	0x00000000	0x0FFFFFFF	256M	Not Connected	
DDR2_SDRAM	C_MEM_BASEADDR	0x00000000	0x0FFFFFFF	256M	PPC440MC	ppc440_0_PPC440MC
Push_Buttons_5Bit	C_BASEADDR	0x81400000	0x8140FFFF	64K	SPLB	plb_v46_0
LEDs_Positions	C_BASEADDR	0x81420000	0x8142FFFF	64K	SPLB	plb_v46_0
LEDs_8Bit	C_BASEADDR	0x81440000	0x8144FFFF	64K	SPLB	plb_v46_0
DIP_Switches_8Bit	C_BASEADDR	0x81460000	0x8146FFFF	64K	SPLB	plb_v46_0
xps_gpio_2	C_BASEADDR	0x81480000	0x8148FFFF	64K	SPLB	plb_v46_0
xps_gpio_1	C_BASEADDR	0x814A0000	0x814AFFFF	64K	SPLB	plb_v46_0
xps_gpio_0	C_BASEADDR	0x814E0000	0x814EFFFF	64K	SPLB	plb_v46_0
IIC_EEPROM	C_BASEADDR	0x81600000	0x8160FFFF	64K	SPLB	plb_v46_0
xps_iic_0	C_BASEADDR	0x81620000	0x8162FFFF	64K	SPLB	plb_v46_0
xps_iic_1	C_BASEADDR	0x81640000	0x8164FFFF	64K	SPLB	plb_v46_0
xps_intc_0	C_BASEADDR	0x81800000	0x8180FFFF	64K	SPLB	plb_v46_0
Hard_Ethernet_MAC_fifo	C_BASEADDR	0x81A00000	0x81A0FFFF	64K	SPLB	plb_v46_0
Hard_Ethernet_MAC	C_BASEADDR	0x81C00000	0x81C0FFFF	64K	SPLB	plb_v46_0
SysACE_CompactFlash	C_BASEADDR	0x83600000	0x8360FFFF	64K	SPLB	plb_v46_0
RS232_Uart_2	C_BASEADDR	0x83E00000	0x83E0FFFF	64K	SPLB	plb_v46_0
RS232_Uart_1	C_BASEADDR	0x83E20000	0x83E2FFFF	64K	SPLB	plb_v46_0
xps_ps2_0	C_BASEADDR	0x86A00000	0x86A0FFFF	64K	SPLB	plb_v46_0
SRAM	C_MEM1_BASEADDR	0x86C80000	0x86C8FFFF	64K	SPLB	plb_v46_0
SRAM	C_MEM0_BASEADDR	0x86D00000	0x86DFFFFF	1M	SPLB	plb_v46_0
xps_tft_0	C_SPLB_BASEADDR	0x86E00000	0x86E0FFFF	64K	SPLB	plb_v46_0
ppc440_0	C_SPLB0_RNG0_MPLB_BASEADDR	0x90000000	0x9FFFFFFF	256M	Not Connected	
xps_bram_if_cntlr_1	C_BASEADDR	0xFFFF0000	0xFFFFFFFF	64K	SPLB	plb_v46_0
ppc440_0	C_SPLB1_RNG_MC_BASEADDR			U	Not Connected	

Note: Presentation applies to the ML507

Generate Addresses

- **The Flash is 32 Megabytes**
  - Set C_MEM1_BASEADDR to 32M
  - Click the **Generate Addresses** Button again



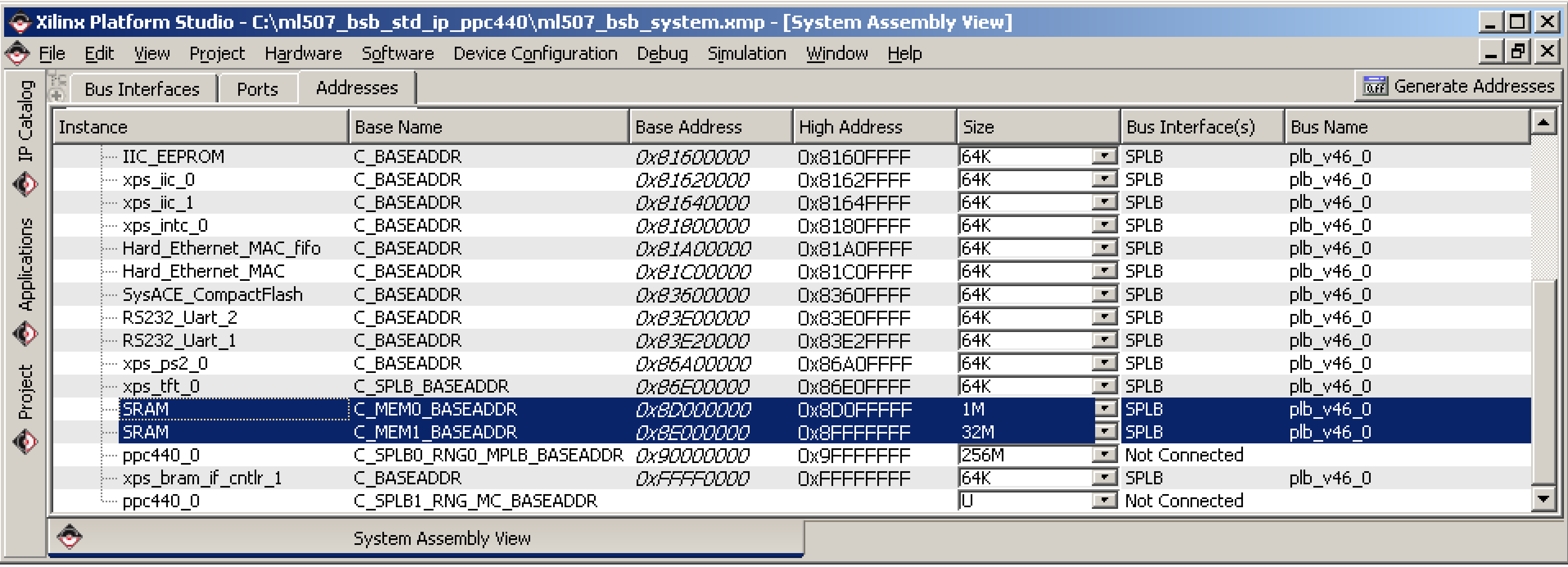
Instance	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name
IIC_EEPROM	C_BASEADDR	*0x81600000*	0x8160FFFF		SPLB	plb_v46_0
xps_iic_0	C_BASEADDR	*0x81620000*	0x8162FFFF		SPLB	plb_v46_0
xps_iic_1	C_BASEADDR	*0x81640000*	0x8164FFFF		SPLB	plb_v46_0
xps_intc_0	C_BASEADDR	*0x81800000*	0x8180FFFF		SPLB	plb_v46_0
Hard_Ethernet_MAC_fifo	C_BASEADDR	*0x81A00000*	0x81A0FFFF		SPLB	plb_v46_0
Hard_Ethernet_MAC	C_BASEADDR	*0x81C00000*	0x81C0FFFF		SPLB	plb_v46_0
SysACE_CompactFlash	C_BASEADDR	*0x83600000*	0x8360FFFF		SPLB	plb_v46_0
RS232_Uart_2	C_BASEADDR	*0x83E00000*	0x83E0FFFF		SPLB	plb_v46_0
RS232_Uart_1	C_BASEADDR	*0x83E20000*	0x83E2FFFF		SPLB	plb_v46_0
xps_ps2_0	C_BASEADDR	*0x86A00000*	0x86A0FFFF		SPLB	plb_v46_0
SRAM	C_MEM1_BASEADDR	*0x86C80000*	0x88C7FFFF	32M	SPLB	plb_v46_0
SRAM	C_MEM0_BASEADDR	*0x86D00000*	0x86DFFFFF	1M	SPLB	plb_v46_0
xps_tft_0	C_SPLB_BASEADDR	*0x86E00000*	0x86E0FFFF	64K	SPLB	plb_v46_0
ppc440_0	C_SPLB0_RNG0_MPLB_BASEADDR	*0x90000000*	0x9FFFFFFF	256M	Not Connected	
xps_bram_if_cntlr_1	C_BASEADDR	*0xFFFF0000*	0xFFFFFFFF	64K	SPLB	plb_v46_0
ppc440_0	C_SPLB1_RNG_MC_BASEADDR			U	Not Connected	

8M
16M
32M
64M
128M
256M
512M
1G
2G
U

Note: Presentation applies to the ML507

Generate Addresses

- **The new addresses appear**
  - The FLASH now has a full 32M address range


Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp - [System Assembly View]
File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help
IP Catalog
Applications
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Bus Interfaces
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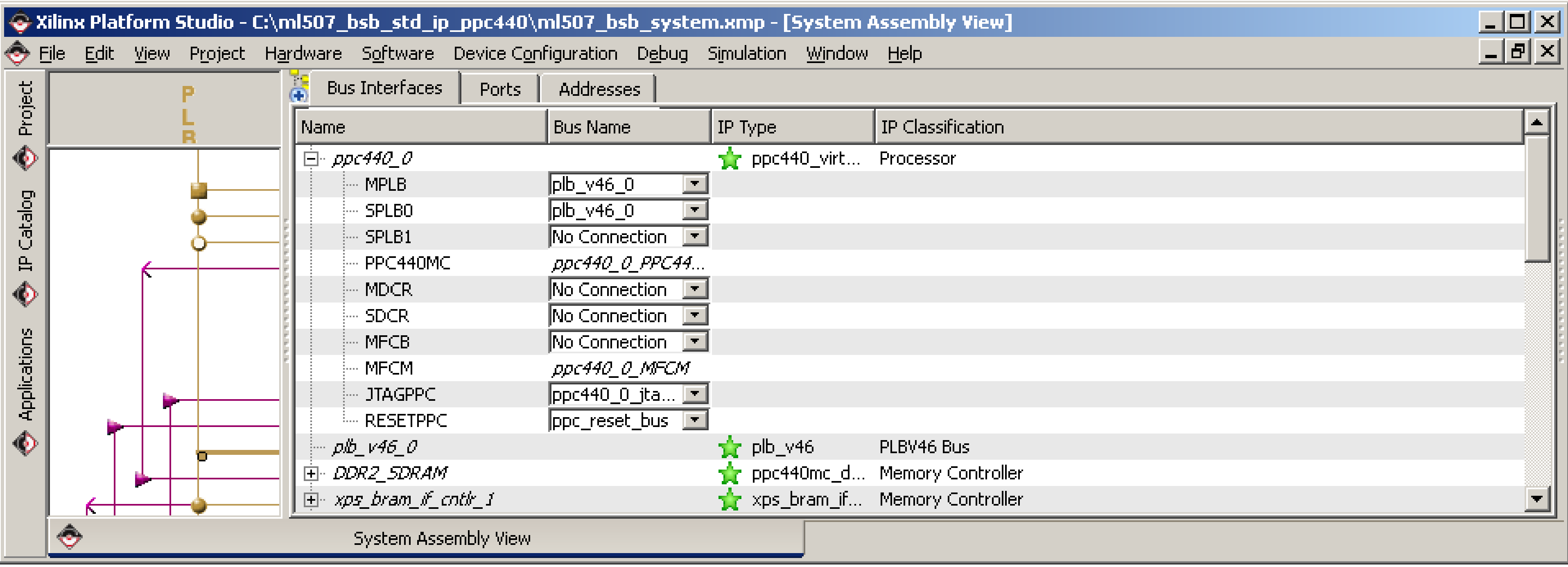
System Assembly View

Instance	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name
IIC_EEPROM	C_BASEADDR	0x81600000	0x8160FFFF	64K	SPLB	plb_v46_0
xps_iic_0	C_BASEADDR	0x81620000	0x8162FFFF	64K	SPLB	plb_v46_0
xps_iic_1	C_BASEADDR	0x81640000	0x8164FFFF	64K	SPLB	plb_v46_0
xps_intc_0	C_BASEADDR	0x81800000	0x8180FFFF	64K	SPLB	plb_v46_0
Hard_Ethernet_MAC_fifo	C_BASEADDR	0x81A00000	0x81A0FFFF	64K	SPLB	plb_v46_0
Hard_Ethernet_MAC	C_BASEADDR	0x81C00000	0x81C0FFFF	64K	SPLB	plb_v46_0
SysACE_CompactFlash	C_BASEADDR	0x83600000	0x8360FFFF	64K	SPLB	plb_v46_0
RS232_Uart_2	C_BASEADDR	0x83E00000	0x83E0FFFF	64K	SPLB	plb_v46_0
RS232_Uart_1	C_BASEADDR	0x83E20000	0x83E2FFFF	64K	SPLB	plb_v46_0
xps_ps2_0	C_BASEADDR	0x86A00000	0x86A0FFFF	64K	SPLB	plb_v46_0
xps_tft_0	C_SPLB_BASEADDR	0x86E00000	0x86E0FFFF	64K	SPLB	plb_v46_0
SRAM	C_MEM0_BASEADDR	0x8D000000	0x8D0FFFFF	1M	SPLB	plb_v46_0
SRAM	C_MEM1_BASEADDR	0x8E000000	0x8FFFFFFF	32M	SPLB	plb_v46_0
ppc440_0	C_SPLB0_RNG0_MPLB_BASEADDR	0x90000000	0x9FFFFFFF	256M	Not Connected	
xps_bram_if_cntlr_1	C_BASEADDR	0xFFFF0000	0xFFFFFFFF	64K	SPLB	plb_v46_0
ppc440_0	C_SPLB1_RNG_MC_BASEADDR			U	Not Connected	

Note: Presentation applies to the ML507

Generate Addresses

- **Expand this instance:**
  - **ppc440_0**
  - Connect **SPLB0** to **plb_v46_0**

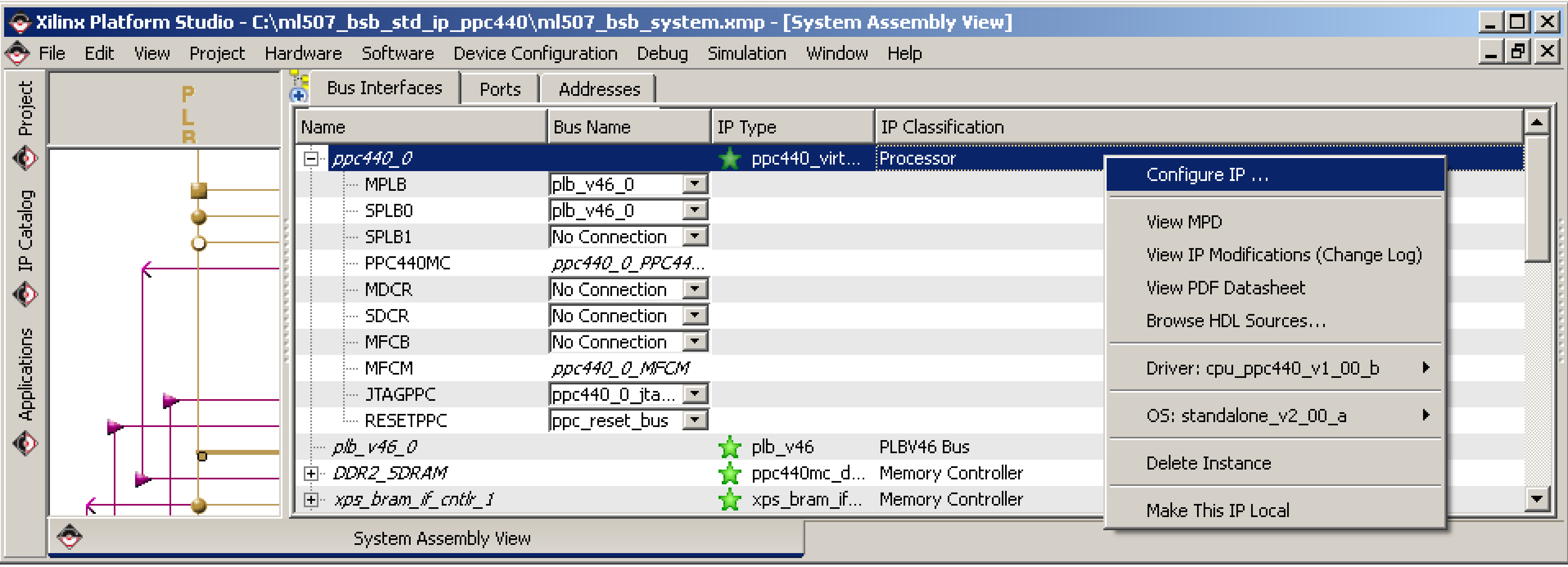


Name	Bus Name	IP Type	IP Classification
⊟ *ppc440_0*		ppc440_virt...	Processor
MPLB	plb_v46_0		
SPLB0	plb_v46_0		
SPLB1	No Connection		
PPC440MC	*ppc440_0_PPC44...*		
MDCR	No Connection		
SDCR	No Connection		
MFCB	No Connection		
MFCM	*ppc440_0_MFCM*		
JTAGPPC	ppc440_0_jta...		
RESETPPC	ppc_reset_bus		
plb_v46_0		plb_v46	PLBV46 Bus
⊞ *DDR2_SDRAM*		ppc440mc_d...	Memory Controller
⊞ *xps_bram_if_cntlr_1*		xps_bram_if...	Memory Controller

Note: See AR 32699 for details on SPLB0 and Address Generation

Generate Addresses

- **Configure the PPC440 SPLB0 Interface**
  - Right-click on the **ppc440_0**
  - Select **Configure IP…**

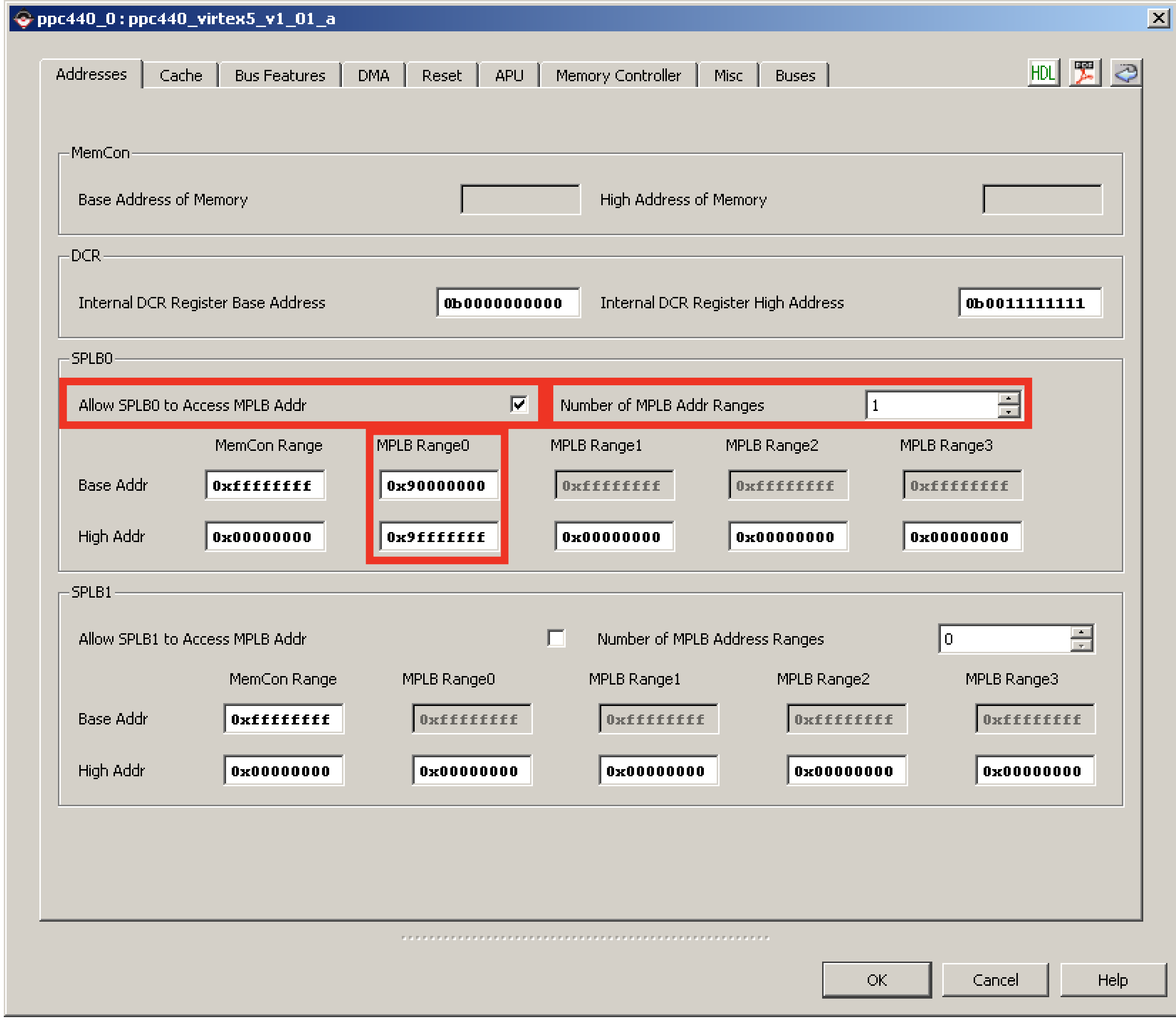


Name	Bus Name	IP Type	IP Classification
ppc440_0		ppc440_virt...	Processor
MPLB	plb_v46_0		
SPLB0	plb_v46_0		
SPLB1	No Connection		
PPC440MC	ppc440_0_PPC44...		
MDCR	No Connection		
SDCR	No Connection		
MFCB	No Connection		
MFCM	ppc440_0_MFCM		
JTAGPPC	ppc440_0_jta...		
RESETPPC	ppc_reset_bus		
plb_v46_0		plb_v46	PLBV46 Bus
DDR2_SDRAM		ppc440mc_d...	Memory Controller
xps_bram_if_cntlr_1		xps_bram_if...	Memory Controller

Note: Presentation applies to the ML507

Generate Addresses

- **Make the following settings**
  - Check Allow SPLB0 to Access MPLB Addr
  - Set Number of MPLB Addr Ranges to 1
  - Set MPLB0 Range0 from **0x90000000** to **0x9FFFFFFF**



ppc440_0 : ppc440_virtex5_v1_01_a

MemCon

Base Address of Memory High Address of Memory

DCR

Internal DCR Register Base Address 0b0000000000

Internal DCR Register High Address 0b0011111111

SPLB0

Allow SPLB0 to Access MPLB Addr ☑

Number of MPLB Addr Ranges 1

	MemCon Range	MPLB Range0	MPLB Range1	MPLB Range2	MPLB Range3
Base Addr	0xffffffff	0x90000000	0xffffffff	0xffffffff	0xffffffff
High Addr	0x00000000	0x9fffffff	0x00000000	0x00000000	0x00000000

SPLB1

Allow SPLB1 to Access MPLB Addr □

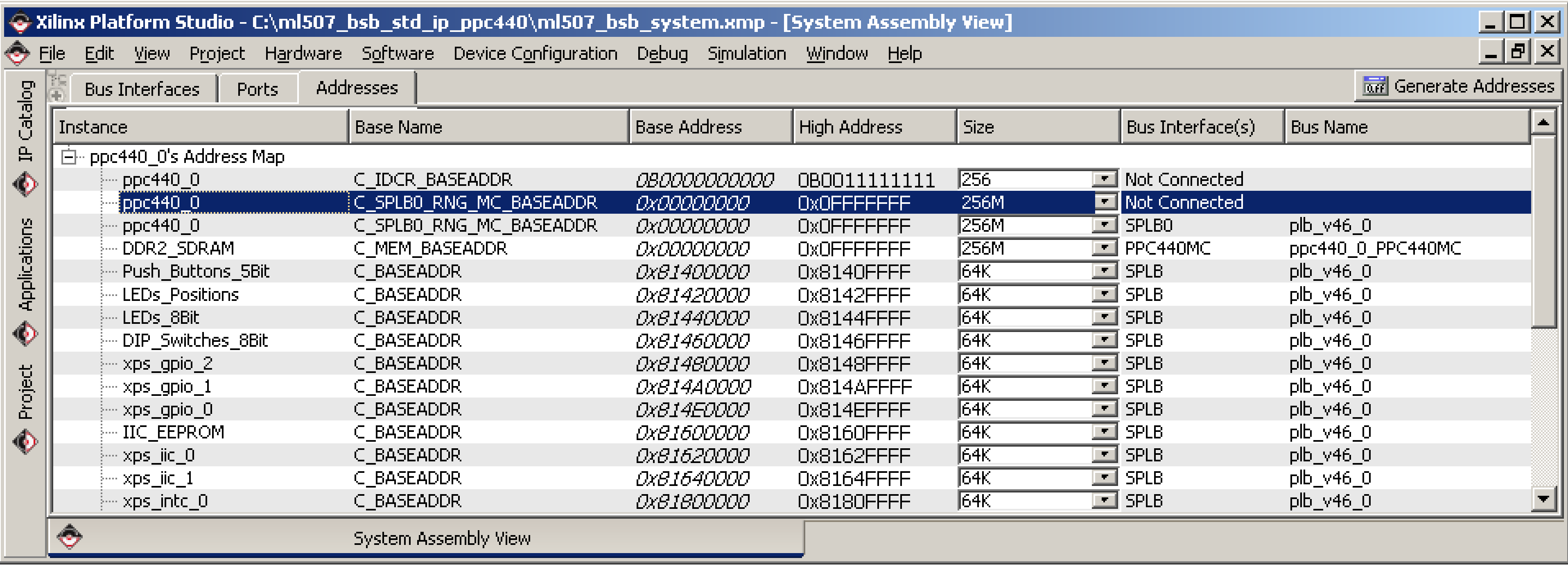
Number of MPLB Address Ranges 0

	MemCon Range	MPLB Range0	MPLB Range1	MPLB Range2	MPLB Range3
Base Addr	0xffffffff	0xffffffff	0xffffffff	0xffffffff	0xffffffff
High Addr	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000

Note: Presentation applies to the ML507

Generate Addresses

- **Select the Addresses tab**
  - Set **C_SPLB0_RNG_MC_BASEADDR** to **256M**
  - Address range should be **0x00000000** to **0x0FFFFFFF**



Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp - [System Assembly View]
File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help
Bus Interfaces
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Generate Addresses
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Applications
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System Assembly View

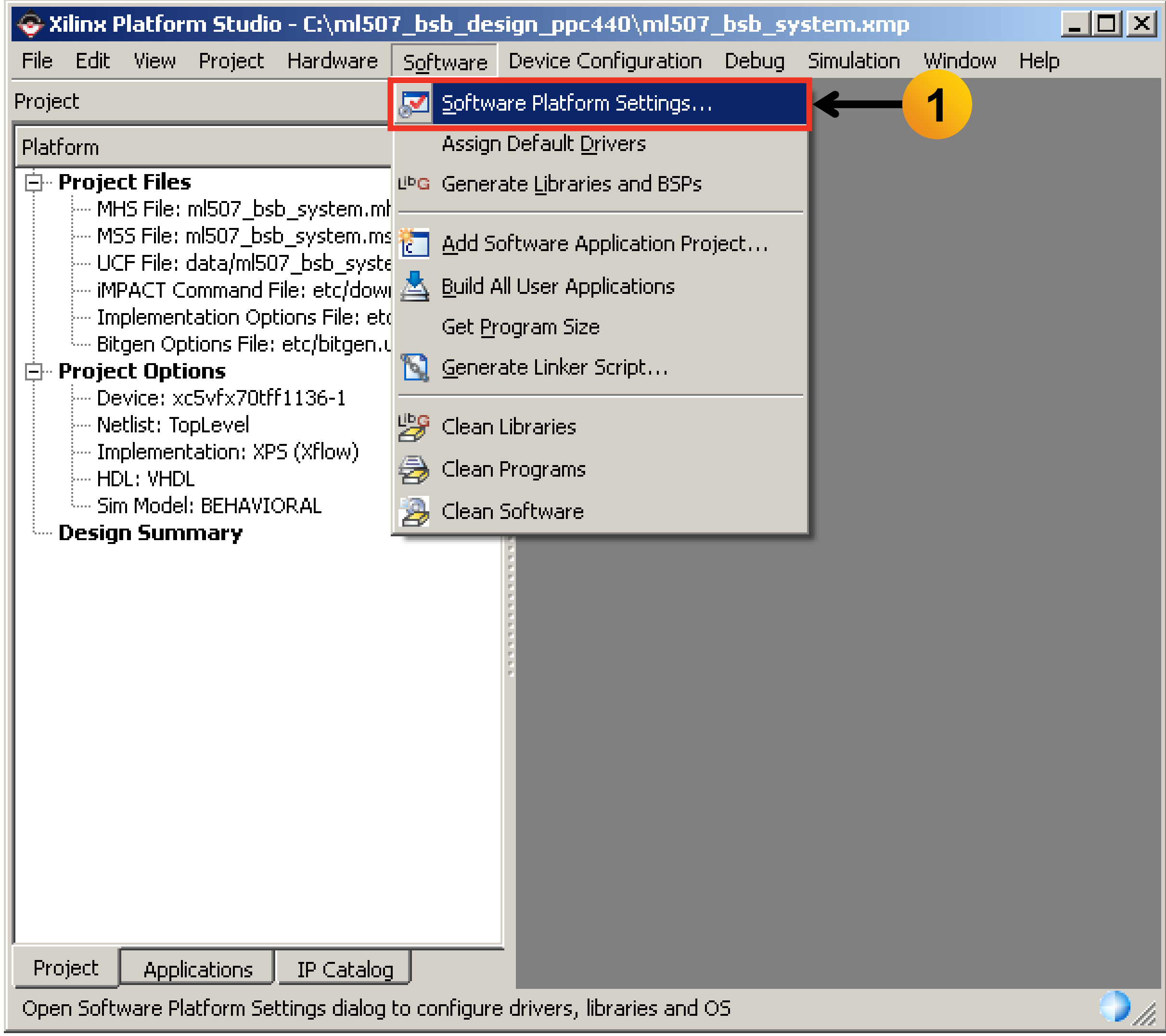
Instance	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name
ppc440_0's Address Map						
ppc440_0	C_IDCR_BASEADDR	0B0000000000	0B0011111111	256	Not Connected	
ppc440_0	C_SPLB0_RNG_MC_BASEADDR	0x00000000	0x0FFFFFFF	256M	Not Connected	
ppc440_0	C_SPLB0_RNG_MC_BASEADDR	0x00000000	0x0FFFFFFF	256M	SPLB0	plb_v46_0
DDR2_SDRAM	C_MEM_BASEADDR	0x00000000	0x0FFFFFFF	256M	PPC440MC	ppc440_0_PPC440MC
Push_Buttons_5Bit	C_BASEADDR	0x81400000	0x8140FFFF	64K	SPLB	plb_v46_0
LEDs_Positions	C_BASEADDR	0x81420000	0x8142FFFF	64K	SPLB	plb_v46_0
LEDs_8Bit	C_BASEADDR	0x81440000	0x8144FFFF	64K	SPLB	plb_v46_0
DIP_Switches_8Bit	C_BASEADDR	0x81460000	0x8146FFFF	64K	SPLB	plb_v46_0
xps_gpio_2	C_BASEADDR	0x81480000	0x8148FFFF	64K	SPLB	plb_v46_0
xps_gpio_1	C_BASEADDR	0x814A0000	0x814AFFFF	64K	SPLB	plb_v46_0
xps_gpio_0	C_BASEADDR	0x814E0000	0x814EFFFF	64K	SPLB	plb_v46_0
IIC_EEPROM	C_BASEADDR	0x81600000	0x8160FFFF	64K	SPLB	plb_v46_0
xps_iic_0	C_BASEADDR	0x81620000	0x8162FFFF	64K	SPLB	plb_v46_0
xps_iic_1	C_BASEADDR	0x81640000	0x8164FFFF	64K	SPLB	plb_v46_0
xps_intc_0	C_BASEADDR	0x81800000	0x8180FFFF	64K	SPLB	plb_v46_0

Note: Presentation applies to the ML507

Software Configuration

Software Platform Settings

- Configure the Software Platform
  - Select **Software → Software Platform Settings…** (1)



Xilinx Platform Studio - C:\ml507_bsb_design_ppc440\ml507_bsb_system.xmp

File
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Device Configuration
Debug
Simulation
Window
Help
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Platform
Project Files
MHS File: ml507_bsb_system.mh
MSS File: ml507_bsb_system.ms
UCF File: data/ml507_bsb_syste
iMPACT Command File: etc/dowı
Implementation Options File: etc
Bitgen Options File: etc/bitgen.u
Project Options
Device: xc5vfx70tff1136-1
Netlist: TopLevel
Implementation: XPS (Xflow)
HDL: VHDL
Sim Model: BEHAVIORAL
Design Summary
Software Platform Settings...
Assign Default Drivers
Generate Libraries and BSPs
Add Software Application Project...
Build All User Applications
Get Program Size
Generate Linker Script...
Clean Libraries
Clean Programs
Clean Software
1
Project
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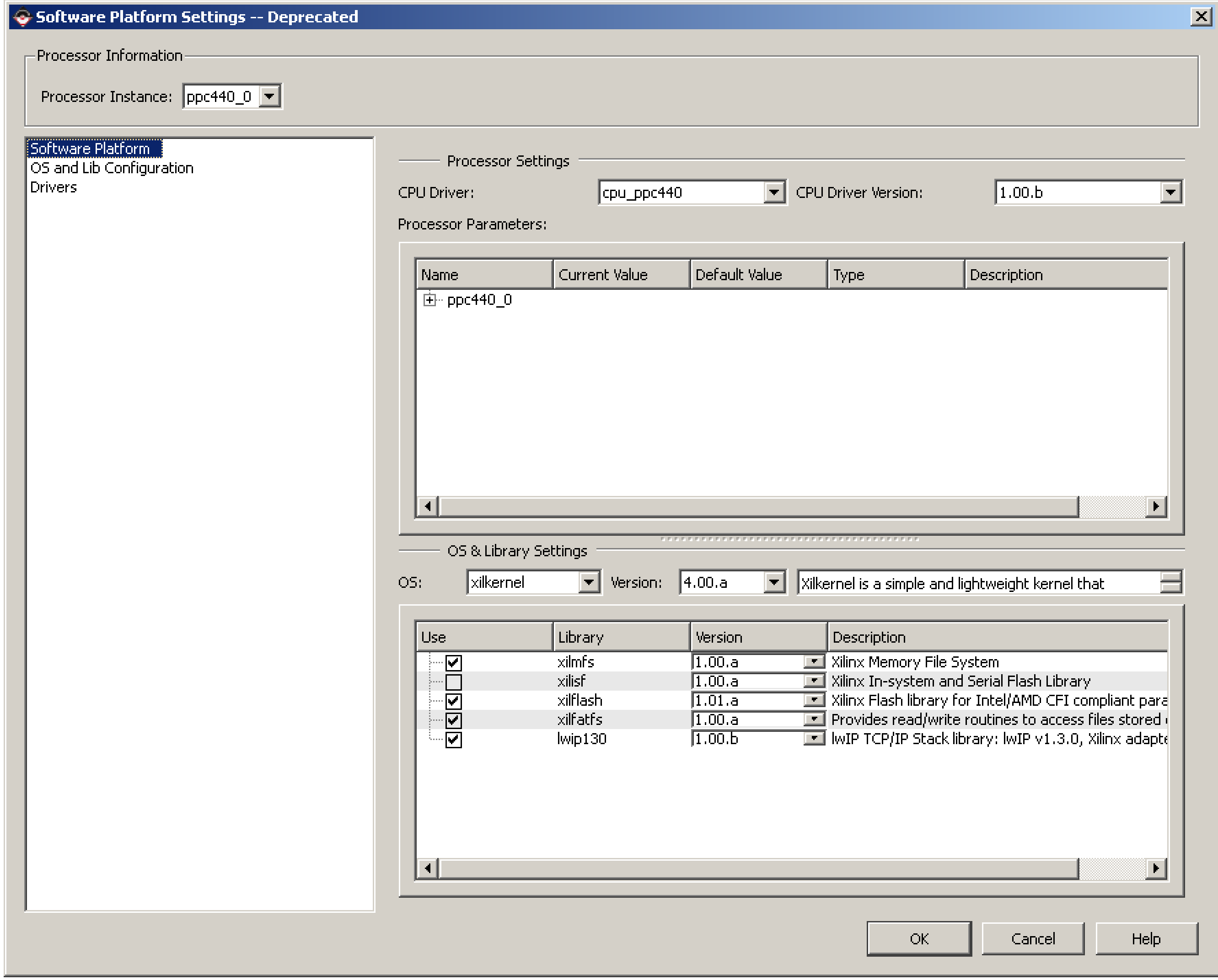
Open Software Platform Settings dialog to configure drivers, libraries and OS

Note: Presentation applies to the ML507

Software Platform Settings

- **Under Software Platform**
  - Set OS to **xilkernel**
  - Select **xilmfs**, **xilflash**, **xilfatfs**, and **lwip130**



Software Platform Settings -- Deprecated

Processor Information

Processor Instance: ppc440_0

Processor Settings

CPU Driver: cpu_ppc440 CPU Driver Version: 1.00.b

Processor Parameters:

Name	Current Value	Default Value	Type	Description
⊞ ppc440_0				

OS & Library Settings

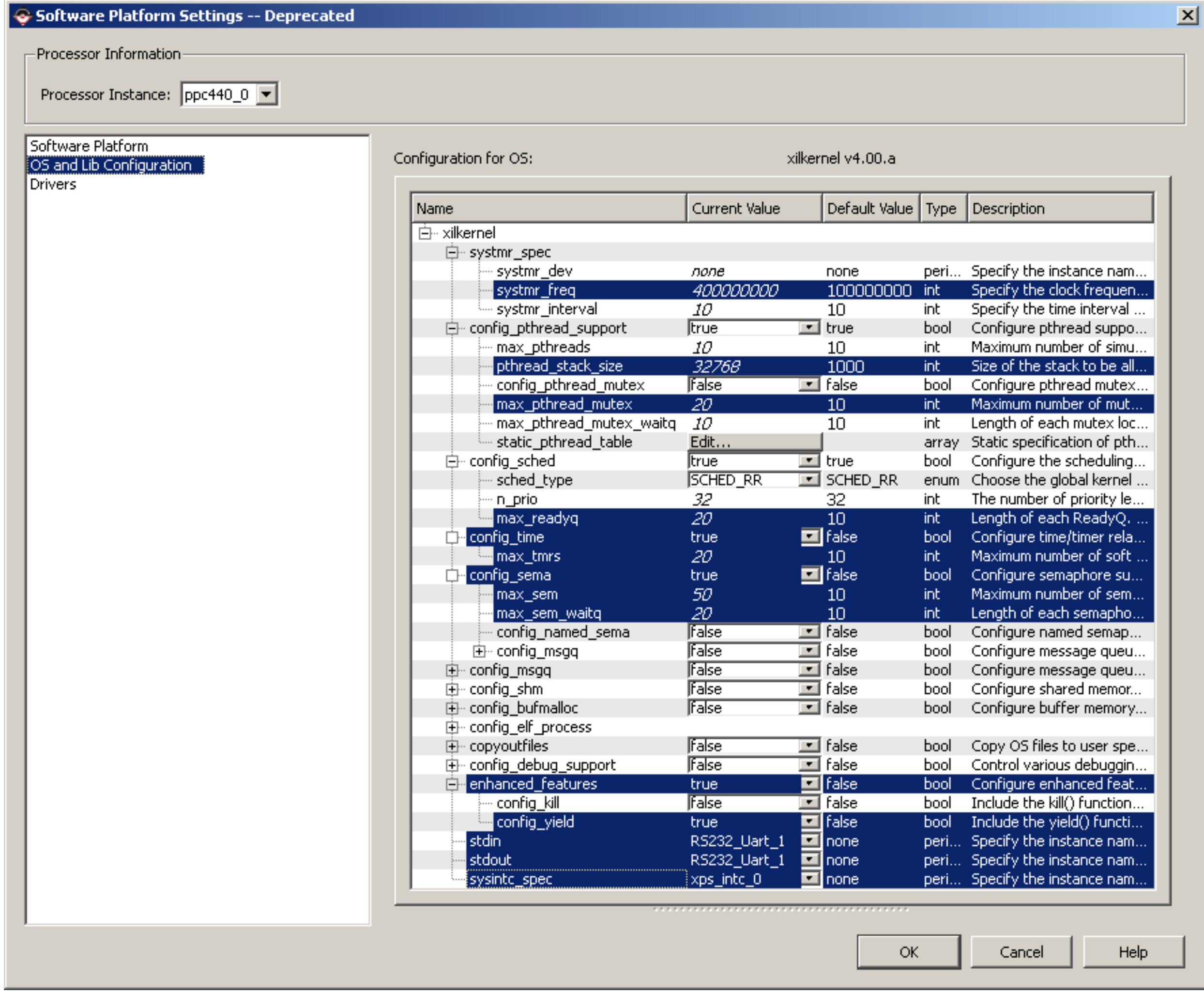
OS: xilkernel Version: 4.00.a Xilkernel is a simple and lightweight kernel that

Use	Library	Version	Description
☑	xilmfs	1.00.a	Xilinx Memory File System
□	xilisf	1.00.a	Xilinx In-system and Serial Flash Library
☑	xilflash	1.01.a	Xilinx Flash library for Intel/AMD CFI compliant para
☑	xilfatfs	1.00.a	Provides read/write routines to access files stored
☑	lwip130	1.00.b	lwIP TCP/IP Stack library: lwIP v1.3.0, Xilinx adapte

Note: Presentation applies to the ML507

Software Platform Settings

- **Under OS and Libraries, Configuration for OS, set these xilkernel settings:**
  - systmr_freq = **400000000**
  - pthread_stack_size = **32768**
  - max_pthread_mutex = **20**
  - max_readyq = **20**
  - config_time = **true**
  - max_tmrs = **20**
  - config_sema = **true**
  - max_sem = **50**
  - max_sem_waitq = **20**
  - enhanced_features = **true**
  - config_yield = **true**
  - stdin = **RS232_Uart_1**
  - stdout = **RS232_Uart_1**
  - sysintc_spec = **xps_intc_0**



Processor Instance: ppc440_0

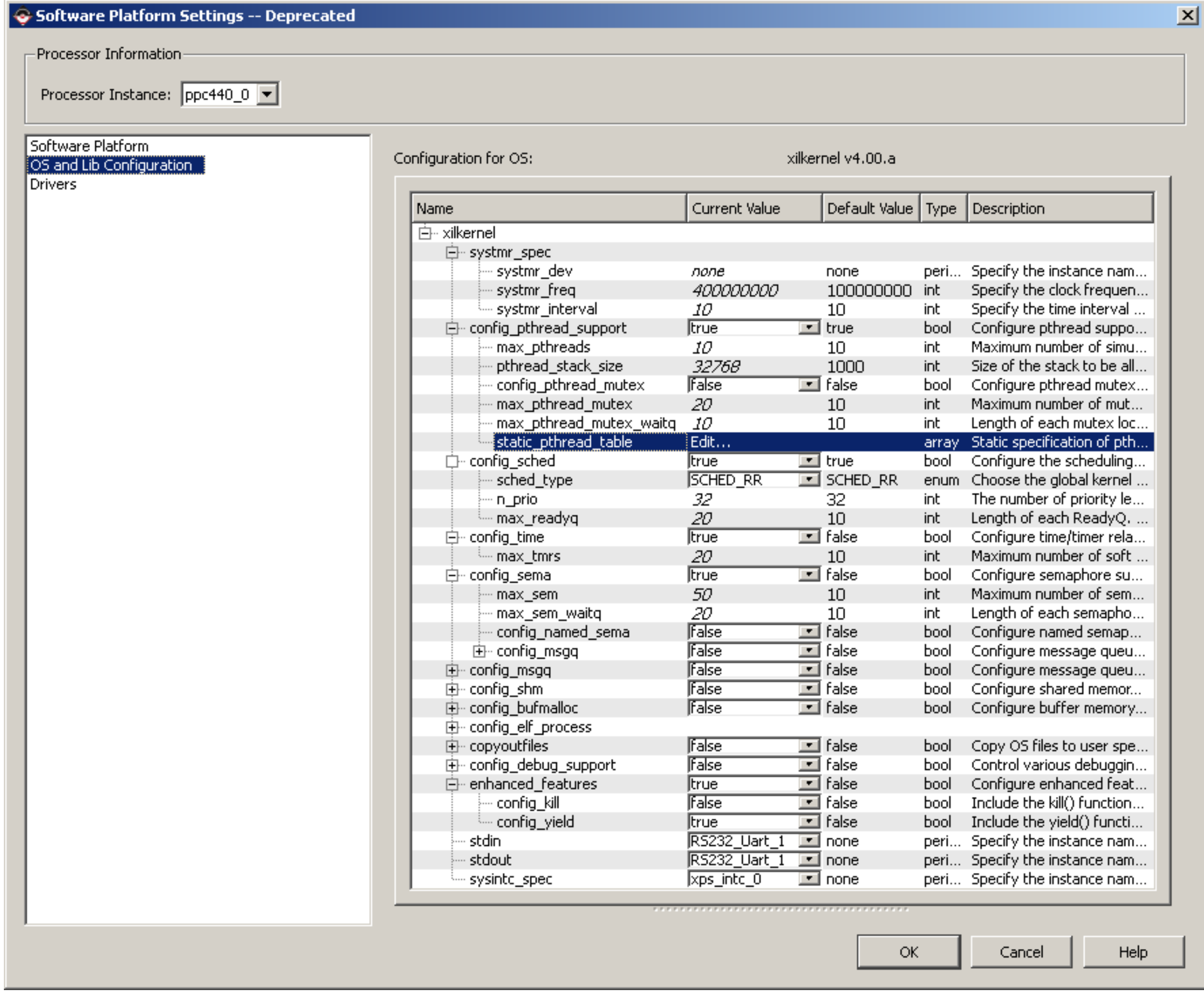
Configuration for OS: xilkernel v4.00.a

Name	Current Value	Default Value	Type	Description
xilkernel				
systmr_spec				
systmr_dev	none	none	peri...	Specify the instance nam...
systmr_freq	400000000	100000000	int	Specify the clock frequen...
systmr_interval	10	10	int	Specify the time interval ...
config_pthread_support	true	true	bool	Configure pthread suppo...
max_pthreads	10	10	int	Maximum number of simu...
pthread_stack_size	32768	1000	int	Size of the stack to be all...
config_pthread_mutex	false	false	bool	Configure pthread mutex...
max_pthread_mutex	20	10	int	Maximum number of mut...
max_pthread_mutex_waitq	10	10	int	Length of each mutex loc...
static_pthread_table	Edit...		array	Static specification of pth...
config_sched	true	true	bool	Configure the scheduling...
sched_type	SCHED_RR	SCHED_RR	enum	Choose the global kernel ...
n_prio	32	32	int	The number of priority le...
max_readyq	20	10	int	Length of each ReadyQ. ...
config_time	true	false	bool	Configure time/timer rela...
max_tmrs	20	10	int	Maximum number of soft ...
config_sema	true	false	bool	Configure semaphore su...
max_sem	50	10	int	Maximum number of sem...
max_sem_waitq	20	10	int	Length of each semapho...
config_named_sema	false	false	bool	Configure named semap...
config_msgq	false	false	bool	Configure message queu...
config_msgq	false	false	bool	Configure message queu...
config_shm	false	false	bool	Configure shared memor...
config_bufmalloc	false	false	bool	Configure buffer memory...
config_elf_process				
copyoutfiles	false	false	bool	Copy OS files to user spe...
config_debug_support	false	false	bool	Control various debuggin...
enhanced_features	true	false	bool	Configure enhanced feat...
config_kill	false	false	bool	Include the kill() function...
config_yield	true	false	bool	Include the yield() functi...
stdin	RS232_Uart_1	none	peri...	Specify the instance nam...
stdout	RS232_Uart_1	none	peri...	Specify the instance nam...
sysintc_spec	xps_intc_0	none	peri...	Specify the instance nam...

Note: Presentation applies to the ML507

Software Platform Settings

- **Under OS and Libraries, Configuration for OS**
  - – Click static_pthread_table



Software Platform Settings -- Deprecated

Processor Information

Processor Instance: ppc440_0

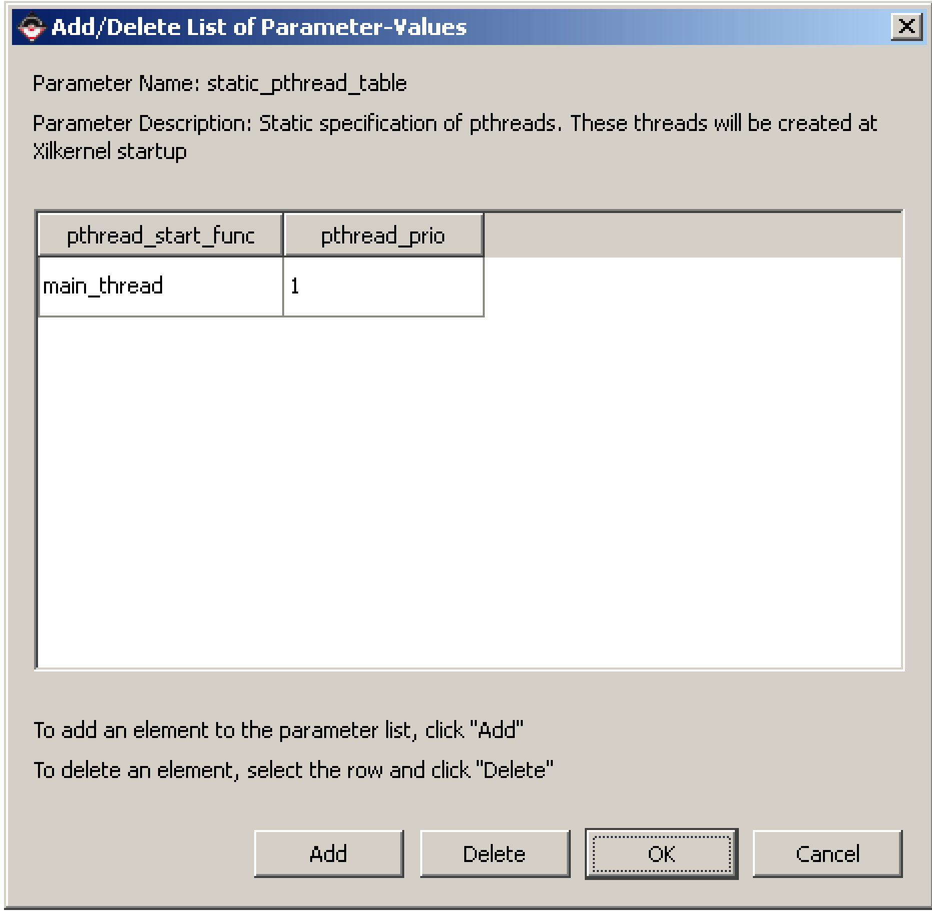
Configuration for OS: xilkernel v4.00.a

Name	Current Value	Default Value	Type	Description
xilkernel				
systmr_spec				
systmr_dev	*none*	none	peri...	Specify the instance nam...
systmr_freq	*400000000*	100000000	int	Specify the clock frequen...
systmr_interval	*10*	10	int	Specify the time interval ...
config_pthread_support	true	true	bool	Configure pthread suppo...
max_pthreads	*10*	10	int	Maximum number of simu...
pthread_stack_size	*32768*	1000	int	Size of the stack to be all...
config_pthread_mutex	false	false	bool	Configure pthread mutex...
max_pthread_mutex	*20*	10	int	Maximum number of mut...
max_pthread_mutex_waitq	*10*	10	int	Length of each mutex loc...
static_pthread_table	Edit...		array	Static specification of pth...
config_sched	true	true	bool	Configure the scheduling...
sched_type	SCHED_RR	SCHED_RR	enum	Choose the global kernel ...
n_prio	*32*	32	int	The number of priority le...
max_readyq	*20*	10	int	Length of each ReadyQ. ...
config_time	true	false	bool	Configure time/timer rela...
max_tmrs	*20*	10	int	Maximum number of soft ...
config_sema	true	false	bool	Configure semaphore su...
max_sem	*50*	10	int	Maximum number of sem...
max_sem_waitq	*20*	10	int	Length of each semapho...
config_named_sema	false	false	bool	Configure named semap...
config_msgq	false	false	bool	Configure message queu...
config_msgq	false	false	bool	Configure message queu...
config_shm	false	false	bool	Configure shared memor...
config_bufmalloc	false	false	bool	Configure buffer memory...
config_elf_process				
copyoutfiles	false	false	bool	Copy OS files to user spe...
config_debug_support	false	false	bool	Control various debuggin...
enhanced_features	true	false	bool	Configure enhanced feat...
config_kill	false	false	bool	Include the kill() function...
config_yield	true	false	bool	Include the yield() functi...
stdin	RS232_Uart_1	none	peri...	Specify the instance nam...
stdout	RS232_Uart_1	none	peri...	Specify the instance nam...
sysintc_spec	xps_intc_0	none	peri...	Specify the instance nam...

Note: Presentation applies to the ML507

Software Platform Settings

- **Edit the static_pthread_table**
  - Click Add
  - Set **pthread_start_func = main_thread**
  - Set **pthread_prio = 1**



Add/Delete List of Parameter-Values

Parameter Name: static_pthread_table

Parameter Description: Static specification of pthreads. These threads will be created at Xilkernel startup

pthread_start_func	pthread_prio
main_thread	1

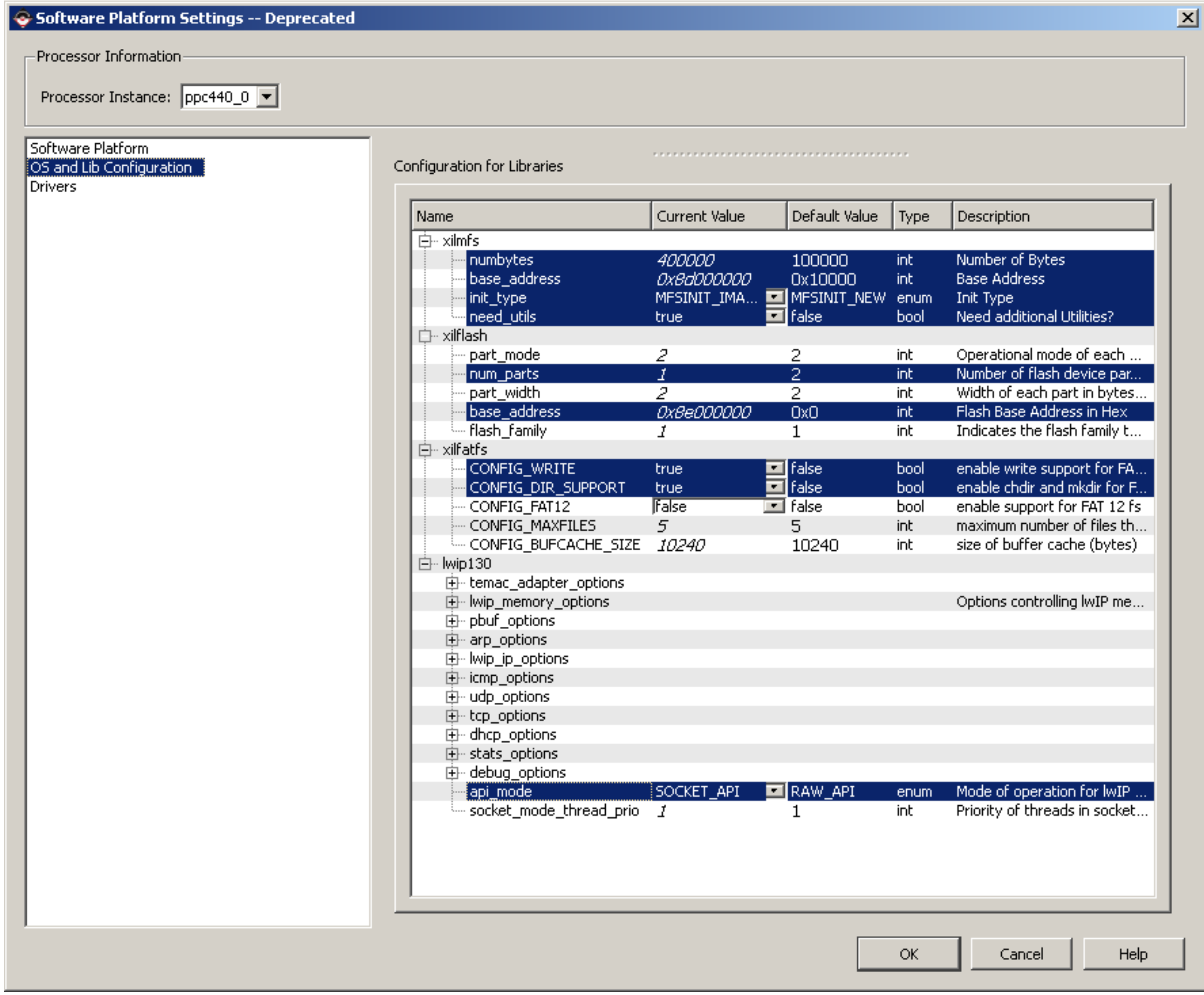
To add an element to the parameter list, click "Add"

To delete an element, select the row and click "Delete"

Note: Presentation applies to the ML507

Software Platform Settings

- **Under OS and Libraries, Configuration for Libraries, make these settings**
  - numbytes = **400000**
  - base_address = **0x8d000000**
    - **sram flash address**
  - int_type to **MFSINIT_IMAGE**
  - need_utils = **true**
  - num_parts: 1
  - base_address = **0x8e000000**
    - sram address
  - CONFIG_WRITE = **true**
  - CONFIG_DIR_SUPPORT = **true**
  - api_mode = **SOCKET_API**



Software Platform Settings -- Deprecated

Processor Information

Processor Instance: ppc440_0

Software Platform
OS and Lib Configuration
Drivers

Configuration for Libraries

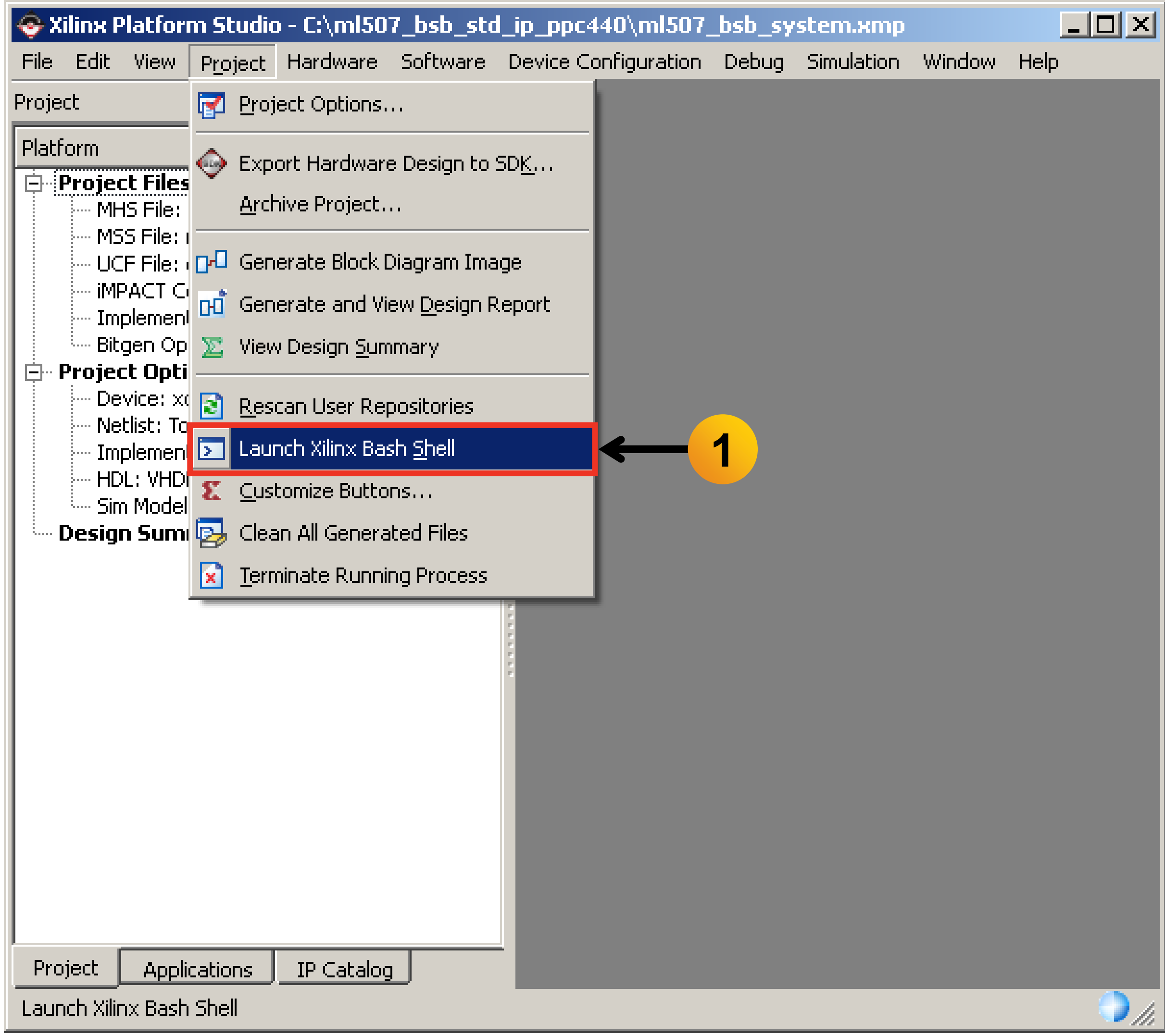
Name	Current Value	Default Value	Type	Description
xilmfs				
numbytes	400000	100000	int	Number of Bytes
base_address	0x8d000000	0x10000	int	Base Address
init_type	MFSINIT_IMA...	MFSINIT_NEW	enum	Init Type
need_utils	true	false	bool	Need additional Utilities?
xilflash				
part_mode	2	2	int	Operational mode of each ...
num_parts	1	2	int	Number of flash device par...
part_width	2	2	int	Width of each part in bytes...
base_address	0x8e000000	0x0	int	Flash Base Address in Hex
flash_family	1	1	int	Indicates the flash family t...
xilfatfs				
CONFIG_WRITE	true	false	bool	enable write support for FA...
CONFIG_DIR_SUPPORT	true	false	bool	enable chdir and mkdir for F...
CONFIG_FAT12	false	false	bool	enable support for FAT 12 fs
CONFIG_MAXFILES	5	5	int	maximum number of files th...
CONFIG_BUFCACHE_SIZE	10240	10240	int	size of buffer cache (bytes)
lwip130				
temac_adapter_options				
lwip_memory_options				Options controlling lwIP me...
pbuf_options				
arp_options				
lwip_ip_options				
icmp_options				
udp_options				
tcp_options				
dhcp_options				
stats_options				
debug_options				
api_mode	SOCKET_API	RAW_API	enum	Mode of operation for lwIP ...
socket_mode_thread_prio	1	1	int	Priority of threads in socket...

Note: Presentation applies to the ML507

Create MFS Image

Create MFS Image

- **Open an EDK shell**
  - Select Project → Launch EDK Shell (1)



Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp

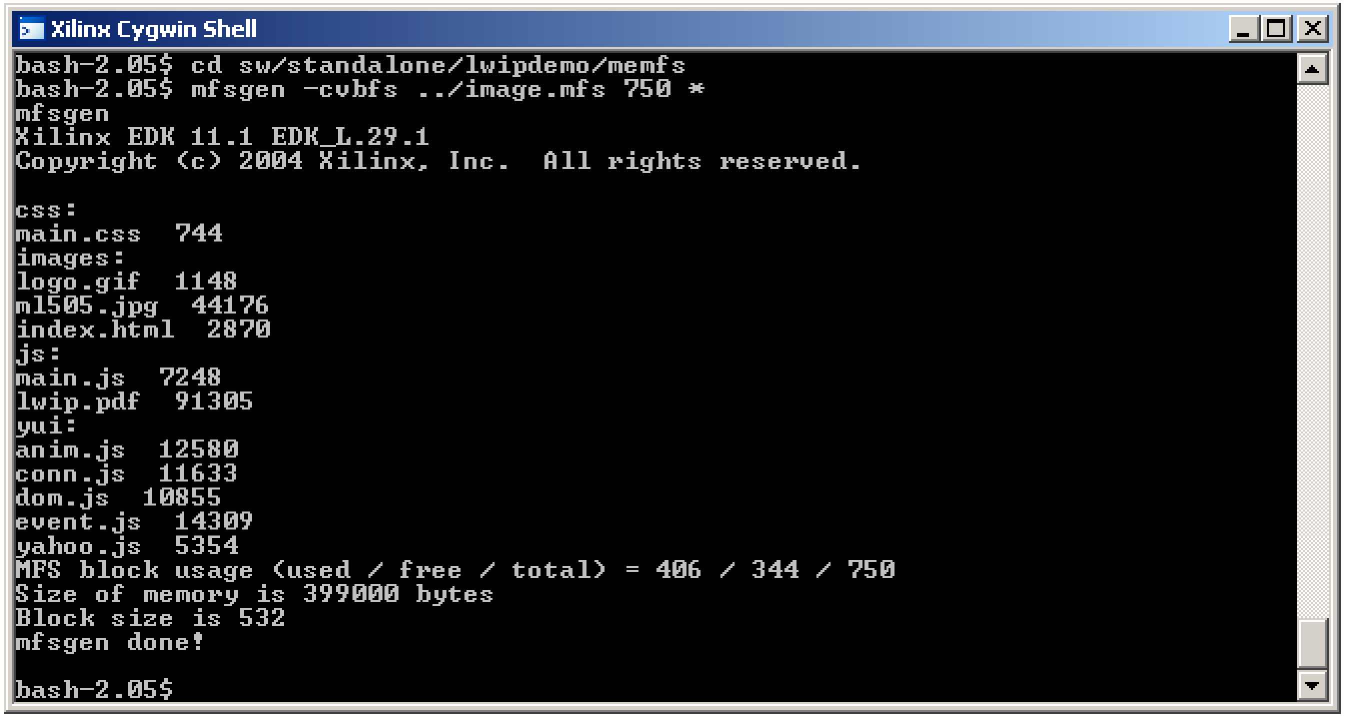
Note: Presentation applies to the ML507

Create MFS Image

- **At the bash prompt, type (1):**

  cd sw/standalone/lwipdemo/memfs

  mfsgen -cvbfs ../image.mfs 750 *

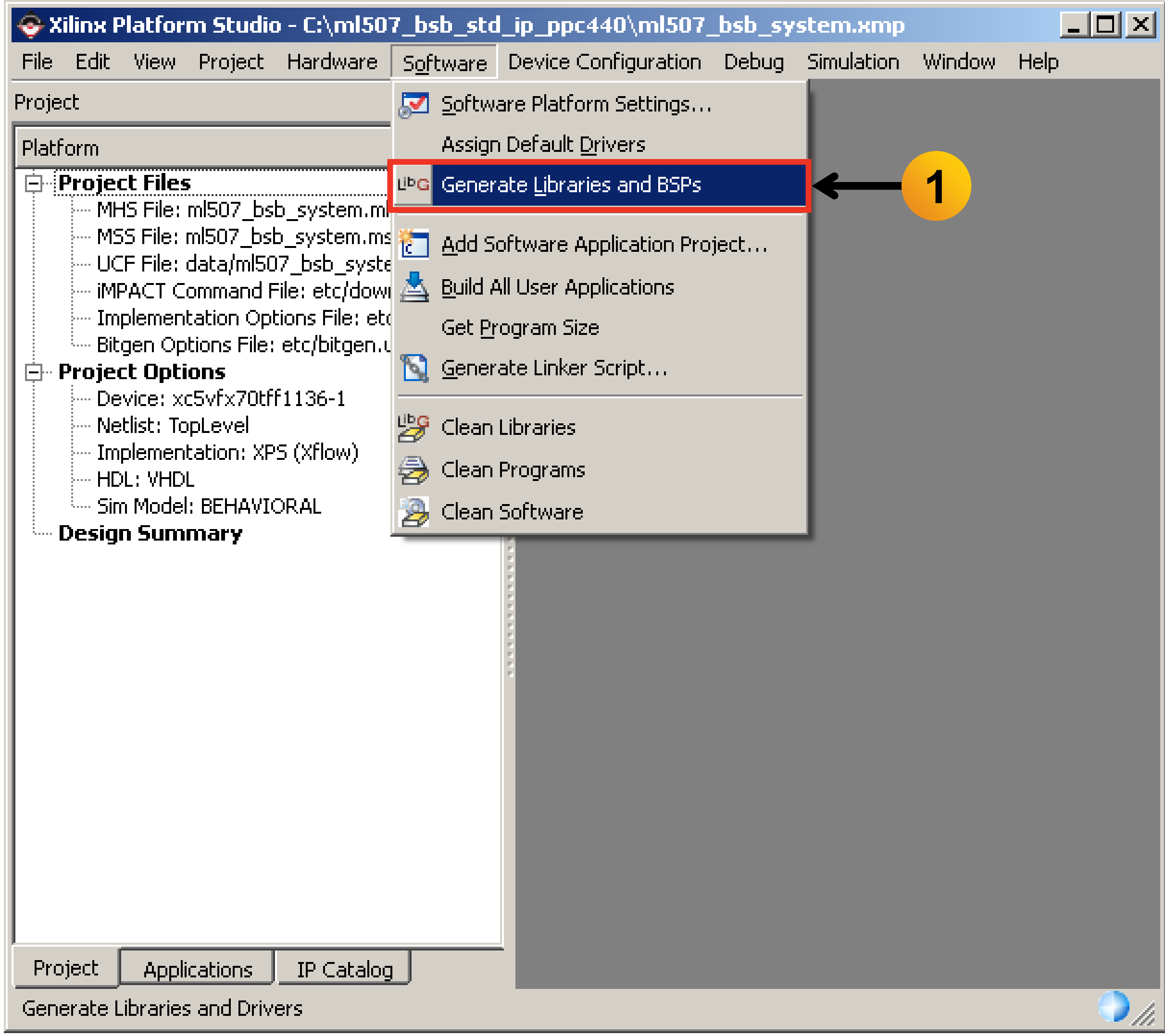


```
bash-2.05$ cd sw/standalone/lwipdemo/memfs
bash-2.05$ mfsgen -cvbfs ../image.mfs 750 *
mfsgen
Xilinx EDK 11.1 EDK_L.29.1
Copyright (c) 2004 Xilinx, Inc.  All rights reserved.

css:
main.css  744
images:
logo.gif  1148
ml505.jpg  44176
index.html  2870
js:
main.js  7248
lwip.pdf  91305
yui:
anim.js  12580
conn.js  11633
dom.js  10855
event.js  14309
yahoo.js  5354
MFS block usage (used / free / total) = 406 / 344 / 750
Size of memory is 399000 bytes
Block size is 532
mfsgen done!

bash-2.05$
```

Compile Standard IP Design

Generate the ELF Files

- **Generate the libraries needed to create the bitstream**
  - Select **Software** → **Generate Libraries and BSPs** (1)



Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp

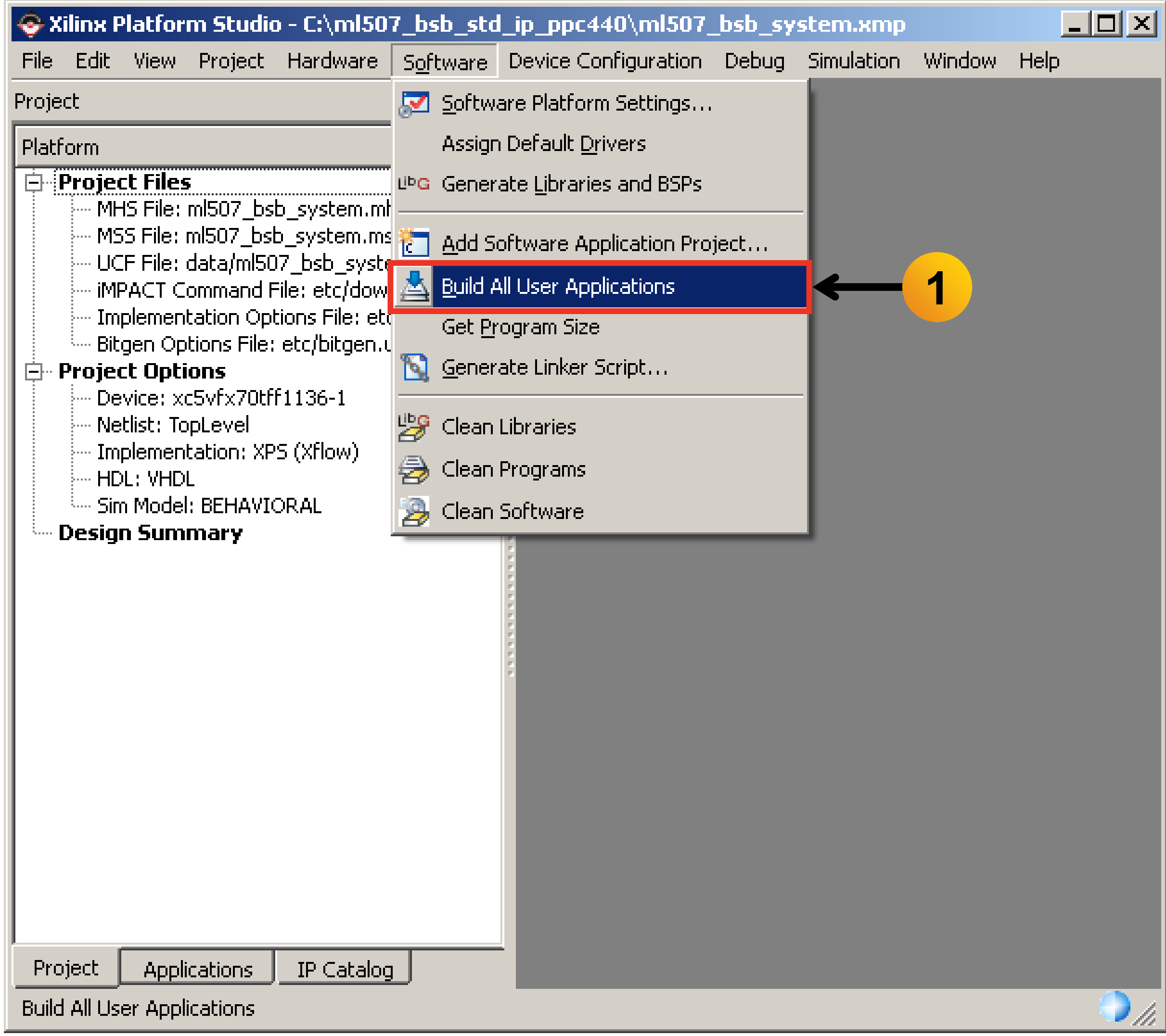
File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help
Project
Platform
Project Files
MHS File: ml507_bsb_system.mh
MSS File: ml507_bsb_system.ms
UCF File: data/ml507_bsb_syste
iMPACT Command File: etc/dowr
Implementation Options File: etc
Bitgen Options File: etc/bitgen.u
Project Options
Device: xc5vfx70tff1136-1
Netlist: TopLevel
Implementation: XPS (Xflow)
HDL: VHDL
Sim Model: BEHAVIORAL
Design Summary
Software Platform Settings...
Assign Default Drivers
Generate Libraries and BSPs
Add Software Application Project...
Build All User Applications
Get Program Size
Generate Linker Script...
Clean Libraries
Clean Programs
Clean Software
1
Project
Applications
IP Catalog

Generate Libraries and Drivers

Note: Presentation applies to the ML507

Generate the ELF Files

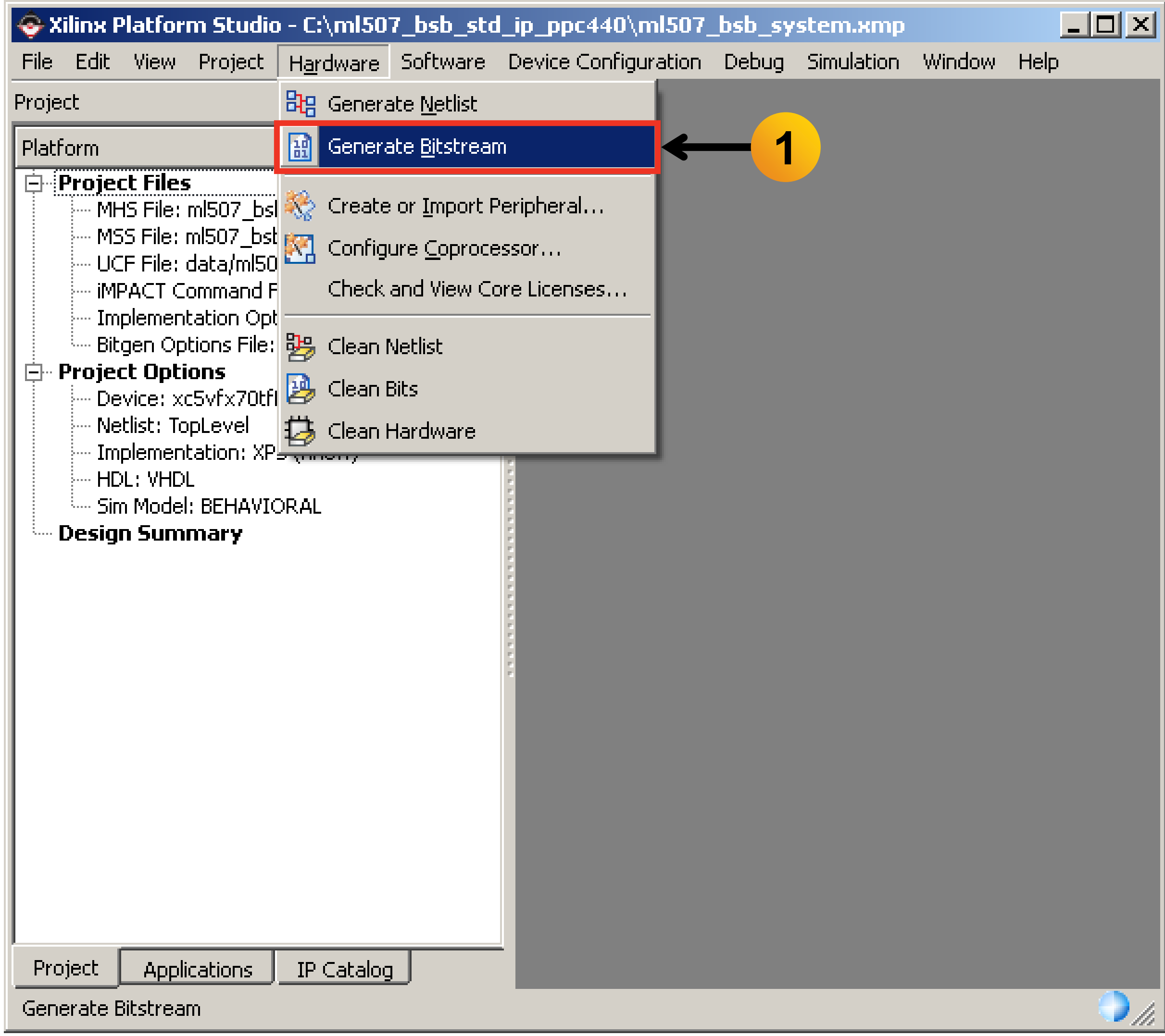
- **Compile the Software Applications and create an executable (executable.elf)**
  - Select **Software → Build All User Applications** (1)


Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp
File
Edit
View
Project
Hardware
Software
Device Configuration
Debug
Simulation
Window
Help
Project
Platform
Project Files
MHS File: ml507_bsb_system.mh
MSS File: ml507_bsb_system.ms
UCF File: data/ml507_bsb_syste
iMPACT Command File: etc/dow
Implementation Options File: etc
Bitgen Options File: etc/bitgen.u
Project Options
Device: xc5vfx70tff1136-1
Netlist: TopLevel
Implementation: XPS (Xflow)
HDL: VHDL
Sim Model: BEHAVIORAL
Design Summary
Software Platform Settings...
Assign Default Drivers
Generate Libraries and BSPs
Add Software Application Project...
Build All User Applications
Get Program Size
Generate Linker Script...
Clean Libraries
Clean Programs
Clean Software
1
Project
Applications
IP Catalog
Build All User Applications

Note: Presentation applies to the ML507

Generate the Bitstream

- **Create the hardware design, ml507_bsb_system.bit that is located in <project directory>/implementation**
  - Select **Hardware → Generate Bitstream** (1)

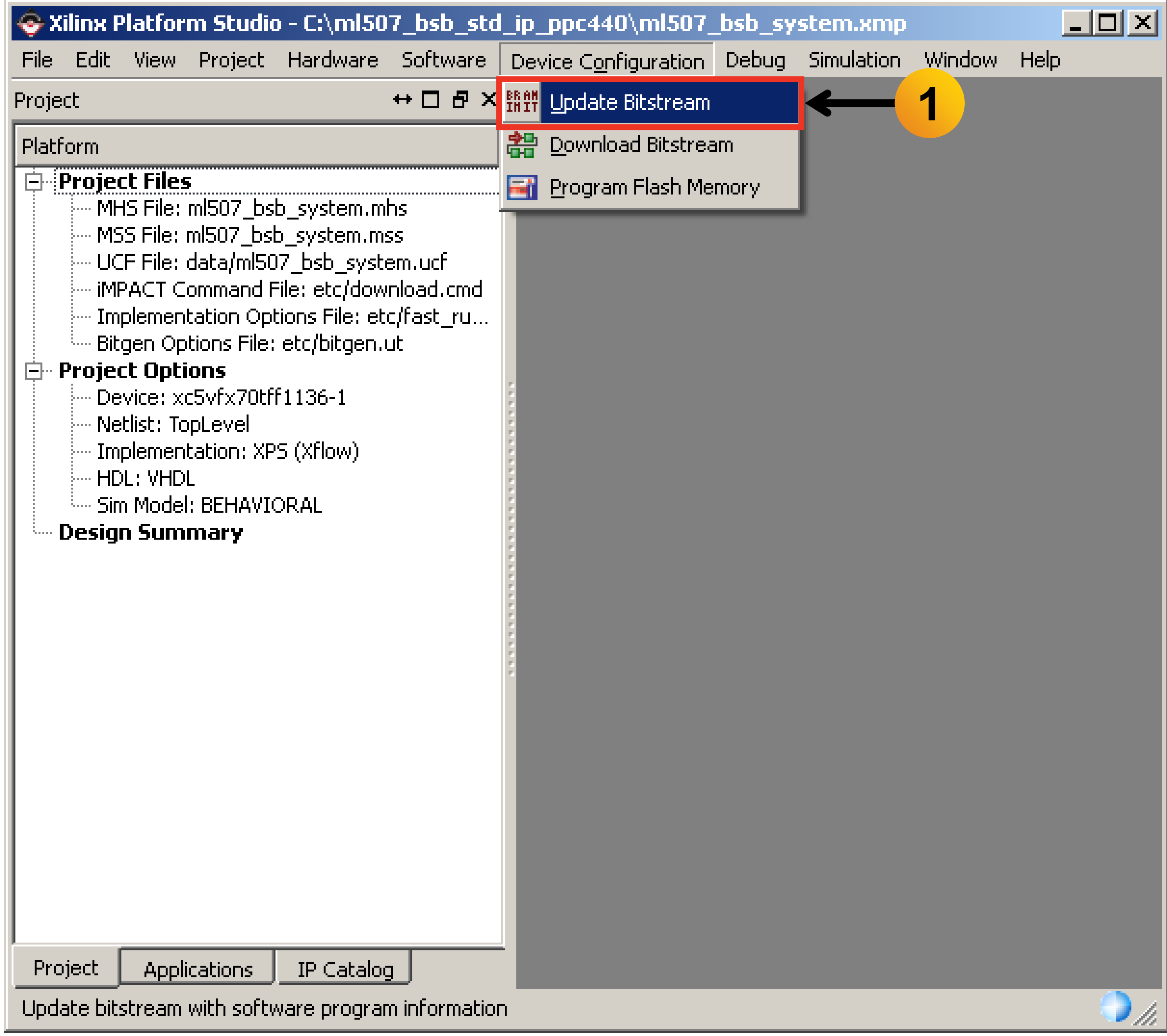


Loading a Bootloop ELF into the Block RAM

- A concatenated software/hardware file, known as an ACE file, is useful for loading large programs, such as a Linux, VxWorks, or U-Boot into the external memory
- A bootloop program must be used to occupy the processor until the software is loaded into memory
- The following pages show how to initialize a bootloop program into Block RAM and to test its existence

Loading a Bootloop ELF into the Block RAM

- Update the bitstream (download.bit) with a bootloop ELF file (ppc440_0.elf)
  - Select **Device Configuration → Update Bitstream** (1)



Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Project

Platform

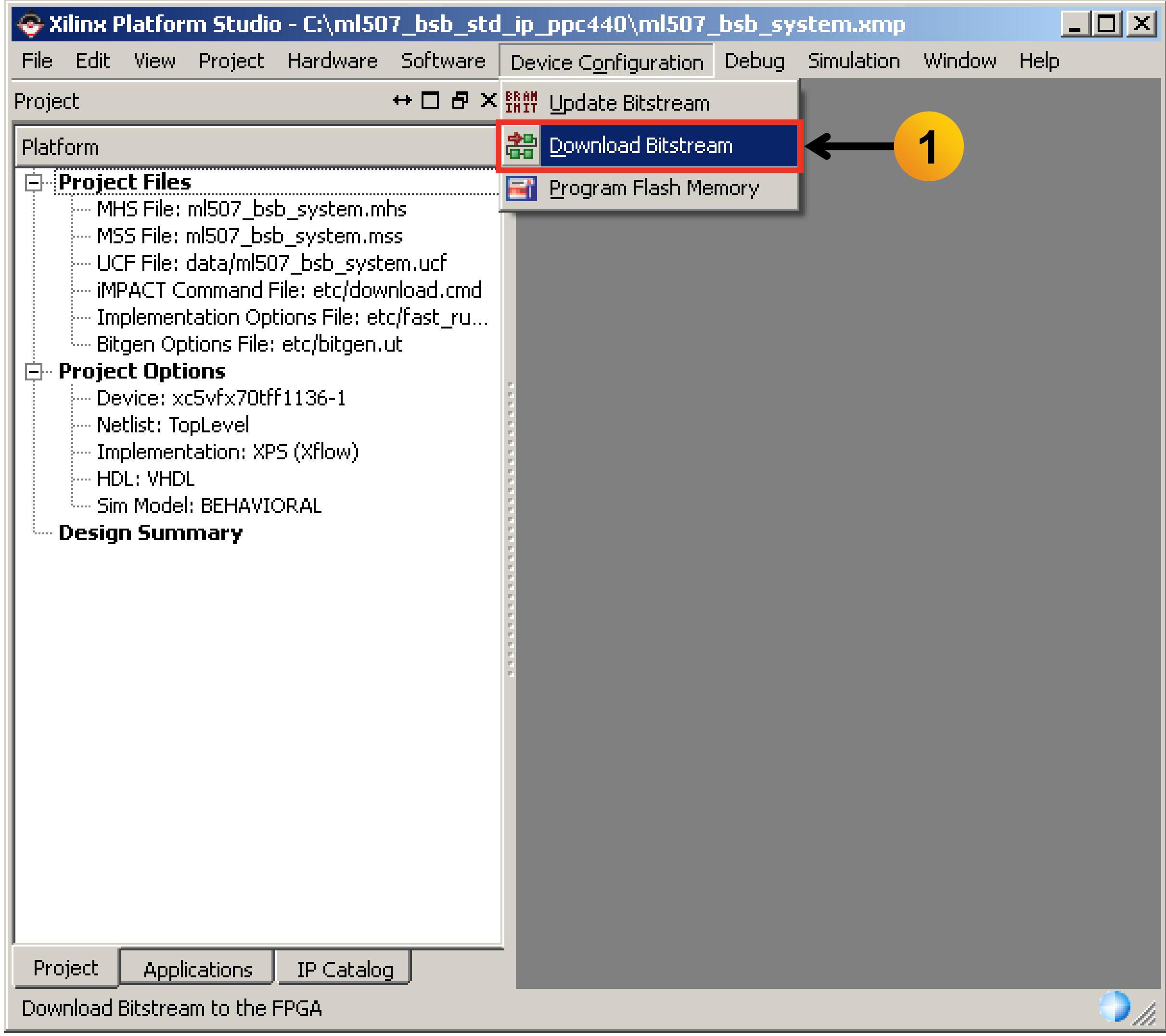
- Project Files
  - MHS File: ml507_bsb_system.mhs
  - MSS File: ml507_bsb_system.mss
  - UCF File: data/ml507_bsb_system.ucf
  - iMPACT Command File: etc/download.cmd
  - Implementation Options File: etc/fast_ru...
  - Bitgen Options File: etc/bitgen.ut
- Project Options
  - Device: xc5vfx70tff1136-1
  - Netlist: TopLevel
  - Implementation: XPS (Xflow)
  - HDL: VHDL
  - Sim Model: BEHAVIORAL
- Design Summary

Update bitstream with software program information

Note: Presentation applies to the ML507

Loading a Bootloop ELF into the Block RAM

- **Load the new design onto the FPGA and load the bootloop program into the Block RAM**
  - Select **Device Configuration** → **Download Bitstream** (1)



Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help
Project
Platform
Update Bitstream
Download Bitstream
Program Flash Memory
1
Project Applications IP Catalog

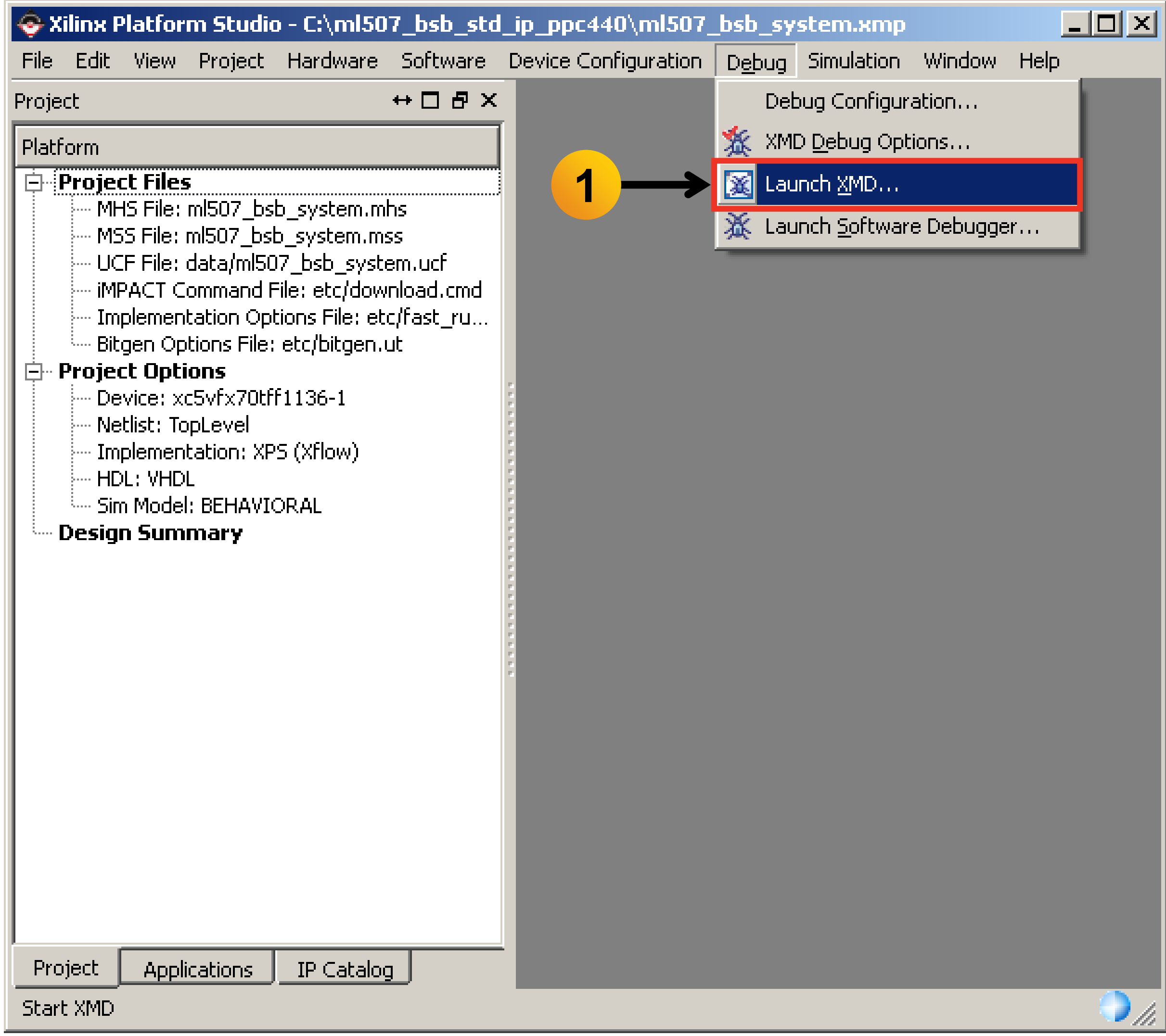
- Project Files
  - MHS File: ml507_bsb_system.mhs
  - MSS File: ml507_bsb_system.mss
  - UCF File: data/ml507_bsb_system.ucf
  - iMPACT Command File: etc/download.cmd
  - Implementation Options File: etc/fast_ru...
  - Bitgen Options File: etc/bitgen.ut
- Project Options
  - Device: xc5vfx70tff1136-1
  - Netlist: TopLevel
  - Implementation: XPS (Xflow)
  - HDL: VHDL
  - Sim Model: BEHAVIORAL
- Design Summary

Download Bitstream to the FPGA

Note: Presentation applies to the ML507

Loading a Bootloop ELF into the Block RAM

- **A memory read can be executed to test if bootloop was successfully loaded**
  - Select **Debug → Launch XMD** (1)



Xilinx Platform Studio - C:\ml507_bsb_std_ip_ppc440\ml507_bsb_system.xmp

Project

Platform

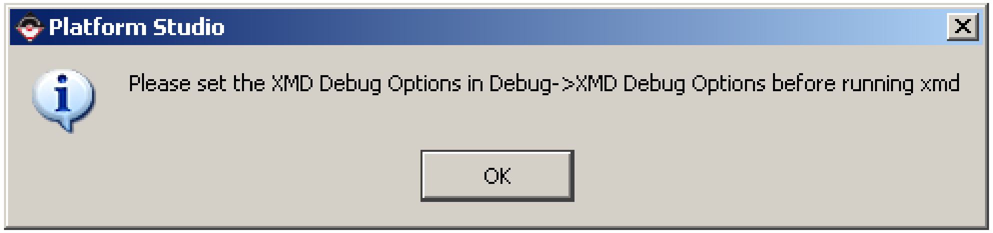
- Project Files
  - MHS File: ml507_bsb_system.mhs
  - MSS File: ml507_bsb_system.mss
  - UCF File: data/ml507_bsb_system.ucf
  - iMPACT Command File: etc/download.cmd
  - Implementation Options File: etc/fast_ru...
  - Bitgen Options File: etc/bitgen.ut
- Project Options
  - Device: xc5vfx70tff1136-1
  - Netlist: TopLevel
  - Implementation: XPS (Xflow)
  - HDL: VHDL
  - Sim Model: BEHAVIORAL
- Design Summary

Start XMD

Note: Presentation applies to the ML507

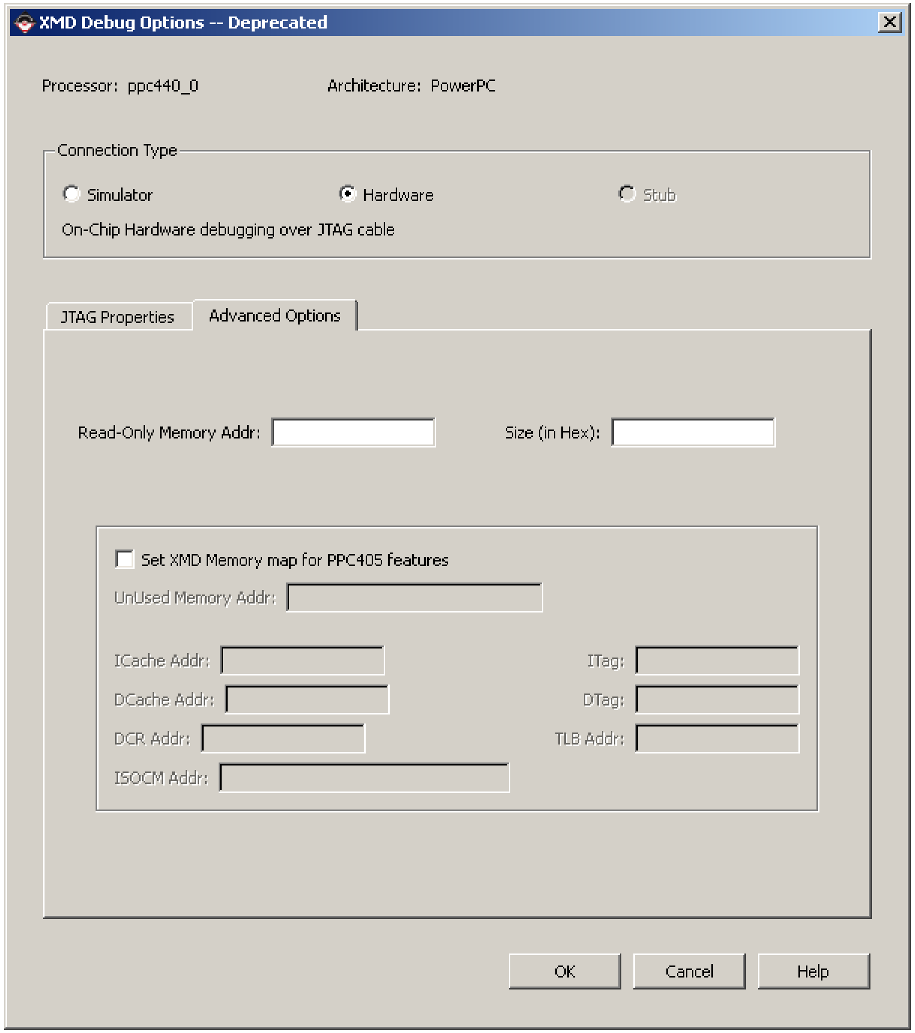
Loading a Bootloop ELF into the Block RAM

- **The first time XMD runs on a project, the XMD Debug options must be set**



Platform Studio

Please set the XMD Debug Options in Debug->XMD Debug Options before running xmd



XMD Debug Options -- Deprecated

Processor: ppc440_0

Architecture: PowerPC

Connection Type

○ Simulator ● Hardware ○ Stub

On-Chip Hardware debugging over JTAG cable

Read-Only Memory Addr:

Size (in Hex):

□ Set XMD Memory map for PPC405 features

UnUsed Memory Addr:

ICache Addr:

ITag:

DCache Addr:

DTag:

DCR Addr:

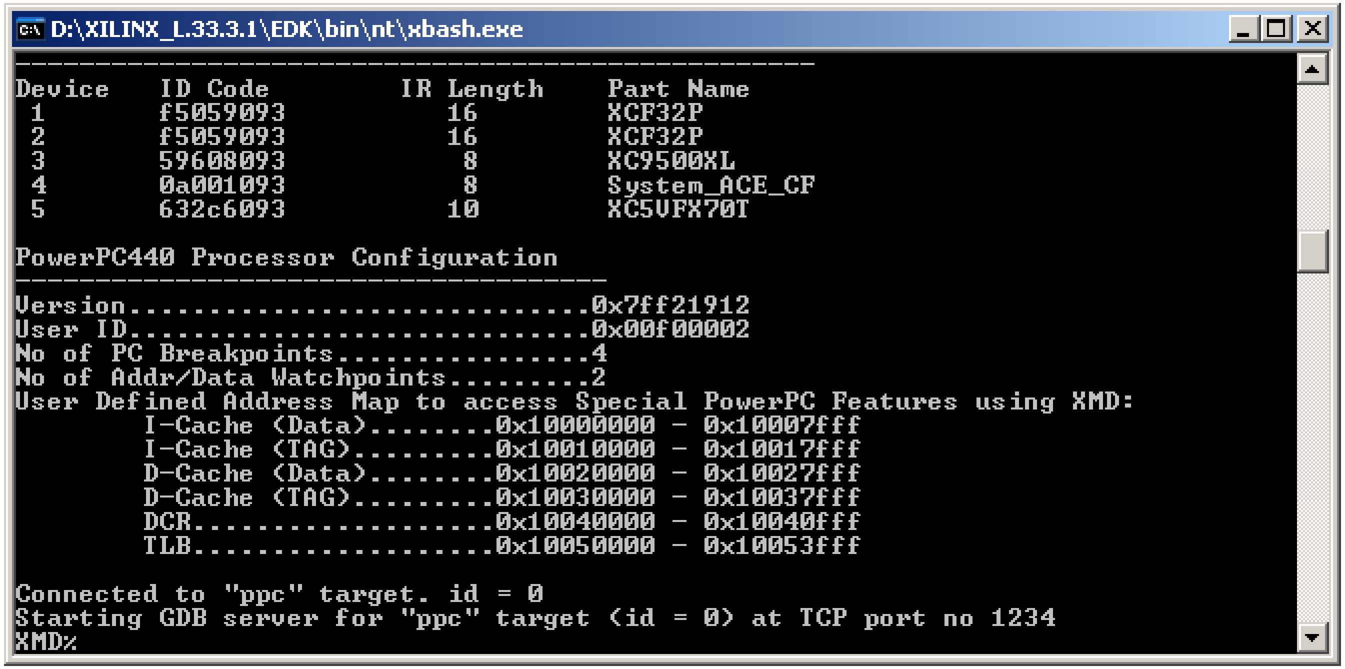
TLB Addr:

ISOCM Addr:

Note: Presentation applies to the ML507

Loading a Bootloop ELF into the Block RAM

- **XMD opens and connects to the processor, using the default options**



```
--------------------------------------------------
Device   ID Code        IR Length    Part Name
 1       f5059093         16         XCF32P
 2       f5059093         16         XCF32P
 3       59608093          8         XC9500XL
 4       0a001093          8         System_ACE_CF
 5       632c6093         10         XC5VFX70T

PowerPC440 Processor Configuration
-------------------------------------
Version.............................0x7ff21912
User ID.............................0x00f00002
No of PC Breakpoints................4
No of Addr/Data Watchpoints.........2
User Defined Address Map to access Special PowerPC Features using XMD:
        I-Cache (Data)........0x10000000 - 0x10007fff
        I-Cache (TAG).........0x10010000 - 0x10017fff
        D-Cache (Data)........0x10020000 - 0x10027fff
        D-Cache (TAG).........0x10030000 - 0x10037fff
        DCR...................0x10040000 - 0x10040fff
        TLB...................0x10050000 - 0x10053fff

Connected to "ppc" target. id = 0
Starting GDB server for "ppc" target (id = 0) at TCP port no 1234
XMD%
```

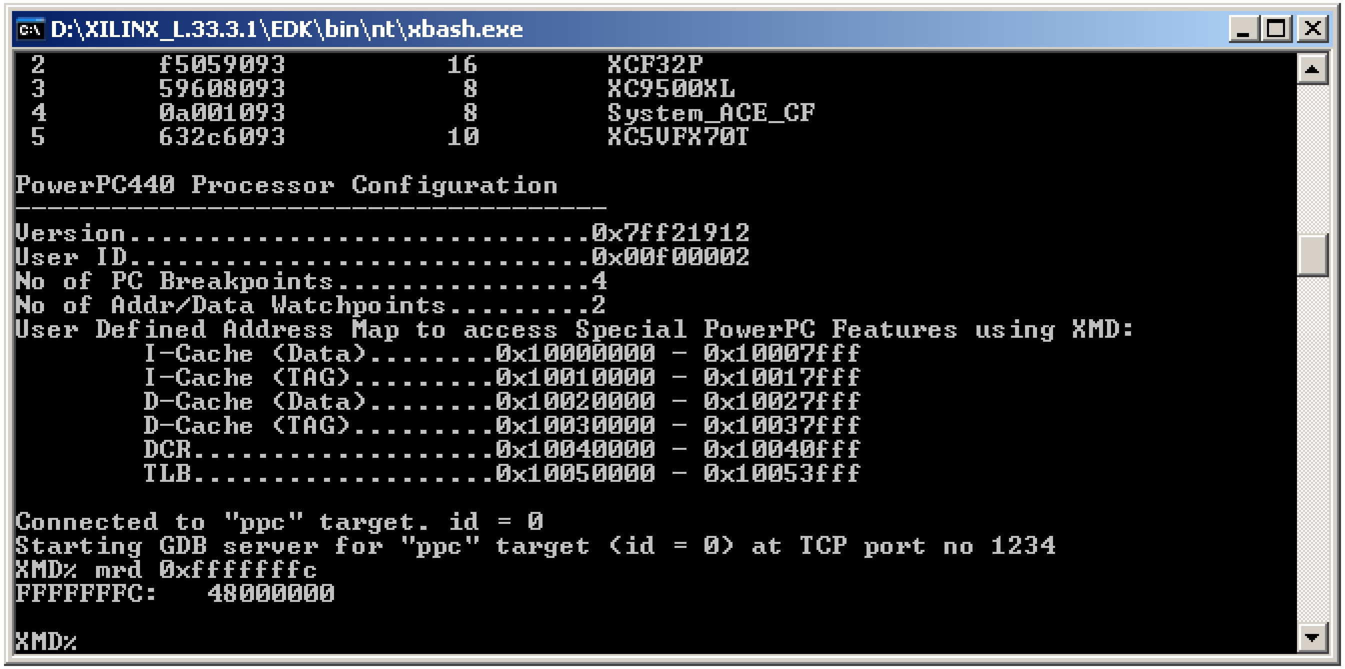
Note: Presentation applies to the ML507

Loading a Bootloop ELF into the Block RAM

- To execute a memory read, type

  mrd 0xfffffffc

- This will read the memory address at the reset vector; the value should be 0x48000000 as shown below



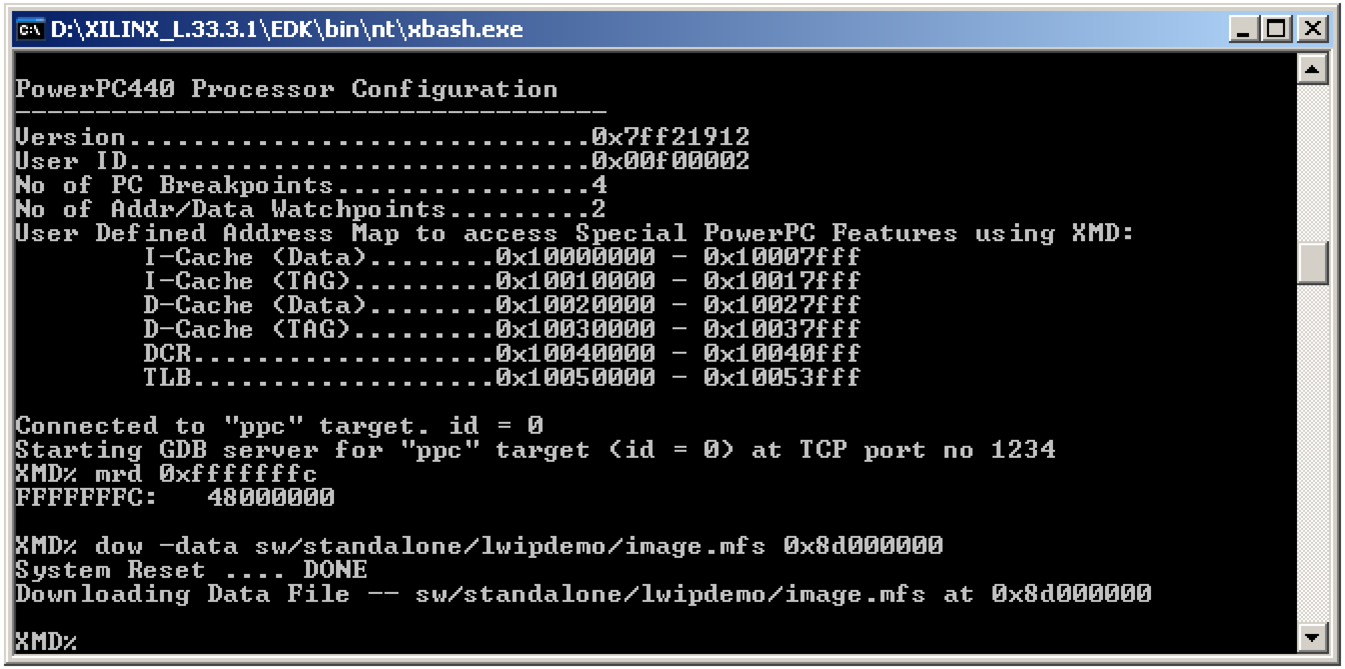
```
 2        f5059093          16         XCF32P
 3        59608093           8         XC9500XL
 4        0a001093           8         System_ACE_CF
 5        632c6093          10         XC5VFX70T

PowerPC440 Processor Configuration
-------------------------------------
Version....................................0x7ff21912
User ID....................................0x00f00002
No of PC Breakpoints.................4
No of Addr/Data Watchpoints..........2
User Defined Address Map to access Special PowerPC Features using XMD:
        I-Cache (Data)........0x10000000 - 0x10007fff
        I-Cache (TAG).........0x10010000 - 0x10017fff
        D-Cache (Data)........0x10020000 - 0x10027fff
        D-Cache (TAG).........0x10030000 - 0x10037fff
        DCR...................0x10040000 - 0x10040fff
        TLB...................0x10050000 - 0x10053fff

Connected to "ppc" target. id = 0
Starting GDB server for "ppc" target (id = 0) at TCP port no 1234
XMD% mrd 0xfffffffc
FFFFFFFC:   48000000

XMD%
```

Note: Presentation applies to the ML507

Running the Lwipdemo Application

- **Download the MFS image:**

  dow -data sw/standalone/lwipdemo/image.mfs 0x8d000000



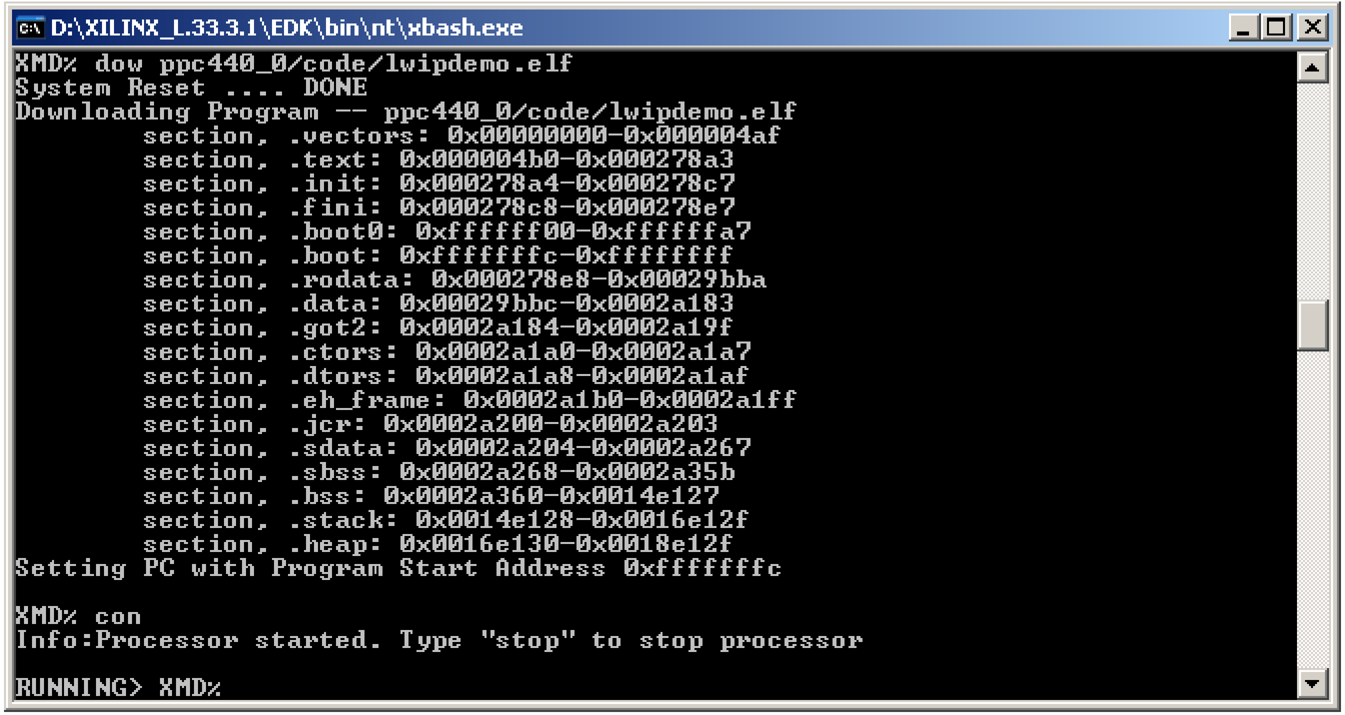
```
PowerPC440 Processor Configuration
-------------------------------------
Version.............................0x7ff21912
User ID.............................0x00f00002
No of PC Breakpoints................4
No of Addr/Data Watchpoints.........2
User Defined Address Map to access Special PowerPC Features using XMD:
        I-Cache (Data)........0x10000000 - 0x10007fff
        I-Cache (TAG).........0x10010000 - 0x10017fff
        D-Cache (Data)........0x10020000 - 0x10027fff
        D-Cache (TAG).........0x10030000 - 0x10037fff
        DCR...................0x10040000 - 0x10040fff
        TLB...................0x10050000 - 0x10053fff

Connected to "ppc" target. id = 0
Starting GDB server for "ppc" target (id = 0) at TCP port no 1234
XMD% mrd 0xfffffffc
FFFFFFFC:   48000000

XMD% dow -data sw/standalone/lwipdemo/image.mfs 0x8d000000
System Reset .... DONE
Downloading Data File -- sw/standalone/lwipdemo/image.mfs at 0x8d000000

XMD%
```

Running the Lwipdemo Application

- **Download and run the Lwipdemo Application:**

dow ppc440_0/code/lwipdemo.elf

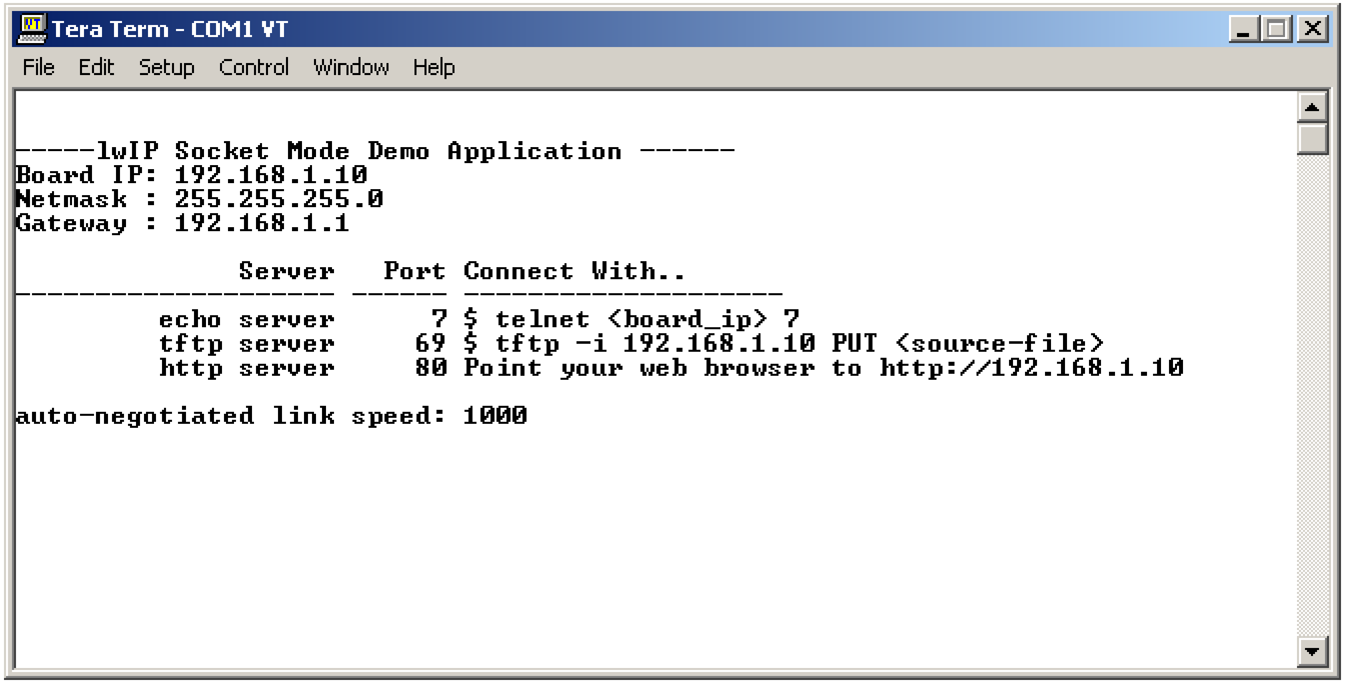
con



```
XMD% dow ppc440_0/code/lwipdemo.elf
System Reset .... DONE
Downloading Program -- ppc440_0/code/lwipdemo.elf
        section, .vectors: 0x00000000-0x000004af
        section, .text: 0x000004b0-0x000278a3
        section, .init: 0x000278a4-0x000278c7
        section, .fini: 0x000278c8-0x000278e7
        section, .boot0: 0xffffff00-0xffffffa7
        section, .boot: 0xfffffffc-0xffffffff
        section, .rodata: 0x000278e8-0x00029bba
        section, .data: 0x00029bbc-0x0002a183
        section, .got2: 0x0002a184-0x0002a19f
        section, .ctors: 0x0002a1a0-0x0002a1a7
        section, .dtors: 0x0002a1a8-0x0002a1af
        section, .eh_frame: 0x0002a1b0-0x0002a1ff
        section, .jcr: 0x0002a200-0x0002a203
        section, .sdata: 0x0002a204-0x0002a267
        section, .sbss: 0x0002a268-0x0002a35b
        section, .bss: 0x0002a360-0x0014e127
        section, .stack: 0x0014e128-0x0016e12f
        section, .heap: 0x0016e130-0x0018e12f
Setting PC with Program Start Address 0xfffffffc

XMD% con
Info:Processor started. Type "stop" to stop processor

RUNNING> XMD%
```

Running the Lwipdemo Application

- View the output in the terminal window

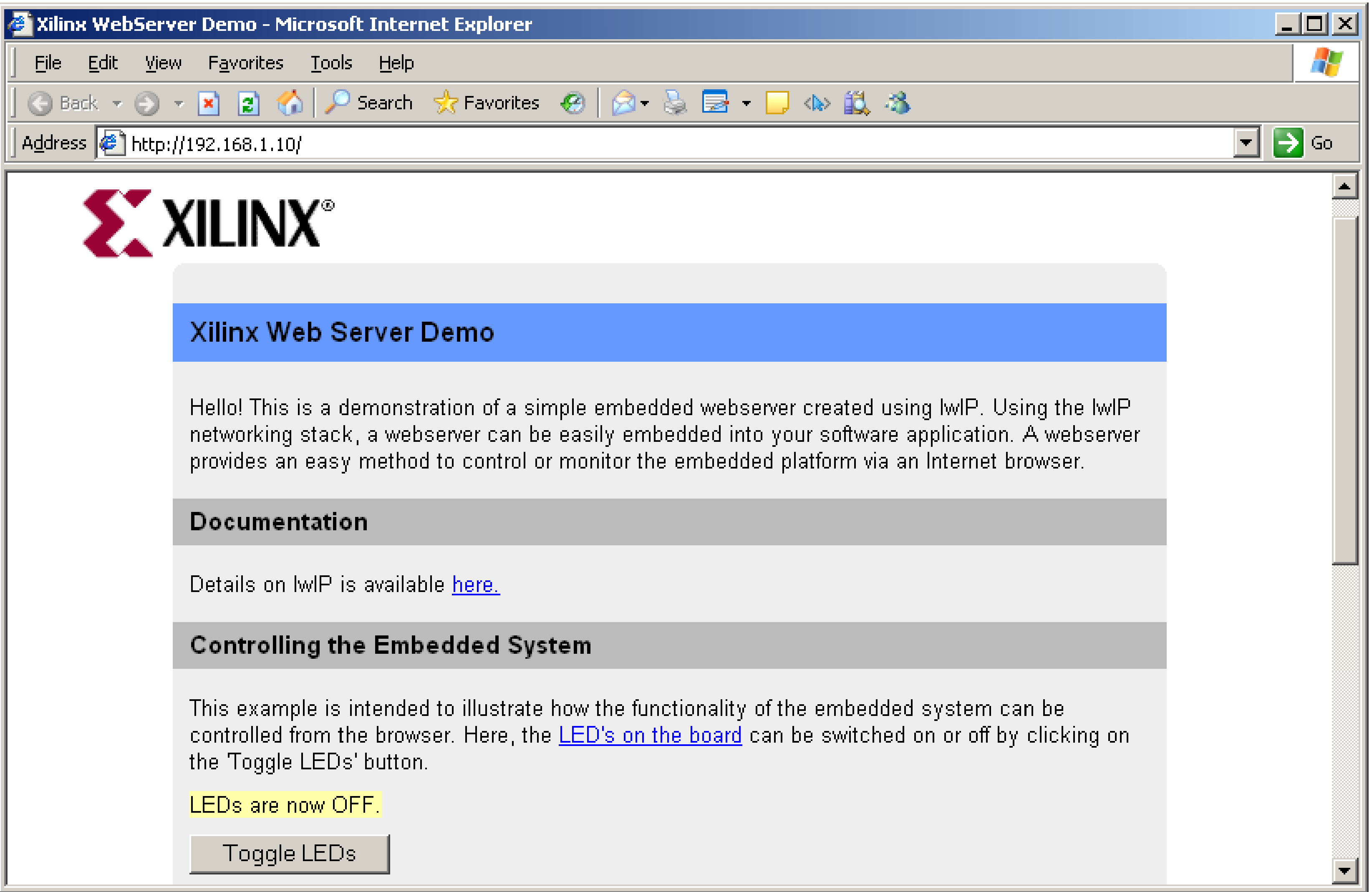


```
-----lwIP Socket Mode Demo Application ------
Board IP: 192.168.1.10
Netmask : 255.255.255.0
Gateway : 192.168.1.1

              Server   Port Connect With..
-------------------- ------ --------------------
         echo server      7 $ telnet <board_ip> 7
         tftp server     69 $ tftp -i 192.168.1.10 PUT <source-file>
         http server     80 Point your web browser to http://192.168.1.10

auto-negotiated link speed: 1000
```

Note: Presentation applies to the ML505, ML506, and ML507

Running the Lwipdemo Application

- Open a web browser to address 192.168.1.10



Xilinx WebServer Demo - Microsoft Internet Explorer
File Edit View Favorites Tools Help
Back Search Favorites
Address http://192.168.1.10/
Go
XILINX®

Xilinx Web Server Demo

Hello! This is a demonstration of a simple embedded webserver created using lwIP. Using the lwIP networking stack, a webserver can be easily embedded into your software application. A webserver provides an easy method to control or monitor the embedded platform via an Internet browser.

Documentation

Details on lwIP is available here.

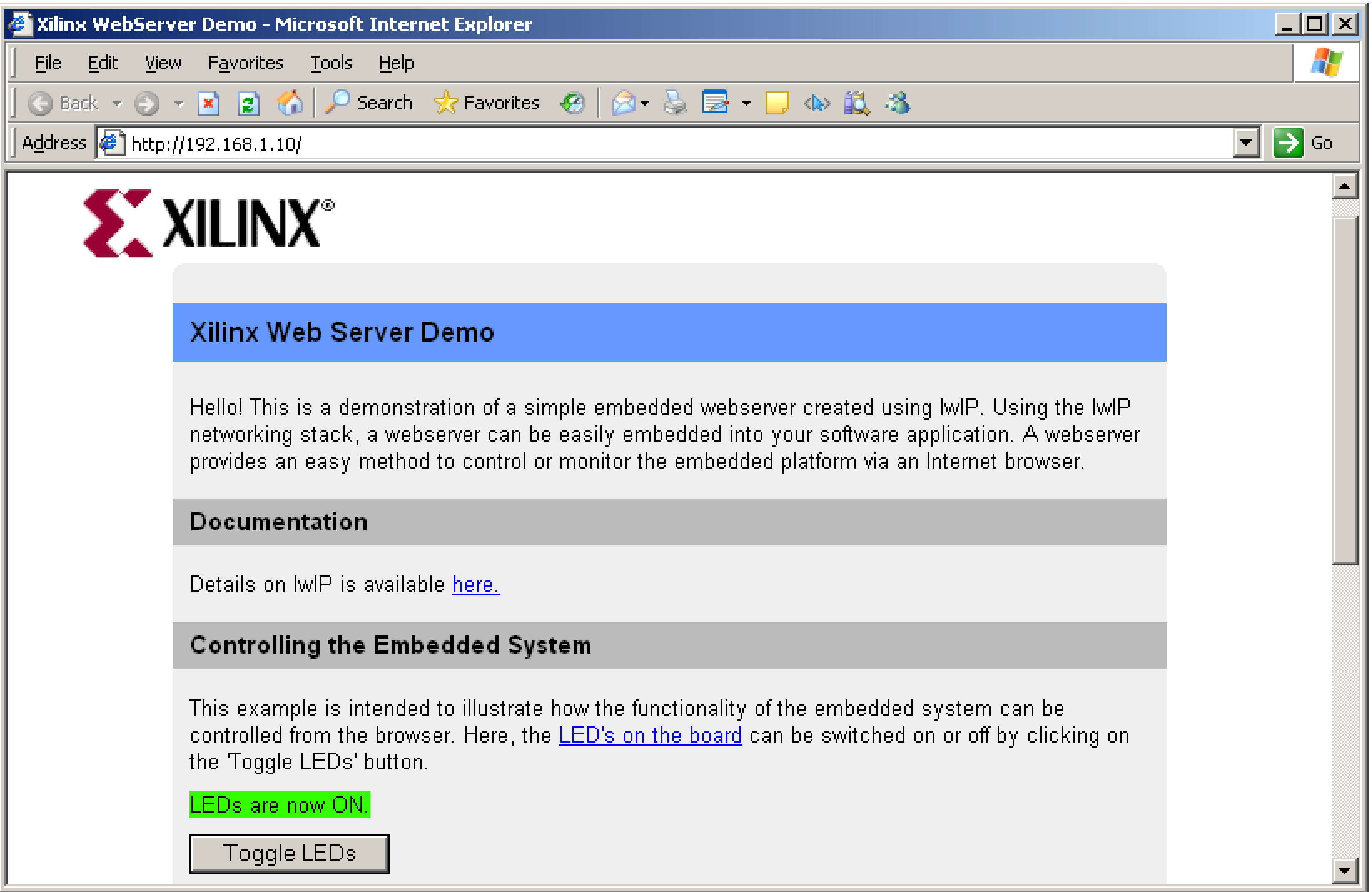
Controlling the Embedded System

This example is intended to illustrate how the functionality of the embedded system can be controlled from the browser. Here, the LED's on the board can be switched on or off by clicking on the 'Toggle LEDs' button.

LEDs are now OFF.

Running the Lwipdemo Application

- Click the Toggle LEDs button; view change on ML507



Xilinx WebServer Demo - Microsoft Internet Explorer
File Edit View Favorites Tools Help
Back
Search
Favorites
Address
http://192.168.1.10/
Go
XILINX®

Xilinx Web Server Demo

Hello! This is a demonstration of a simple embedded webserver created using lwIP. Using the lwIP networking stack, a webserver can be easily embedded into your software application. A webserver provides an easy method to control or monitor the embedded platform via an Internet browser.

Documentation

Details on lwIP is available here.

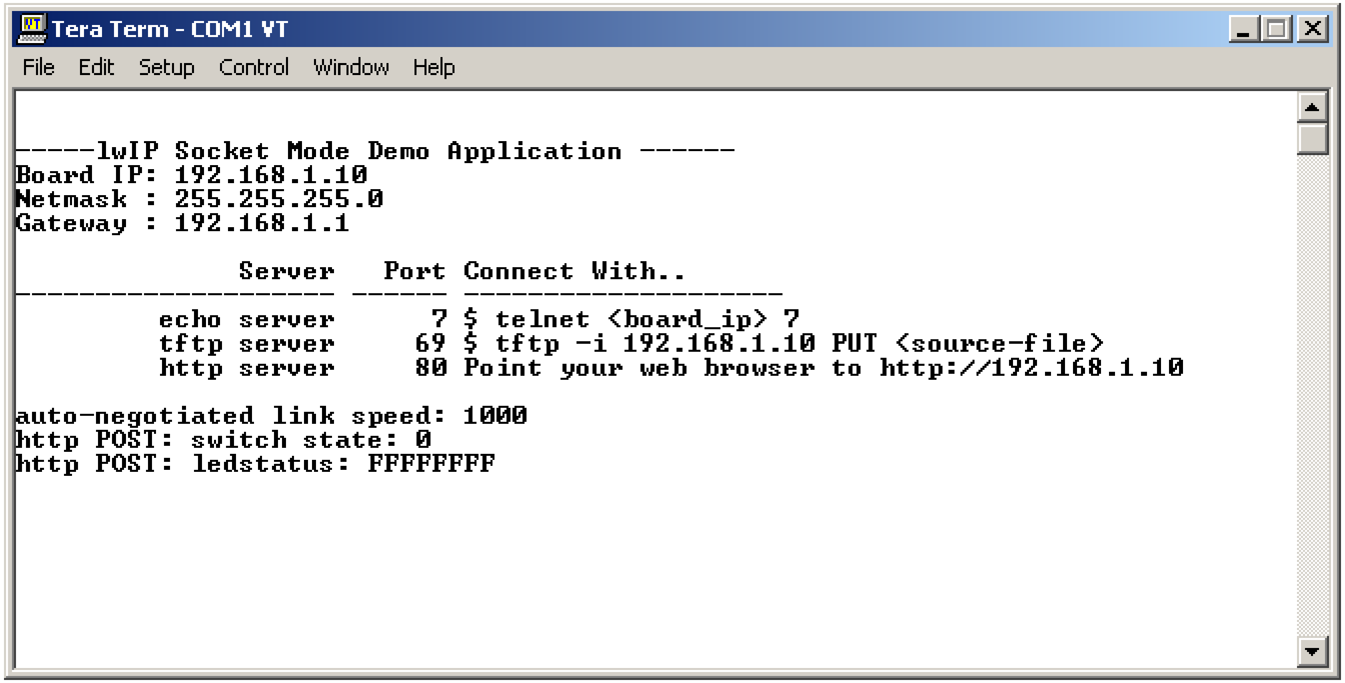
Controlling the Embedded System

This example is intended to illustrate how the functionality of the embedded system can be controlled from the browser. Here, the LED's on the board can be switched on or off by clicking on the 'Toggle LEDs' button.

LEDs are now ON.

Running the Lwipdemo Application

- The Lwipdemo application shows the web transaction for the button push



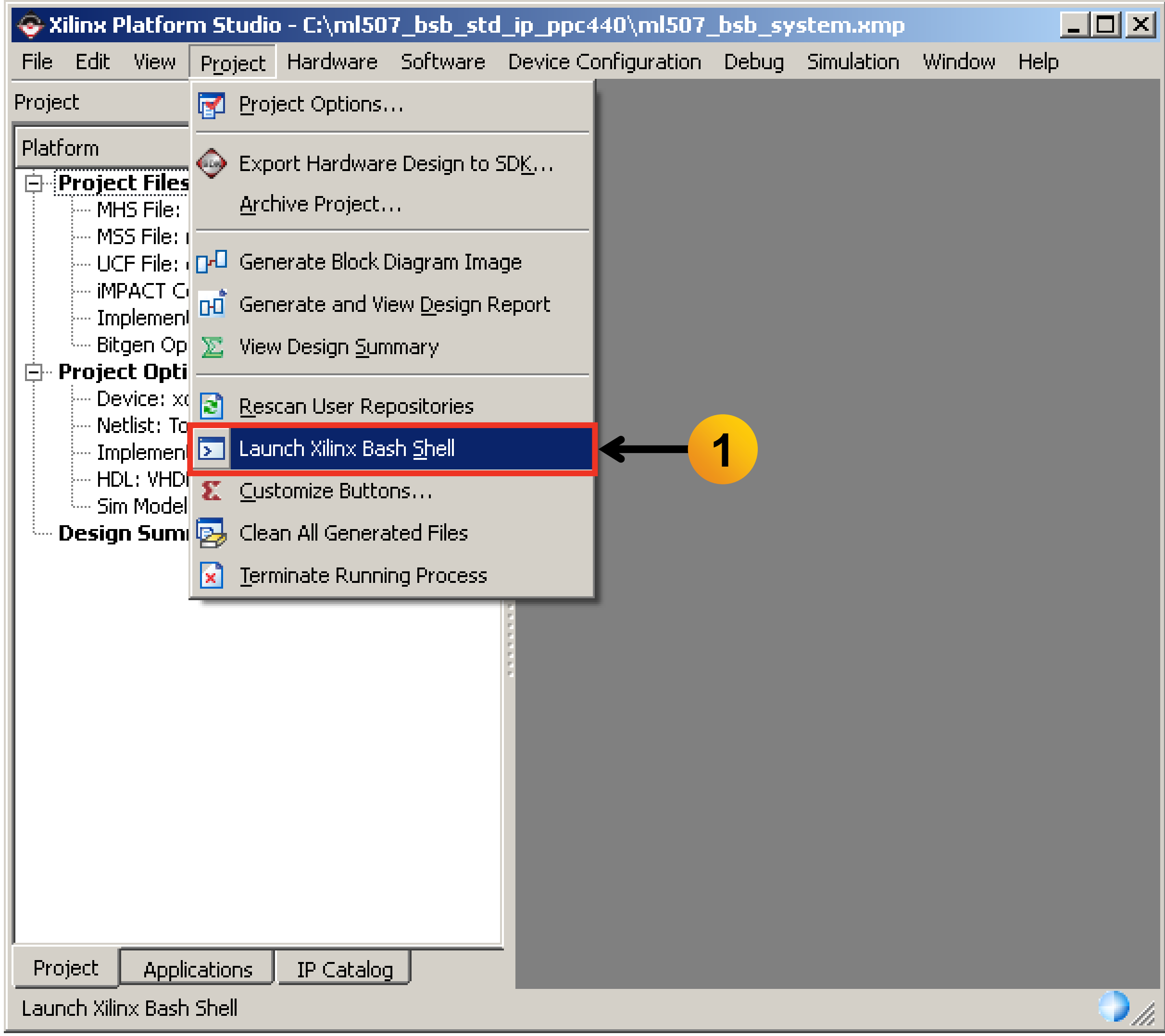
```
-----lwIP Socket Mode Demo Application ------
Board IP: 192.168.1.10
Netmask : 255.255.255.0
Gateway : 192.168.1.1

              Server   Port Connect With..
-------------------- ------ --------------------
         echo server      7 $ telnet <board_ip> 7
         tftp server     69 $ tftp -i 192.168.1.10 PUT <source-file>
         http server     80 Point your web browser to http://192.168.1.10

auto-negotiated link speed: 1000
http POST: switch state: 0
http POST: ledstatus: FFFFFFFF
```

Note: Presentation applies to the ML505, ML506, and ML507

Create an ACE File

Create an ACE File

- **Open an EDK shell**
  - Select **Project → Launch Xilinx BASH Shell** (1)



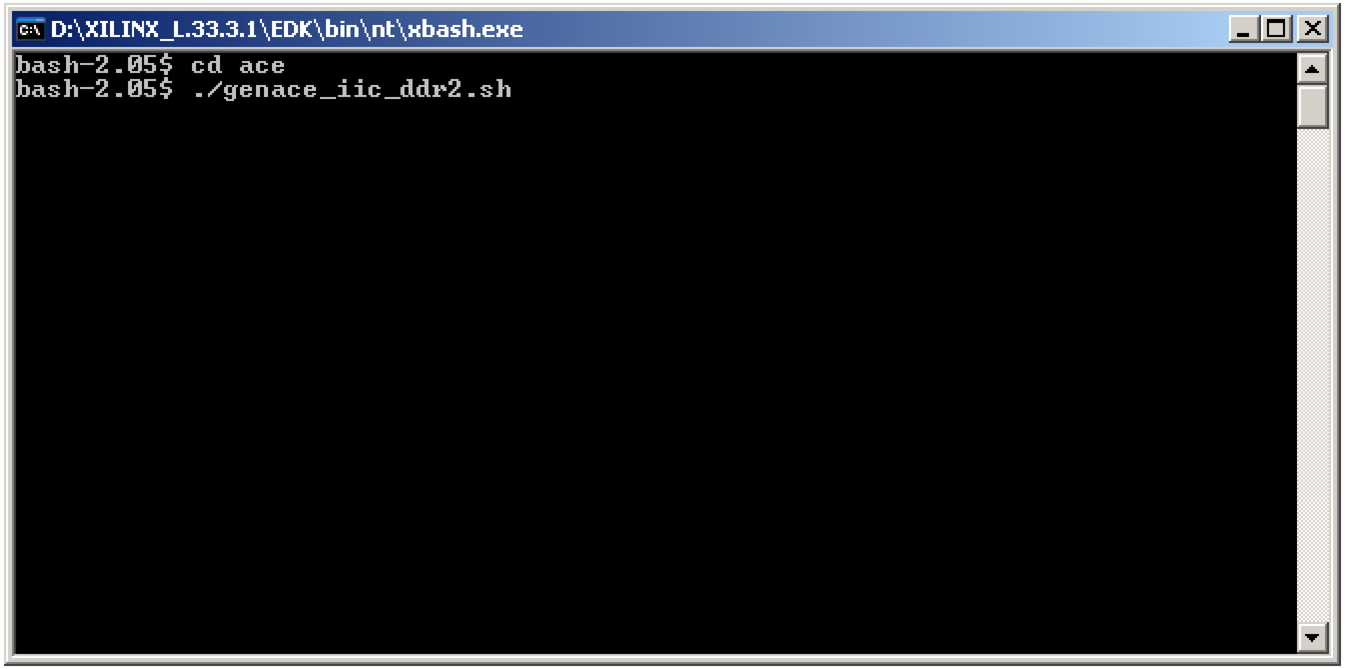
Note: Presentation applies to the ML507

Create an ACE File

- At the bash prompt, type (1):

  cd ace

  ./genace_iic_ddr2.sh



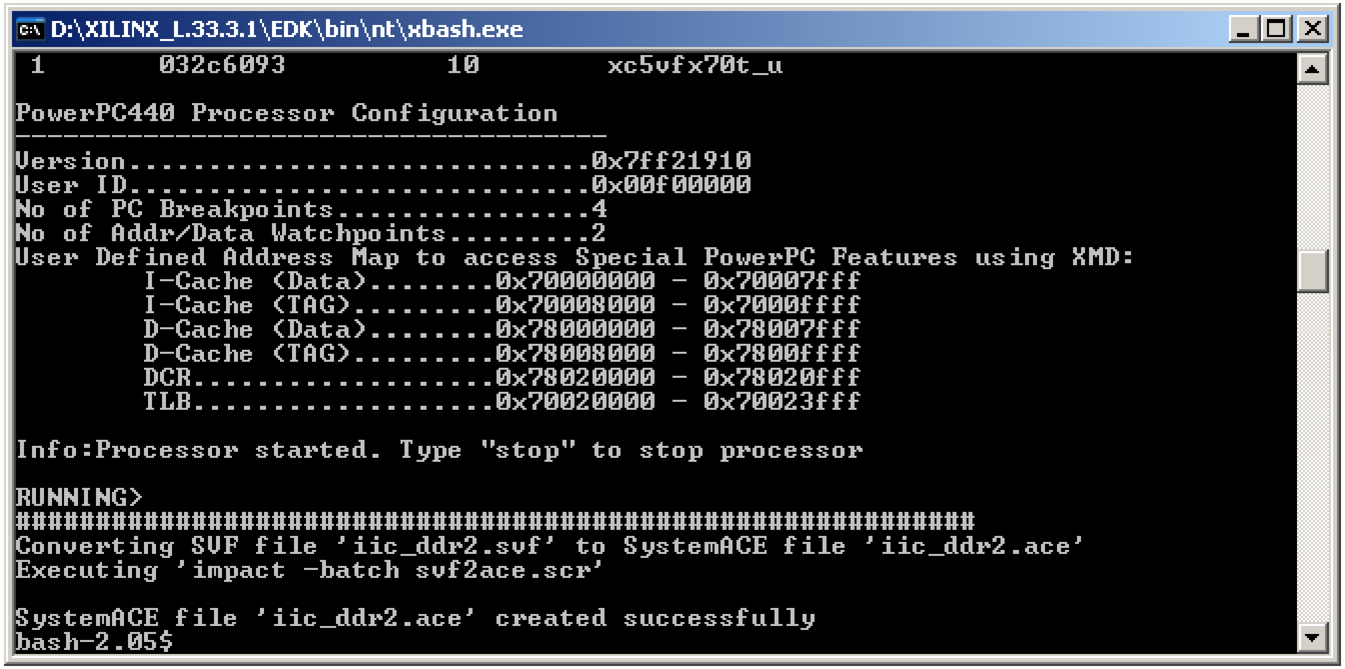
D:\XILINX_L.33.3.1\EDK\bin\nt\xbash.exe

```
bash-2.05$ cd ace
bash-2.05$ ./genace_iic_ddr2.sh
```

Note: Presentation applies to the ML507

Create an ACE File

- **This creates a concatenated (HW+SW) ACE file**
  - Input: iic_ddr2.elf, download.bit
- **genace_iic_ddr2.sh uses XMD and a genace.tcl script with ML507 appropriate options to generate an ACE file**



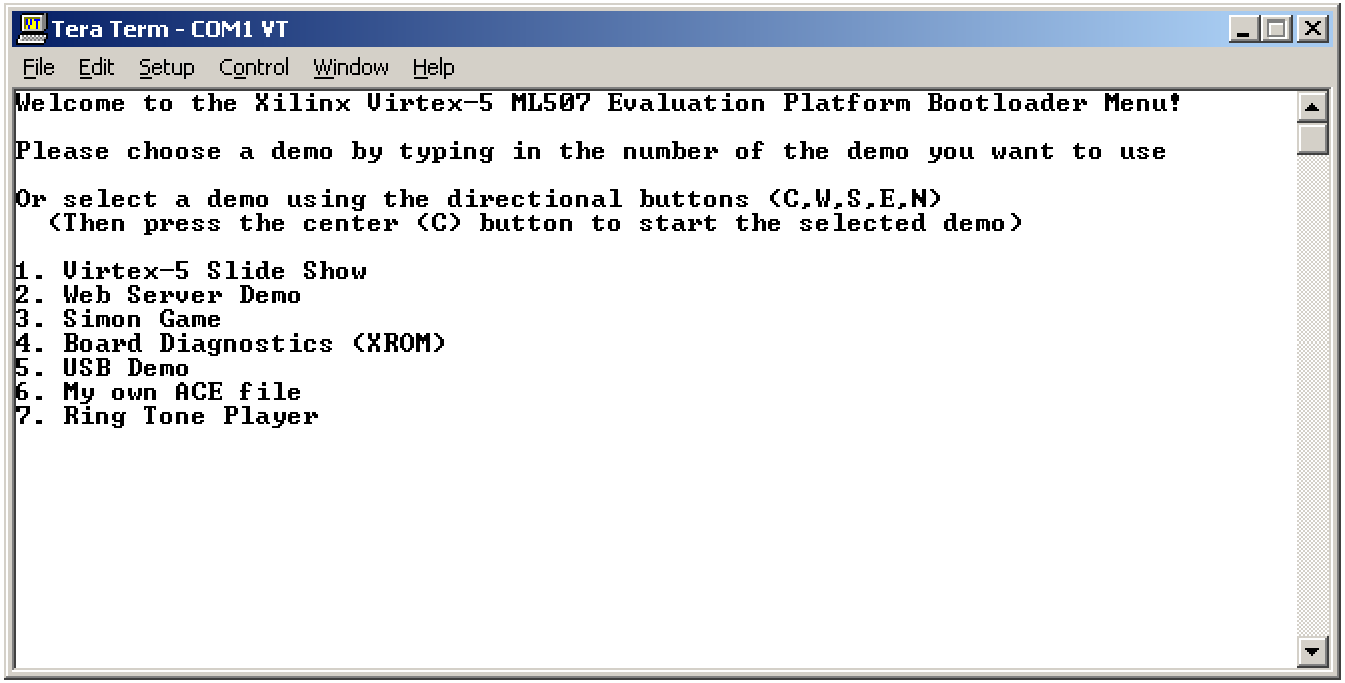
```
 1       032c6093          10        xc5vfx70t_u

PowerPC440 Processor Configuration
-------------------------------------
Version.............................0x7ff21910
User ID.............................0x00f00000
No of PC Breakpoints................4
No of Addr/Data Watchpoints.........2
User Defined Address Map to access Special PowerPC Features using XMD:
        I-Cache (Data)........0x70000000 - 0x70007fff
        I-Cache (TAG).........0x70008000 - 0x7000ffff
        D-Cache (Data)........0x78000000 - 0x78007fff
        D-Cache (TAG).........0x78008000 - 0x7800ffff
        DCR...................0x78020000 - 0x78020fff
        TLB...................0x70020000 - 0x70023fff

Info:Processor started. Type "stop" to stop processor

RUNNING>
############################################################
Converting SVF file 'iic_ddr2.svf' to SystemACE file 'iic_ddr2.ace'
Executing 'impact -batch svf2ace.scr'

SystemACE file 'iic_ddr2.ace' created successfully
bash-2.05$
```

Run ACE File

- **Copy iic_ddr2.ace to the ML50X\cfg6 directory on your CompactFlash card**
  - Important: Delete any existing ace files in this cfg6 directory
  - Note: Use a CompactFlash reader to mount the CompactFlash as a disk drive

Run ACE File

- **Use the new ACE file**
  - Eject the CompactFlash from your PC and insert it back into the ML507
  - Type **6** to run the newly created ACE file

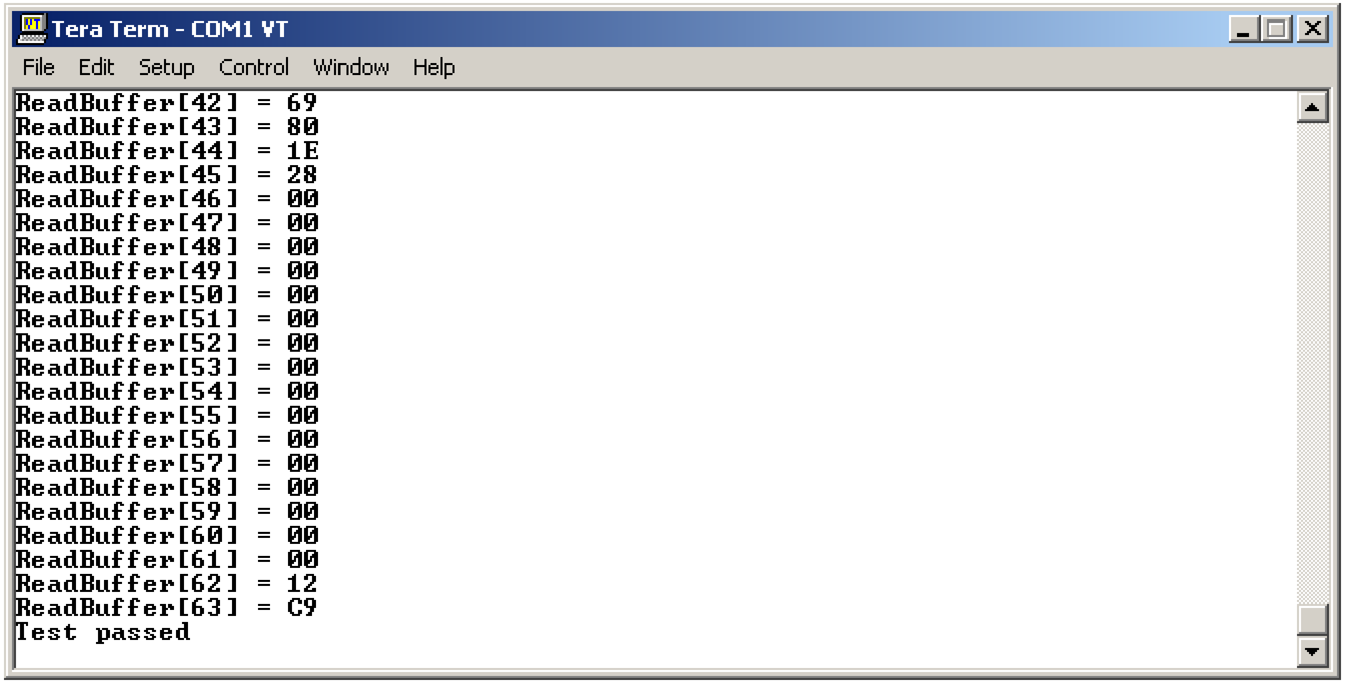


```
Welcome to the Xilinx Virtex-5 ML507 Evaluation Platform Bootloader Menu!

Please choose a demo by typing in the number of the demo you want to use

Or select a demo using the directional buttons (C,W,S,E,N)
  (Then press the center (C) button to start the selected demo)

1. Virtex-5 Slide Show
2. Web Server Demo
3. Simon Game
4. Board Diagnostics (XROM)
5. USB Demo
6. My own ACE file
7. Ring Tone Player
```

Note: Presentation applies to the ML507

Run ACE File

- iic_ddr2 output after booting ACE file



```
ReadBuffer[42] = 69
ReadBuffer[43] = 80
ReadBuffer[44] = 1E
ReadBuffer[45] = 28
ReadBuffer[46] = 00
ReadBuffer[47] = 00
ReadBuffer[48] = 00
ReadBuffer[49] = 00
ReadBuffer[50] = 00
ReadBuffer[51] = 00
ReadBuffer[52] = 00
ReadBuffer[53] = 00
ReadBuffer[54] = 00
ReadBuffer[55] = 00
ReadBuffer[56] = 00
ReadBuffer[57] = 00
ReadBuffer[58] = 00
ReadBuffer[59] = 00
ReadBuffer[60] = 00
ReadBuffer[61] = 00
ReadBuffer[62] = 12
ReadBuffer[63] = C9
Test passed
```

References

Documentation

- **Platform Studio**
  - Embedded Development Kit (EDK) Resources

    http://www.xilinx.com/tools/platform.htm
  - Embedded System Tools Reference Manual

    http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/est_rm.pdf
  - EDK Concepts, Tools, and Techniques

    http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/edk_ctt.pdf

Documentation

- **PLB v4.6 IP**
  - XPS Multi-CHannel External Memory Controller (XPS MCH EMC) – DS575
    http://www.xilinx.com/support/documentation/ip_documentation/xps_mch_emc.pdf
  - XPS Thin Film Transistor (TFT) Controller – DS695
    www.xilinx.com/support/documentation/ip_documentation/xps_tft.pdf
  - XPS PS2 Controller – DS707
    www.xilinx.com/support/documentation/ip_documentation/xps_ps2.pdf
  - XPS IIC Bus Interface – DS606
    http://www.xilinx.com/support/documentation/ip_documentation/xps_iic.pdf
  - XPS General Purpose Input/Output (GPIO) – DS569
    http://www.xilinx.com/support/documentation/ip_documentation/xps_gpio.pdf

Additional Documentation

Documentation

- **Virtex-5**
  - Silicon Devices

    http://www.xilinx.com/products/devices.htm
  - Virtex-5 Multi-Platform FPGA

    http://www.xilinx.com/products/virtex5/index.htm
  - Virtex-5 Family Overview: LX, LXT, SXT, and FXT Platforms

    http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf
  - Virtex-5 FPGA DC and Switching Characteristics Data Sheet

    http://www.xilinx.com/support/documentation/data_sheets/ds202.pdf

Documentation

- **Virtex-5**
  - Virtex-5 FPGA User Guide

    http://www.xilinx.com/support/documentation/user_guides/ug190.pdf
  - Virtex-5 FPGA Configuration User Guide

    http://www.xilinx.com/support/documentation/user_guides/ug191.pdf
  - Virtex-5 System Monitor User Guide

    http://www.xilinx.com/support/documentation/user_guides/ug192.pdf
  - Virtex-5 Packaging and Pinout Specification

    http://www.xilinx.com/support/documentation/user_guides/ug195.pdf

Documentation

- **Virtex-5 RocketIO**
  - RocketIO GTP Transceivers
    http://www.xilinx.com/products/virtex5/lxt.htm
  - RocketIO GTP Transceiver User Guide – UG196
    http://www.xilinx.com/support/documentation/user_guides/ug196.pdf
  - RocketIO GTX Transceivers
    http://www.xilinx.com/products/virtex5/fxt.htm
  - RocketIO GTX Transceiver User Guide – UG198
    http://www.xilinx.com/support/documentation/user_guides/ug198.pdf

Documentation

- **Design Resources**
  - IDS - ISE Design Suite

    http://www.xilinx.com/tools/designtools.htm
  - ISE Manuals

    http://www.xilinx.com/support/documentation/dt_ise11-1.htm
  - ISE Command Line Tools User Guide

    http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/devref.pdf
  - ISE Development System Libraries Guide

    http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/virtex5_hdl.pdf

Documentation

- **Additional Design Resources**
  - Customer Support
    http://www.xilinx.com/support
  - Xilinx Design Services:
    http://www.xilinx.com/xds
  - Titanium Dedicated Engineering:
    http://www.xilinx.com/titanium
  - Education Services:
    http://www.xilinx.com/education
  - Xilinx On Board (Board and kit locator):
    http://www.xilinx.com/products/devkits/boardsearch.htm

Documentation

- **Platform Studio**
  - Embedded Development Kit (EDK) Resources

    http://www.xilinx.com/tools/platform.htm
  - Embedded System Tools Reference Manual

    http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/est_rm.pdf
  - EDK Concepts, Tools, and Techniques

    http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/edk_ctt.pdf

Documentation

- **PowerPC 440**
  - Embedded Processor Block in Virtex-5 FPGAs Reference Guide – UG200
    http://www.xilinx.com/support/documentation/user_guides/ug200.pdf
  - PPC440 Virtex-5 Wrapper – DS621
    http://www.xilinx.com/support/documentation/ip_documentation/ppc440_virtex5.pdf
  - DDR2 Memory Controller for PowerPC 440 Processors – DS567
    http://www.xilinx.com/support/documentation/ip_documentation/ppc440mc_ddr2.pdf

Documentation

- **MicroBlaze**
  - MicroBlaze Processor

    http://www.xilinx.com/tools/microblaze.htm
  - MicroBlaze Processor Reference Guide – UG081

    http://www.xilinx.com/support/documentation/sw_manuals/mb_ref_guide.pdf

Documentation

- **ChipScope Pro**
  - ChipScope Pro 10.1i Serial IO Toolkit User Manual

    http://www.xilinx.com/ise/verification/chipscope_pro_siotk_10_1_ug213.pdf
  - ChipScope Pro 11.1 ChipScope Pro Software and Cores User Guide

    http://www.xilinx.com/support/documentation/
    sw_manuals/xilinx11/chipscope_pro_sw_cores_11_1_ug029.pdf

Documentation

- **Memory Solutions**
  - Demos on Demand – Memory Interface Solutions with Xilinx FPGAs
    http://www.demosondemand.com/clients/xilinx/001/page_new2/index.asp#35
  - Xilinx Memory Corner
    http://www.xilinx.com/products/design_resources/mem_corner
  - Additional Memory Resources
    http://www.xilinx.com/support/software/memory/protected/index.htm
  - Xilinx Memory Interface Generator (MIG) 3.0 User Guide
    http://www.xilinx.com/support/documentation/ip_documentation/ug086.pdf
  - Memory Interfaces Made Easy with Xilinx FPGAs and
    the Memory Interface Generator
    http://www.xilinx.com/support/documentation/white_papers/wp260.pdf

Documentation

- **Ethernet**
  - Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Data Sheet
    http://www.xilinx.com/support/documentation/ip_documentation/v5_emac_ds550.pdf
  - Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Getting Started Guide
    http://www.xilinx.com/support/documentation/ip_documentation/v5_emac_gsg340.pdf
  - Virtex-5 Tri-Mode Ethernet Media Access Controller User Guide
    http://www.xilinx.com/support/documentation/user_guides/ug194.pdf
  - LightWeight IP (lwIP) Application Examples – XAPP1026
    http://www.xilinx.com/support/documentation/application_notes/xapp1026.pdf

Documentation

- **PCIe**
  - LogiCORE Endpoint Block Plus for PCI Express Data Sheet
    http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_ds551.pdf
  - LogiCORE Endpoint Block Plus for PCI Express Designs
    http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_ug341.pdf
  - LogiCORE Endpoint Block Plus Getting Started Guide for PCI Express Designs
    http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_gsg343.pdf
  - Virtex-5 Integrated Endpoint Block User Guide for PCI Express Designs
    http://www.xilinx.com/support/documentation/user_guides/ug197.pdf

Documentation

- **System Generator**
  - System Generator for DSP
    http://www.xilinx.com/tools/sysgen.htm
  - Xilinx System Generator for DSP Getting Started Guide – UG639
    http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/sysgen_ref.pdf
  - Xilinx System Generator for DSP Getting Started Guide – UG639
    http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/sysgen_gs.pdf
  - Virtex-5 XtremeDSP Design Considerations User Guide – UG193
    http://www.xilinx.com/support/documentation/user_guides/ug193.pdf

Documentation

- **PLB v4.6 IP**
  - Processor Local Bus (PLB) v4.6 – DS531

    http://www.xilinx.com/support/documentation/ip_documentation/plb_v46.pdf
  - Multi-Port Memory Controller (MPMC) – DS643

    http://www.xilinx.com/support/documentation/ip_documentation/mpmc.pdf
  - XPS Multi-CHannel External Memory Controller (XPS MCH EMC) – DS575

    http://www.xilinx.com/support/documentation/ip_documentation/xps_mch_emc.pdf
  - XPS LocalLink TEMAC – DS537

    http://www.xilinx.com/support/documentation/ip_documentation/xps_ll_temac.pdf

Documentation

- **PLB v4.6 IP**
  - XPS LocalLink FIFO – DS568
    http://www.xilinx.com/support/documentation/ip_documentation/xps_ll_fifo.pdf
  - XPS IIC Bus Interface – DS606
    http://www.xilinx.com/support/documentation/ip_documentation/xps_iic.pdf
  - XPS SYSACE (System ACE) Interface Controller – DS583
    http://www.xilinx.com/support/documentation/ip_documentation/xps_sysace.pdf
  - XPS Timer/Counter – DS573
    http://www.xilinx.com/support/documentation/ip_documentation/xps_timer.pdf

Documentation

- **PLB v4.6 IP**
  - XPS Interrupt Controller – DS572
    http://www.xilinx.com/support/documentation/ip_documentation/xps_intc.pdf
  - Using and Creating Interrupt-Based Systems Application Note
    http://www.xilinx.com/support/documentation/application_notes/xapp778.pdf
  - XPS General Purpose Input/Output (GPIO) – DS569
    http://www.xilinx.com/support/documentation/ip_documentation/xps_gpio.pdf
  - XPS External Peripheral Controller (EPC) – DS581
    http://www.xilinx.com/support/documentation/ip_documentation/xps_epc.pdf

Documentation

- **PLB v4.6 IP**
  - XPS 16550 UART – DS577

    http://www.xilinx.com/support/documentation/ip_documentation/xps_uart16550.pdf
  - XPS Thin Film Transistor (TFT) Controller – DS695

    www.xilinx.com/support/documentation/ip_documentation/xps_tft.pdf
  - XPS PS2 Controller – DS707

    www.xilinx.com/support/documentation/ip_documentation/xps_ps2.pdf
  - XPS Block RAM (BRAM) Interface Controller – DS596

    www.xilinx.com/support/documentation/ip_documentation/xps_bram_if_cntlr.pdf

Documentation

- **OPB Bridge IP**
  - PLBV46 to OPB Bridge – DS403

    http://www.xilinx.com/support/documentation/ip_documentation/plbv46_opb_bridge.pdf
  - On-Chip Peripheral Bus V2.0 with OPB Arbiter – DS401

    http://www.xilinx.com/support/documentation/ip_documentation/opb_v20.pdf

Documentation

- IP
  - Local Memory Bus – DS445
    http://www.xilinx.com/support/documentation/ip_documentation/lmb_v10.pdf
  - Block RAM Block – DS444
    http://www.xilinx.com/support/documentation/ip_documentation/bram_block.pdf
  - Microprocessor Debug Module – DS641
    http://www.xilinx.com/support/documentation/ip_documentation/mdm.pdf
  - LMB Block RAM Interface Controller – DS452
    http://www.xilinx.com/support/documentation/ip_documentation/lmb_bram_if_cntlr.pdf

Documentation

- **IP**
  - JTAGPPC Controller – DS298

    http://www.xilinx.com/support/documentation/ip_documentation/jtagppc_cntlr.pdf
  - Processor System Reset Module – DS402

    http://www.xilinx.com/support/documentation/ip_documentation/proc_sys_reset.pdf
  - Clock Generator v2.0 – DS614

    http://www.xilinx.com/support/documentation/ip_documentation/clock_generator.pdf

Documentation

- IP
  - Utility Vector Logic – DS481

    http://www.xilinx.com/support/documentation/ip_documentation/util_vector_logic.pdf
  - Utility IO Multiplexer – DS694

    http://www.xilinx.com/support/documentation/ip_documentation/util_io_mux.pdf

Documentation

- **ML505/506/507**
  - ML505 Overview
    http://www.xilinx.com/ml505
  - ML506 Overview
    http://www.xilinx.com/ml506
  - ML507 Overview
    http://www.xilinx.com/ml507
  - ML505/506/507 Evaluation Platform User Guide – UG347
    http://www.xilinx.com/support/documentation/boards_and_kits/ug347.pdf
  - ML505/506/507 Getting Started Tutorial – UG348
    http://www.xilinx.com/support/documentation/boards_and_kits/ug348.pdf
  - ML505/506/507 Reference Design User Guide – UG349
    http://www.xilinx.com/support/documentation/boards_and_kits/ug349.pdf

Documentation

- **ML505/506/507**
  - ML505/506/507 Schematics

    http://www.xilinx.com/support/documentation/boards_and_kits/ml50x_schematics.pdf
  - ML505/506/507 Bill of Material

    http://www.xilinx.com/support/documentation/boards_and_kits/ml505_501_bom.xls