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Carry Ripple Adder Implementation
using Data Driven Dynamic Logic
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Abstract

In this report three different equations for full adders will each be implemented using both the Data Driven Dynamic Logic (D3L) and the Split-Level Data Driven Dynamic Logic (SPD3L); for a total of 6 different implementations of a full adder. All designs will utilize hierarchical design methodology by starting with the implementation of 1-bit full adders, and then constructing 4-bit adders utilizing the smaller 1-bit adders. The 6 different circuit implementations will then be compared in terms of power, leakage, and delay.

Introduction

The purpose of this project will be to implement three different full adder equations and design them using both D3L and SPD3L and to compare them against each other to determine which will be the most efficient, based off of the power, delay, and leakage. These 4-bit adders will be designed and implemented using hierarchical design methodology to construct the schematics, Synopsys HSPICE to measure the average power, Synopsys NanoSim to measure average power as well as leakage current, and CSCOPE to obtain the delay timings of the operation of the full adders.

The schematic entry and creation of the circuits will be using the FreePDK45. This is a free and open source library that has different type of standard cell designs of PMOS and NMOS transistors. These standard cells are based on 45 nm technology.

The 4-bit adders will be built from a 1-bit adder in a Carry Ripple orientation. The first step in this process was to construct the 1-bit adders and ensure that they were functioning as desired. In this report the power, delay, leakage, and circuit implementation of the 1-bit adders will be discussed as well as the full 4-bit addition.

Three different circuit equations will be implemented using the two different circuit types. The first is a typical full adder design utilizing a 3-input XOR for the sum and a combination of AND and OR gates for the Cout. The second splits up the operation of the first circuit into sub-functions so some sharing of circuits can be taken advantage of. Finally the third circuit implementation utilized the output of Cout in the equation for the sum. All three equations can be seen below. [1]

$$S = A \oplus B \oplus C_i \quad C_{out} = (AB + BC_i + AC_i) \quad (1)$$

$$P = (A \oplus B) \quad G = AB \quad S = P \oplus C_i \quad C_{out} = G + PC_i \quad (2)$$

$$S = ABC_i + \overline{C_{out}}(A + B + C_i) \quad C_{out} = (AB + BC_i + AC_i) \quad (3)$$

Background

Data Driven Dynamic Logic (D3L)

Data driven Dynamic Logic builds upon the concept of domino logic. Domino logic circuits utilize a sequence of pre-charge and evaluation phases that are driven by a clock signal, the PDN usually uses a NMOS transistor to cut off or allow for the PDN logic to evaluate or not. In D3L, instead of the clock signal a certain set of input signals is required in the PUN to determine the pre-charge or evaluation phase. This allows for the omission of the footer transistor and the clock signal. The signals which are used in the PUN are always going to be a subset of the input data signals from the PDN. The PDN is where the typical pull down logic is put; this is the same as the domino circuit type. The PUN inputs then have to be selected from these pull down paths, for proper functionality there needs to be one input per leakage path to ground represented in the PUN. The implementation of a general D3L circuit with the circuit equation $F = (I_{1,1} \dots I_{k,1}) + \dots + (I_{1,m} \dots I_{n,m})$, can be seen below in Figure 1. [3]

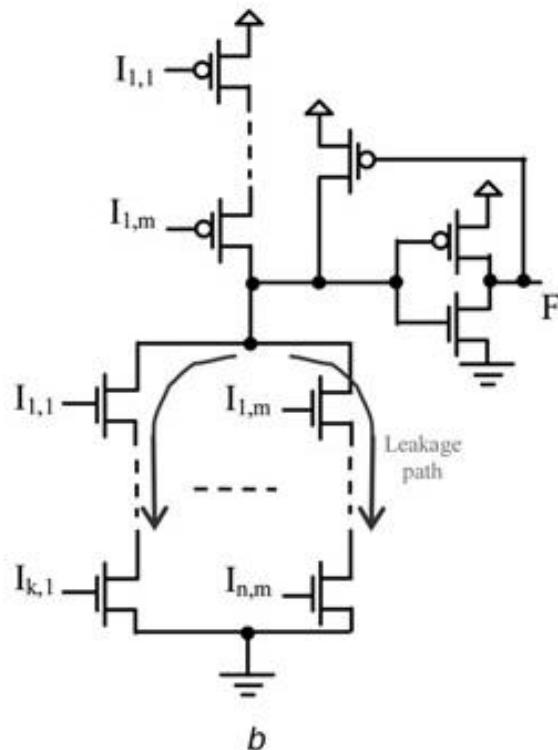


Figure 1: D3L Implementation of F

Split-Path Date Driven Dynamic Logic (SPD3L)

Much like the D3L, SPD3L further develops this family of circuits by splitting up the series connected PMOS transistors in the PUN to multiple PUN's. This minimizes the delay and the energy penalty caused by the PUN, especially if there are a large number of leakage paths in the PDN. [1] To split up the PUN, the PDN is broken down into multiple circuits. For X leakage path in the PDN D3L there will be now be X SPD3L networks, one with each PDN path, with a single PMOS transistor for the pre-charge phase. Each of the circuits Dynamic Nodes are then fed into a NAND gate to obtain the correct functionality. The implementation of a SP-D3L circuit with the circuit equation $F = (I_{1,1} \dots I_{k,1}) + \dots + (I_{1,m} \dots I_{n,m})$, can be seen below in Figure 2. [3]

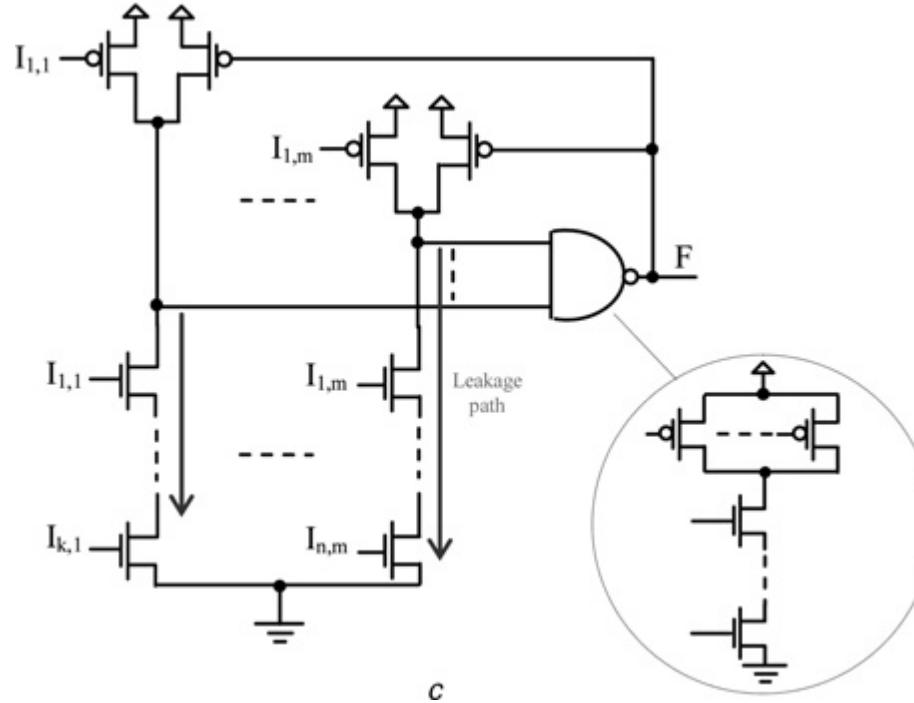


Figure 2: SP-D3L implementation of F

Carry Ripple Adder

A Carry Ripple Adder (CRA) is the basic implementation of a linear set of full adder strung together to form a complete 4-bit adder. A Full Adder takes three inputs, and generates two outputs, a sum and a carry out. The implementation of a general 1-bit adder can be seen below in Figure 3 [4].

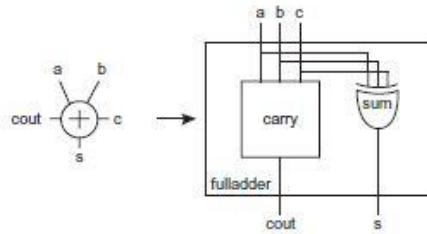


Figure 3: Full-Adder Implementation

In both the D3L and SPD3L the inputs on the PUN require a monotonically rising input; this means for circuits that require both a logic input and the inverted signal of that input signal, it is required to construct a dual-rail implementation. In the case when both A and !A are needed in a PUN, both the A and !A need to be ensured

to be monotonically rising. If these are cascaded from a previous stage it cannot simply be put through an inverter, but instead needs to be outputted from a previous stage D3L or SPD3L circuit. This causes the full adder to change slightly. This means the implementation of a full adder will be slightly altered. This will add a !Cout signal as well as a !Ci input signal. This can be seen in the block diagram below in Figure 4.

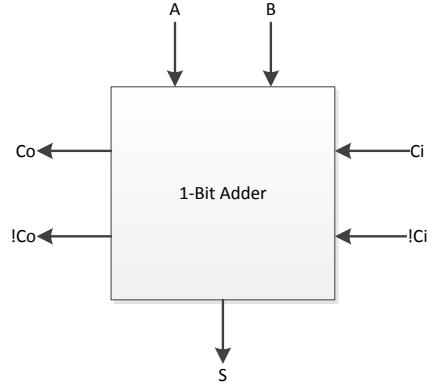


Figure 4: 1-Bit Full Adder D3L/SPD3L Block Diagram

In order to generate a 4-bit adder these 1-bit adders are cascaded so that the Co of the first stage is fed into the Ci of the next stage, etc. Below in Figure 5 is the block diagram used for the 4-bit adder implementation.

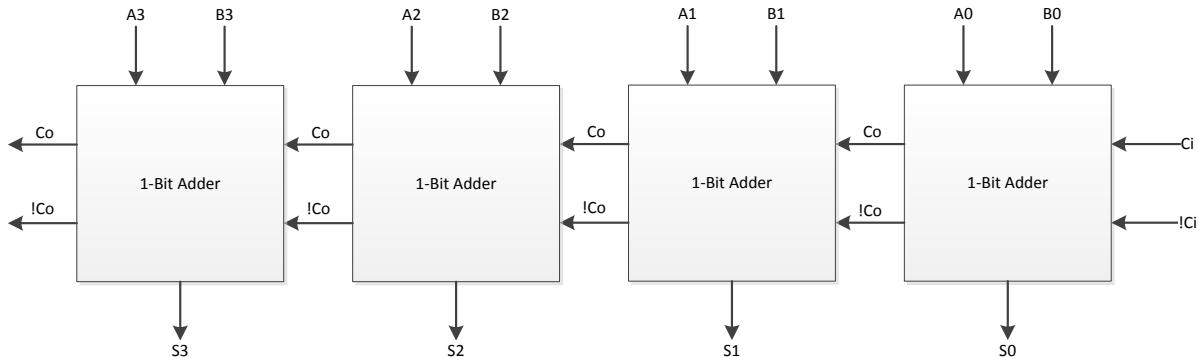


Figure 5: 4-Bit Full Adder D3L/SPD3L Block Diagram

Architectural Exploration of Adders

For all of the circuit implementations a precharge signal that acts as a control signal was added to control whether the circuit was in pre-charge phase or evaluation phase. This signal was fed into an AND gate along with the input signal of whatever input signal was used in the PUN. When the precharge signal is not asserted the AND gate forces all the inputs to 0, making the PUN connected to Vdd, thus causing the DN to be 1 and in the pre-charge phase. When the pre-charge control signal is asserted, this allows the input value to pass through the AND gate and drive the network and evaluate the circuit. The basic set-up can be seen below in Figure 6.

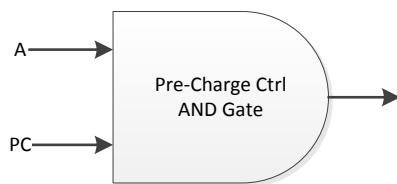


Figure 6: Pre-Charge Control Gate

Circuit 1 Implementation

D3L:

The first circuit implemented can be seen in Equation 1 and was based off of the design presented in [3]. This is a typical structure for a full-adder. To optimize this circuit, both the S and Co equations could share some logic structure, limiting the amount of the transistors needed in the circuit. The circuit schematics can be found under Appendix 1: Circuit 1 D3L.

It can be seen in the schematics that the Sum, Cout, and !Cout circuits all have two main leakage paths, this means that there needs to be one input selected from each path to be an input for the PUN resulting in two PMOS transistors in series. For the Sum circuit A and !A were selected to be in the PUN, this was the most logical choice as A and !A were shared by the four logic paths. If other signals were selected, in order to obtain one from each leakage path, there would have needed to be four PMOS transistors in the PUN, resulting in an inefficient circuit. The same design methodology was implemented in both the Cout and !Cout circuits. In the case for the Cout in Equation 1, the inverted and non-inverted signals are exact opposite. This special case allows for the structure to be the same and just change the inputs of the transistors. Thus in the PUN for the Cout B and A were chosen, and for the !Cout, !B and !A were chosen.

Since just A, B, !A, and !B were used in the PUN, these were the only signals that needed to be controlled by the pre-charge circuitry. The Ci and !Ci were not in the PUN so were not prudent in the pre-charge phase setting the DN to Vdd. The control structure can also be found under Appendix 1: Circuit 1 D3L.

The sizing of the transistors were based on the standard 2:1 Inverter. The PMOS transistors each have a size of 4 in the PUN, a sizing of 3 in the PDN for the sum circuit and a sizing of 2 in the PDN for the Cout and !Cout circuit. The keeper transistor is supposed to be 1/10th of the size for best results, however Synopsys Virtuoso did not allow for any transistor size less than 1.

SPD3L:

The second implementation of Equation 1 utilizes the split-path and was based off of the design presented in [3], this allows for the PUN to be split up into smaller transistors sizes. The circuit schematics can be found under Appendix 1: Circuit 1 SPD3L.

In the D3L circuit there were two leakage paths for each the S, Cout, and !Cout circuits. These were all split up into their own circuit and then the DN nodes combined through a NAND gate to obtain proper circuit functionality. For the sum circuit, the first path S1, used A in the PUN, and the second path S2, used !A in the PUN. The same implementation was done in the Cout and !Cout circuits. For the Cout function, the first path C1, used A in the PUN, and the second path S2, used B for the PUN. Finally the Cout circuit used the inverted signals of the Cout circuit like before in the D3L implementation. The first path C3, used !A in the PUN, and the second path S4, used !B in the PUN.

The sizing of the transistors were based on the standard 2:1 Inverter. All of the PDN circuit sizing stayed the same, it was the PUN network PMOS sizes that were able to be reduced in size. All of the PUN sizing were cut in half, thus they were reduced to a size of 2. This should cut back on the power needed for the PUN.

Circuit 2 Implementation

D3L:

The second circuit implemented can be seen in Equation 2. This function utilizes sub-functions. For example, it splits up the XOR for the sum calculation into two different functions, one to calculate XOR between two inputs, and then another function to calculate the XOR between the output of the previous and the input of another input; when combined together it will create a 3-input XOR. A similar method is done in with the calculation of the Cout, it uses the results from two other sub-functions to calculate the final Cout value. Like in the Circuit 1 implementation, some of the functions need support for a dual-rail output so the circuits can be cascaded together. For the calculation of P this is done to produce both P and !P. By producing a dual-rail output some transistors are able to be shared; thus cutting down on the power used by the circuit. The circuit schematics can be found under Appendix 1: Circuit 2 D3L.

In the case for G and !G the circuit output did not have the same characteristics as the Cout and !Cout in Circuit 1. Each G and !G had to be designed separate. This was also the case for this new Cout and !Cout equation in Equation 2. Both of the circuits had to be designed separately, thus they each have different schematics since the inputs could not just be changed like in Circuit 1. For G and !Cout they each just had one leakage path so the PUN was relatively smaller than the others. The equations for !G and !Cout can be seen below.

$$\overline{G} = \overline{B} + \overline{A} \quad (4)$$

$$\overline{C_{out}} = \overline{G}(\overline{P} + \overline{C_{in}}) \quad (5)$$

In the calculation of S, it was decided that since P and !P already needed to be calculated that these signals should drive the PUN in the Sum circuit. If the Ci and !Ci signals were used in the PUN then the control circuitry with the pre-charge would have had to been utilized, resulting in the addition of two more AND Gates (12 more transistors). The number of signals that needed to be inputted through this control circuitry was limited to just three; A, !A, and !B. The control circuitry can be seen in Appendix 1: Circuit 2 D3L.

Once again the circuits were sized to math a 2:1 Inverter. When there were two PMOS transistors in the PUN the sizes were 4; this was the case in the circuits P, !P, !G, S, and Cout. In the case for G and !Cout there was just one leakage path so only one of the signals needed to be feed into the PMOS PUN resulting in a sizing of 2.

SPD3L:

The SPD3L implementation of Equation 2 can be seen in Appendix 1: Circuit 2 SPD3L. Much like the SPD3L implementation in used in circuit 1 all of the leakage branches were split up so the PUN transistors would be broken down into smaller sub circuits; reducing the size of the PMOS transistors.

The circuit implementations for G and !Cout just have a single leakage path to ground so these circuits will be exactly the same as the D3L implementation since there are no way to split up the circuits any more than just having a single PMOS transistor in the PUN. The dual-rail implementation of the P (XOR2) was used in D3L, this will also be used in SPD3L. This allows for the sharing of two transistors, the !B and B transistor in P!/P schematic.

Similar to the D3L implementation, the number of input signals that needed to be put through the pre-charge AND gates were limited by just choosing A, !A, and B inputs in the PUN, Along with previously calculated values from cascaded inputs. For example, in the S circuit the P and !P are used as the pre-charge signal in the PUN instead of the Ci and !Ci signals. Since the values for the P and !P needed to be calculated anyways, it works out that when initially the input values for the circuit P are in the pre-charge phase, the pre-charge phase will then cascade through to the S circuit. (A!/A asserted 0 -> P to be asserted 0 -> S is in pre-charge). By utilizing this, it reduces the number of transistors needed in the control logic. (If C!/C were used, the control logic for the pre-charge signal would increase the number of transistors by 12).

As previously discussed, the circuit was sized to a 2:1 Inverter. Since in SPD3L, the number of transistors is going to be one PMOS in the PUN, the size of all of the PMOS transistors in the PUN are going to be 2. The PDN networks all have varying NMOS transistor size, but in general the PDN all have a size of 2 as well, with the exception of the PDN in the Cout circuit where there is just a single transistor connected to ground in the of the split paths; this transistor has a size of 1. This also occurs in the !G circuit.

Bonus Design

D3L:

The bonus design is a special kind of full-adder implementation. This can be seen in Equation 3. It utilizes the calculated value of !Cout to compute the sum. The $\text{Cout}/\text{!Cout}$ circuit is the same implementation as the one used in a standard full adder, such as in the circuit implemented with Equation 1.

The design of the Sum circuitry was fairly straight forward. The PDN would have two leakage paths to ground. One of the paths would be A, B, and C all connected in series, and the other path would have !Cout connected in series with the A,B, and C all connected in parallel. With this implementation, any of the signals selected from the first path would be a viable option from the first path (in this case A was chosen). However, in the second path, in order to limit the number of transistors required in the PUN, !Cout was selected since it was common with the parallel circuitry of A,B, and C. As stated before the design of the $\text{Cout}/\text{!Cout}$ circuit are exactly the same implementation as the design in Circuit 1.

For the sum circuit sizing, there are two PMOS transistors in the PUN resulting in a sizing of 4 for both of them. In the PDN, the first path has three NMOS transistors connected in series resulting in a sizing of 3 for those. And in the second path, all of the paths to ground have just two transistors, so this results in a sizing of 2 for all of the transistors in the PDN of the second path to ground. The discussion of the PDN and PUN for the $\text{Cout}/\text{!Cout}$ circuit can be found in the Circuit 1 section since the circuit implementation are the same and the circuit schematics can be found in Appendix 1: Circuit 1 D3L. Finally, the circuit schematic for the new Sum circuit for the D3L implementation of Equation 3 can be found in Appendix 1: Circuit 3 D3L.

SPD3L:

Similarly to the rest of the SPD3L circuits, the main driving force behind this logic structure is to break up the PUN to reduce the sizing of the PMOS transistors in series. In the case for Circuit 3 (Bonus Circuit) the sum circuitry had two leakage paths to ground. These were split up into two circuits and the DN nodes connected through a standard NAND gate. This circuitry can be seen in Appendix 1: Circuit 3 SPD3L.

By splitting up the PUN, the PMOS transistors sizes could be reduced from 4 down to 2. As discussed in the D3L section, the A signal was used in the first path with the three series connected devices, and the !Cout signal was used in the second path in order to limit the number of paths due to the !Cout transistor being shared between all three A, B, and Ci transistors connected in series in the second leakage path. All of the transistor sizes were kept the same in the DPN.

As before, the $\text{Cout}/\text{!Cout}$ circuitry was identical to the SPD3L implementation done in Circuit 1, for the discussion on the sizing can be found in the Circuit 1 section. The schematics for $\text{Cout}/\text{!Cout}$ can be found under Appendix 1: Circuit 1 SPD3L.

Functional Validation and Verification

In order to validate the circuits, test bench cases were developed to verify proper functioning. The validation started with the 1-bit adder to ensure the proper implementation of this. The test benches were then scaled up to the 4-bit adders. Below in Figure 7 is the general layout of the 1-bit test. For each of the six circuits created the Full Adder (seen below as a square) was swapped out with the respective circuit that was being test. It was then from here that the simulation was run and a netlist was obtained.

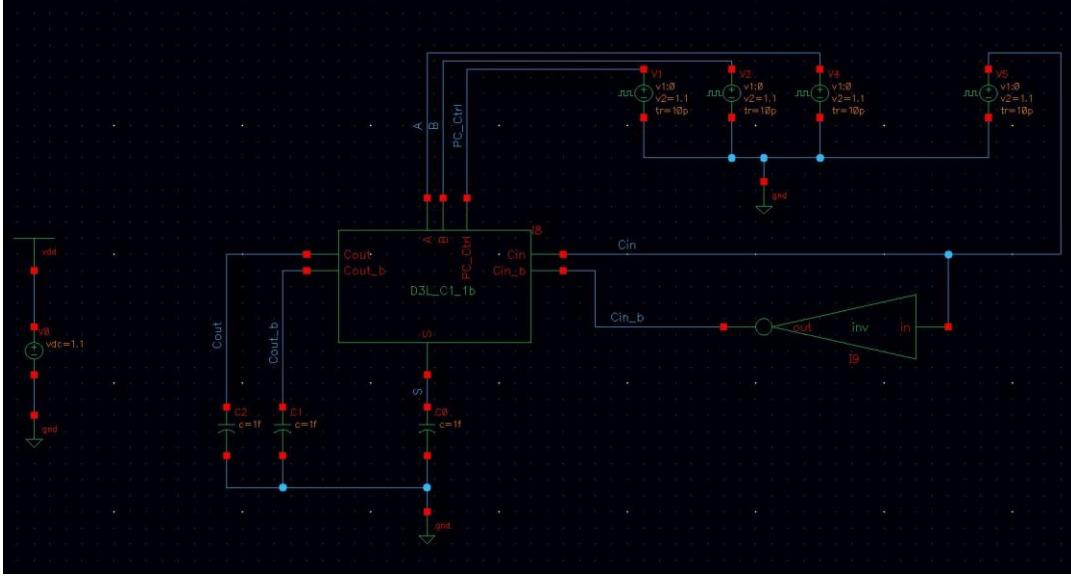


Figure 7: 1-Bit testing circuit

To ensure that the circuits were working properly, the circuit inputs also needed to be set-up in the correct way due to the nature of the pre-charge and the evaluation signals. To be safe the waveforms were developed to ensure that the A, B, and Ci only changed when the pre-charge signal was not asserted (meaning the circuits were in the pre-charge state). When the pre-charge signal is asserted (1.1 V) then the circuits would be evaluated. The following table highlights the rise time, fall time, pulse width, and period of each of the signals for the 1-bit adder.

1-bit Input Waveform Characteristics

Signals	Rise Time (pS)	Fall Time (pS)	Pulse Width (pS)	Period (pS)
PC Signal	10	10	200	400
A	10	10	240	400
B	10	10	240	400
Ci	10	10	240	400

An example of the pulses can be found in Appendix 2: Logic Verification where signal A is 0 during evaluation, B is 1.1 during evaluation, and Ci is 0 during evaluation.

To make running through all eight test benches more streamline a sweep function was developed. Since the same test bench circuit was used and the full adder was switched in with a different cell all of the net names were the same. This allowed for one sweeping function to be developed and copied into each respective netlist. The sweeping function defines both the asserted and the non-asserted value for each of the inputs besides the pre-charge signal since that was constant throughout each test circuit. The sweeping function is defined below.

```
.TRAN 1e-12 800e-12 START=0.0 SWEEP DATA=D
.DATA D
+A1 !A1 B1 !B1 C1 !C1    ** A B C
+0 1.1 0 1.1 0 1.1    ** 0 0 0
+0 1.1 0 1.1 1.1 0    ** 0 0 1
+0 1.1 1.1 0 0 1.1    ** 0 1 0
+0 1.1 1.1 0 1.1 0    ** 0 1 1
+1.1 0 0 1.1 0 1.1    ** 1 0 0
+1.1 0 0 1.1 1.1 0    ** 1 0 1
+1.1 0 1.1 0 0 1.1    ** 1 1 0
+1.1 0 1.1 0 1.1 0    ** 1 1 1
.ENDDATA
```

To take advantage of this feature, the variables defined in the first line were then plugged into the PULSE definition later on in the HSPICE file. The pulse definition used in all of the 1-bit adders can be seen below.

```
v4 a 0 PULSE !A1 A1 0 10e-12 10e-12 240e-12 400e-12
v2 b 0 PULSE !B1 B1 0 10e-12 10e-12 240e-12 400e-12
v5 cin 0 PULSE !C1 C1 0 10e-12 10e-12 240e-12 400e-12
```

To verify that each circuit worked properly the CSCOPE program was used to plot the inputs, and the outputs of the 1-bit adder. For each of the test cases above all the lines were commented out besides the one that was being tested to make it simpler to identify on the scope, the .output file was then re-compiled and the updated graph was reloaded on the scope. This process was performed for each of the eight test cases below and for each of the six circuit types. All the circuits were verified to function properly; however only a single test case for each circuit was captured as a screenshot to help limit the amount of screenshots attached to the appendix. Below is a table that summarizes the circuits, which test was captured, and the results that were taken from the capture that can be seen in Appendix 2: Logic Verification.

1-Bit Adder Verification

Circuit	A	B	Cin	S	Cout	<i>Cout</i>
C1 D3L	0	1	0	1	0	1
C1 SPD3L	1	1	1	1	1	0
C2 D3L	1	0	1	0	1	0
C2 SPD3L	1	0	0	1	0	1
C3 D3L	0	0	1	1	0	1
C3 SPD3L	0	0	0	0	0	1

Since all of the 1-bit adders were verified to be correct the 4-bit adder was constructed using 1-bit adders. This circuit is the implementation seen in Figure 5. It is a carry ripple adder, so the outputs of the 1st stage are inputted into the 2nd stage etc.

Once again the waveforms were created in a way to ensure that the input values did not change while the circuit was in the evaluation mode to make sure the circuit was working properly in pre-charge/evaluation phases. The following table highlights the rise time, fall time, pulse width, and period of each of the signals for the 1-bit. In general they are identical to the ones used in the 1-bit implementation however now that it is a 4-bit adder there are more signals that need to be accounted for.

4-bit Input Waveform Characteristics

Signals	Rise Time (pS)	Fall Time (pS)	Pulse Width (pS)	Period (pS)
PC Signal	10	10	200	400
A0	10	10	240	400
A1	10	10	240	400
A2	10	10	240	400
A3	10	10	240	400
B0	10	10	240	400
B1	10	10	240	400
B2	10	10	240	400
B3	10	10	240	400
Ci	10	10	240	400
<i>Ci</i>	10	10	240	400

In the case of the 4-bit adder, since all of the inputs were verified to be correct in the 1-bit adder, there were only five test cases chosen for testing the 4-bit adder. To make running through these five test benches more streamline

another sweep function was developed. The same test bench circuit was used and the full adders were swapped for each of the six different circuits. This meant that all of the nets within the circuit were the same and the following two code snippets could be copied into each of the .hspice files in order to sweep the test cases.

```
.TRAN 1e-12 800e-12 START=0.0 SWEEP DATA=D
.DATA D
+A3 A2 A1 A0 B3 B2 B1 B0 Ci !A3 !A2 !A1 !A0 !B3 !B2 !B1 !B0 !Ci
+0 0 0 1.1 0 1.1 0 1.1 0 1.1 1.1 1.1 0 1.1 0 1.1 0 1.1 **1+ 5 + 0
+1.1 0 1.1 0 0 0 1.1 1.1 1.1 0 1.1 0 1.1 1.1 1.1 0 0 0 **10+3 + 1
+0 0 0 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 0 1.1 1.1 0 0 0 **0+15 + 1
+1.1 1.1 1.1 1.1 1.1 0 1.1 1.1 1.1 1.1 0 0 0 1.1 0 0 0 0 **7+15 + 1
+1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 0 0 0 0 0 0 0 0 0 **15+ 15 + 1
.ENDDATA
```

To take advantage of the sweeping feature, the variables defined in the first line were then plugged into the PULSE definition later on in the HSPICE file. The pulse definition used in all of the 4-bit adders can be seen below.

```
v17 a3 0 PULSE !A3 A3 0 10e-12 10e-12 240e-12 400e-12
v14 a2 0 PULSE !A2 A2 0 10e-12 10e-12 240e-12 400e-12
v7 a1 0 PULSE !A1 A1 0 10e-12 10e-12 240e-12 400e-12
v13 a0 0 PULSE !A0 A0 0 10e-12 10e-12 240e-12 400e-12

v16 b3 0 PULSE !B3 B3 0 10e-12 10e-12 240e-12 400e-12
v15 b2 0 PULSE !B2 B2 0 10e-12 10e-12 240e-12 400e-12
v6 b1 0 PULSE !B1 B1 0 10e-12 10e-12 240e-12 400e-12
v12 b0 0 PULSE !B0 B0 0 10e-12 10e-12 240e-12 400e-12

v5 ci 0 PULSE !Ci Ci 0 10e-12 10e-12 240e-12 400e-12
v18 ci_b 0 PULSE Ci_ !Ci_ 0 10e-12 10e-12 240e-12 400e-12
```

To verify that each circuit worked properly the CSCOPE program was used to plot the inputs, and the outputs of the 4-bit adder. For each of the test cases above, all the lines were commented out besides the one that was being tested to make it simpler to identify on the scope, the .output file was then re-compiled and the updated graph was reloaded on the scope. This process was performed for each of the five test cases below and for each of the six circuit types. All the circuits were verified to function properly; however only a single test case for each circuit was captured as a screenshot to help limit the amount of screenshots attached to the appendix. Below is a table that summarizes the circuits, which test was captured, and the results that were taken from the capture that can be seen in Appendix 2: Logic Verification.

4-Bit Adder Verification

Circuit	A	B	Cin	S	Cout	<i>!Cout</i>
C1 D3L	0001	0101	0	0110	0	1
C1 SPD3L	1010	0011	1	1110	0	1
C2 D3L	0000	1111	1	0000	1	0
C2 SPD3L	0111	1111	1	0111	1	0
C3 D3L	1111	1111	1	1111	1	0
C3 SPD3L	1010	0011	1	1110	0	1

Performance Results

Average Power

In order to compare these six circuits, multiple tests were performed included power, leakage, and delay analysis. In order to perform the power analysis two methods were used. The first utilized the built in .Measure function in HSPICE to measure the average power and the max power of the circuit over a given interval. This is done by using the following code: [1]

```

.PRINT TRAN POWER
.MEASURE TRAN avgpwr AVG POWER FROM 0 TO 800e-12
.MEASURE TRAN maxpwr MAX POWER FROM 0 TO 800e-12
.MEASURE TRAN avg_vdd AVG P(v0) FROM 0 TO 800e-12

```

The second method was to use a program called NanoSim. This was used to verify the validity of the previous average power calculation. Unfortunately NanoSim did not support the sweep function so each of the test cases had to be manually inputted. This can be seen in the .sp files attached in Appendix 3: HSPICE Netlist Files. The netlist attached have the functions that were altered for nanosim computation commented out. The process of running nanosim will be discussed in the next section.

The sweep function that was defined in the previous section can again be used with the .measure statement. With the sweep statement and the entire test benches all-ready set up the netlist file only had to be run once through HSPICE to perform all of the power calculations for the given circuit. All of the data was then retrieved from the .output file and recorded. This was done for all the six implementation of the 1-bit adder as well as all six implementations of the 4-bit adder. These results can be found in Appendix 4: Performance Results Average Power. For each the 1-bit and the 4-bit circuits the average of the average power, max power, and average Vdd were taken to produce the following tables.

1-Bit Average of the Average Results

Circuits	Avg Pwr(Nano Sim) (uW)		Avg Pwr(uW)	Max Pwr(uW)	Avg Vdd(uW)	# of Trans
D3L 1-Bit	C1	65.669	65.567625	552.7875	-63.277375	63
	C2	86.455	86.2955	538.31125	-84.05975	75
	C3	62.289	62.247375	532.68375	-59.962625	60
SPD3L 1-Bit	C1	65.161	65.245625	553.21125	-62.888125	72
	C2	83.561	83.452375	518.55375	-81.150125	90
	C3	62.075	62.21875	532.835	-57.519375	69

In the case of the 1-bit adder it can be seen that overall the SPD3L circuit outperformed the D3L. This is a very predictable result as the SPD3L is designed to do as such. Since in all of our circuit implementations the PUN network only had a single PMOS transistor, and it had a smaller size when compared to the PUN's in the D3L. As far as circuits go both the D3L and SPD3L implementations of circuit three had a lower average power than the standard full adder implementation seen in Circuit 1, about a 5% decrease in average power usage. Circuit 2 was by far the worst implementation, using about 30% more power on average than the standard full adder seen in Circuit 1. This is due to the increase in the logic needed to perform the operation (about 20% increase in the number of transistors used when compared to Circuit 1).

4-Bit Average of the Average Results

Circuits	Avg Pwr(Nano Sim) (uW)		Avg Pwr(uW)	Max Pwr(uW)	Avg Vdd(uW)
D3L 1-Bit	C1	251.4274	249.634	1945.98	-242.842
	C2	331.548	327.96	1757.6	-322.242
	C3	247.086	245.09	1947.1	-238.11
SPD3L 1-Bit	C1	253.928	252.328	1948.64	-245.48
	C2	310.272	307.19	1657.38	-301.392
	C3	246.832	245.354	1948.78	-238.284

Similar results can be seen in the 4-bit implementation of the adder with the exception of the SPD3L circuit 1 implementation which used slightly more power than the D3L circuit. In Appendix 4: Performance Results Average Power, the average power for Circuit 1 SPD3L implementation was higher due to the test cases of adding 7+15+1 and 15+15+1, using significantly more power. This implies that this circuit is heavily dependent on the input values; however since only a handful of test cases were used to test the 4-bit adder, it could be argued that if the amount of test cases were expanded this number would average out to be about the same, or even less than the D3L implementation of Circuit 1, as seen in the 1-bit analysis. Nanosim and the .measure results were very comparable and if they varied, it was only by a few uW, this could be due to different power measurement techniques with in the two different implementations.

Taking the average power results only, both the implementations of Circuit 3 outperformed the other two implementations. Circuit 3 was by far the worst implementation out of the three in terms of average power usage.

Leakage Current

Nanosim was used to verify the measurements of the average power as well as to calculate the leakage current of each of the circuits. As mentioned in the previous section, NanoSim was not compatible with the sweep function so each of the test cases had to be implemented separately. To run NanoSim the following code was used to produce the results [1].

```
% nanosim nspice ./input.sp ./power.cfg o ./power
```

For each test case all of the data was then retrieved from the power.log file and recorded. This was done for all the six implementation of the 1-bit adder as well as all six implementations of the 4-bit adder. These results can be found in Appendix 4: Performance Results NanoSim Outputs. For each the 1-bit and the 4-bit circuits the averages of all of the results were obtained and can be seen below in the tables.

1-Bit Average of the Average Results from NanoSim

Circuits		Avg S C(uA)	Avg C C (uA)	Avg W C (uA)	Avg SWC (uA)	Avg DWC(uW)	WC %
D3L 1-Bit	C1	-59.695	-62.534	-4.808	-0.000053375	-4.808	6.862
	C2	-78.588	-74.556	-11.437	-0.0002655	-11.437	13.219
	C3	-56.627	-57.572	-5.139	-0.000197625	-5.139	7.934
SPD3L 1-Bit	C1	-59.236	-60.525	-5.499	-0.0001785	-5.498	8.093
	C2	-75.965	-69.841	-11.612	-0.000338375	-11.610	14.219
	C3	-56.43	-55.805	-5.986	-0.000244	-5.986	9.409

The main leakage occurred by the Dynamic waster current. This is caused when the dynamic node is precharged high and then left floating, the voltage on the dynamic node will drift over time due to subthreshold, gate, and junction leakage [4]. In our circuit implementations this is reduced by the keeper circuit. In an ideal case the keeper would be 1/10th of the size of the other transistors but in our circuits they were set to the lowest value they could (Virtuoso only allowed for the transistor to be 1).

The wasted current percentage can be seen to be the least in the circuit 1 of the D3L implementation with a wasted current percentage of just 6.86%. The D3L implementations of all of the circuits are all better than their counter parts in SPD3L; this is due to the number of dynamic nodes increasing, since each path to ground in the PDN requires its own PUN and keeper, thus another Dynamic node with possibility for leakage. The D3L circuits are about 13% better in terms of wasted current than the SPD3L implementation. This is also why the Circuit 2 implementation has such a higher value because there is a lot more logic implemented in Circuit 2 than any of the other circuits.

1-Bit Average of the Average Results from NanoSim

Circuits		Avg S C(uA)	Avg C C (uA)	Avg W C (uA)	Avg SWC (uA)	Avg DWC(uW)	WC %
D3L 4-Bit	C1	-228.568	-236.000	-21.255	-0.000646	-21.255	8.11
	C2	-301.408	-283.786	-48.526	-0.0009126	-48.526	14.5748
	C3	-224.6236	-228.51	-22.656	-0.0006482	-22.656	8.958
SPD3L 4-Bit	C1	-230.842	-230.98	-23.628	-0.0008202	-23.6294	9.1609
	C2	-296.914	-257.615	-45.314	0.0007038	-45.3114	14.9546
	C3	-224.3748	-221.431	-40.4784	-0.0008218	-24.458	9.836

Like in the 1-Bit case, scaling up to the 4-bit case yields similar results. The wasted current percentage is lower in the D3L implementations than the SPD3L implementations but by a less margin, only about 9%. And once again the circuit 2 implementation in both cases results in a significant increase compared to the other two circuit implementations.

A way to improve the dynamic wasted current would be to add a sleep transistor which creates a virtual supply. This would drastically reduce the leakage current. Another way to reduce the leakage current would be to make the keeper transistors significantly smaller than they were able to be modeled in the program. In terms of wasted current the Circuit 1 implementations are the best when compared to the others; however the Circuit 3 implementations are not far behind. Taking into consideration the average power discussed in the previous section, Circuit 3 would be a good overall decision since it has less power usage and has an almost comparable wasted current percentage to Circuit 1.

Delay Results

The program CSCOE was used to obtain the delay. The sweep function was able to be utilized to an extent with this program, for each established test case that was developed for the average power calculation all of the other test cases were commented out except the one that was being evaluated. This allowed for an easy transition between test cases, the HSPICE output needed to be calculated each time the next test bench was being run. In the CSCOE program the waveforms were then reloaded and the delays calculated. All of the delays can be found in Appendix 4: Performance Results Delay Results. The delay was calculated only when the output signals was being asserted, for example when the SUM should be not asserted there was no delay calculation. The Average of all of the delays calculated can be seen below in the 1-Bit and 4-Bit implementations. The Evaluation Delay was calculated for when the pre-charge signal was asserted to when the respective output was asserted. The Precharge delay was when the precharge signal made the transition from one to zero, and the respective output also made that transition. This was not the optimum precharge calculation since it should have been measured from the Dynamic Node, however these results still hold since the difference between the dynamic node transitioning and the output transitioning is going to an offset of the delay of an inverter or the delay of a NAND gate.

1-Bit Average Delay

Circuits		Evaluation Delay(pS)			Precharge Delay(pS)		
		PC->Co	PC->Co_b	PC->S	PC->Co	PC->Co_b	PC->S
D3L 1-Bit	C1	41.1585	45.6095	47.88775	34.37275	38.462	36.184
	C2	74.6595	67.1355	77.635	58.98275	53.48175	61.43975
	C3	41.89775	44.94025	70.84775	40.832	38.49625	54.6335
SPD3L 1-Bit	C1	39.40725	43.7535	44.53375	32.24125	35.8995	34.99225
	C2	65.96375	63.78075	71.2615	53.57375	50.31625	56.29075
	C3	39.889	42.1585	66.191	37.906	35.15025	51.574

It can be seen that the Evaluation Delay of Circuit 1 and Circuit 3 for both the calculation of Cout and !Cout have about the same delay for both the D3L and SPD3L implementation. However these circuit differ greatly in the calculation of the Sum. For the D3L implementation Circuit 1 was about 47% faster than Circuit 3, and for the SPD3L implementation Circuit 1 was about 48% faster than Circuit 3. Since the equation for Circuit 3 depends on the output of !Cout thus this value needs to be calculated first in order for the proper output of the sum value.

The Precharge delay was better for all of the cases in the SPD3L circuits. And like the Evaluation delay, circuit 1 had the best overall performance in the 1-bit case.

4-Bit Average Delay

Circuits		Evaluation Delay(pS)						Precharge Delay(pS)					
		PC->Co	PC->Co_b	PC->S3	PC->S2	PC->S1	PC->S0	PC->Co	PC->Co_b	PC->S3	PC->S2	PC->S1	PC->S0
D3L 4-Bit	C1	82.00	61.79	68.97	69.30	64.08	43.13	39.40	39.75	40.07	41.12	40.60	40.2815
	C2	101.42	83.10	95.96	97.09	100.35	73.38	59.53	49.92	60.22	61.67	61.24	61.215
	C3	81.94	61.41	88.54	75.28	67.11	49.55	40.59	38.58	51.33	49.13	46.30	43.111
SPD3L 4-Bit	C1	75.95	58.62	69.66	69.22	62.94	40.78	37.12	37.40	37.58	38.51	38.25	38.0405
	C2	95.29	73.23	84.23	82.58	83.93	64.48	54.49	48.61	56.12	55.41	55.26	55.4715
	C3	75.89	57.20	82.63	75.65	63.22	41.81	38.07	35.15	47.19	46.63	43.13	39.69

From the table above, it can be seen that in general the results discussed from the 1-bit full adder hold true. For the 4-bit adder the table below is a snapshot of the one of the worst case delay, the addition of 0 + 15 + 1. In this test case the Carry is going to propagate all of the way through the circuit, thus providing the maximum delays of the circuit.

4-Bit Maximum Delay Case

Circuits		Evaluation Delay(pS)		Precharge Delay(pS)	
		PC->Co	PC->Co	PC->Co	PC->Co
D3L 4-Bit	C1	136.64		38.967	
	C2	137.66		62.234	
	C3	135.44		39.409	
SPD3L 4-Bit	C1	115.92		35.966	
	C2	142.17		55.838	
	C3	114.29		36.306	

The D3L implementations of all of the circuits Evaluation Delay are all about the same, however the precharge delay for Circuit 2 is by far the worst compared to the others. The implementations of SPD3L for both Circuit 1 and Circuit 3 are also about the same, with Circuit 2 underperforming again. In this test case it only takes into consideration the calculation of the Cout value, for which the implementation of SPD3L Circuit 3 is the fastest for the Evaluating at only 114.29 pS. However this does not take into the consideration of any of the calculations of the Sum values.

As discussed previously since Circuit 3 needs the value of !Cout in order to calculate the value of the Sum it makes this circuit slower than the standard circuit 1 implementation but faster than the circuit 2 implementation. Assuming the full-adder is being used as a general adder with randomized inputs or unpredictable inputs, Circuit 1 implementation is the fastest, it has comparable power results compared to circuit 3, and it has the least amount of wasted current. As far as the circuit implementations of D3L and SPD3L, SPD3L has slightly faster delay results than D3L, but it has a larger average power usage and larger wasted current.

Conclusion and Future Work

The Full-adder is a key component to any digital design since it is one of the main driving forces behind CPU operations. By testing the full adder in this report it has been shown that there are many ways to implement a full-adder design; each of which has its tradeoffs.

Overall all six implementation for the 1-bit adder and all six implementations of the 4-bit adder functioned very well and the results obtained were very viable. Each of the different circuit types had its trades offs with the exception of Circuit 2 which through all the tests was shown to provide the greatest average power, the largest waster current, and slowest delay values.

Choosing between Circuit 1 and Circuit 2 have their benefits and draw backs. Given that a full adder is for general purpose use Circuit 1 would be the best choice as it gives the fastest results for the power and leakage provided. This is most likely why Equation 1 has been seen as the standard throughout digital design for the implementation of any full-adder circuit. It provides the best results overall. However, if the inputs were known and a majority of the time the Cout propagated all the way through the circuit, Circuit 3 would be a viable choice as it would provide the smallest delay for the average power and leakage current.

Future work may be on optimizing the circuit sizing, circuit techniques such as skewed gates and other techniques may be able to be utilized to provide better results. Also a main piece of work to help reduce the wasted current would be to implement a virtual supply by adding a sleep signal and a sleep transistor to the circuit. This would cut off most of the dynamic leakage current. This implementation can be seen in [3].

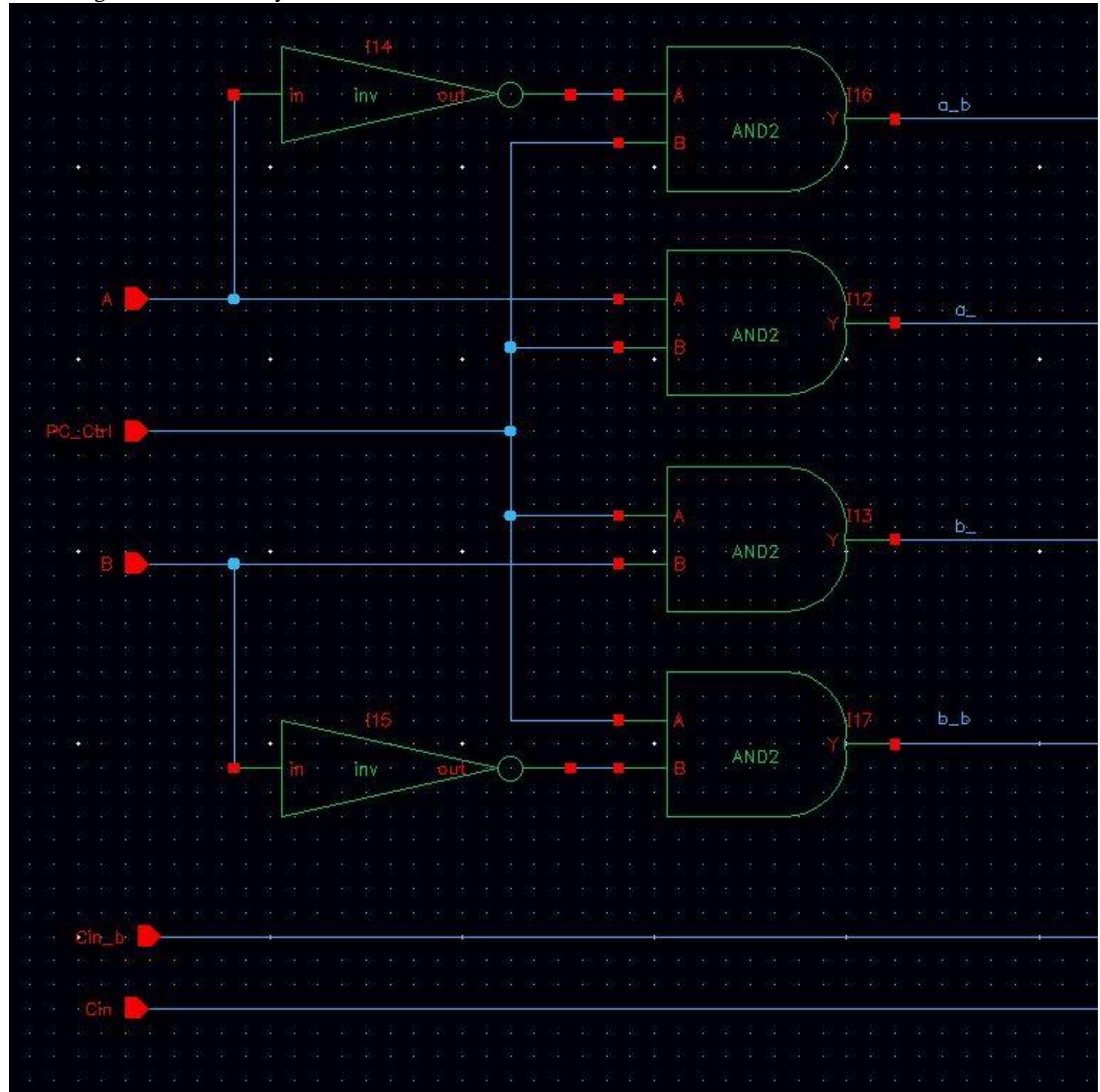
References

- [1] ECE 429, Fall 2012 Final Project Guide. Dr. Erdal Oruklu. 11/20/2012
- [2] Ramin Rafati Sied Mehdi Fakhraie Kenneth Carless Smith, “A 16-Bit Barrel-Shifter Implemented in Data-Driven Dynamic Logic (D3L)”, IEEE Transactions On Circuits And Systems—I: Regular Papers, Vol. 53, No. 10, October 2006.
- [3] F. Frustaci M. Lanuzza P. Zicari S. Perri P. Corsonello, “Low-power split-path data-driven dynamic logic”, IET Circuits Devices Syst., 2009, Vol. 3, Iss. 6, pp. 303–312
- [4] CMOS VLSI Design: A Circuits and Systems Perspective. Neil Weste, David Harris. 2011.

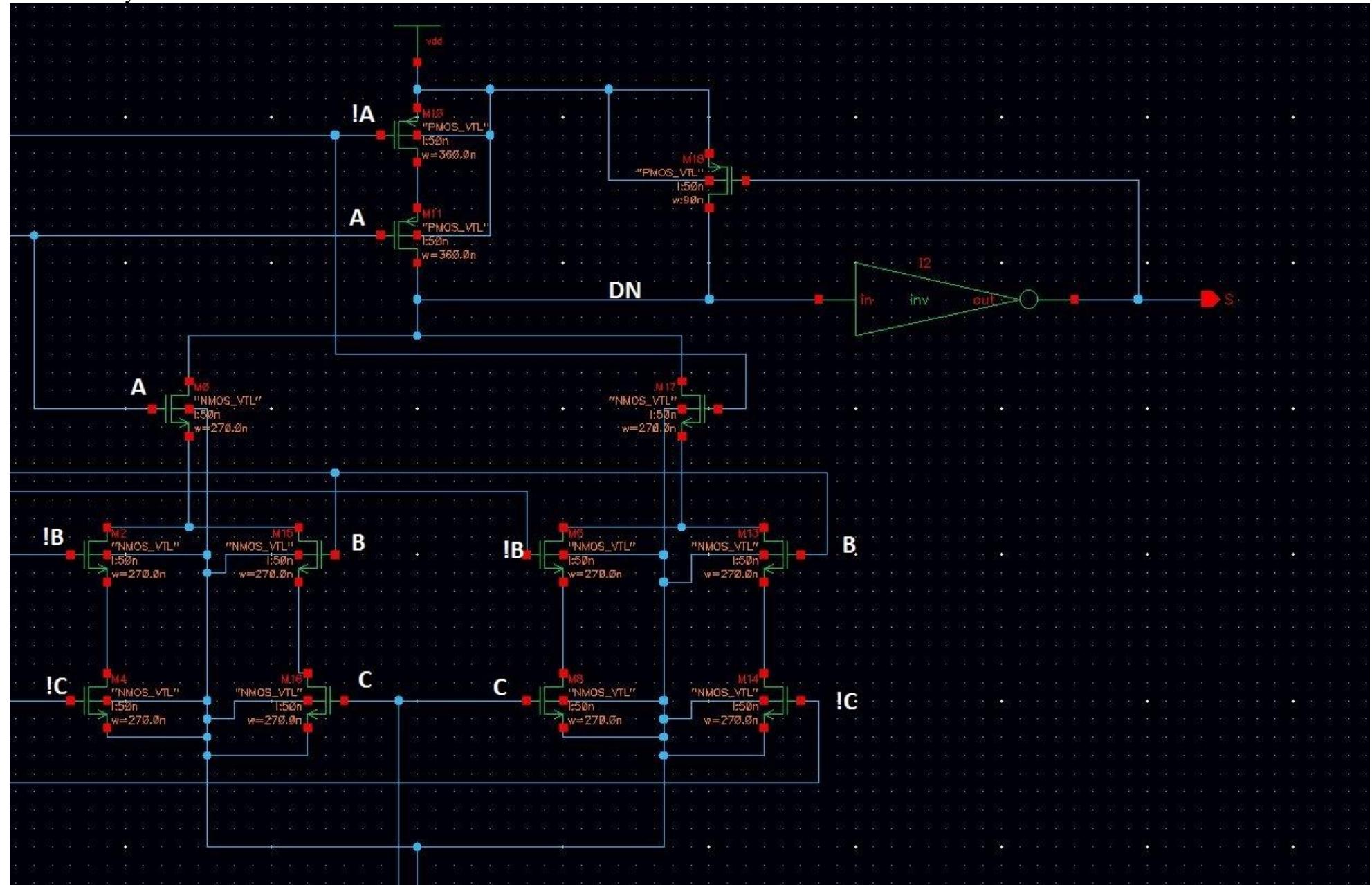
Appendix 1: Circuit Architecture

Circuit 1: D3L

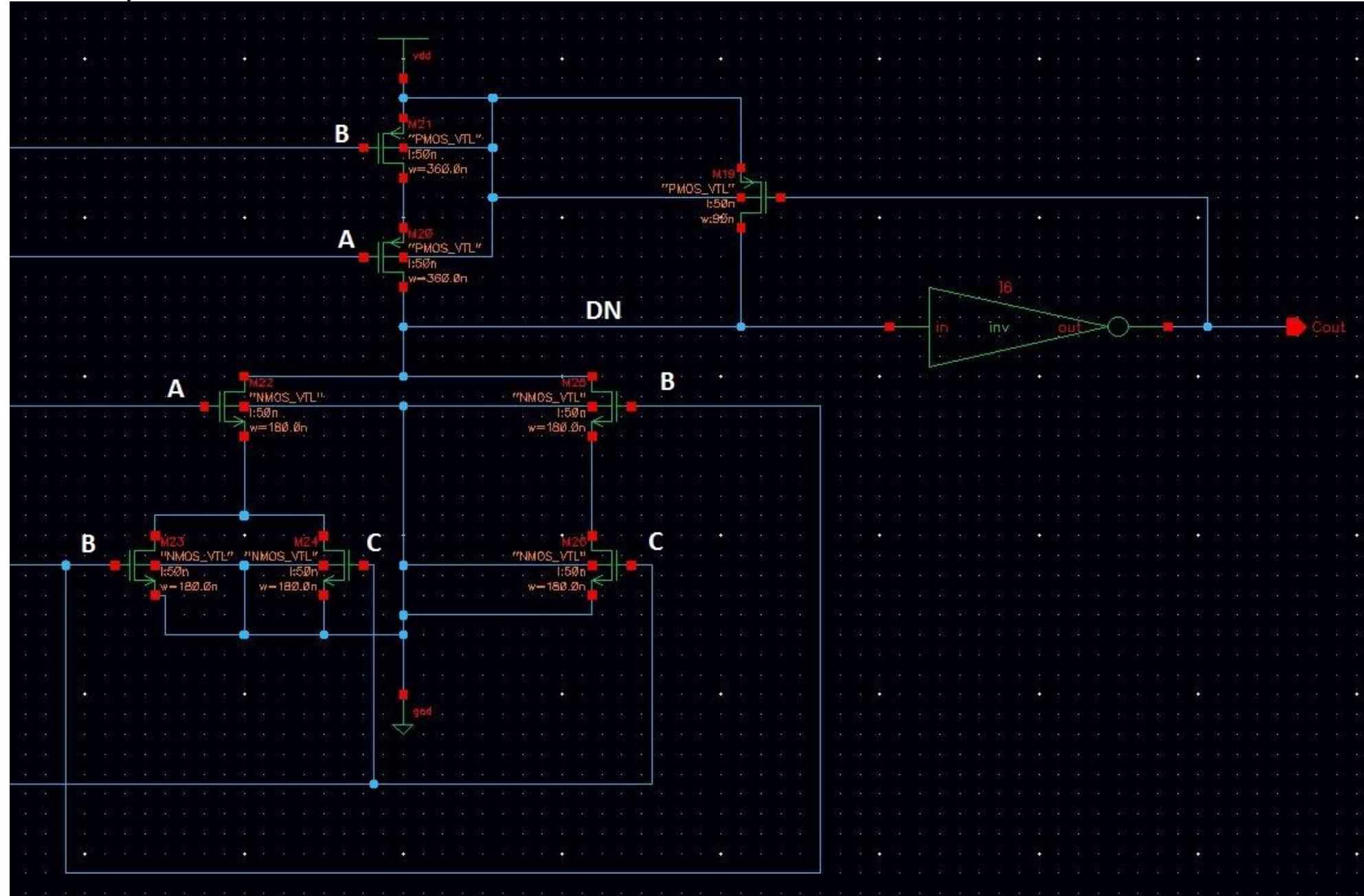
Pre-Charge Control Circuitry



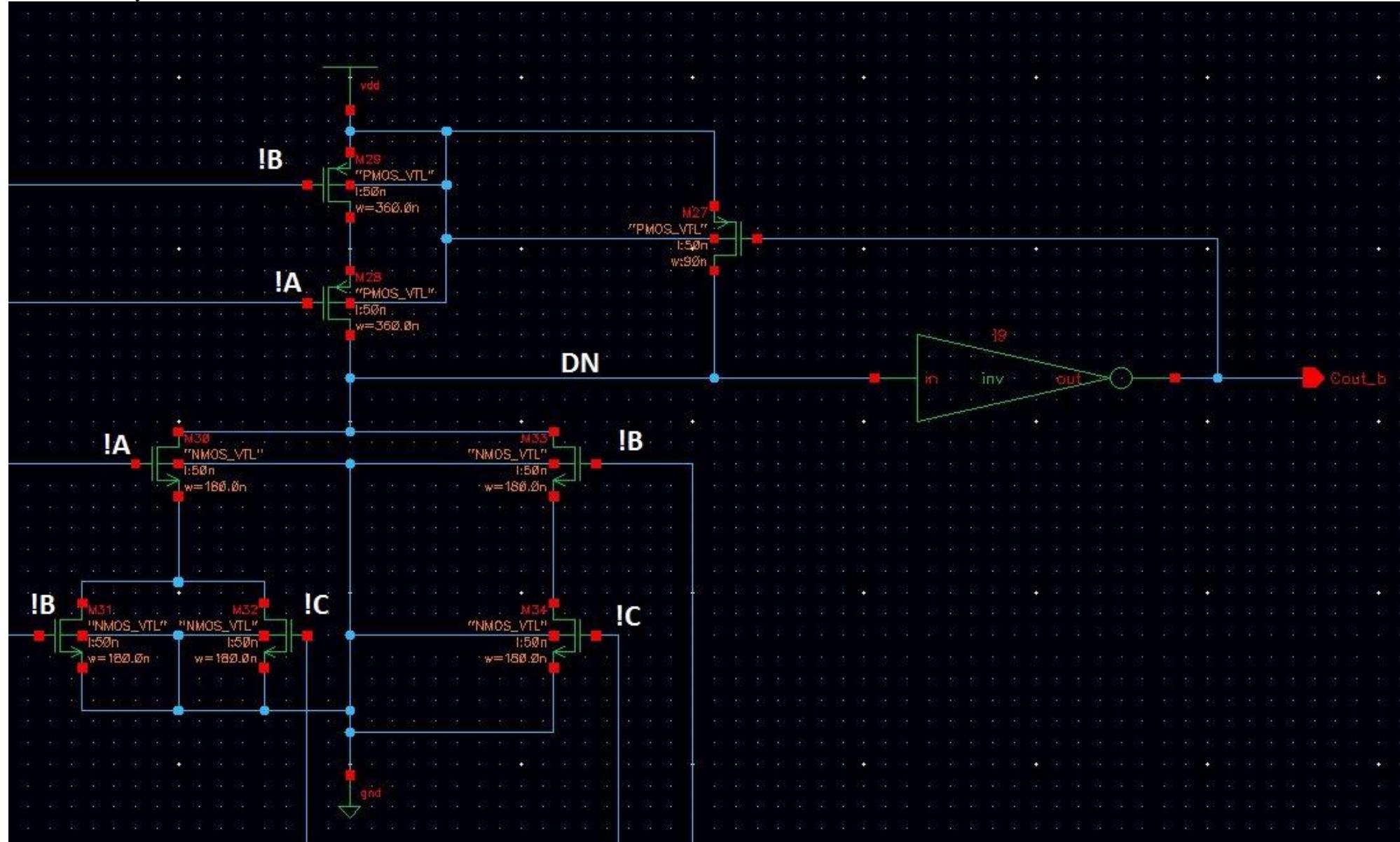
Sum Circuitry



Cout Circuitry

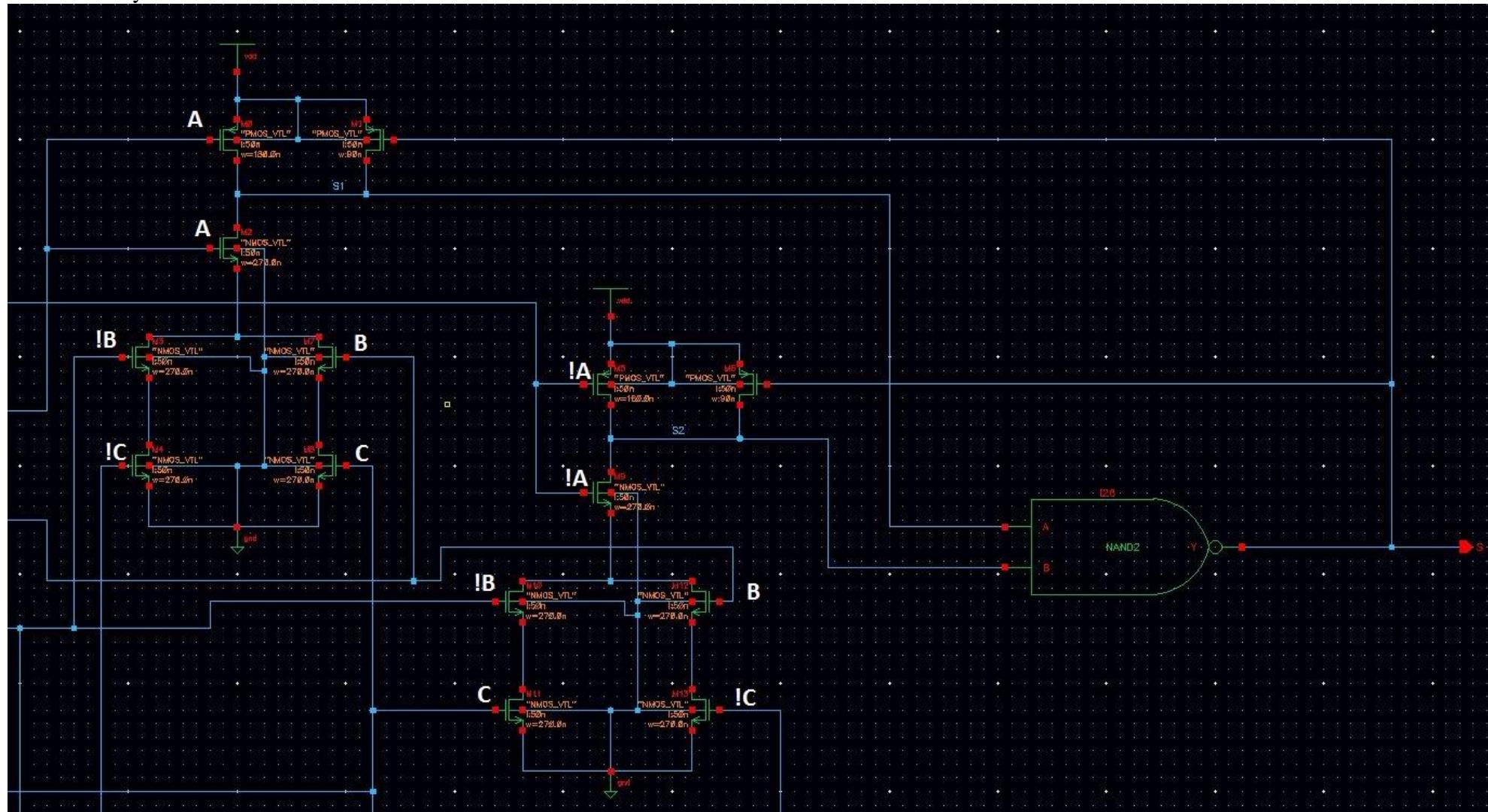


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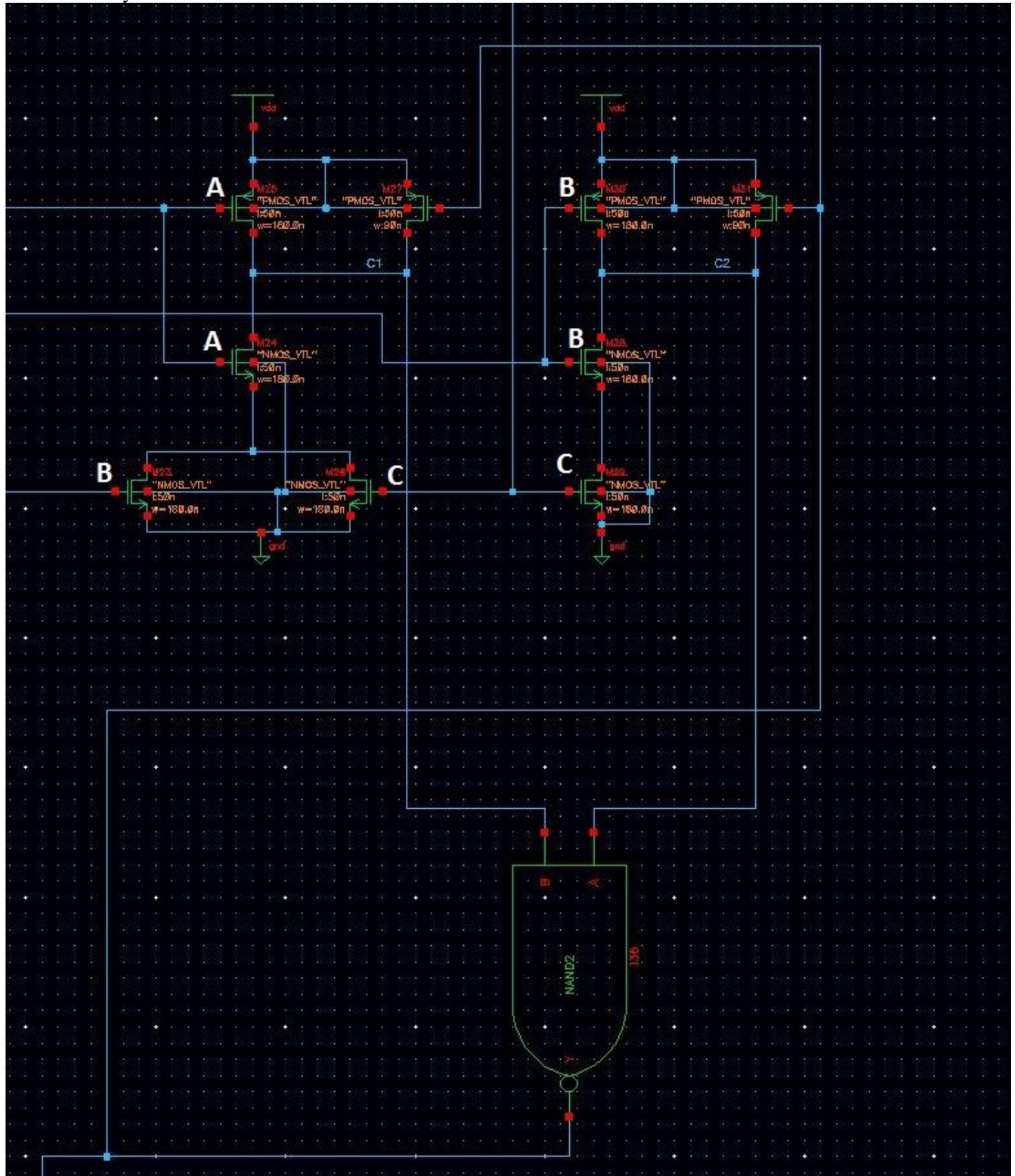


Circuit 1: SPD3L

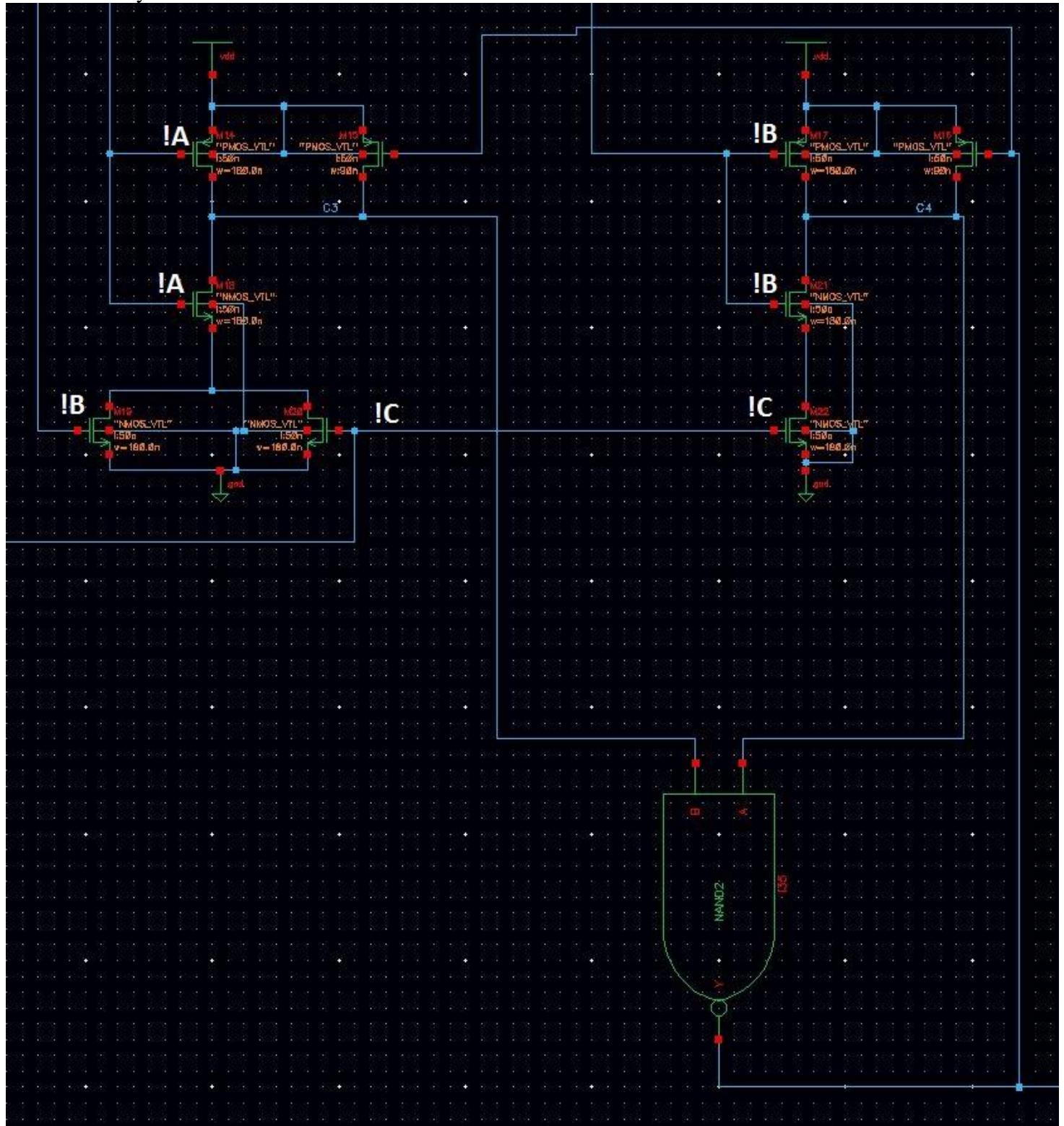
Sum Circuitry



Cout Circuitry

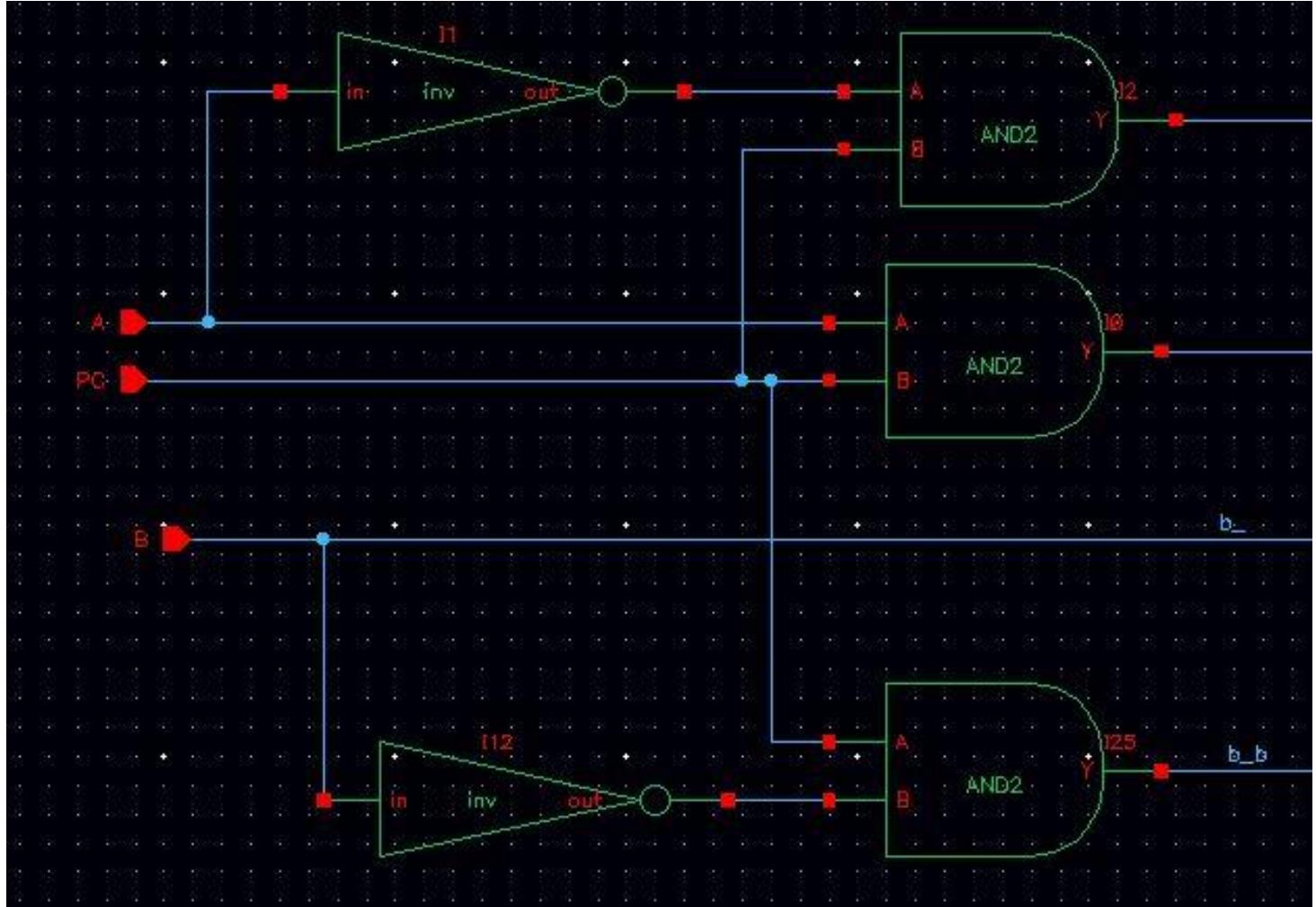


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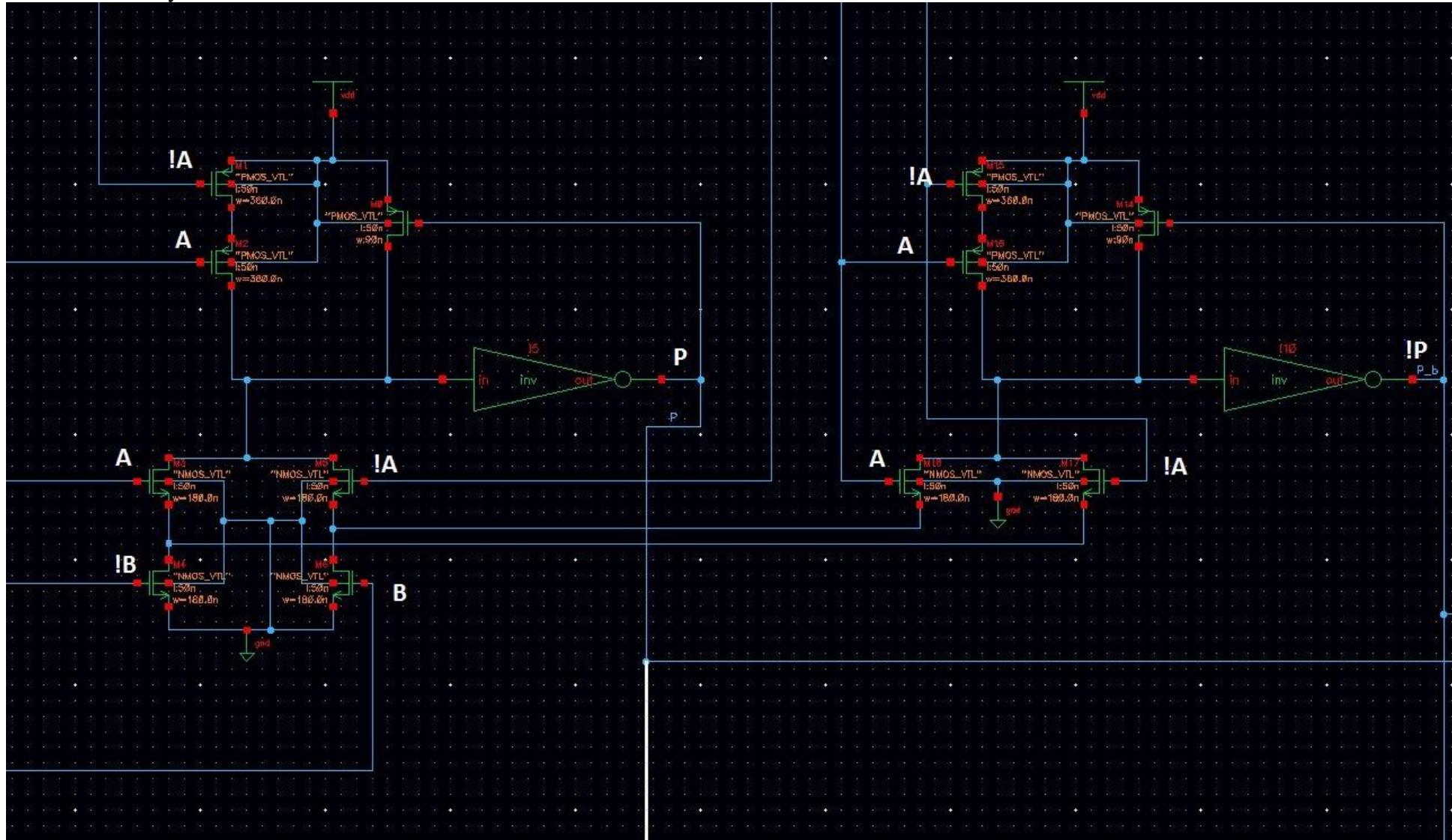


Circuit 2: D3L

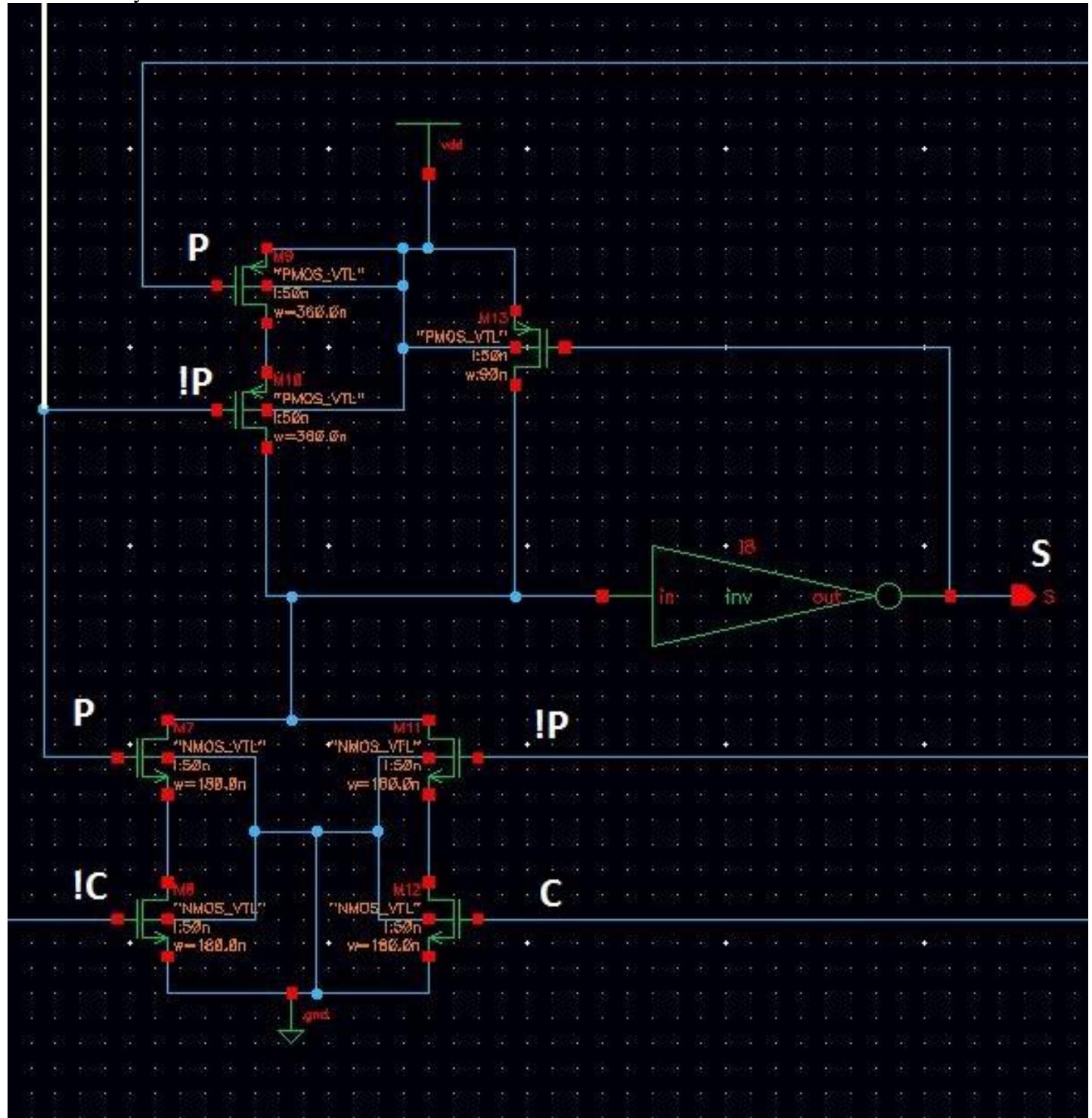
Pre-Charge Control Circuitry



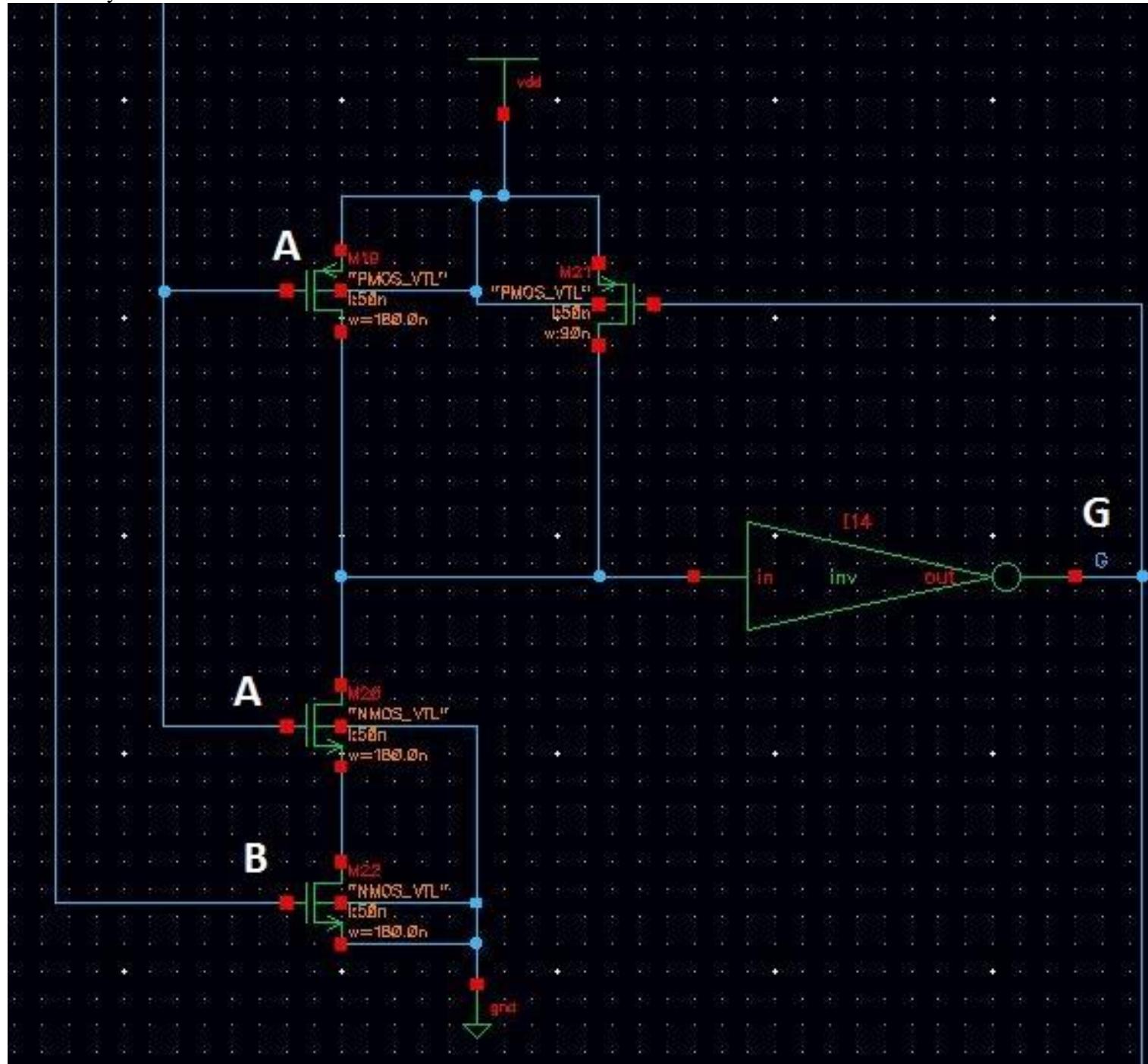
P and !P Circuitry



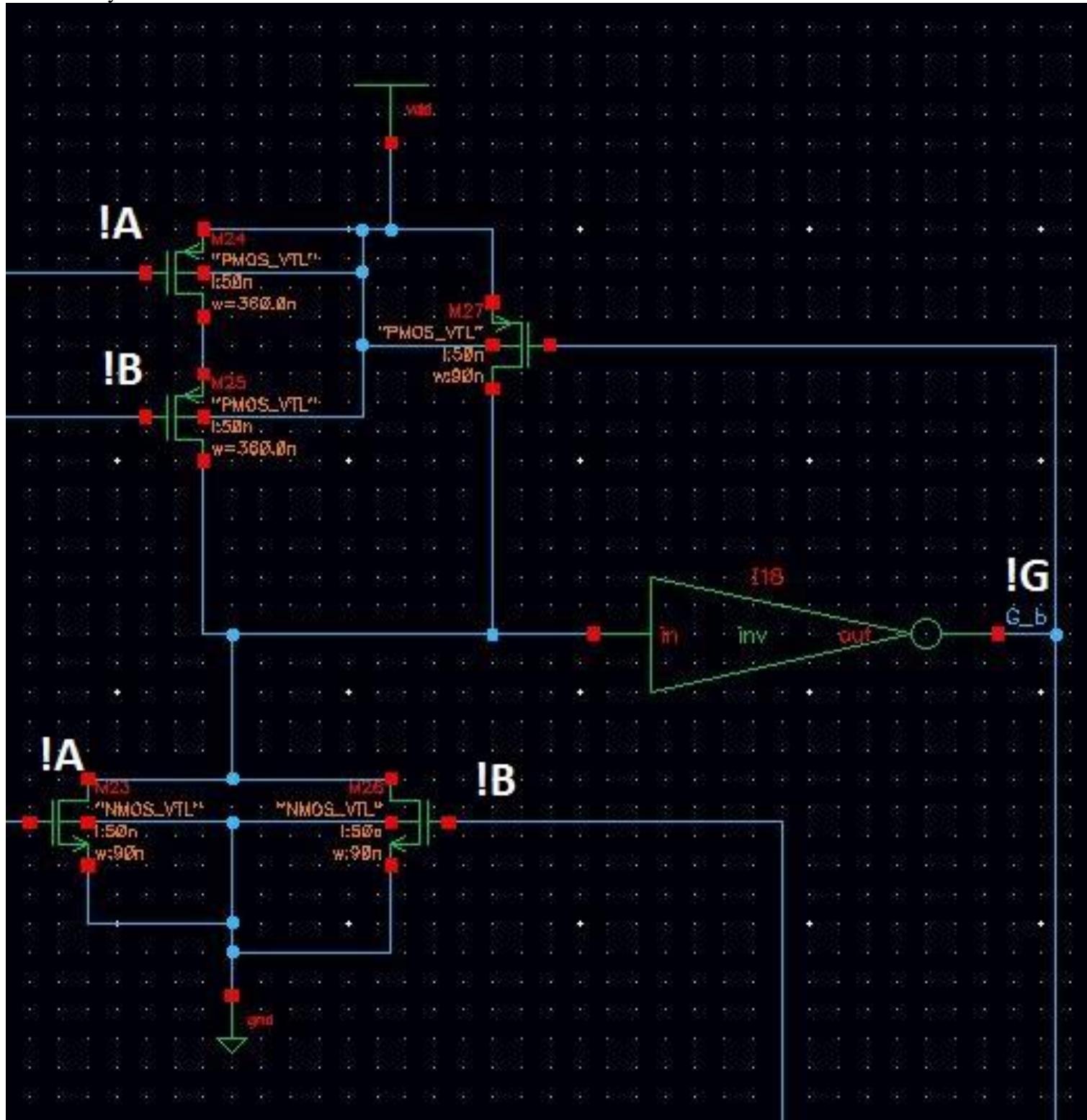
Sum Circuitry



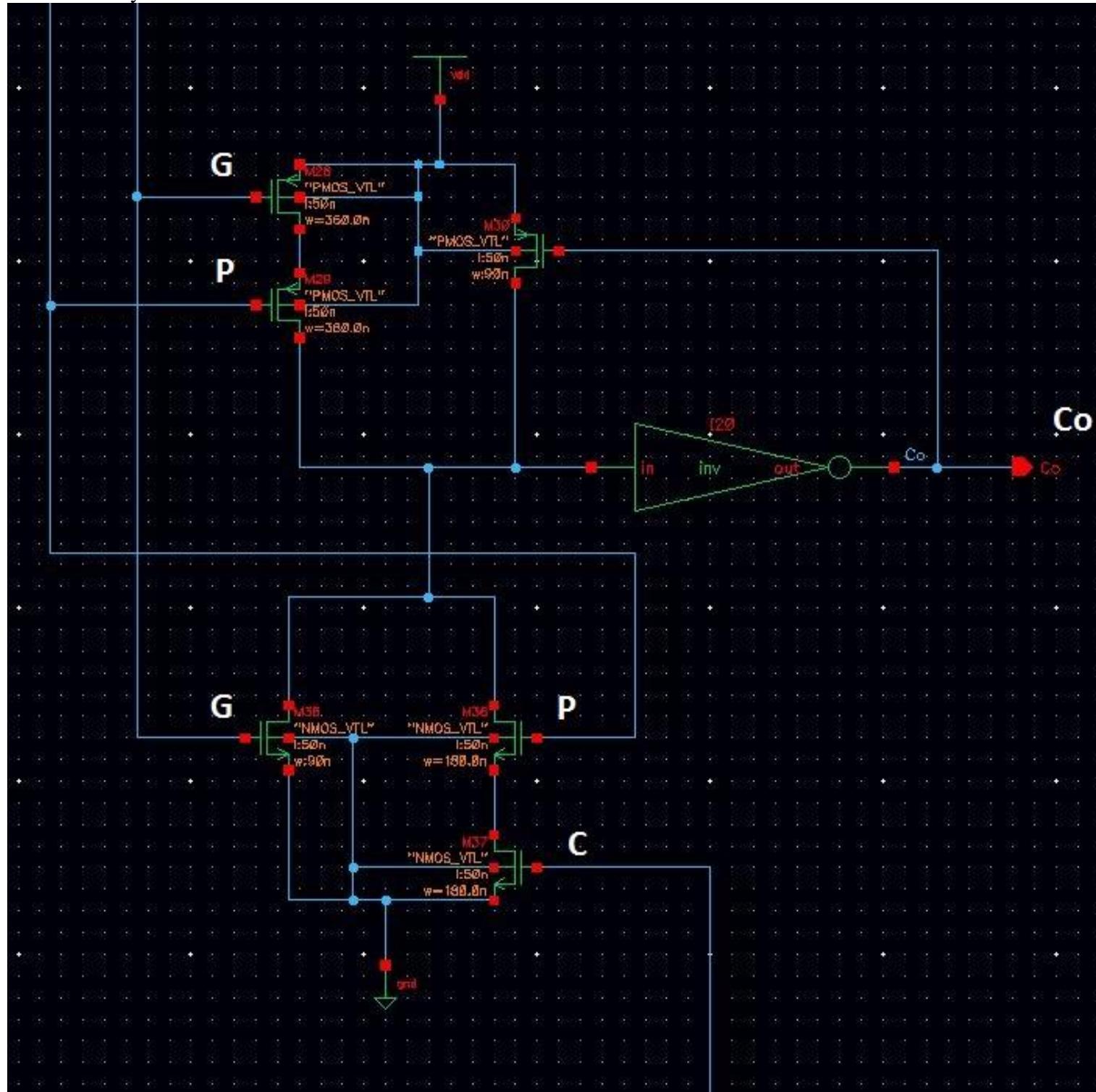
G Circuitry



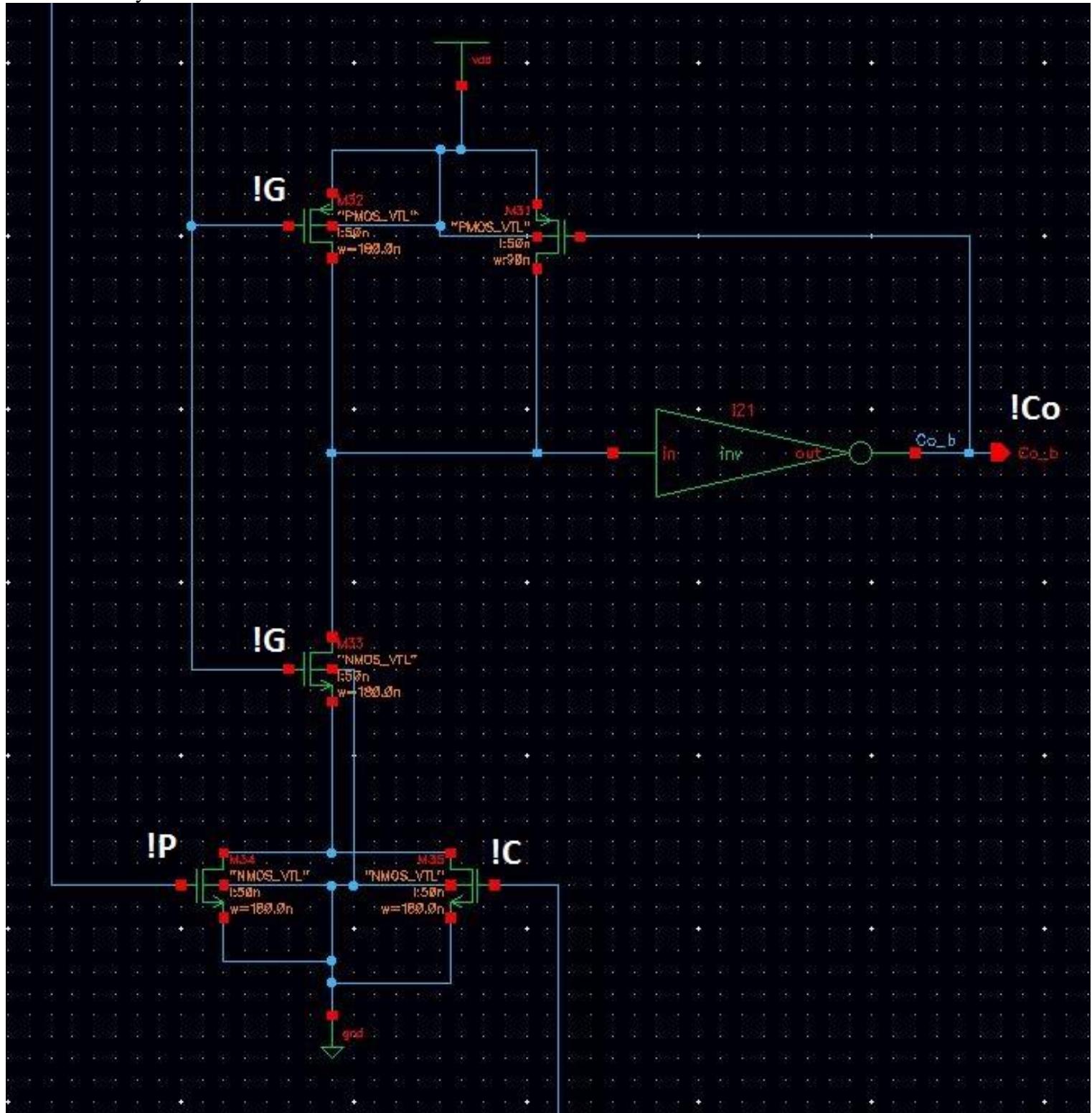
!G Circuitry



Cout Circuitry

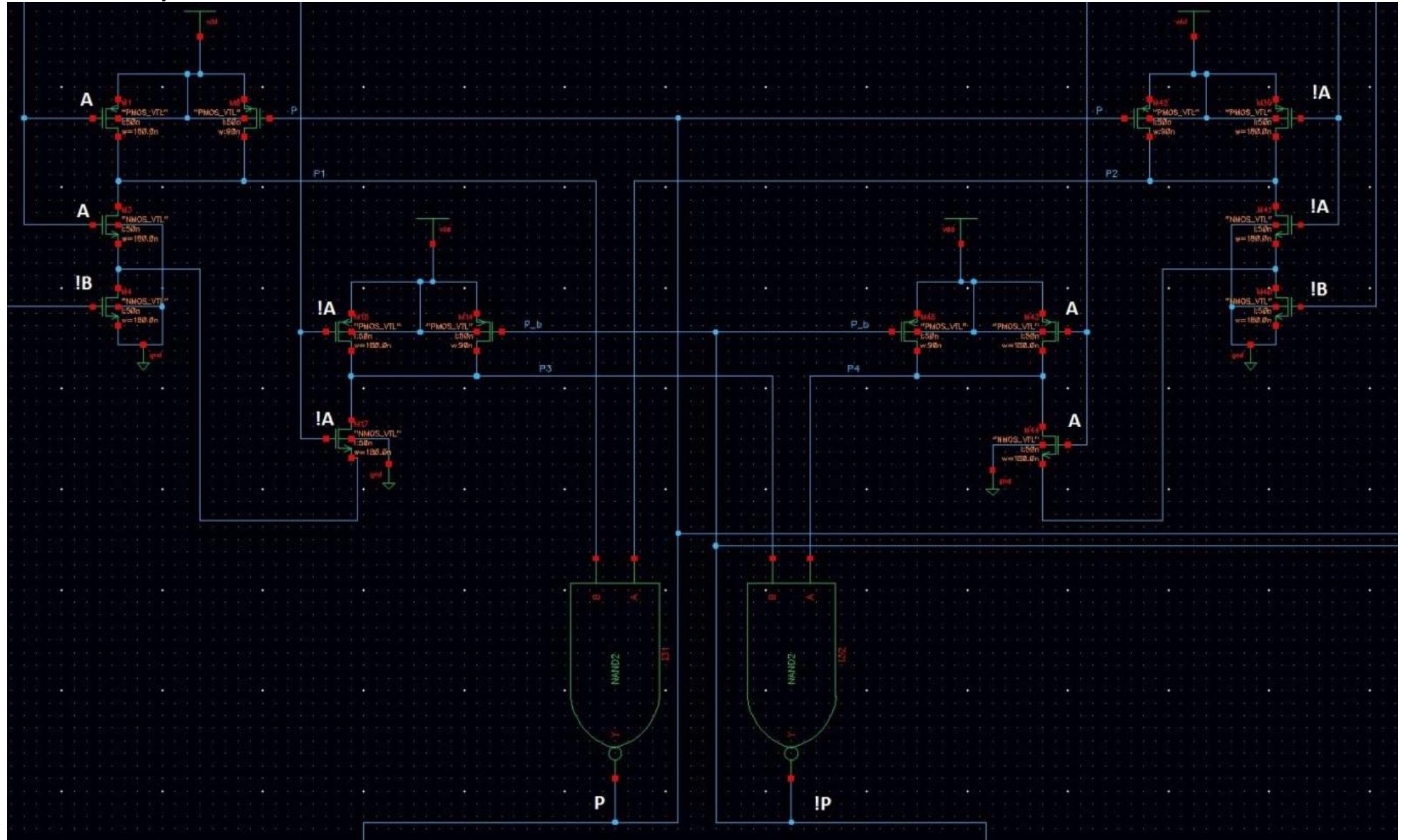


!Cout Circuitry

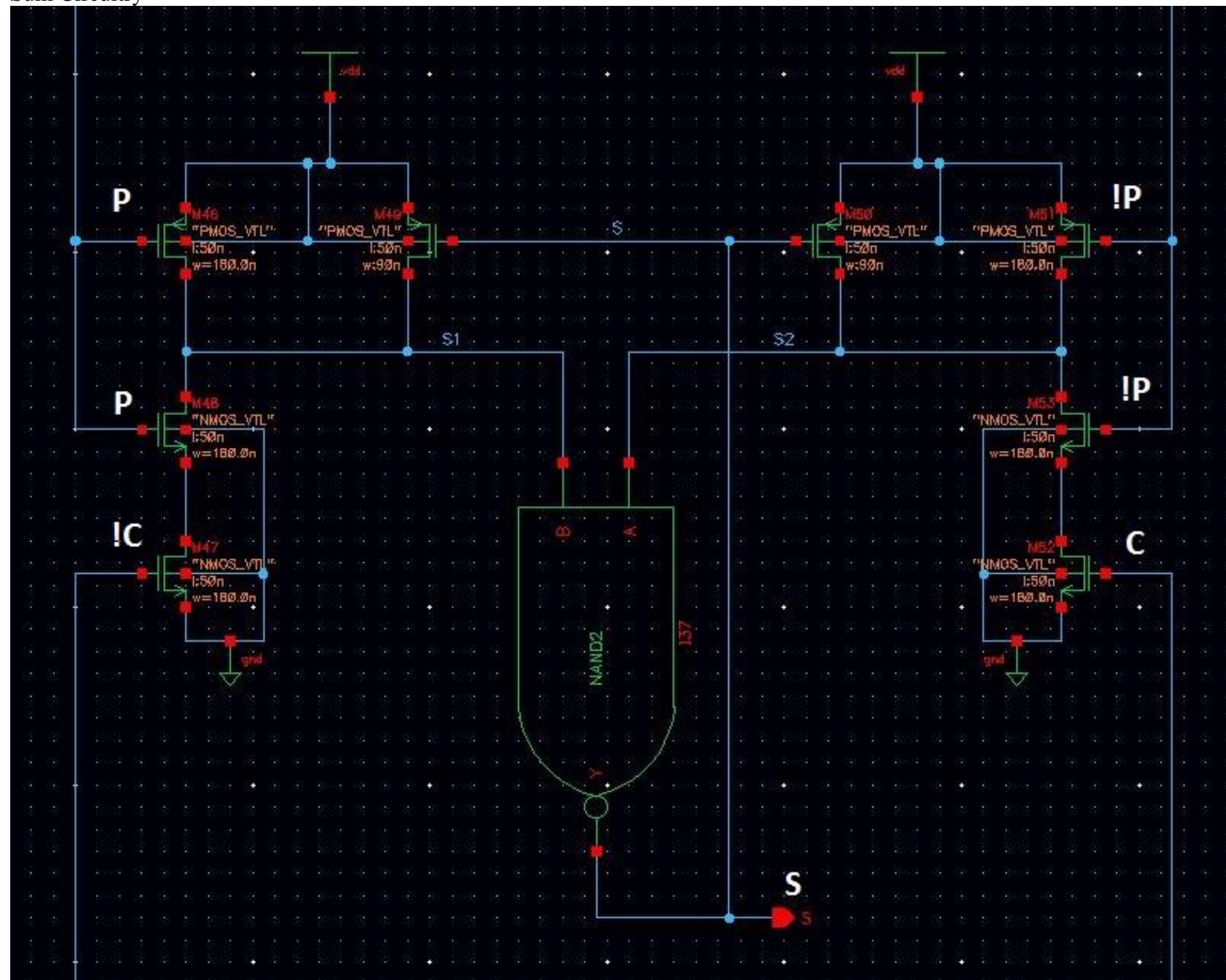


Circuit 2: SPD3L

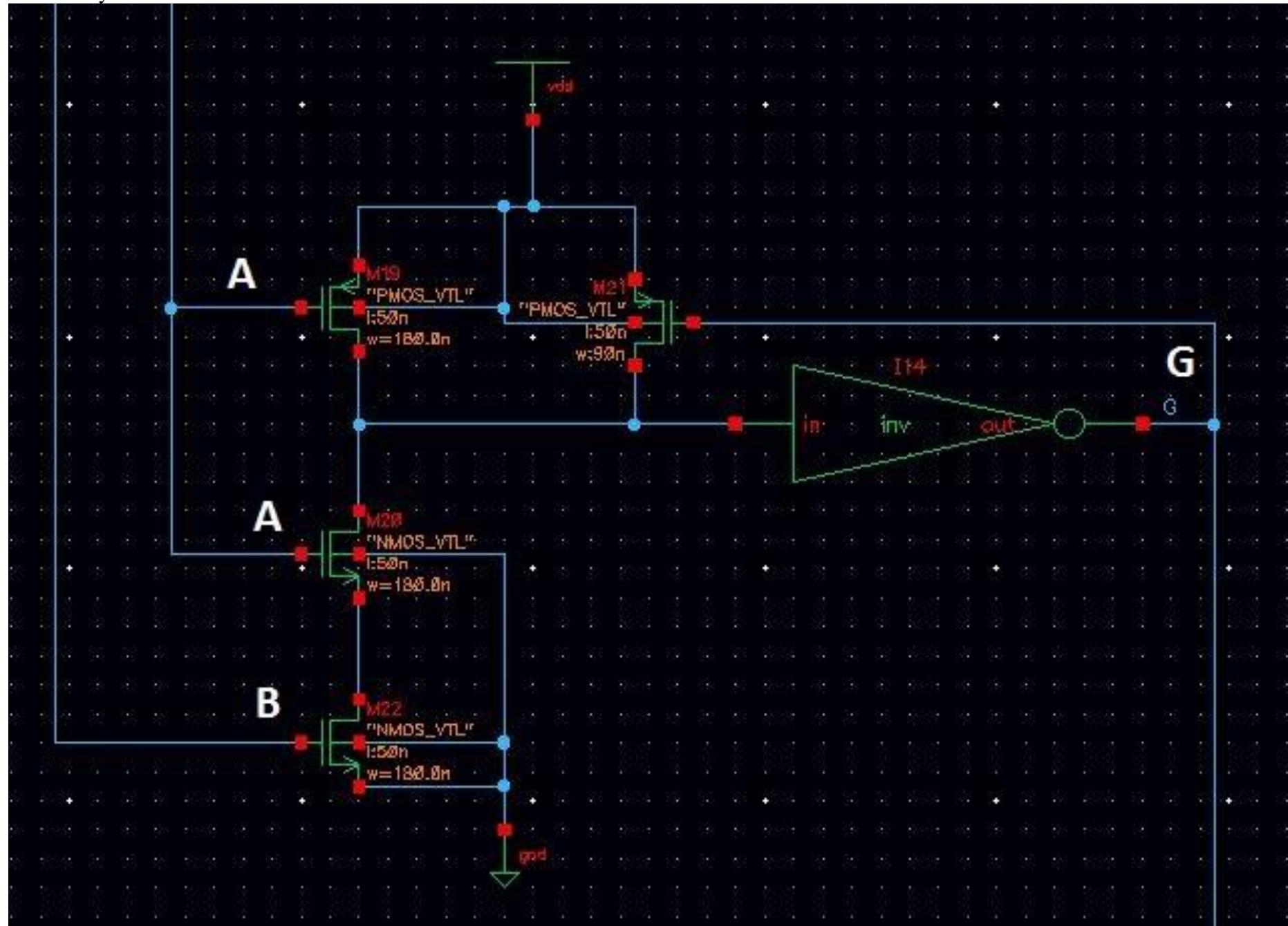
P and !P Circuitry



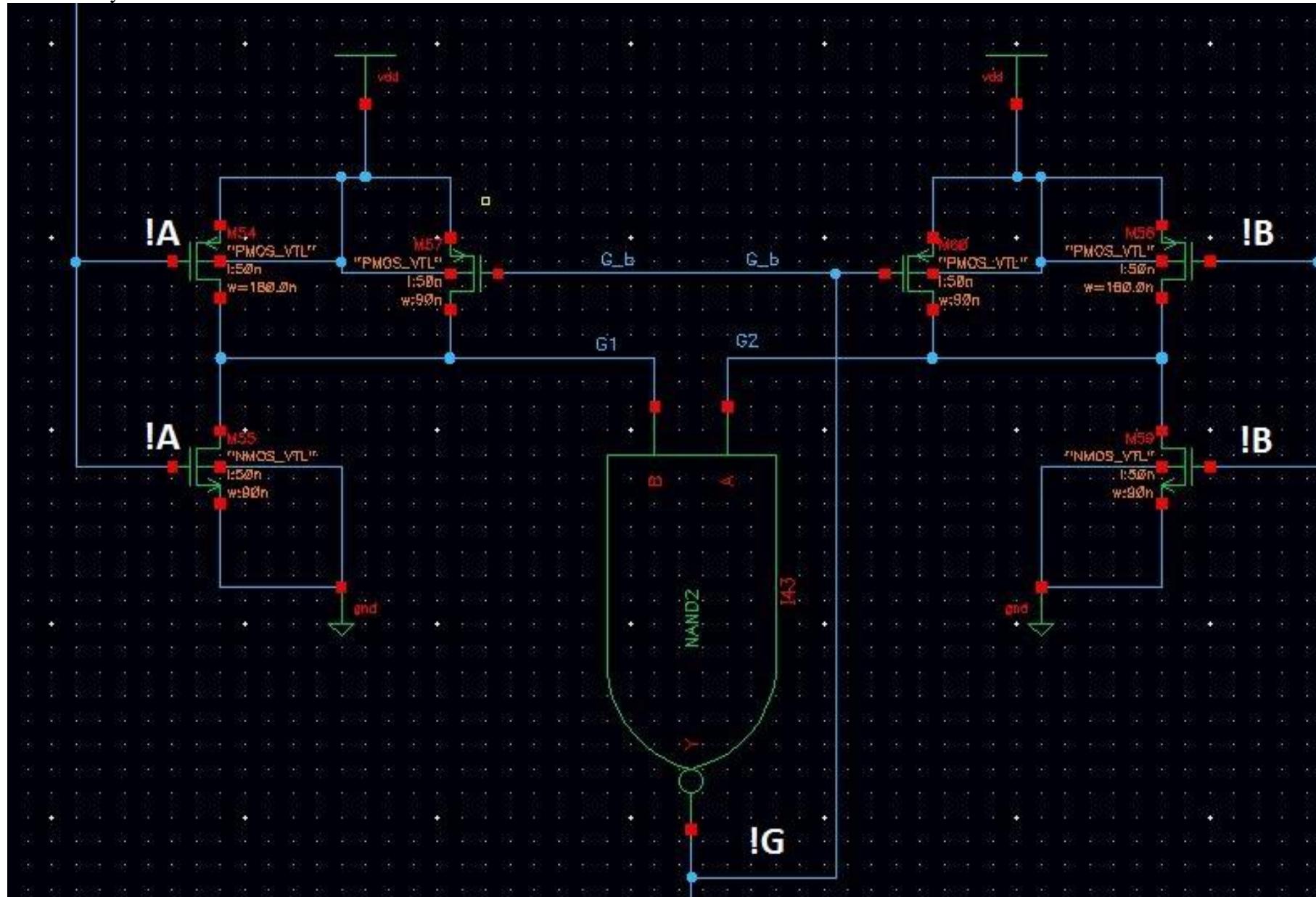
Sum Circuitry



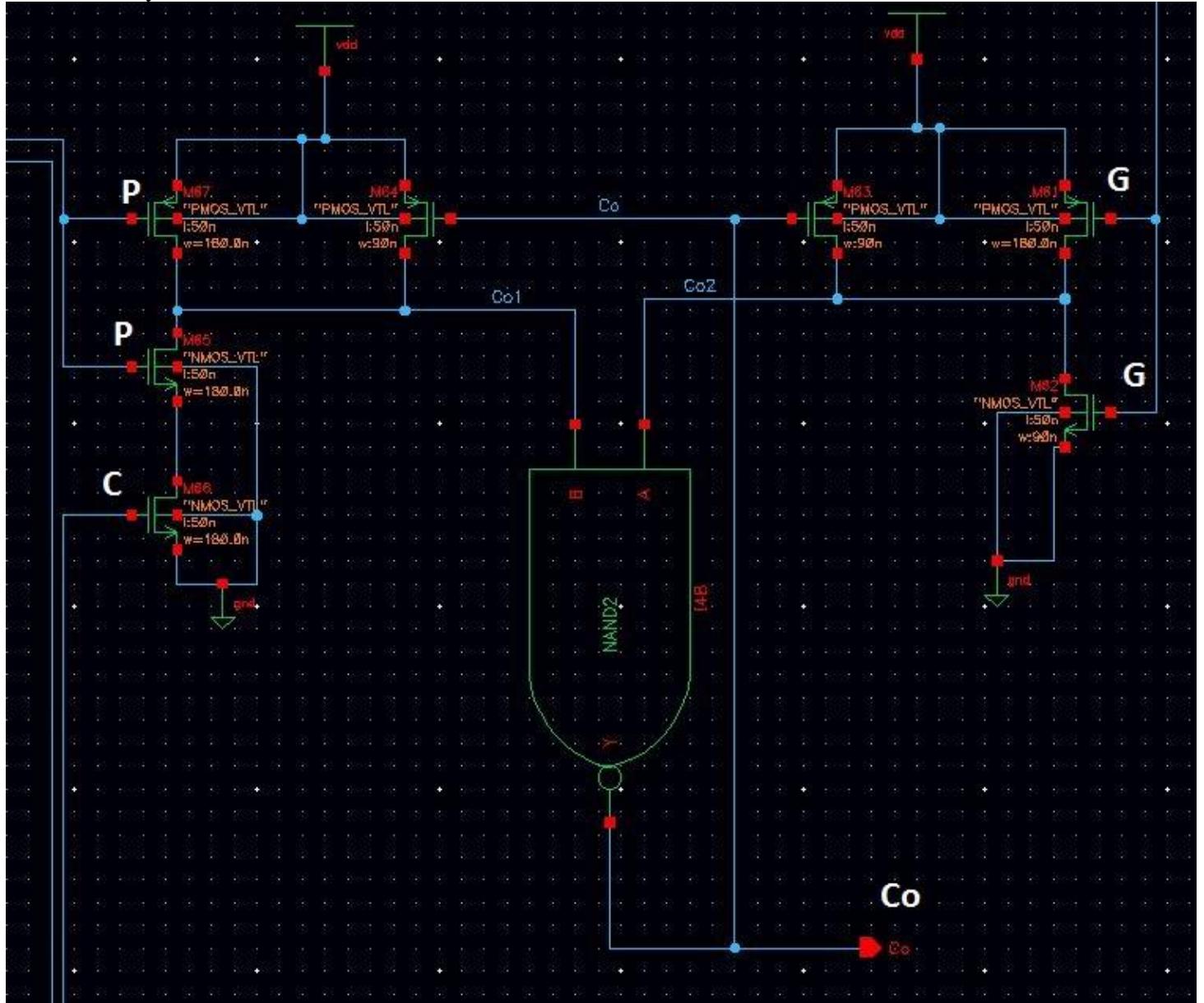
G Circuitry



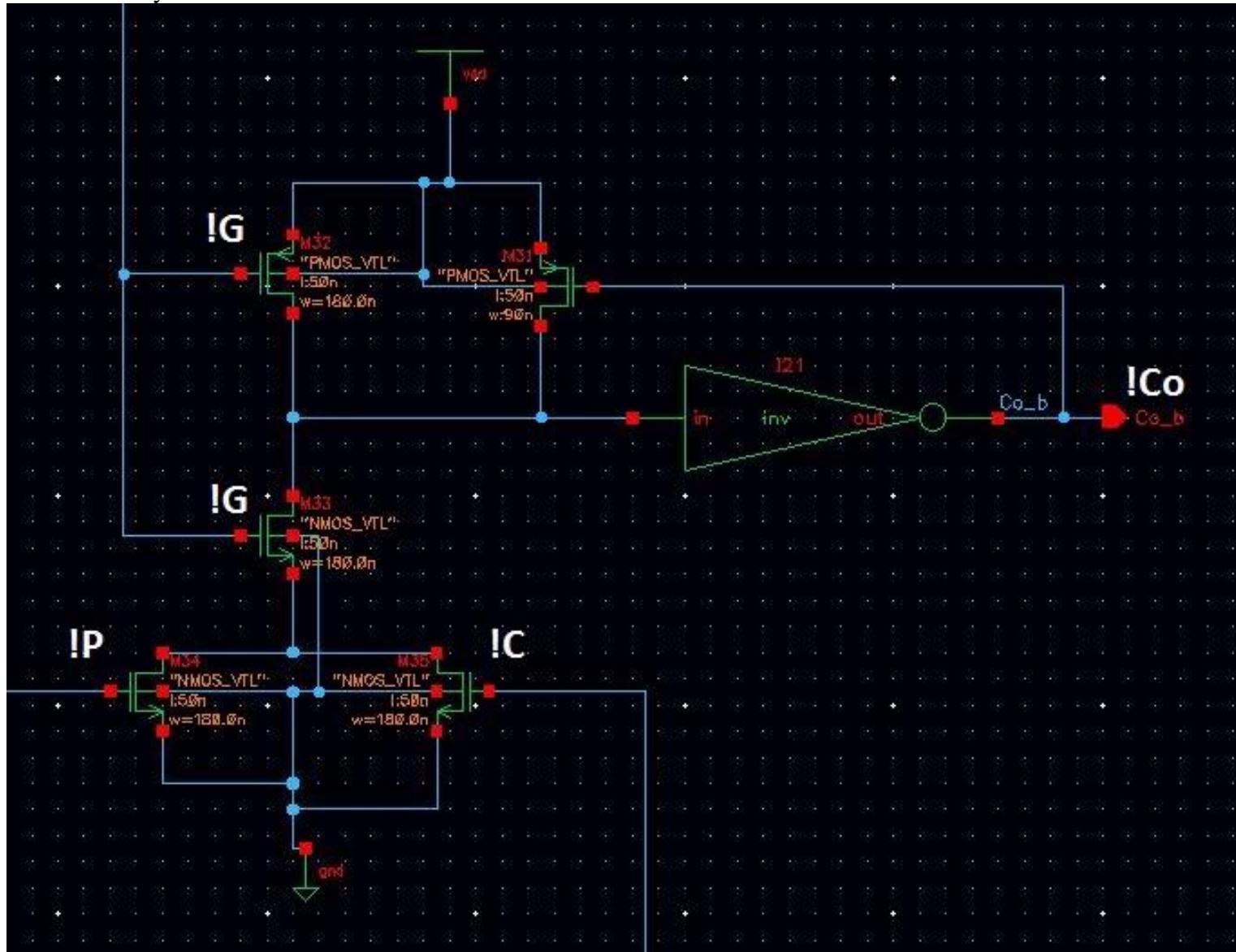
!G Circuitry



Cout Circuitry

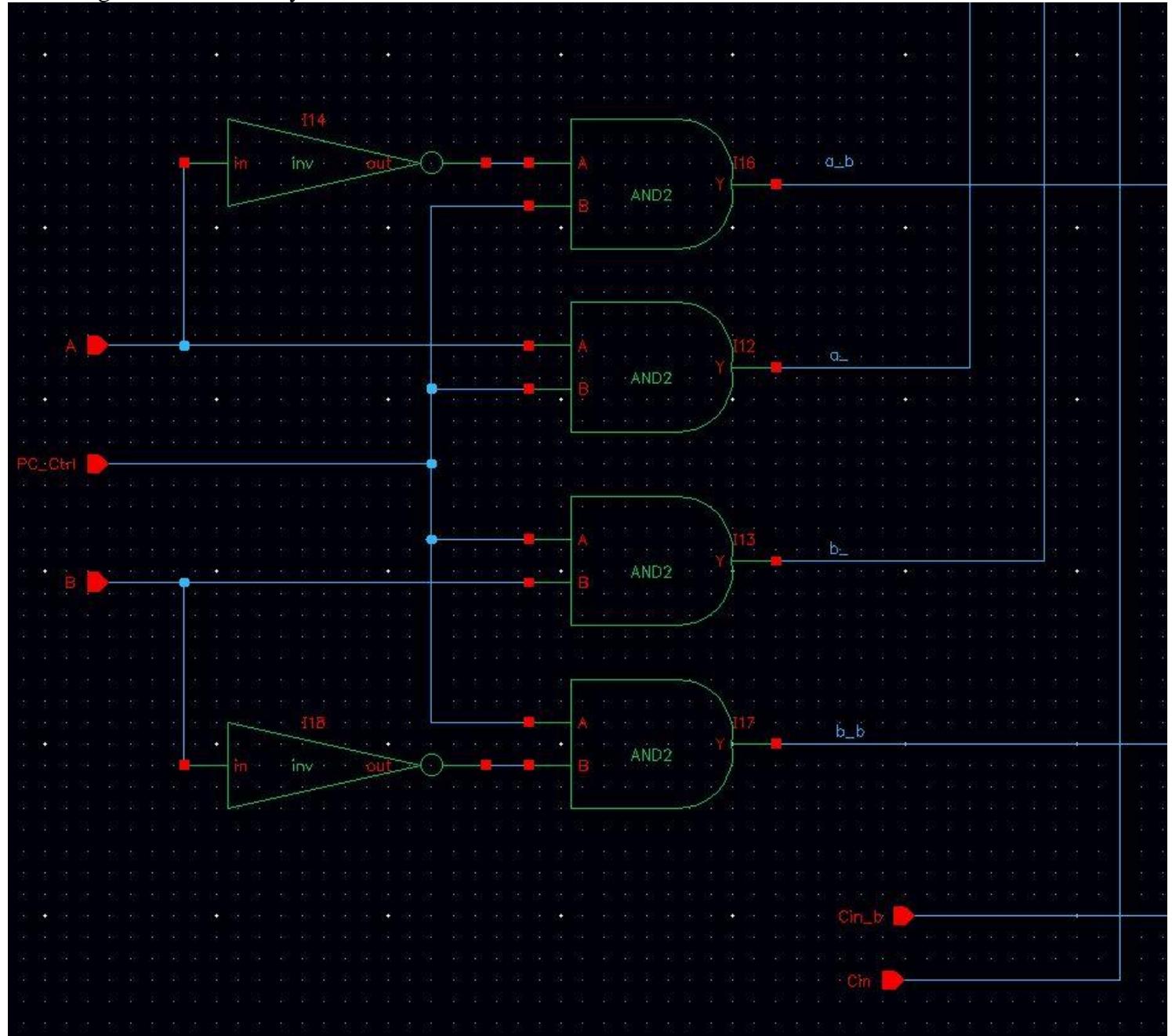


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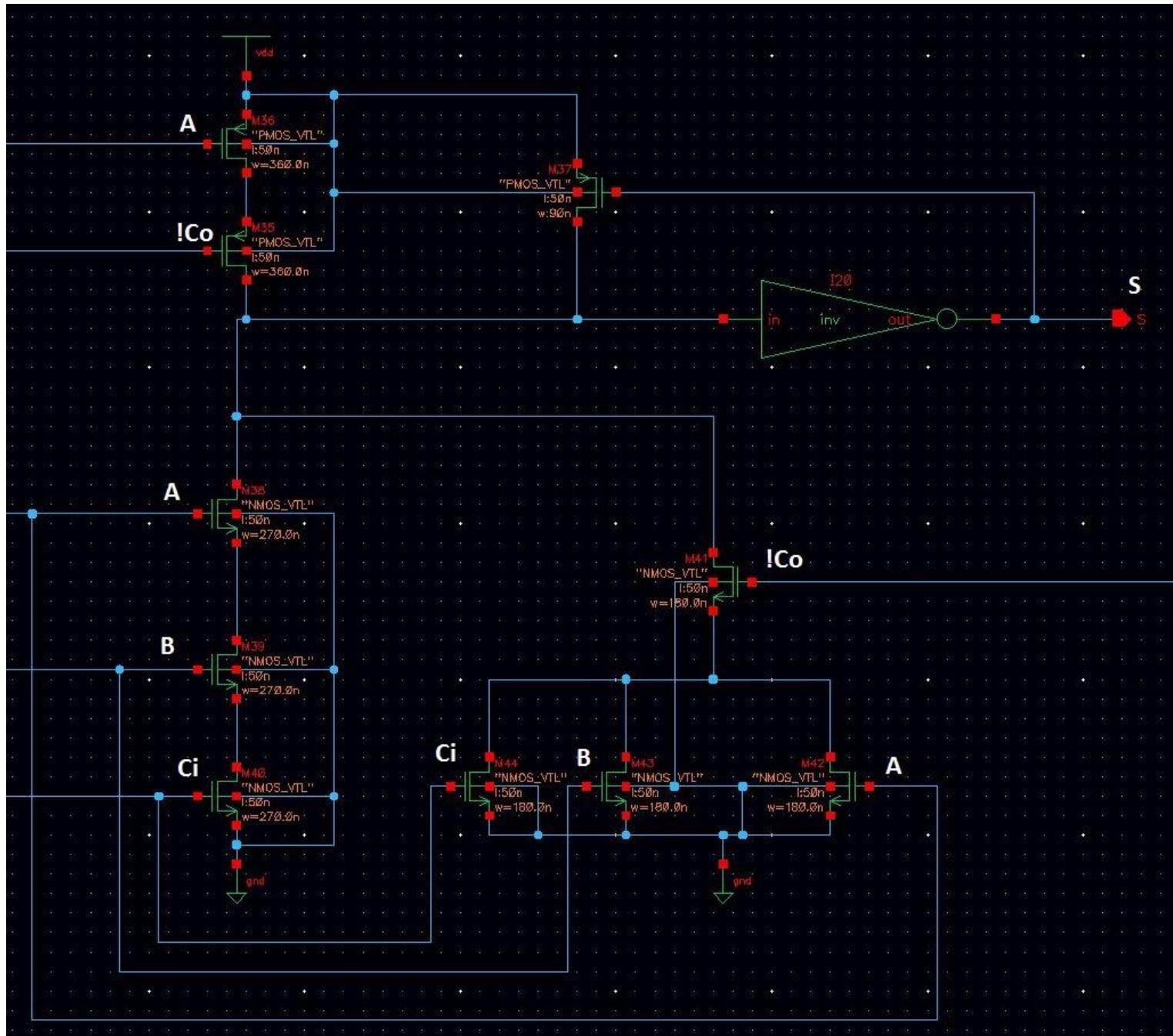


Bonus: D3L

Pre-Charge Control Circuitry

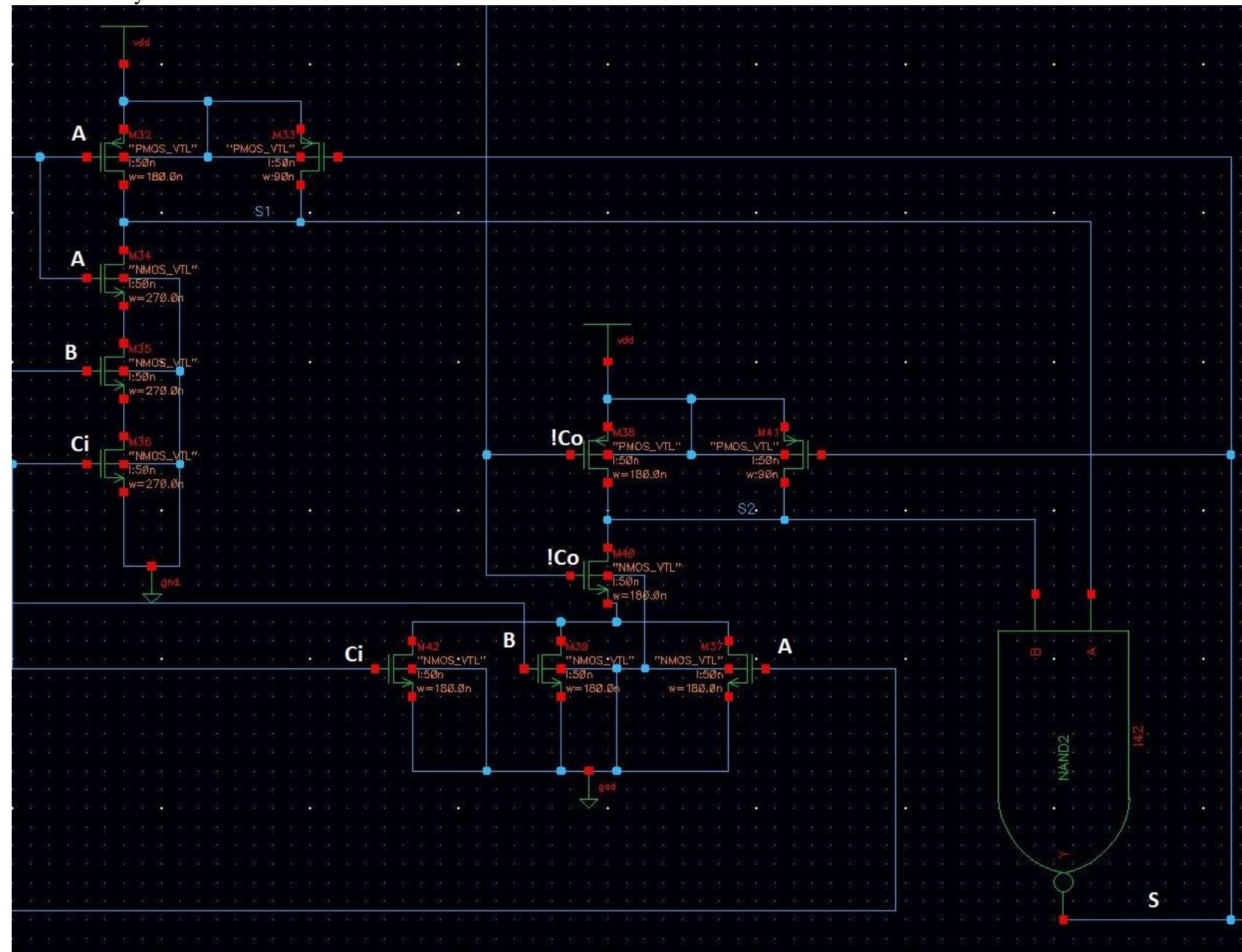


Sum Circuitry



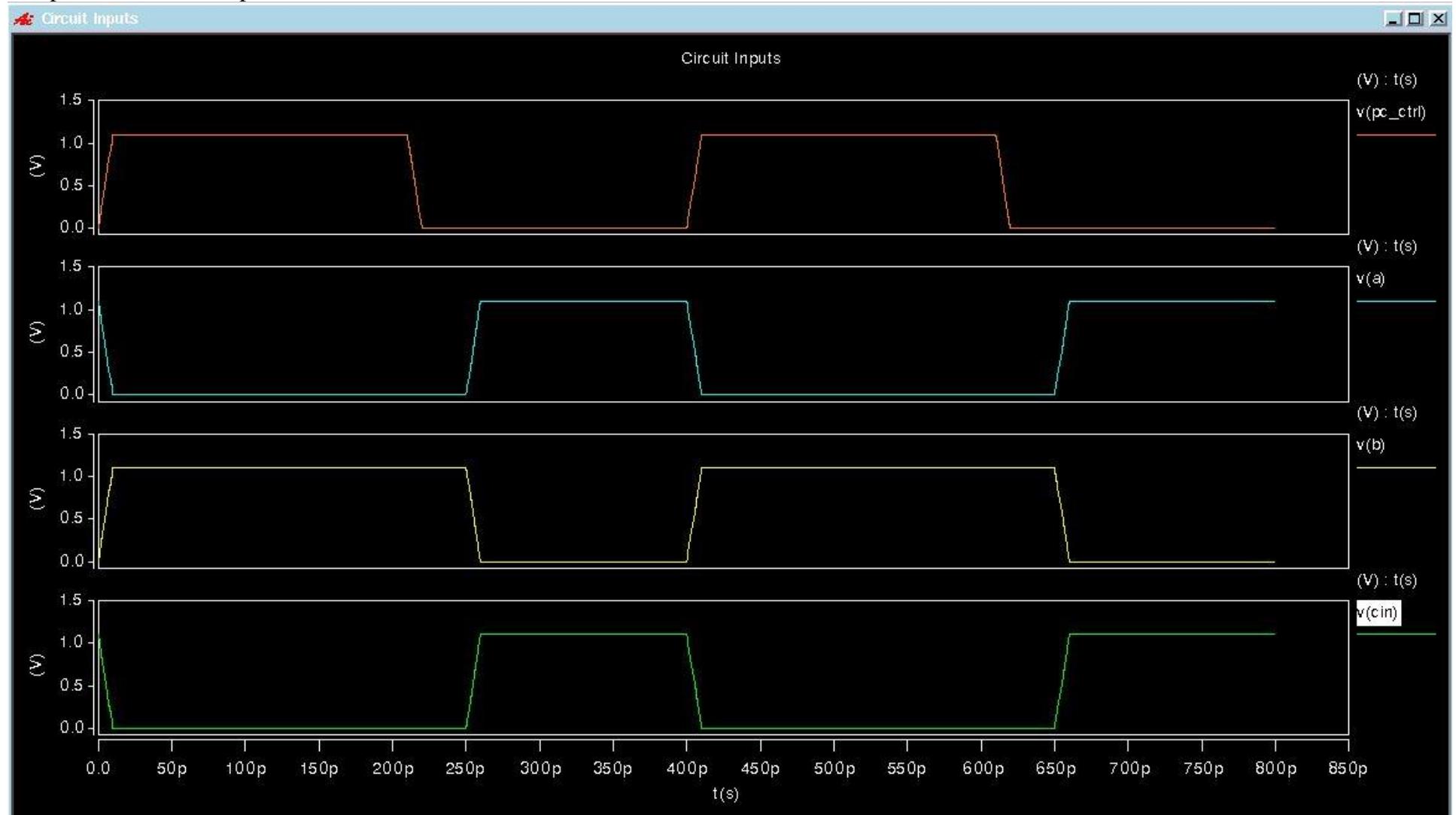
Bonus: SPD3L

Sum Circuitry

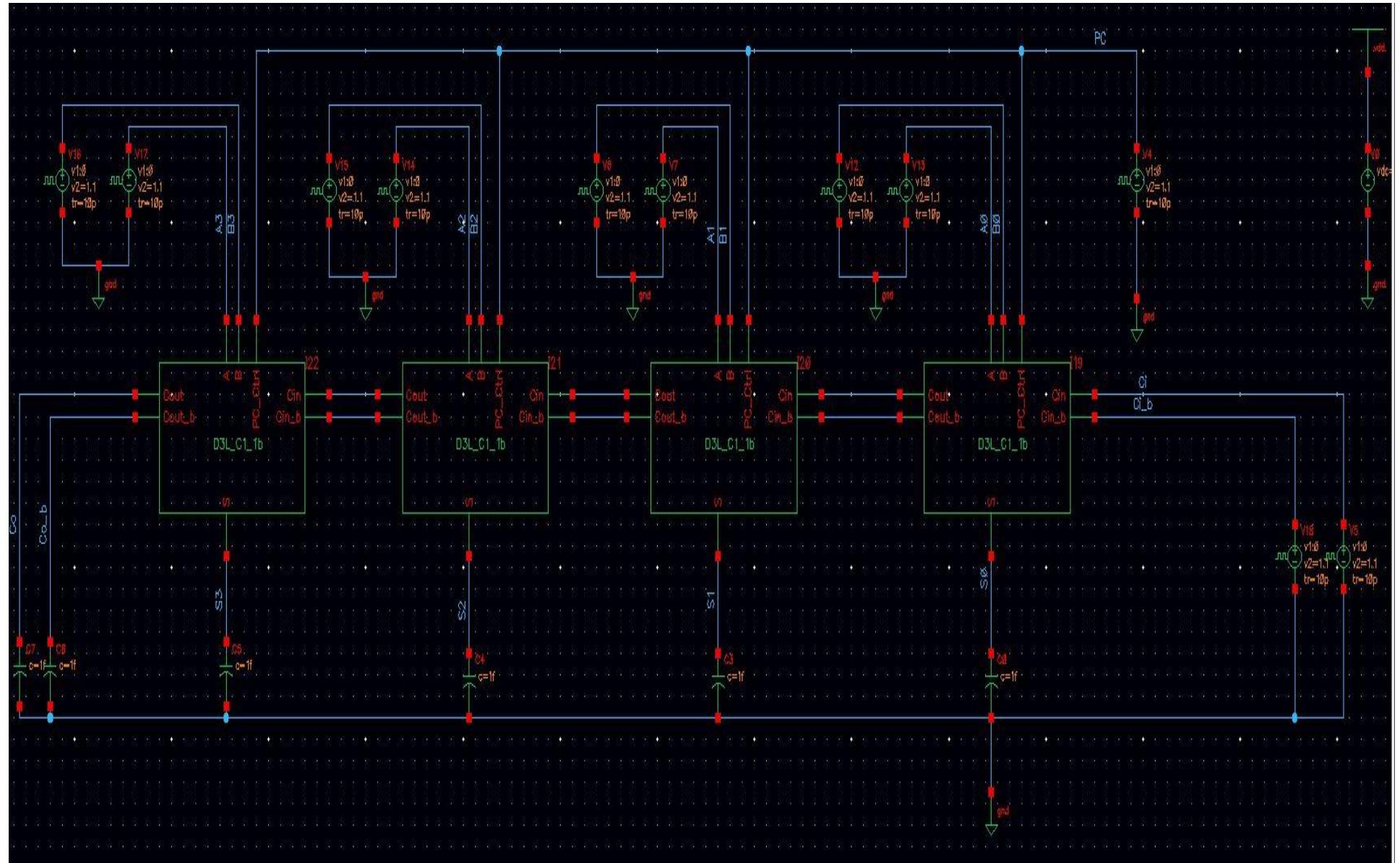


Appendix 2: Logic Verification

Sample of the Circuit Input Waveforms

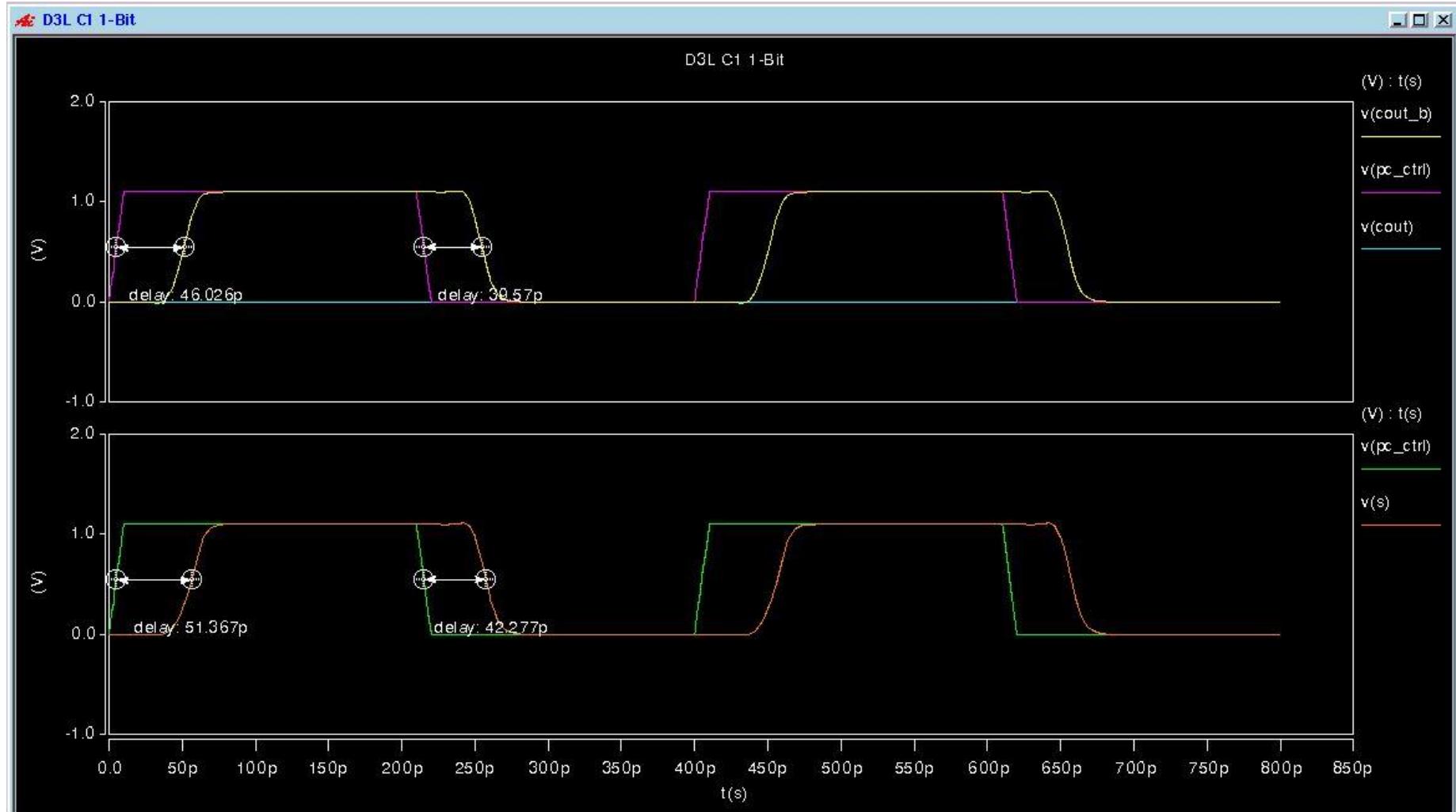


4-bit Logic Verification

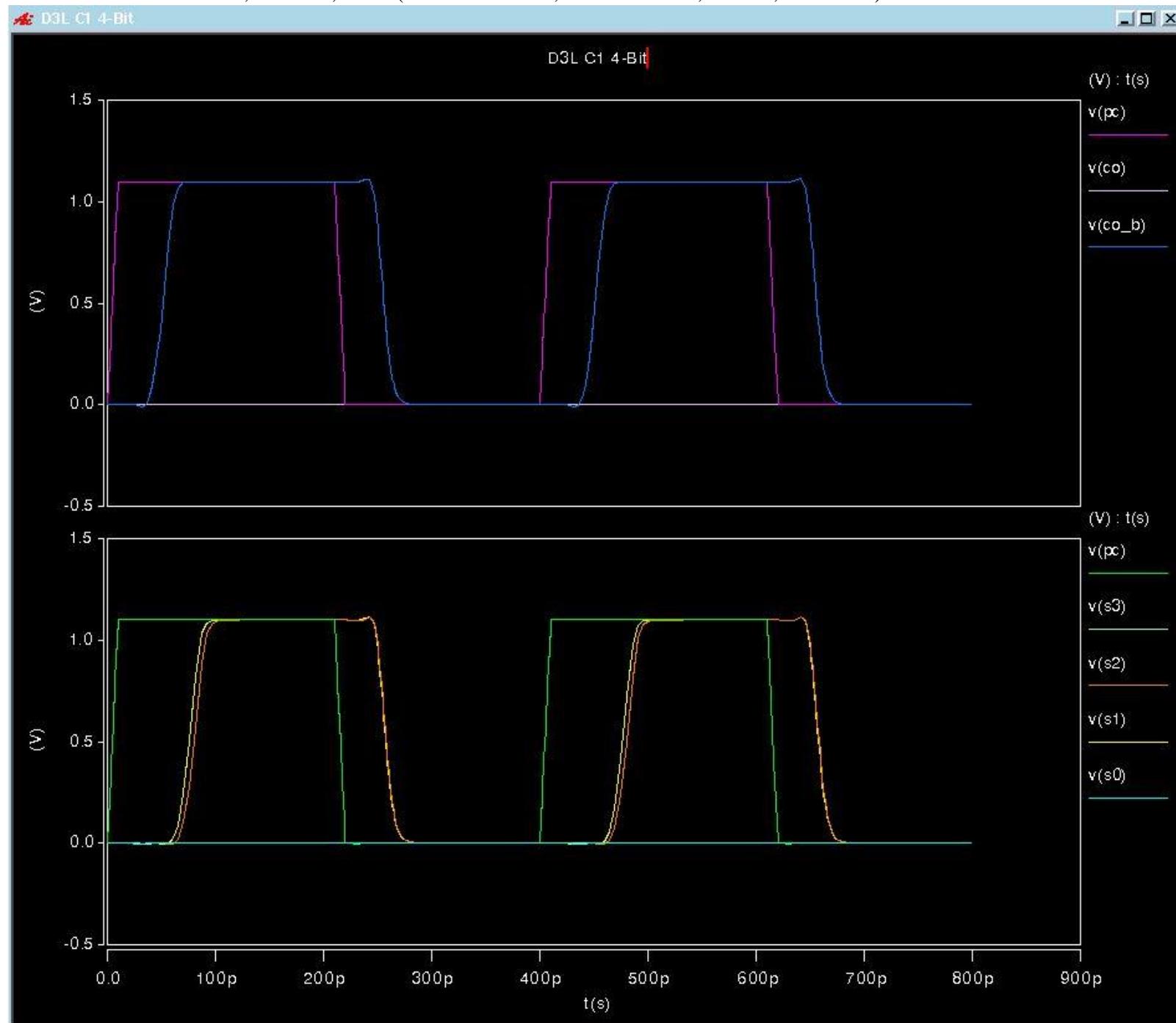


Circuit 1: D3L

1-Bit Full-Adder A= 0, B= 1, C = 0 (S = 1.1, Cout = 0, !Cout = 1.1)

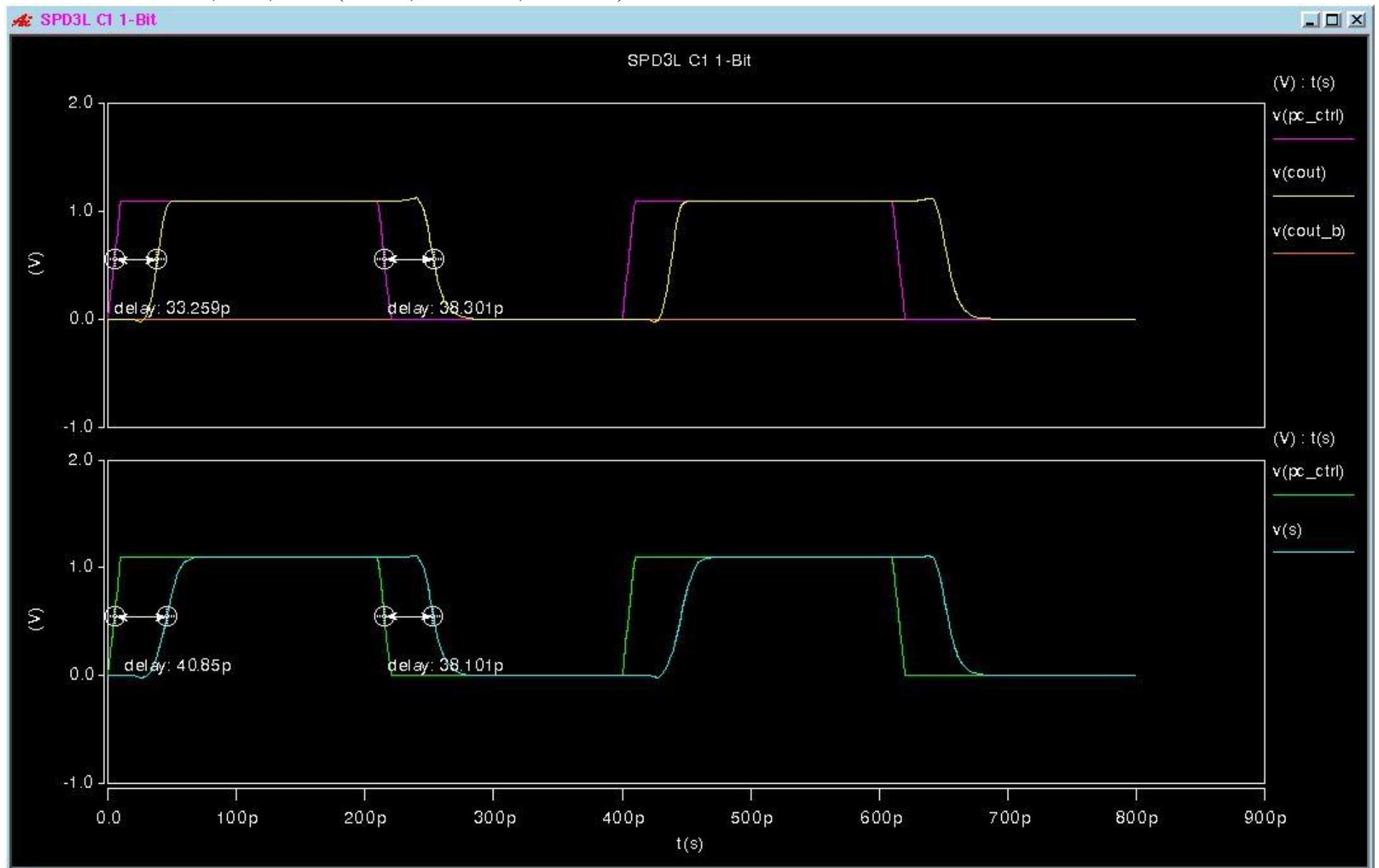


4-Bit Full-Adder A=0001, B=0101, C=0 (S1 and S2 = 1.1, S3 and S0 = 0, Co = 0, !Co = 1.1)

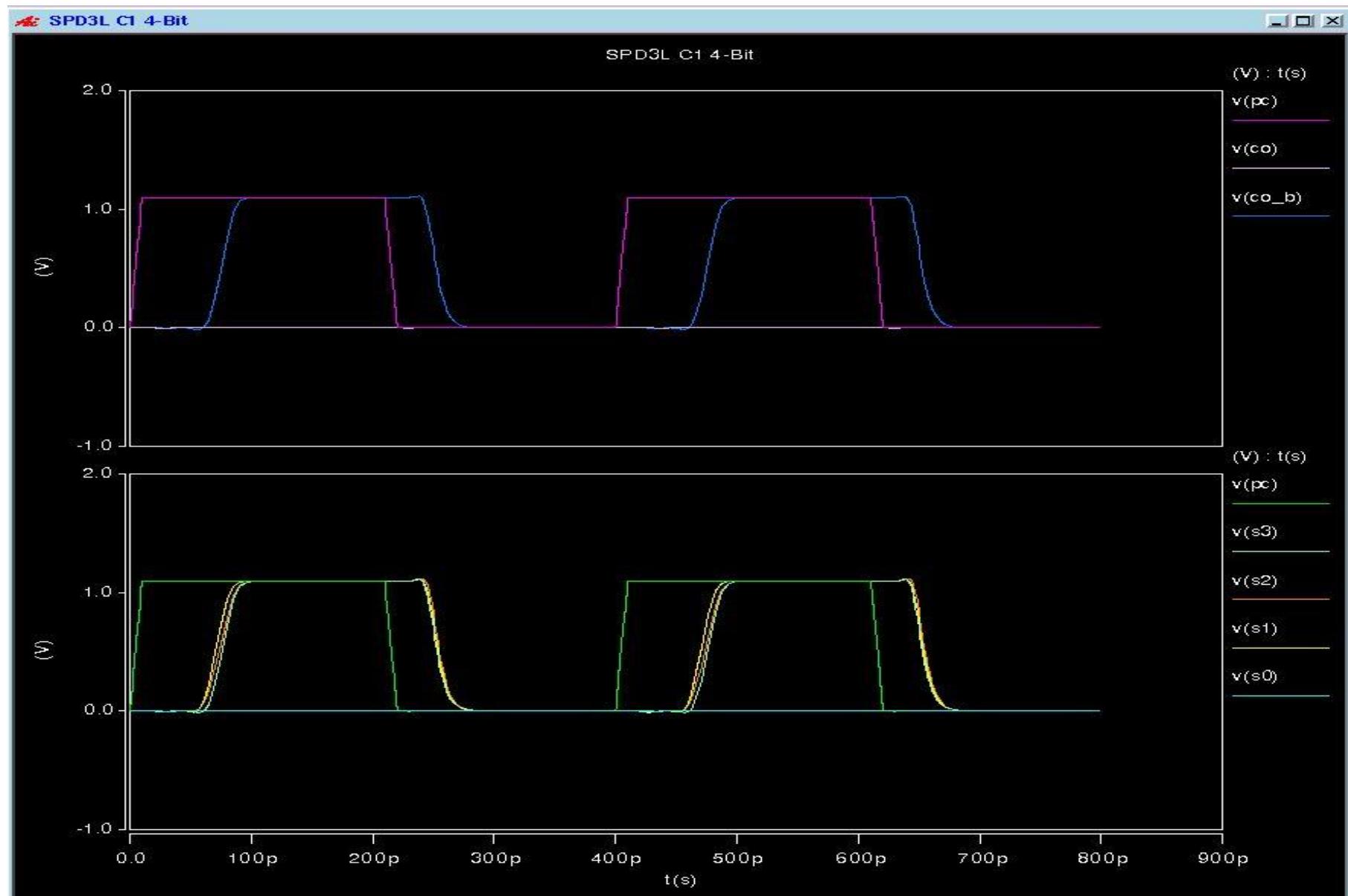


Circuit 1: SPD3L

1-Bit Full-Adder A= 1, B= 1, C = 1 (S = 1.1, Cout = 1.1, !Cout = 0)

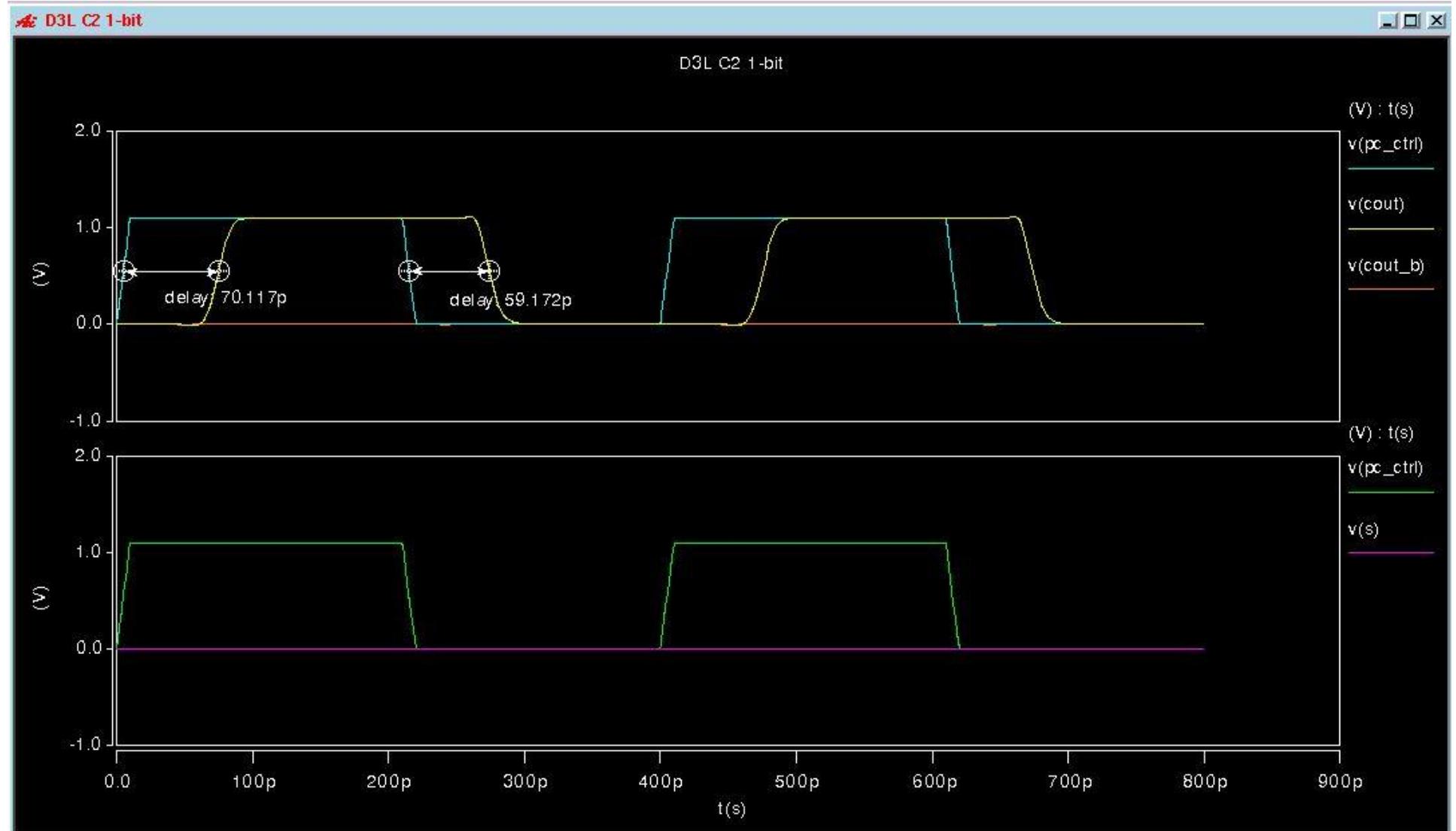


4-Bit Full-Adder A=1010, B=0011, C=1 (S1 and S2 and S3 = 1.1, S0 = 0, Co = 0, !Co = 1.1)

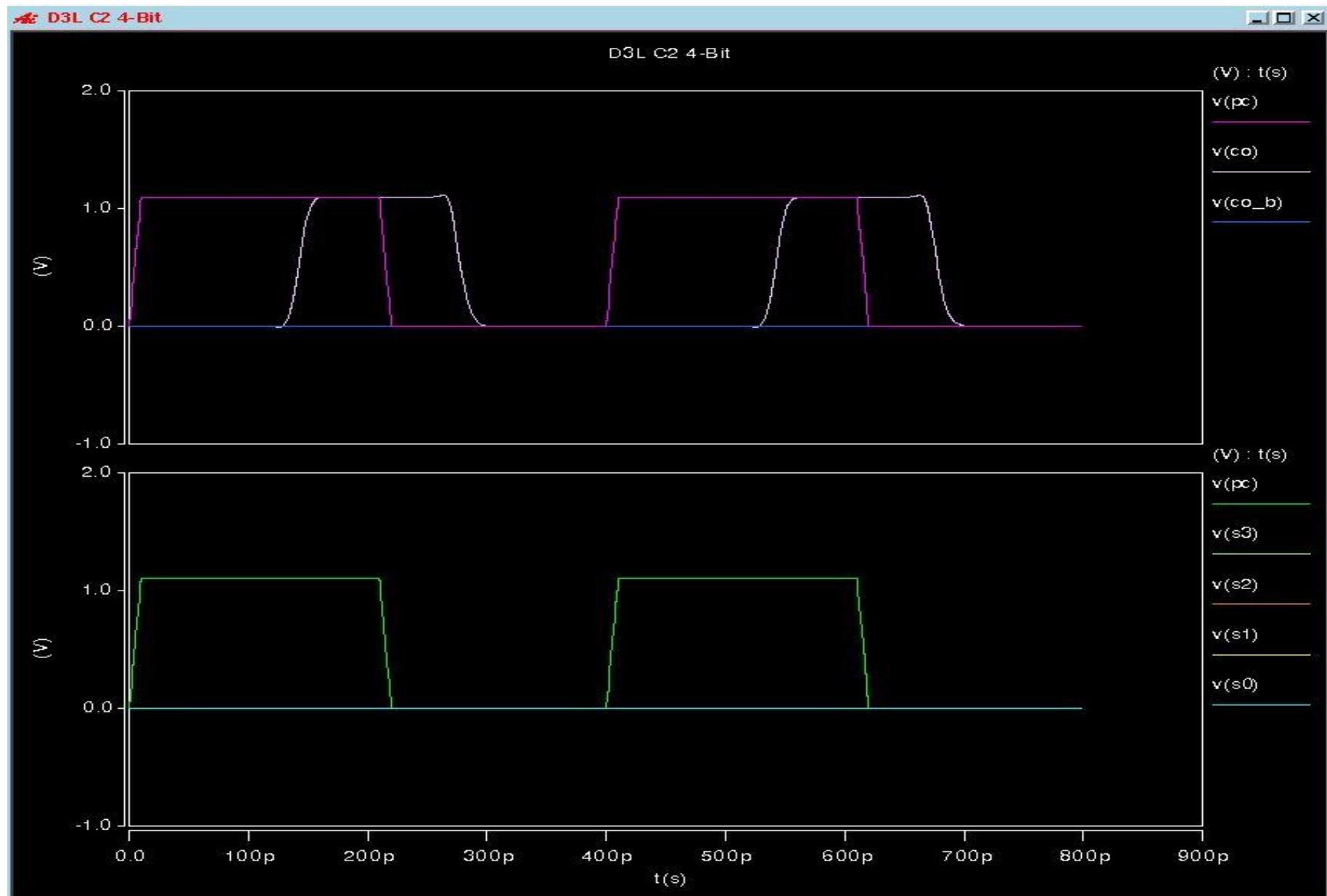


Circuit 2: D3L

1-Bit Full-Adder A= 1, B= 0, C = 1 (S = 0, Cout = 1.1, !Cout = 0)

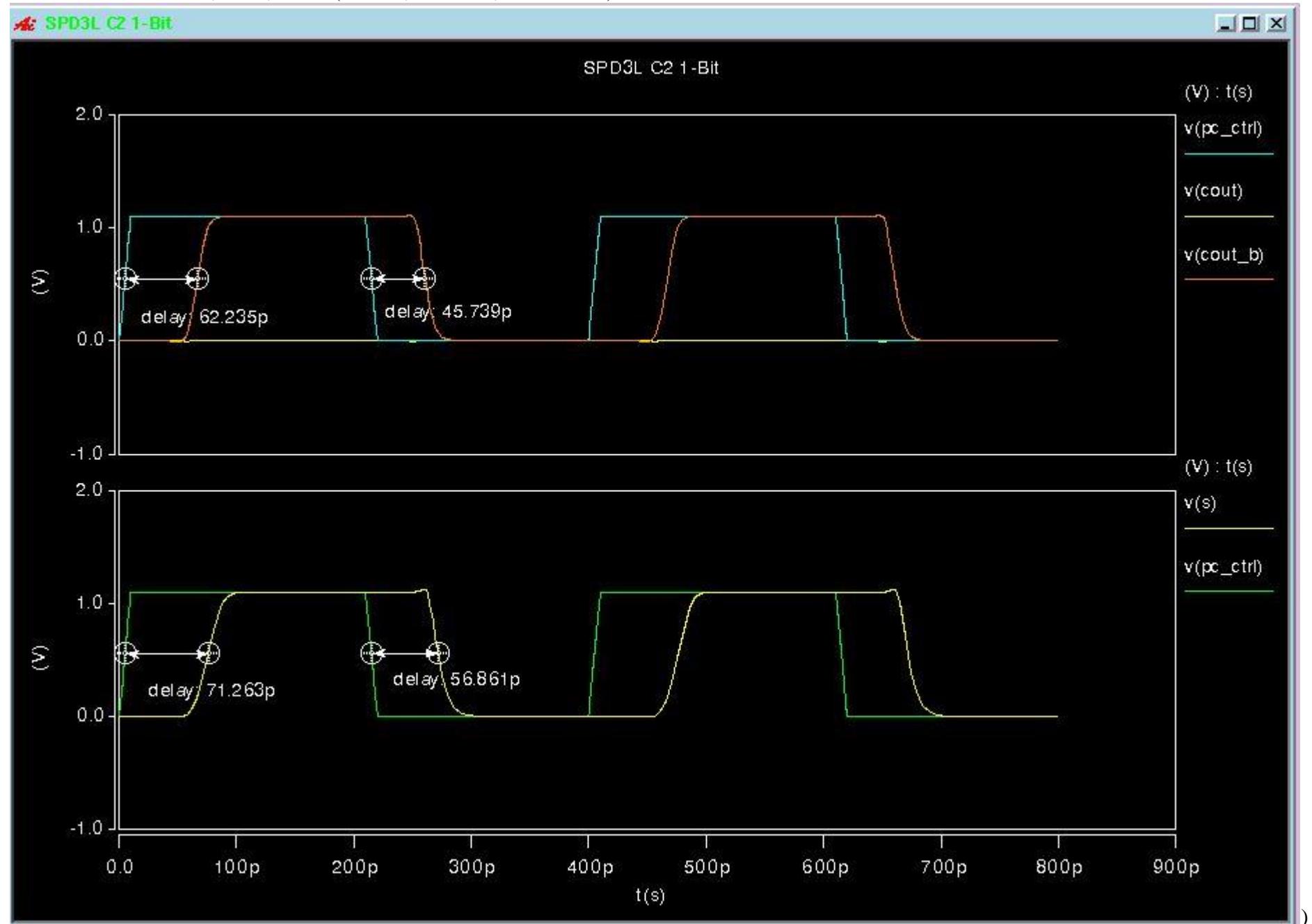


4-Bit Full-Adder A=0000, B=1111, C=1 (S0 and S1 and S2 and S3 = 0, Co = 1.1, !Co = 0)

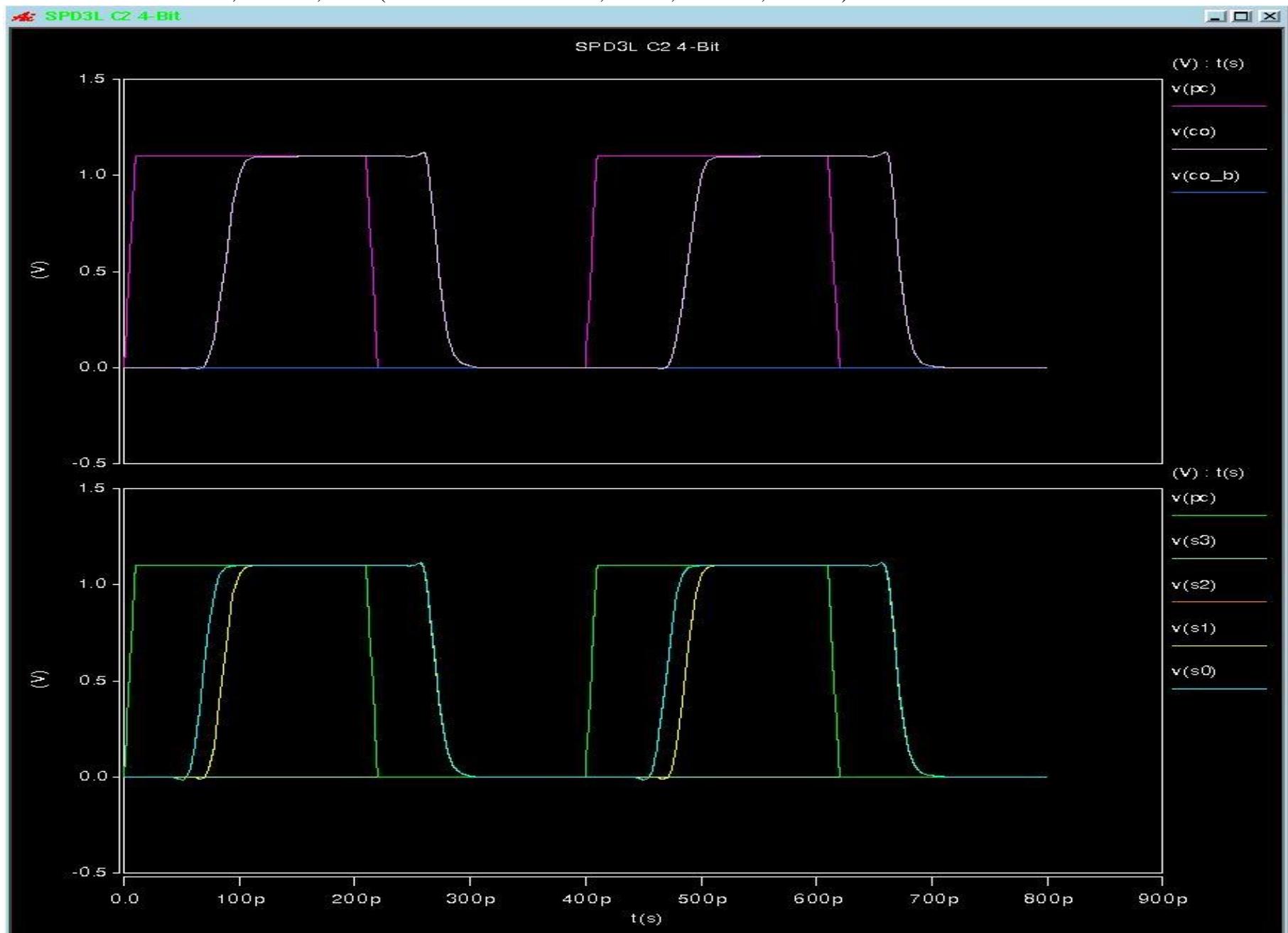


Circuit 2: SPD3L

1-Bit Full-Adder A= 1, B= 0, C = 0 (S = 1.1, Cout = 0, !Cout = 1.1)

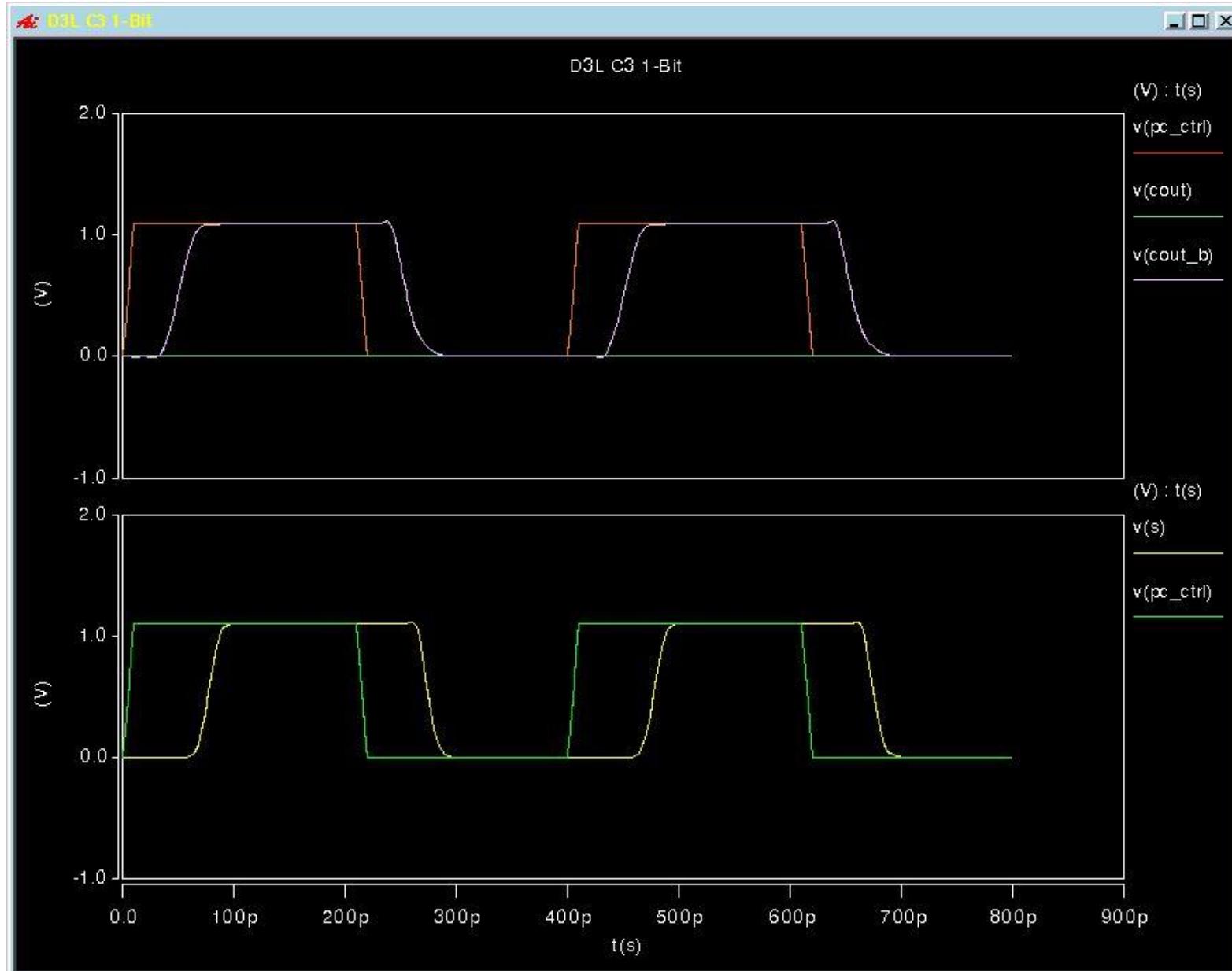


4-Bit Full-Adder A=0111, B=1111, C=1 (S0 and S1 and S2 = 1.1, S3 = 0, Co = 1.1, !Co = 0)

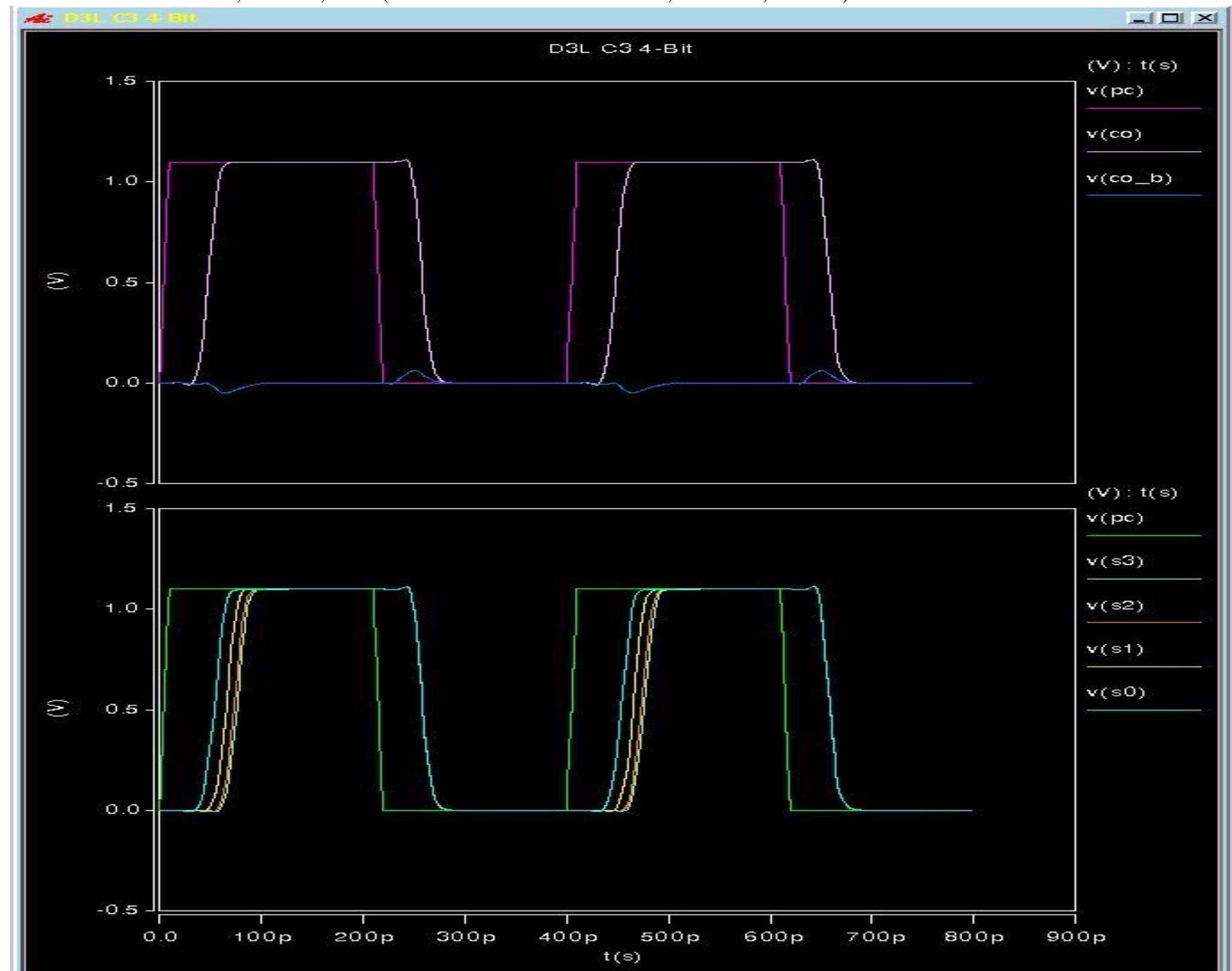


Bonus: D3L

1-Bit Full-Adder A= 0, B= 0, C = 1 (S = 1.1, Cout = 0, !Cout = 1.1)

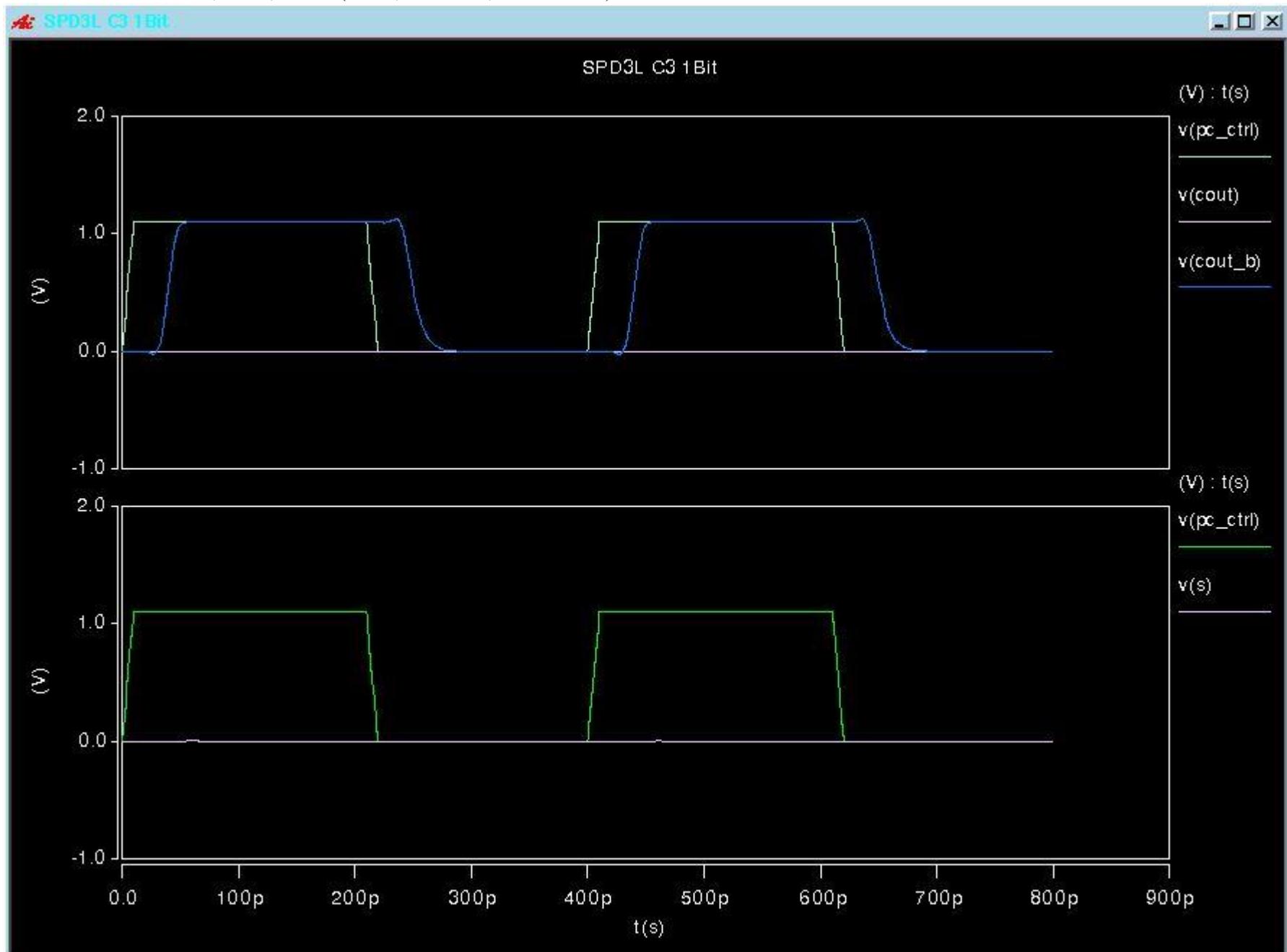


4-Bit Full-Adder A=1111, B=1111, C=1 (S1 and S2 and S3 and S4 = 1.1, Co = 1.1, !Co = 0)

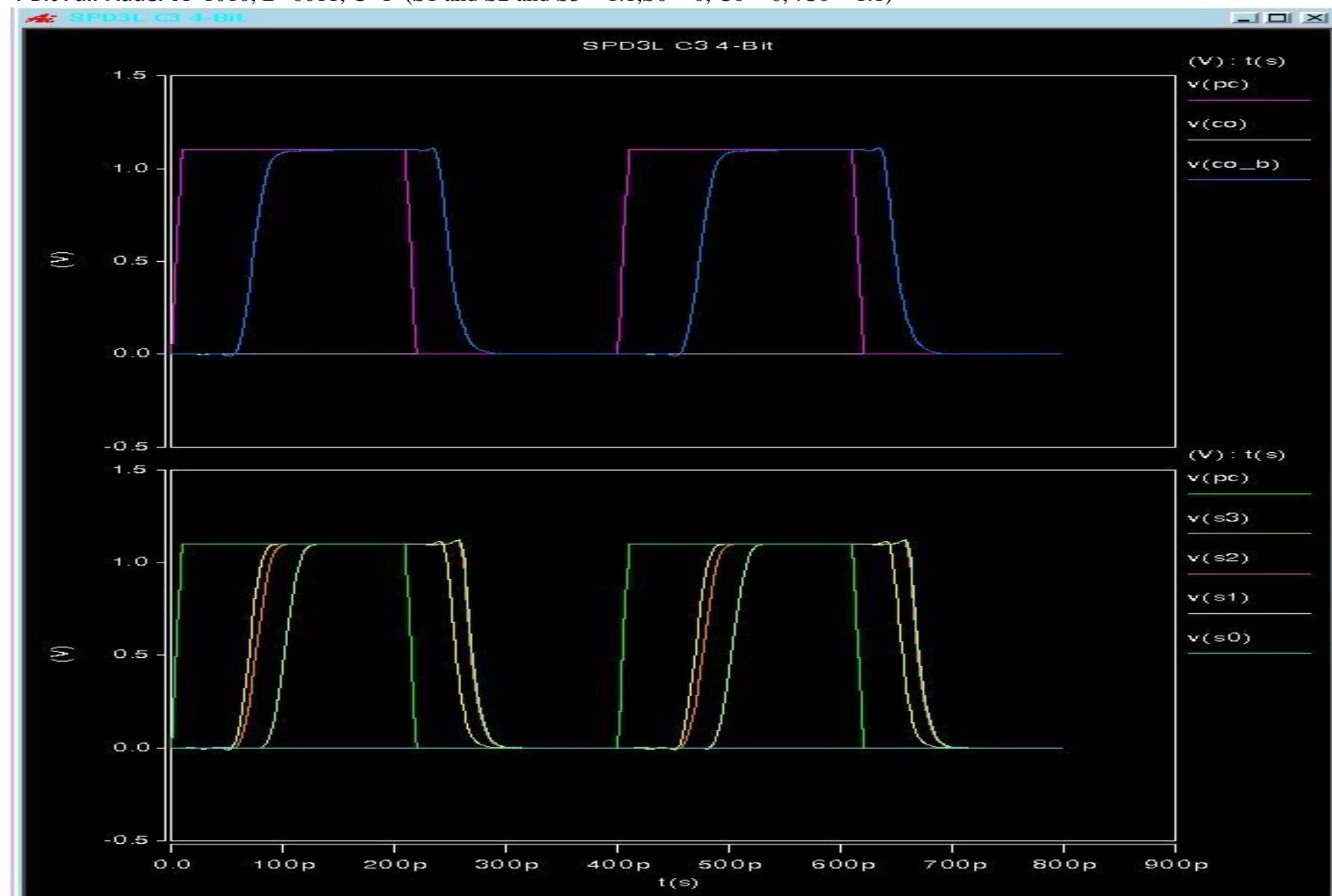


Bonus: SPD3L

1-Bit Full-Adder A= 0, B= 0, C = 0 (S = 0, Cout = 0, !Cout = 1.1)



4-Bit Full-Adder A=1010, B=0011, C=1 (S1 and S2 and S3 = 1.1, S0 = 0, Co = 0, !Co = 1.1)



Appendix 3: HSPICE Netlist Files

Circuit 1: D3L

1-Bit Circuit

```
** Generated for: hspiceD
** Generated on: Apr 21 21:45:10 2013
** Design library name: my
** Design cell name: D3L_C1_1b_test
** Design view name: schematic
.GLOBAL vdd!

.TRAN 1e-12 800e-12 START=0.0 SWEEP DATA=D
.DATA D
+A1 !A1 B1 !B1 C1 !C1 ** A B C
+0 1.1 0 1.1 0 1.1 ** 0 0 0
+0 1.1 0 1.1 1.1 0 ** 0 0 1
+0 1.1 1.1 0 0 1.1 ** 0 1 0
+0 1.1 1.1 0 1.1 0 ** 0 1 1
+1.1 0 0 1.1 0 1.1 ** 1 0 0
+1.1 0 0 1.1 1.1 0 ** 1 0 1
+1.1 0 1.1 0 0 1.1 ** 1 1 0
+1.1 0 1.1 0 1.1 0 ** 1 1 1
.ENDDATA

.OP

.TEMP 25.0
.OPTION
+ ARTIST=2
+ INGOLD=2
+ PARHIER=LOCAL
+ PSF=2
+ POST
.INCLUDE "/apps/FreePDK45/ncsu_basekit/models/hspice/hspice_nom.include"

**.PRINT TRAN POWER
**.MEASURE TRAN avgpwr AVG POWER FROM 0 TO 800e-12
**.MEASURE TRAN maxpwr MAX POWER FROM 0 TO 800e-12
**.MEASURE TRAN avg_vdd AVG P(v0) FROM 0 TO 800e-12

** Library name: my
** Cell name: inv
** View name: schematic
.subckt inv in out
m0 out in vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m1 out in 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
.ends inv
** End of subcircuit definition.
```

```

** Library name: my
** Cell name: NAND2
** View name: schematic
.subckt NAND2 a b y
m0 y a vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m1 y b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m3 net11 b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m2 y a net11 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
.ends NAND2
** End of subcircuit definition.

** Library name: my
** Cell name: AND2
** View name: schematic
.subckt AND2 a b y
xi0 a b net7 NAND2
xi1 net7 y inv
.ends AND2
** End of subcircuit definition.

** Library name: my
** Cell name: D3L_C1_1b
** View name: schematic
.subckt D3L_C1_1b a b cin cin_b cout cout_b pc_ctrl s
m34 net062 cin_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m33 net044 b_b net062 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m32 net012 cin_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m31 net012 b_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m30 net044 a_b net012 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m26 net064 cin 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m25 net045 b_ net064 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m24 net016 cin 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m23 net016 b_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m22 net045 a_ net016 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m14 net40 cin_b 0 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m8 net41 cin 0 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15 PD=480e-
9 PS=480e-9 M=1
m13 net30 b_ net40 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m6 net30 b_b net41 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1

```

```

m15 net12 b_ net34 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m4 net38 cin_b 0 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m16 net34 cin 0 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m2 net12 b_b net38 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m17 net31 a_b net30 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m0 net31 a_ net12 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m29 net063 b_b vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m28 net044 a_b net063 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m27 net044 cout_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m21 net065 b_ vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m20 net045 a_ net065 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m19 net045 cout vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m18 net31 s vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m11 net31 a_ net39 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m10 net39 a_b vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
xi14 a net067 inv
xi9 net044 cout_b inv
xi6 net045 cout inv
xi15 b net068 inv
xi2 net31 s inv
xi17 pc_ctrl net068 b_b AND2
xi13 pc_ctrl b_b_ AND2
xi12 a pc_ctrl a_ AND2
xi16 net067 pc_ctrl a_b AND2
.ends D3L_C1_1b
** End of subcircuit definition.

** Library name: my
** Cell name: D3L_C1_1b_test
** View name: schematic
xi8 a b cin cin_b cout cout_b pc_ctrl s D3L_C1_1b
v0 vdd! 0 DC=1.1

v1 pc_ctrl 0 PULSE 0 1.1 0 10e-12 10e-12 200e-12 400e-12

v4 a 0 PULSE !A1 A1 0 10e-12 10e-12 240e-12 400e-12
v2 b 0 PULSE !B1 B1 0 10e-12 10e-12 240e-12 400e-12
v5 cin 0 PULSE !C1 C1 0 10e-12 10e-12 240e-12 400e-12

**Used for NanoSim Calculations
***v4 a 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v2 b 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

```

```

**v5 cin 0 PULSE 0    1.1 0 10e-12 10e-12 240e-12 400e-12

c2 cout 0 1e-15
c1 cout_b 0 1e-15
c0 s 0 1e-15
xi9 cin cin_b inv
.END

```

4-Bit Circuit

```

** Generated for: hspiceD
** Generated on: Apr 26 09:42:59 2013
** Design library name: my
** Design cell name: D3L_C1_4b_test
** Design view name: schematic
.GLOBAL vdd!

.TRAN 1e-12 800e-12 START=0.0 SWEEP DATA=D
.DATA D
+A3_ A2_ A1_ A0_ B3_ B2_ B1_ B0_ Ci_ !A3_ !A2_ !A1_ !A0_ !B3_ !B2_ !B1_ !B0_
!Ci_
+0 0 0 1.1 0 1.1 0 1.1 0 1.1 1.1 1.1 0 1.1 0 1.1 0
1.1 ** 1 + 5 + 0
+1.1 0 1.1 0 0 0 1.1 1.1 1.1 0 1.1 0 1.1 1.1 1.1 0 0
0 ** 10 + 3 + 1
+0 0 0 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 0 0 0 0
0 ** 0 + 15 + 1
+1.1 1.1 1.1 1.1 0 1.1 1.1 1.1 1.1 0 0 0 0 1.1 0 0 0
0 ** 7 + 15 + 1
+1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 0 0 0 0 0 0 0
0 ** 15 + 15 + 1
.ENDDATA

**.PRINT TRAN POWER
**.MEASURE TRAN avgpwr AVG POWER FROM 0 TO 800e-12
**.MEASURE TRAN maxpwr MAX POWER FROM 0 TO 800e-12
**.MEASURE TRAN avg_vdd AVG P(v0) FROM 0 TO 800e-12

.OP

 TEMP 25.0
.OPTION
+ ARTIST=2
+ INGOLD=2
+ PARHIER=LOCAL
+ PSF=2
+ POST
.INCLUDE "/apps/FreePDK45/ncsu_basekit/models/hspice/hspice_nom.include"

** Library name: my
** Cell name: inv
** View name: schematic
.subckt inv in out
m0 out in vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1

```

```

m1 out in 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
.ends inv
** End of subcircuit definition.

** Library name: my
** Cell name: NAND2
** View name: schematic
.subckt NAND2 a b y
m0 y a vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m1 y b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m3 net11 b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m2 y a net11 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
.ends NAND2
** End of subcircuit definition.

** Library name: my
** Cell name: AND2
** View name: schematic
.subckt AND2 a b y
x10 a b net7 NAND2
x11 net7 y inv
.ends AND2
** End of subcircuit definition.

** Library name: my
** Cell name: D3L_C1_1b
** View name: schematic
.subckt D3L_C1_1b a b cin cin_b cout cout_b pc_ctrl s
m34 net062 cin_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m33 net044 b_b net062 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m32 net012 cin_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m31 net012 b_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m30 net044 a_b net012 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m26 net064 cin 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m25 net045 b_ net064 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m24 net016 cin 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m23 net016 b_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m22 net045 a_ net016 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m14 net40 cin_b 0 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m8 net41 cin 0 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15 PD=480e-
9 PS=480e-9 M=1

```

```

m13 net30 b_ net40 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m6 net30 b_b net41 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m15 net12 b_ net34 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m4 net38 cin_b 0 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m16 net34 cin 0 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m2 net12 b_b net38 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m17 net31 a_b net30 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m0 net31 a_ net12 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m29 net063 b_b vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m28 net044 a_b net063 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m27 net044 cout_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m21 net065 b_ vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m20 net045 a_ net065 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m19 net045 cout vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m18 net31 s vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m11 net31 a_ net39 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m10 net39 a_b vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
xi14 a net067 inv
xi19 net044 cout_b inv
xi16 net045 cout inv
xi15 b net068 inv
xi12 net31 s inv
xi17 pc_ctrl net068 b_b AND2
xi13 pc_ctrl b_b_ AND2
xi12 a pc_ctrl a_ AND2
xi16 net067 pc_ctrl a_b AND2
.ends D3L_C1_1b
** End of subcircuit definition.

** Library name: my
** Cell name: D3L_C1_4b_test
** View name: schematic
xi19 a0 b0 ci ci_b net20 net21 pc s0 D3L_C1_1b
xi21 a2 b2 net021 net022 net17 net16 pc s2 D3L_C1_1b
xi20 a1 b1 net20 net21 net021 net022 pc s1 D3L_C1_1b
xi22 a3 b3 net17 net16 co co_b pc s3 D3L_C1_1b
v0 vdd! 0 DC=1.1

v4 pc 0 PULSE 0 1.1 0 10e-12 10e-12 200e-12 400e-12

```

```

v17 a3 0 PULSE !A3_ A3_ 0 10e-12 10e-12 240e-12 400e-12
v14 a2 0 PULSE !A2_ A2_ 0 10e-12 10e-12 240e-12 400e-12
v7 a1 0 PULSE !A1_ A1_ 0 10e-12 10e-12 240e-12 400e-12
v13 a0 0 PULSE !A0_ A0_ 0 10e-12 10e-12 240e-12 400e-12

v16 b3 0 PULSE !B3_ B3_ 0 10e-12 10e-12 240e-12 400e-12
v15 b2 0 PULSE !B2_ B2_ 0 10e-12 10e-12 240e-12 400e-12
v6 b1 0 PULSE !B1_ B1_ 0 10e-12 10e-12 240e-12 400e-12
v12 b0 0 PULSE !B0_ B0_ 0 10e-12 10e-12 240e-12 400e-12

v5 ci 0 PULSE !Ci_ Ci_ 0 10e-12 10e-12 240e-12 400e-12
v18 ci_b 0 PULSE Ci_ !Ci_ 0 10e-12 10e-12 240e-12 400e-12

**Below Used for NanoSim Testing
*****
**Test1
***v17 a3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v14 a2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v7 a1 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v13 a0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

***v16 b3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v6 b1 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

***v5 ci 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v18 ci_b 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
*****
```

**Test2

```

***v17 a3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v14 a2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v7 a1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v13 a0 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12

***v16 b3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v15 b2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

***v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****
```

**Test3

```

***v17 a3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v14 a2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v7 a1 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v13 a0 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12

***v16 b3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

***v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
```

```

**v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****
**Test4
**v17 a3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v14 a2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v7 a1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v13 a0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v16 b3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****
```

```

**Test5
**v17 a3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v14 a2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v7 a1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v13 a0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v16 b3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****
```

```

c7 co 0 1e-15
c6 co_b 0 1e-15
c5 s3 0 1e-15
c4 s2 0 1e-15
c3 s1 0 1e-15
c0 s0 0 1e-15
.END
```

Circuit 1: SPD3L

1-Bit Circuit

```

** Generated for: hspiceD
** Generated on: Apr 24 09:07:33 2013
** Design library name: my
** Design cell name: SPD3L_C1_1b_test
** Design view name: schematic
.GLOBAL vdd!
```

```

.TRAN 1e-12 800e-12 START=0.0 SWEEP DATA=D
.DATA D
+A1 !A1 B1 !B1 C1 !C1
```

```

+0 1.1 0 1.1 0 1.1
+0 1.1 0 1.1 1.1 0
+0 1.1 1.1 0 0 1.1
+0 1.1 1.1 0 1.1 0
+1.1 0 0 1.1 0 1.1
+1.1 0 0 1.1 1.1 0
+1.1 0 1.1 0 0 1.1
+1.1 0 1.1 0 1.1 0
.ENDDATA

.OP

.TEMP 25.0
.OPTION
+ ARTIST=2
+ INGOLD=2
+ PARHIER=LOCAL
+ PSF=2
+ POST
.INCLUDE "/apps/FreePDK45/ncsu_basekit/models/hspice/hspice_nom.include"

**.PRINT TRAN POWER
**.MEASURE TRAN avgpwr AVG POWER FROM 0 TO 800e-12
**.MEASURE TRAN maxpwr MAX POWER FROM 0 TO 800e-12
**.MEASURE TRAN avg_vdd AVG P(v0) FROM 0 TO 800e-12

** Library name: my
** Cell name: inv
** View name: schematic
.subckt inv in out
m0 out in vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m1 out in 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
.ends inv
** End of subcircuit definition.

** Library name: my
** Cell name: NAND2
** View name: schematic
.subckt NAND2 a b y
m0 y a vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m1 y b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m3 net11 b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m2 y a net11 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
.ends NAND2
** End of subcircuit definition.

** Library name: my
** Cell name: AND2
** View name: schematic
.subckt AND2 a b y
xi0 a b net7 NAND2

```

```

x11 net7 y inv
.ends AND2
** End of subcircuit definition.

** Library name: my
** Cell name: SPD3L_C1_1b
** View name: schematic
.subckt SPD3L_C1_1b a b ci ci_b co co_b pc s
m1 s1 s vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m0 s1 a_ vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m6 s2 s vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m17 c4 b_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m14 c3 a_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m31 c2 co vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-
9 PS=300e-9 M=1
m16 c4 co_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m27 c1 co vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-
9 PS=300e-9 M=1
m30 c2 b_ vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m5 s2 a_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m25 c1 a_ vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m15 c3 co_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m8 net10 ci 0 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15 PD=480e-9
PS=480e-9 M=1
m7 net3 b_ net10 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m4 net11 ci_b 0 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m3 net3 b_b net11 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m2 s1 a_ net3 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15 PD=480e-9
PS=480e-9 M=1
m10 net050 b_b net035 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m9 s2 a_b net050 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m19 net08 b_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m22 net061 ci_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m18 c3 a_b net08 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m26 net044 ci 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m21 c4 b_b net061 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1

```

```

m20 net08 ci_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m13 net034 ci_b 0 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m12 net050 b_ net034 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m11 net035 ci 0 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m24 c1 a_ net044 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m29 net075 ci 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m28 c2 b_ net075 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m23 net044 b_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
xi20 b net015 inv
xi19 a net016 inv
xi26 s1 s2 s NAND2
xi36 c2 c1 co NAND2
xi35 c4 c3 co_b NAND2
xi21 net016 pc a_b AND2
xi18 pc b b_ AND2
xi17 a pc a_ AND2
xi22 pc net015 b_b AND2
.ends SPD3L_C1_1b
** End of subcircuit definition.

** Library name: my
** Cell name: SPD3L_C1_1b_test
** View name: schematic
xi10 a b cin cin_b cout cout_b pc_ctrl s SPD3L_C1_1b
v0 vdd! 0 DC=1.1

v1 pc_ctrl 0 PULSE 0 1.1 0 10e-12 10e-12 200e-12 400e-12

v4 a 0 PULSE !A1 A1 0 10e-12 10e-12 240e-12 400e-12
v2 b 0 PULSE !B1 B1 0 10e-12 10e-12 240e-12 400e-12
v5 cin 0 PULSE !C1 C1 0 10e-12 10e-12 240e-12 400e-12

**Below for nanoSim testing
**v4 a 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v2 b 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v5 cin 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

c2 cout 0 1e-15
c1 cout_b 0 1e-15
c0 s 0 1e-15
xi9 cin cin_b inv
.END

```

4-Bit Circuit

```

** Generated for: hspiceD
** Generated on: Apr 26 11:09:28 2013
** Design library name: my

```

```

** Design cell name: SPD3L_C1_4b_test
** Design view name: schematic
.GLOBAL vdd!

.TRAN 1e-12 800e-12 START=0.0 SWEEP DATA=D
.DATA D
+A3_ A2_ A1_ A0_ B3_ B2_ B1_ B0_ Ci_ !A3_ !A2_ !A1_ !A0_ !B3_ !B2_ !B1_ !B0_
!Ci_
+0 0 0 1.1 0 1.1 0 1.1 0 1.1 1.1 1.1 0 1.1 0 1.1 0 1.1 0 1.1 0
1.1
+1.1 0 1.1 0 0 0 1.1 1.1 1.1 0 1.1 0 1.1 1.1 1.1 0 1.1 0 1.1 0 0
0
+0 0 0 0 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 0 1.1 1.1 1.1 0 0 0
0
+1.1 1.1 1.1 1.1 0 1.1 1.1 1.1 1.1 0 0 0 0 1.1 0 0 0 0 0 0
0
+1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 0 0 0 0 0 0 0 0 0 0 0
0
.ENDDATA

**.PRINT TRAN POWER
**.MEASURE TRAN avgpwr AVG POWER FROM 0 TO 800e-12
**.MEASURE TRAN maxpwr MAX POWER FROM 0 TO 800e-12
**.MEASURE TRAN avg_vdd AVG P(v0) FROM 0 TO 800e-12

.OP

.TEMP 25.0
.OPTION
+ ARTIST=2
+ INGOLD=2
+ PARHIER=LOCAL
+ PSF=2
+ POST
.INCLUDE "/apps/FreePDK45/ncsu_basekit/models/hspice/hspice_nom.include"

** Library name: my
** Cell name: inv
** View name: schematic
.subckt inv in out
m0 out in vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m1 out in 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
.ends inv
** End of subcircuit definition.

** Library name: my
** Cell name: NAND2
** View name: schematic
.subckt NAND2 a b y
m0 y a vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m1 y b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1

```

```

m3 net11 b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m2 y a net11 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
.ends NAND2
** End of subcircuit definition.

** Library name: my
** Cell name: AND2
** View name: schematic
.subckt AND2 a b y
xi0 a b net7 NAND2
xi1 net7 y inv
.ends AND2
** End of subcircuit definition.

** Library name: my
** Cell name: SPD3L_C1_1b
** View name: schematic
.subckt SPD3L_C1_1b a b ci ci_b co co_b pc s
m1 s1 s vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m0 s1 a_ vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m6 s2 s vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m17 c4 b_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m14 c3 a_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m31 c2 co vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m16 c4 co_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m27 c1 co vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m30 c2 b_ vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m5 s2 a_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m25 c1 a_ vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m15 c3 co_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m8 net10 ci 0 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15 PD=480e-9
PS=480e-9 M=1
m7 net3 b_ net10 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m4 net11 ci_b 0 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m3 net3 b_b net11 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m2 s1 a_ net3 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15 PD=480e-9
PS=480e-9 M=1
m10 net050 b_b net035 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1

```

```

m9 s2 a_b net050 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m19 net08 b_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m22 net061 ci_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m18 c3 a_b net08 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m26 net044 ci 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m21 c4 b_b net061 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m20 net08 ci_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m13 net034 ci_b 0 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m12 net050 b_ net034 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m11 net035 ci 0 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m24 c1 a_ net044 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m29 net075 ci 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m28 c2 b_ net075 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m23 net044 b_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
xi20 b net015 inv
xi19 a net016 inv
xi26 s1 s2 s NAND2
xi36 c2 c1 co NAND2
xi35 c4 c3 co_b NAND2
xi21 net016 pc a_b AND2
xi18 pc b b_ AND2
xi17 a pc a_ AND2
xi22 pc net015 b_b AND2
.ends SPD3L_C1_1b
** End of subcircuit definition.

** Library name: my
** Cell name: SPD3L_C1_4b_test
** View name: schematic
xi26 a3 b3 net24 net25 co co_b pc s3 SPD3L_C1_1b
xi25 a2 b2 net22 net23 net24 net25 pc s2 SPD3L_C1_1b
xi24 a1 b1 net20 net21 net22 net23 pc s1 SPD3L_C1_1b
xi23 a0 b0 ci ci_b net20 net21 pc s0 SPD3L_C1_1b
v0 vdd! 0 DC=1.1

v4 pc 0 PULSE 0 1.1 0 10e-12 10e-12 200e-12 400e-12

v17 a3 0 PULSE !A3_ A3_ 0 10e-12 10e-12 240e-12 400e-12
v14 a2 0 PULSE !A2_ A2_ 0 10e-12 10e-12 240e-12 400e-12
v7 a1 0 PULSE !A1_ A1_ 0 10e-12 10e-12 240e-12 400e-12
v13 a0 0 PULSE !A0_ A0_ 0 10e-12 10e-12 240e-12 400e-12

v16 b3 0 PULSE !B3_ B3_ 0 10e-12 10e-12 240e-12 400e-12

```

```

v15 b2 0 PULSE !B2_ B2_ 0 10e-12 10e-12 240e-12 400e-12
v6 b1 0 PULSE !B1_ B1_ 0 10e-12 10e-12 240e-12 400e-12
v12 b0 0 PULSE !B0_ B0_ 0 10e-12 10e-12 240e-12 400e-12

v5 ci 0 PULSE !Ci_ Ci_ 0 10e-12 10e-12 240e-12 400e-12
v18 ci_b 0 PULSE Ci_ !Ci_ 0 10e-12 10e-12 240e-12 400e-12
**Testing for NanoSim
*****
**Test1
***v17 a3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v14 a2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v7 a1 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v13 a0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

***v16 b3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v6 b1 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

***v5 ci 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v18 ci_b 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
*****
```

**Test2

```

***v17 a3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v14 a2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v7 a1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v13 a0 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12

***v16 b3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v15 b2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

***v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****
```

**Test3

```

***v17 a3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v14 a2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v7 a1 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v13 a0 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12

***v16 b3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

***v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****
```

**Test4

```

***v17 a3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v14 a2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v7 a1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
```

```

**v13 a0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v16 b3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****  

**Test5
**v17 a3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v14 a2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v7 a1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v13 a0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v16 b3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****  

c7 co 0 1e-15
c6 co_b 0 1e-15
c5 s3 0 1e-15
c4 s2 0 1e-15
c3 s1 0 1e-15
c0 s0 0 1e-15
.END

```

Circuit 2: D3L

1-Bit Circuit

```

** Generated for: hspiceD
** Generated on: Apr 25 10:24:18 2013
** Design library name: my
** Design cell name: D3L_C2_1b_test
** Design view name: schematic
.GLOBAL vdd!

```

```

.TRAN 1e-12 800e-12 START=0.0 SWEEP DATA=D
.DATA D
+A1 !A1 B1 !B1 C1 !C1
+0 1.1 0 1.1 0 1.1
+0 1.1 0 1.1 1.1 0
+0 1.1 1.1 0 0 1.1
+0 1.1 1.1 0 1.1 0
+1.1 0 0 1.1 0 1.1
+1.1 0 0 1.1 1.1 0
+1.1 0 1.1 0 0 1.1

```

```

+1.1 0      1.1    0      1.1   0
.ENDDATA

.OP

.TEMP 25.0
.OPTION
+    ARTIST=2
+    INGOLD=2
+    PARHIER=LOCAL
+    PSF=2
+    POST
.INCLUDE "/apps/FreePDK45/ncsu_basekit/models/hspice/hspice_nom.include"

**.PRINT TRAN POWER
**.MEASURE TRAN avgpwr AVG POWER FROM 0 TO 800e-12
**.MEASURE TRAN maxpwr MAX POWER FROM 0 TO 800e-12
**.MEASURE TRAN avg_vdd AVG P(v0) FROM 0 TO 800e-12

** Library name: my
** Cell name: NAND2
** View name: schematic
.subckt NAND2 a b y
m0 y a vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m1 y b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m3 net11 b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m2 y a net11 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
.ends NAND2
** End of subcircuit definition.

** Library name: my
** Cell name: inv
** View name: schematic
.subckt inv in out
m0 out in vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m1 out in 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
.ends inv
** End of subcircuit definition.

** Library name: my
** Cell name: AND2
** View name: schematic
.subckt AND2 a b y
x10 a b net7 NAND2
x11 net7 y inv
.ends AND2
** End of subcircuit definition.

** Library name: my
** Cell name: D3L_C2_1b
** View name: schematic

```

```

.subckt D3L_C2_1b a b_ ci ci_b co co_b pc s
m32 net064 g_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m31 net064 co_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m30 net049 co vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m29 net049 p net080 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m28 net080 g vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m27 net051 g_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m25 net051 b_b net066 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m24 net066 a_b vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m21 net044 g vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m19 net044 a_ vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m16 net019 a_ net032 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m15 net032 a_b vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m14 net019 p_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m13 net015 s vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m10 net015 p net023 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m9 net023 p_b vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m2 net07 a_ net15 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m1 net15 a_b vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m0 net07 p vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m38 net049 g 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m37 net088 ci 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m36 net049 p net088 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m35 net060 ci_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m34 net060 p_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m33 net064 g_b net060 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m26 net051 b_b 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m23 net051 a_b 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m22 net067 b_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1

```

```

m20 net044 a_ net067 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m18 net019 a_ net16 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m17 net019 a_b net17 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m12 net022 ci 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m11 net015 p_b net022 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m8 net024 ci_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m7 net015 p net024 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m6 net16 b_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m5 net07 a_b net16 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m4 net17 b_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m3 net07 a_ net17 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
xi25 pc net0101 b_b AND2
xi2 net18 pc a_b AND2
xi0 a pc a_ AND2
xi21 net064 co_b inv
xi20 net049 co inv
xi18 net051 g_b inv
xi14 net044 g inv
xi12 b_ net0101 inv
xi10 net019 p_b inv
xi8 net015 s inv
xi5 net07 p inv
xi1 a net18 inv
.ends D3L_C2_1b
** End of subcircuit definition.

** Library name: my
** Cell name: D3L_C2_1b_test
** View name: schematic
xi12 a b cin cin_b cout cout_b pc_ctrl s D3L_C2_1b
v0 vdd! 0 DC=1.1

v1 pc_ctrl 0 PULSE 0 1.1 0 10e-12 10e-12 200e-12 400e-12

v4 a 0 PULSE !A1 A1 0 10e-12 10e-12 240e-12 400e-12
v2 b 0 PULSE !B1 B1 0 10e-12 10e-12 240e-12 400e-12
v5 cin 0 PULSE !C1 C1 0 10e-12 10e-12 240e-12 400e-12
**For NanoSim Testing
***v4 a 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v2 b 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v5 cin 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

c2 cout 0 1e-15
c1 cout_b 0 1e-15
c0 s 0 1e-15
xi9 cin cin_b inv

```

```
.END
```

4-Bit Circuit

```
** Generated for: hspiceD
** Generated on: Apr 26 11:15:23 2013
** Design library name: my
** Design cell name: D3L_C2_4b_test
** Design view name: schematic
.GLOBAL vdd!

.TRAN 1e-12 800e-12 START=0.0 SWEEP DATA=D
.DATA D
+A3_ A2_ A1_ A0_ B3_ B2_ B1_ B0_ Ci_ !A3_ !A2_ !A1_ !A0_ !B3_ !B2_ !B1_ !B0_
!Ci_
+0 0 0 1.1 0 1.1 0 1.1 0 1.1 1.1 1.1 0 1.1 0 1.1 0 1.1 0
1.1
+1.1 0 1.1 0 0 0 1.1 1.1 1.1 0 1.1 0 1.1 1.1 1.1 0 1.1 0 0
0
+0 0 0 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 0 1.1 0 0 0 0
0
+1.1 1.1 1.1 1.1 0 1.1 1.1 1.1 1.1 0 0 0 0 1.1 0 0 0 0
0
+1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 0 0 0 0 0 0 0 0 0
0
.ENDDATA

**.PRINT TRAN POWER
**.MEASURE TRAN avgpwr AVG POWER FROM 0 TO 800e-12
**.MEASURE TRAN maxpwr MAX POWER FROM 0 TO 800e-12
**.MEASURE TRAN avg_vdd AVG P(v0) FROM 0 TO 800e-12

.OP

.TEMP 25.0
.OPTION
+ ARTIST=2
+ INGOLD=2
+ PARHIER=LOCAL
+ PSF=2
+ POST
.INCLUDE "/apps/FreePDK45/ncsu_basekit/models/hspice/hspice_nom.include"

** Library name: my
** Cell name: NAND2
** View name: schematic
.subckt NAND2 a b y
m0 y a vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m1 y b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m3 net11 b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
```

```

m2 y a net11 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
.ends NAND2
** End of subcircuit definition.

** Library name: my
** Cell name: inv
** View name: schematic
.subckt inv in out
m0 out in vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m1 out in 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
.ends inv
** End of subcircuit definition.

** Library name: my
** Cell name: AND2
** View name: schematic
.subckt AND2 a b y
xi0 a b net7 NAND2
xi1 net7 y inv
.ends AND2
** End of subcircuit definition.

** Library name: my
** Cell name: D3L_C2_1b
** View name: schematic
.subckt D3L_C2_1b a b_ ci ci_b co co_b pc s
m32 net064 g_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m31 net064 co_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m30 net049 co vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m29 net049 p net080 vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m28 net080 g vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m27 net051 g_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m25 net051 b_b net066 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m24 net066 a_b vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m21 net044 g vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m19 net044 a_ vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m16 net019 a_ net032 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m15 net032 a_b vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m14 net019 p_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m13 net015 s vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1

```

```

m10 net015 p net023 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m9 net023 p_b vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m2 net07 a_ net15 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m1 net15 a_b vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m0 net07 p vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m38 net049 g 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m37 net088 ci 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m36 net049 p net088 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m35 net060 ci_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m34 net060 p_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m33 net064 g_b net060 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m26 net051 b_b 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m23 net051 a_b 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m22 net067 b_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m20 net044 a_ net067 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m18 net019 a_ net16 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m17 net019 a_b net17 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m12 net022 ci 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m11 net015 p_b net022 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m8 net024 ci_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m7 net015 p net024 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m6 net16 b_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m5 net07 a_b net16 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m4 net17 b_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m3 net07 a_ net17 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
xi25 pc net0101 b_b AND2
xi12 net18 pc a_b AND2
xi0 a pc a_ AND2
xi21 net064 co_b inv
xi20 net049 co inv
xi18 net051 g_b inv
xi14 net044 g inv

```

```

xi12 b_ net0101 inv
xi10 net019 p_b inv
xi8 net015 s inv
xi5 net07 p inv
xi1 a net18 inv
.ends D3L_C2_1b
** End of subcircuit definition.

** Library name: my
** Cell name: D3L_C2_4b_test
** View name: schematic
xi30 a3 b3 net24 net25 co co_b pc s3 D3L_C2_1b
xi29 a2 b2 net22 net23 net24 net25 pc s2 D3L_C2_1b
xi28 a1 b1 net20 net21 net22 net23 pc s1 D3L_C2_1b
xi27 a0 b0 ci ci_b net20 net21 pc s0 D3L_C2_1b
v0 vdd! 0 DC=1.1

v4 pc 0 PULSE 0 1.1 0 10e-12 10e-12 200e-12 400e-12

v17 a3 0 PULSE !A3_ A3_ 0 10e-12 10e-12 240e-12 400e-12
v14 a2 0 PULSE !A2_ A2_ 0 10e-12 10e-12 240e-12 400e-12
v7 a1 0 PULSE !A1_ A1_ 0 10e-12 10e-12 240e-12 400e-12
v13 a0 0 PULSE !A0_ A0_ 0 10e-12 10e-12 240e-12 400e-12

v16 b3 0 PULSE !B3_ B3_ 0 10e-12 10e-12 240e-12 400e-12
v15 b2 0 PULSE !B2_ B2_ 0 10e-12 10e-12 240e-12 400e-12
v6 b1 0 PULSE !B1_ B1_ 0 10e-12 10e-12 240e-12 400e-12
v12 b0 0 PULSE !B0_ B0_ 0 10e-12 10e-12 240e-12 400e-12

v5 ci 0 PULSE !Ci_ Ci_ 0 10e-12 10e-12 240e-12 400e-12
v18 ci_b 0 PULSE Ci_ !Ci_ 0 10e-12 10e-12 240e-12 400e-12

**For nanosim testing
*****
**Test1
**v17 a3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v14 a2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v7 a1 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v13 a0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v16 b3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v6 b1 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
*****

**Test2
**v17 a3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v14 a2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v7 a1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v13 a0 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12

**v16 b3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12

```

```

**v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****  

**Test3
**v17 a3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v14 a2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v7 a1 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v13 a0 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12

**v16 b3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****  

**Test4
**v17 a3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v14 a2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v7 a1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v13 a0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v16 b3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****  

**Test5
**v17 a3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v14 a2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v7 a1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v13 a0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v16 b3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****  

c7 co 0 1e-15
c6 co_b 0 1e-15
c5 s3 0 1e-15
c4 s2 0 1e-15
c3 s1 0 1e-15

```

```
c0 s0 0 1e-15
.END
```

Circuit 2: SPD3L

1-Bit Circuit

```
** Generated for: hspiceD
** Generated on: Apr 25 15:33:01 2013
** Design library name: my
** Design cell name: SPD3L_C2_1b_test
** Design view name: schematic
.GLOBAL vdd!

.TRAN 1e-12 800e-12 START=0.0 SWEEP DATA=D
.DATA D
+A1 !A1 B1 !B1 C1 !C1
+0 1.1 0 1.1 0 1.1
+0 1.1 0 1.1 1.1 0
+0 1.1 1.1 0 0 1.1
+0 1.1 1.1 0 1.1 0
+1.1 0 0 1.1 0 1.1
+1.1 0 0 1.1 1.1 0
+1.1 0 1.1 0 0 1.1
+1.1 0 1.1 0 1.1 0
.ENDDATA

**.PRINT TRAN POWER
**.MEASURE TRAN avgpwr AVG POWER FROM 0 TO 800e-12
**.MEASURE TRAN maxpwr MAX POWER FROM 0 TO 800e-12
**.MEASURE TRAN avg_vdd AVG P(v0) FROM 0 TO 800e-12

.OP

.TEMP 25.0
.OPTION
+ ARTIST=2
+ INGOLD=2
+ PARHIER=LOCAL
+ PSF=2
+ POST
.INCLUDE "/apps/FreePDK45/ncsu_basekit/models/hspice/hspice_nom.include"

** Library name: my
** Cell name: NAND2
** View name: schematic
.subckt NAND2 a b y
m0 y a vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m1 y b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m3 net11 b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m2 y a net11 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
.ends NAND2
```

```

** End of subcircuit definition.

** Library name: my
** Cell name: inv
** View name: schematic
.subckt inv in out
m0 out in vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m1 out in 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
.ends inv
** End of subcircuit definition.

** Library name: my
** Cell name: AND2
** View name: schematic
.subckt AND2 a b y
xi0 a b net7 NAND2
xi1 net7 y inv
.ends AND2
** End of subcircuit definition.

** Library name: my
** Cell name: SPD3L_C2_1b
** View name: schematic
.subckt SPD3L_C2_1b a b ci ci_b co co_b pc s
m67 col p vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m51 s2 p_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m50 s2 s vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m49 s1 s vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m46 s1 p vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m45 p4 p_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m32 net064 g_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m31 net064 co_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m58 g2 b_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m57 g1 g_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m54 g1 a_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m21 net044 g vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m19 net044 a_ vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m39 p2 a_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m42 p2 p vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1

```

m15 p3 a_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1

m14 p3 p_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1

m64 c01 co vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1

m63 c02 co vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1

m61 c02 g vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1

m60 g2 g_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1

m43 p4 a_ vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1

m1 p1 a_ vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1

m0 p1 p vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1

m66 net0129 ci 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1

m65 c01 p net0129 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1

m53 s2 p_b net0119 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1

m52 net0119 ci 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1

m48 s1 p net0120 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1

m47 net0120 ci_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1

m44 p4 a_ net0110 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1

m35 net060 ci_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1

m34 net060 p_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1

m33 net064 g_b net060 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1

m59 g2 b_b 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1

m55 g1 a_b 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1

m22 net067 b_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1

m20 net044 a_ net067 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1

m17 p3 a_b net17 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1

m40 net0110 b_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1

m62 c02 g 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1

m41 p2 a_b net0110 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1

m4 net17 b_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1

```

m3 p1 a_ net17 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
xi25 pc net0101 b_b AND2
xi2 net18 pc a_b AND2
xi0 a pc a_ AND2
xi21 net064 co_b inv
xi14 net044 g inv
xi12 b_ net0101 inv
xi1 a net18 inv
xi48 co2 col co NAND2
xi37 s2 s1 s NAND2
xi32 p4 p3 p_b NAND2
xi31 p2 p1 p NAND2
xi43 g2 g1 g_b NAND2
.ends SPD3L_C2_1b
** End of subcircuit definition.

** Library name: my
** Cell name: SPD3L_C2_1b_test
** View name: schematic
xi13 a b cin cin_b cout cout_b pc_ctrl s SPD3L_C2_1b
v0 vdd! 0 DC=1.1

v1 pc_ctrl 0 PULSE 0 1.1 0 10e-12 10e-12 200e-12 400e-12

v4 a 0 PULSE !A1 A1 0 10e-12 10e-12 240e-12 400e-12
v2 b 0 PULSE !B1 B1 0 10e-12 10e-12 240e-12 400e-12
v5 cin 0 PULSE !C1 C1 0 10e-12 10e-12 240e-12 400e-12
**For nanosim testing
***v4 a 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v2 b 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v5 cin 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

c2 cout 0 1e-15
c1 cout_b 0 1e-15
c0 s 0 1e-15
xi9 cin cin_b inv
.END

```

4-Bit Circuit

```

** Generated for: hspiceD
** Generated on: Apr 26 11:39:24 2013
** Design library name: my
** Design cell name: SPD3L_C2_4b_test
** Design view name: schematic
.GLOBAL vdd!

```

```

.TRAN 1e-12 800e-12 START=0.0 SWEEP DATA=D
.DATA D
+A3_ A2_ A1_ A0_ B3_ B2_ B1_ B0_ Ci_ !A3_ !A2_ !A1_ !A0_ !B3_ !B2_ !B1_ !B0_
!Ci_
+0 0 0 1.1 0 1.1 0 1.1 0 1.1 1.1 1.1 1.1 0 1.1 0 1.1 0
1.1

```

```

+1.1 0    1.1 0    0    0    1.1 1.1 1.1 0    1.1 0    1.1 1.1 1.1 0    0
0
+0    0    0    0    1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 0    0    0    0
0
+1.1 1.1 1.1 1.1 0    1.1 1.1 1.1 1.1 0    0    0    0    1.1 0    0    0
0
+1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 0    0    0    0    0    0    0
0
**.ENDDATA

**.PRINT TRAN POWER
**.MEASURE TRAN avgpwr AVG POWER FROM 0 TO 800e-12
**.MEASURE TRAN maxpwr MAX POWER FROM 0 TO 800e-12
**.MEASURE TRAN avg_vdd AVG P(v0) FROM 0 TO 800e-12

.OP

.TEMP 25.0
.OPTION
+    ARTIST=2
+    INGOLD=2
+    PARHIER=LOCAL
+    PSF=2
+    POST
.INCLUDE "/apps/FreePDK45/ncsu_basekit/models/hspice/hspice_nom.include"

** Library name: my
** Cell name: NAND2
** View name: schematic
.subckt NAND2 a b y
m0 y a vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m1 y b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m3 net11 b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m2 y a net11 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
.ends NAND2
** End of subcircuit definition.

** Library name: my
** Cell name: inv
** View name: schematic
.subckt inv in out
m0 out in vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m1 out in 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
.ends inv
** End of subcircuit definition.

** Library name: my
** Cell name: AND2
** View name: schematic
.subckt AND2 a b y
xi0 a b net7 NAND2

```

```

xil net7 y inv
.ends AND2
** End of subcircuit definition.

** Library name: my
** Cell name: SPD3L_C2_1b
** View name: schematic
.subckt SPD3L_C2_1b a b_ ci ci_b co co_b pc s
m67 col p vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m51 s2 p_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m50 s2 s vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m49 s1 s vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m46 s1 p vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m45 p4 p_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m32 net064 g_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m31 net064 co_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m58 g2 b_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m57 g1 g_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m54 g1 a_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m21 net044 g vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m19 net044 a_vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m39 p2 a_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m42 p2 p vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m15 p3 a_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m14 p3 p_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m64 co1 co vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m63 co2 co vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m61 co2 g vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m60 g2 g_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m43 p4 a_vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m1 p1 a_vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m0 p1 p vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1

```

```

m66 net0129 ci 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m65 co1 p net0129 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m53 s2 p_b net0119 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m52 net0119 ci 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m48 s1 p net0120 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m47 net0120 ci_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m44 p4 a_ net0110 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m35 net060 ci_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m34 net060 p_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m33 net064 g_b net060 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m59 g2 b_b 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m55 g1 a_b 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m22 net067 b_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m20 net044 a_ net067 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m17 p3 a_b net17 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m40 net0110 b_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m62 co2 g 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m41 p2 a_b net0110 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m4 net17 b_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m3 p1 a_ net17 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
xi25 pc net0101 b_b AND2
xi12 net18 pc a_b AND2
xi10 a pc a_ AND2
xi21 net064 co_b inv
xi14 net044 g inv
xi12 b_ net0101 inv
xi1 a net18 inv
xi48 co2 co1 co NAND2
xi37 s2 s1 s NAND2
xi32 p4 p3 p_b NAND2
xi31 p2 p1 p NAND2
xi43 g2 g1 g_b NAND2
.ends SPD3L_C2_1b
** End of subcircuit definition.

** Library name: my
** Cell name: SPD3L_C2_4b_test

```

```

** View name: schematic
xi34 a3 b3 net24 net25 co co_b pc s3 SPD3L_C2_1b
xi33 a2 b2 net22 net23 net24 net25 pc s2 SPD3L_C2_1b
xi32 a1 b1 net20 net21 net22 net23 pc s1 SPD3L_C2_1b
xi31 a0 b0 ci ci_b net20 net21 pc s0 SPD3L_C2_1b
v0 vdd! 0 DC=1.1

v4 pc 0 PULSE 0 1.1 0 10e-12 10e-12 200e-12 400e-12

v17 a3 0 PULSE !A3_ A3_ 0 10e-12 10e-12 240e-12 400e-12
v14 a2 0 PULSE !A2_ A2_ 0 10e-12 10e-12 240e-12 400e-12
v7 a1 0 PULSE !A1_ A1_ 0 10e-12 10e-12 240e-12 400e-12
v13 a0 0 PULSE !A0_ A0_ 0 10e-12 10e-12 240e-12 400e-12

v16 b3 0 PULSE !B3_ B3_ 0 10e-12 10e-12 240e-12 400e-12
v15 b2 0 PULSE !B2_ B2_ 0 10e-12 10e-12 240e-12 400e-12
v6 b1 0 PULSE !B1_ B1_ 0 10e-12 10e-12 240e-12 400e-12
v12 b0 0 PULSE !B0_ B0_ 0 10e-12 10e-12 240e-12 400e-12

v5 ci 0 PULSE !Ci_ Ci_ 0 10e-12 10e-12 240e-12 400e-12
v18 ci_b 0 PULSE Ci_ !Ci_ 0 10e-12 10e-12 240e-12 400e-12
**For nanosim testing
*****Test1*****
**v17 a3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v14 a2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v7 a1 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v13 a0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v16 b3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v6 b1 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
*****Test2*****
**v17 a3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v14 a2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v7 a1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v13 a0 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12

**v16 b3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****Test3*****
**v17 a3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v14 a2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v7 a1 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12

```

```

**v13 a0 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v16 b3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****  

**Test4
**v17 a3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v14 a2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v7 a1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v13 a0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v16 b3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****  

**Test5
**v17 a3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v14 a2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v7 a1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v13 a0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v16 b3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****  

c7 co 0 1e-15
c6 co_b 0 1e-15
c5 s3 0 1e-15
c4 s2 0 1e-15
c3 s1 0 1e-15
c0 s0 0 1e-15
.END

```

Bonus: D3L

1-Bit Circuit

** Generated for: hspiceD

```

** Generated on: Apr 25 20:34:25 2013
** Design library name: my
** Design cell name: D3L_C3_1b_test
** Design view name: schematic
.GLOBAL vdd!

.TRAN 1e-12 800e-12 START=0.0 SWEEP DATA=D
.DATA D
+A1 !A1 B1 !B1 C1 !C1
+0 1.1 0 1.1 0 1.1
+0 1.1 0 1.1 1.1 0
+0 1.1 1.1 0 0 1.1
+0 1.1 1.1 0 1.1 0
+1.1 0 0 1.1 0 1.1
+1.1 0 0 1.1 1.1 0
+1.1 0 1.1 0 0 1.1
+1.1 0 1.1 0 1.1 0
.ENDDATA

***.PRINT TRAN POWER
***.MEASURE TRAN avgpwr AVG POWER FROM 0 TO 800e-12
***.MEASURE TRAN maxpwr MAX POWER FROM 0 TO 800e-12
***.MEASURE TRAN avg_vdd AVG P(v0) FROM 0 TO 800e-12

.OP

.TEMP 25.0
.OPTION
+ ARTIST=2
+ INGOLD=2
+ PARHIER=LOCAL
+ PSF=2
+ POST
.INCLUDE "/apps/FreePDK45/ncsu_basekit/models/hspice/hspice_nom.include"

** Library name: my
** Cell name: inv
** View name: schematic
.subckt inv in out
m0 out in vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m1 out in 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
.ends inv
** End of subcircuit definition.

** Library name: my
** Cell name: NAND2
** View name: schematic
.subckt NAND2 a b y
m0 y a vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m1 y b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m3 net11 b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1

```

```

m2 y a net11 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
.ends NAND2
** End of subcircuit definition.

** Library name: my
** Cell name: AND2
** View name: schematic
.subckt AND2 a b y
x10 a b net7 NAND2
x11 net7 y inv
.ends AND2
** End of subcircuit definition.

** Library name: my
** Cell name: D3L_C3_1b
** View name: schematic
.subckt D3L_C3_1b a b cin cin_b cout cout_b pc_ctrl s
m34 net062 cin_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m33 net044 b_b net062 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m32 net012 cin_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m31 net012 b_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m30 net044 a_b net012 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m26 net064 cin 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m25 net045 b_net064 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m24 net016 cin 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m23 net016 b_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m22 net045 a_net016 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m38 net034 a_net048 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m40 net047 cin 0 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m39 net048 b_net047 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m44 net051 cin 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m42 net051 a_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m41 net034 cout_b net051 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m43 net051 b_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m29 net063 b_b vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m28 net044 a_b net063 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1

```

```

m27 net044 cout_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m21 net065 b_ vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m20 net045 a_ net065 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m19 net045 cout vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m37 net034 s vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m35 net034 cout_b net049 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-
15 PD=570e-9 PS=570e-9 M=1
m36 net049 a_ vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
xi14 a net067 inv
xi9 net044 cout_b inv
xi6 net045 cout inv
xi18 b net068 inv
xi20 net034 s inv
xi17 pc_ctrl net068 b_b AND2
xi13 pc_ctrl b_b_ AND2
xi12 a pc_ctrl a_ AND2
xi16 net067 pc_ctrl a_b AND2
.ends D3L_C3_1b
** End of subcircuit definition.

** Library name: my
** Cell name: D3L_C3_1b_test
** View name: schematic
xi13 a b cin cin_b cout cout_b pc_ctrl s D3L_C3_1b
v0 vdd! 0 DC=1.1

v1 pc_ctrl 0 PULSE 0 1.1 0 10e-12 10e-12 200e-12 400e-12

v4 a 0 PULSE !A1 A1 0 10e-12 10e-12 240e-12 400e-12
v2 b 0 PULSE !B1 B1 0 10e-12 10e-12 240e-12 400e-12
v5 cin 0 PULSE !C1 C1 0 10e-12 10e-12 240e-12 400e-12
**For nanosim testing
**v4 a 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v2 b 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v5 cin 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

c2 cout 0 1e-15
c1 cout_b 0 1e-15
c0 s 0 1e-15
xi9 cin cin_b inv
.END

```

4-Bit Circuit

```

** Generated for: hspiceD
** Generated on: Apr 26 12:31:42 2013
** Design library name: my
** Design cell name: D3L_C3_4b_test
** Design view name: schematic
.GLOBAL vdd!

```

```

.TRAN 1e-12 800e-12 START=0.0 SWEEP DATA=D
.DATA D
+A3_ A2_ A1_ A0_ B3_ B2_ B1_ B0_ Ci_ !A3_ !A2_ !A1_ !A0_ !B3_ !B2_ !B1_ !B0_
!Ci_
+0 0 0 1.1 0 1.1 0 1.1 0 1.1 1.1 1.1 0 1.1 0 1.1 0 1.1 0 1.1 0
1.1
+1.1 0 1.1 0 0 0 1.1 1.1 1.1 0 1.1 0 1.1 1.1 1.1 0 1.1 0 1.1 0 0
0
+0 0 0 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 0 1.1 1.1 1.1 0 0 0 0
0
+1.1 1.1 1.1 1.1 0 1.1 1.1 1.1 1.1 0 0 0 0 1.1 0 0 0 0 0 0
0
+1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 0 0 0 0 0 0 0 0 0 0 0
0
.ENDDATA

***.PRINT TRAN POWER
***.MEASURE TRAN avgpwr AVG POWER FROM 0 TO 800e-12
***.MEASURE TRAN maxpwr MAX POWER FROM 0 TO 800e-12
***.MEASURE TRAN avg_vdd AVG P(v0) FROM 0 TO 800e-12

.OP

.TEMP 25.0
.OPTION
+ ARTIST=2
+ INGOLD=2
+ PARHIER=LOCAL
+ PSF=2
+ POST
.INCLUDE "/apps/FreePDK45/ncsu_basekit/models/hspice/hspice_nom.include"

** Library name: my
** Cell name: inv
** View name: schematic
.subckt inv in out
m0 out in vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m1 out in 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
.ends inv
** End of subcircuit definition.

** Library name: my
** Cell name: NAND2
** View name: schematic
.subckt NAND2 a b y
m0 y a vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m1 y b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m3 net11 b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m2 y a net11 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1

```

```

.ends NAND2
** End of subcircuit definition.

** Library name: my
** Cell name: AND2
** View name: schematic
.subckt AND2 a b y
xi0 a b net7 NAND2
xi1 net7 y inv
.ends AND2
** End of subcircuit definition.

** Library name: my
** Cell name: D3L_C3_1b
** View name: schematic
.subckt D3L_C3_1b a b cin cin_b cout cout_b pc_ctrl s
m34 net062 cin_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m33 net044 b_b net062 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m32 net012 cin_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m31 net012 b_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m30 net044 a_b net012 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m26 net064 cin 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m25 net045 b_ net064 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m24 net016 cin 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m23 net016 b_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m22 net045 a_ net016 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m38 net034 a_ net048 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m40 net047 cin 0 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m39 net048 b_ net047 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m44 net051 cin 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m42 net051 a_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m41 net034 cout_b net051 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m43 net051 b_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m29 net063 b_b vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m28 net044 a_b net063 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m27 net044 cout_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1

```

```

m21 net065 b_ vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m20 net045 a_ net065 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m19 net045 cout vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m37 net034 s vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m35 net034 cout_b net049 vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
m36 net049 a_ vdd! vdd! PMOS_VTL L=50e-9 W=360e-9 AD=37.8e-15 AS=37.8e-15
PD=570e-9 PS=570e-9 M=1
xi14 a net067 inv
xi9 net044 cout_b inv
xi6 net045 cout inv
xi18 b net068 inv
xi20 net034 s inv
xi17 pc_ctrl net068 b_b AND2
xi13 pc_ctrl b_b_ AND2
xi12 a pc_ctrl a_ AND2
xi16 net067 pc_ctrl a_b AND2
.ends D3L_C3_1b
** End of subcircuit definition.

** Library name: my
** Cell name: D3L_C3_4b_test
** View name: schematic
xi26 a3 b3 net17 net16 co co_b pc s3 D3L_C3_1b
xi25 a2 b2 net021 net022 net17 net16 pc s2 D3L_C3_1b
xi24 a1 b1 net20 net21 net021 net022 pc s1 D3L_C3_1b
xi23 a0 b0 ci ci_b net20 net21 pc s0 D3L_C3_1b
v0 vdd! 0 DC=1.1

v4 pc 0 PULSE 0 1.1 0 10e-12 10e-12 200e-12 400e-12

v17 a3 0 PULSE !A3_ A3_ 0 10e-12 10e-12 240e-12 400e-12
v14 a2 0 PULSE !A2_ A2_ 0 10e-12 10e-12 240e-12 400e-12
v7 a1 0 PULSE !A1_ A1_ 0 10e-12 10e-12 240e-12 400e-12
v13 a0 0 PULSE !A0_ A0_ 0 10e-12 10e-12 240e-12 400e-12

v16 b3 0 PULSE !B3_ B3_ 0 10e-12 10e-12 240e-12 400e-12
v15 b2 0 PULSE !B2_ B2_ 0 10e-12 10e-12 240e-12 400e-12
v6 b1 0 PULSE !B1_ B1_ 0 10e-12 10e-12 240e-12 400e-12
v12 b0 0 PULSE !B0_ B0_ 0 10e-12 10e-12 240e-12 400e-12

v5 ci 0 PULSE !Ci_ Ci_ 0 10e-12 10e-12 240e-12 400e-12
v18 ci_b 0 PULSE Ci_ !Ci_ 0 10e-12 10e-12 240e-12 400e-12
**For nanosim testing
*****  

**Test1
***v17 a3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v14 a2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v7 a1 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v13 a0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

***v16 b3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

```

```

**v6 b1 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
*****  

**Test2
**v17 a3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v14 a2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v7 a1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v13 a0 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12

**v16 b3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****  

**Test3
**v17 a3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v14 a2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v7 a1 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v13 a0 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12

**v16 b3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****  

**Test4
**v17 a3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v14 a2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v7 a1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v13 a0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v16 b3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****  

**Test5
**v17 a3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v14 a2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v7 a1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v13 a0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

```

```

**v16 b3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****
```

c7 co 0 1e-15
c6 co_b 0 1e-15
c5 s3 0 1e-15
c4 s2 0 1e-15
c3 s1 0 1e-15
c0 s0 0 1e-15
.END

Bonus: SPD3L

1-Bit Circuit

```

** Generated for: hspiceD
** Generated on: Apr 25 20:29:32 2013
** Design library name: my
** Design cell name: SPD3L_C3_1b_test
** Design view name: schematic
.GLOBAL vdd!

.TRAN 1e-12 800e-12 START=0.0 SWEEP DATA=D
.DATA D
+A1 !A1 B1 !B1 C1 !C1
+0 1.1 0 1.1 0 1.1
+0 1.1 0 1.1 1.1 0
+0 1.1 1.1 0 0 1.1
+0 1.1 1.1 0 1.1 0
+1.1 0 0 1.1 0 1.1
+1.1 0 0 1.1 1.1 0
+1.1 0 1.1 0 0 1.1
+1.1 0 1.1 0 1.1 0
.ENDDATA

**.PRINT TRAN POWER
**.MEASURE TRAN avgpwr AVG POWER FROM 0 TO 800e-12
**.MEASURE TRAN maxpwr MAX POWER FROM 0 TO 800e-12
**.MEASURE TRAN avg_vdd AVG P(v0) FROM 0 TO 800e-12

.OP

.TEMP 25.0
.OPTION
+ ARTIST=2
+ INGOLD=2
+ PARHIER=LOCAL
+ PSF=2
```

```

+      POST
.INCLUDE "/apps/FreePDK45/ncsu_basekit/models/hspice/hspice_nom.include"

** Library name: my
** Cell name: inv
** View name: schematic
.subckt inv in out
m0 out in vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m1 out in 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
.ends inv
** End of subcircuit definition.

** Library name: my
** Cell name: NAND2
** View name: schematic
.subckt NAND2 a b y
m0 y a vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m1 y b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m3 net11 b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m2 y a net11 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
.ends NAND2
** End of subcircuit definition.

** Library name: my
** Cell name: AND2
** View name: schematic
.subckt AND2 a b y
xi0 a b net7 NAND2
xi1 net7 y inv
.ends AND2
** End of subcircuit definition.

** Library name: my
** Cell name: SPD3L_C3_1b
** View name: schematic
.subckt SPD3L_C3_1b a b ci ci_b co co_b pc s
m33 s1 s vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m32 s1 a_ vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m38 s2 co_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m41 s2 s vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m17 c4 b_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m14 c3 a_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m31 c2 co vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-
9 PS=300e-9 M=1

```

```

m16 c4 co_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m27 c1 co vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-
9 PS=300e-9 M=1
m30 c2 b_ vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m25 c1 a_ vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m15 c3 co_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
PD=300e-9 PS=300e-9 M=1
m42 net046 ci 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m34 s1 a_ net086 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m36 net021 ci 0 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m19 net08 b_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m22 net061 ci_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m18 c3 a_b net08 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m26 net044 ci 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m21 c4 b_b net061 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m20 net08 ci_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m37 net046 a_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m40 s2 co_b net046 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m39 net046 b_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m35 net086 b_ net021 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
PD=480e-9 PS=480e-9 M=1
m24 c1 a_ net044 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m29 net075 ci 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m28 c2 b_ net075 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-
9 PS=390e-9 M=1
m23 net044 b_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
xi20 b net015 inv
xi19 a net016 inv
xi42 s1 s2 s NAND2
xi36 c2 c1 co NAND2
xi35 c4 c3 co_b NAND2
xi21 net016 pc a_b AND2
xi18 pc b_b_ AND2
xi17 a pc a_ AND2
xi22 pc net015 b_b AND2
.ends SPD3L_C3_1b
** End of subcircuit definition.

** Library name: my

```

```

** Cell name: SPD3L_C3_1b_test
** View name: schematic
xi14 a b cin cin_b cout cout_b pc_ctrl s SPD3L_C3_1b
v0 vdd! 0 DC=1.1

v1 pc_ctrl 0 PULSE 0 1.1 0 10e-12 10e-12 200e-12 400e-12

v4 a 0 PULSE !A1 A1 0 10e-12 10e-12 240e-12 400e-12
v2 b 0 PULSE !B1 B1 0 10e-12 10e-12 240e-12 400e-12
v5 cin 0 PULSE !C1 C1 0 10e-12 10e-12 240e-12 400e-12
**For nanosim testing
**v4 a 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v2 b 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v5 cin 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

c2 cout 0 1e-15
c1 cout_b 0 1e-15
c0 s 0 1e-15
xi9 cin cin_b inv
.END

```

4-Bit Circuit

```

** Generated for: hspiceD
** Generated on: Apr 26 12:37:34 2013
** Design library name: my
** Design cell name: SPD3L_C3_4b_test
** Design view name: schematic
.GLOBAL vdd!

.TRAN 1e-12 800e-12 START=0.0 SWEEP DATA=D
.DATA D
+A3_ A2_ A1_ A0_ B3_ B2_ B1_ B0_ Ci_ !A3_ !A2_ !A1_ !A0_ !B3_ !B2_ !B1_ !B0_
!Ci_
+0 0 0 1.1 0 1.1 0 1.1 0 1.1 1.1 1.1 1.1 0 1.1 0 1.1 1.1 0 1.1 0 1.1 0
1.1
+1.1 0 1.1 0 0 0 1.1 1.1 1.1 0 1.1 0 1.1 1.1 1.1 0 1.1 1.1 0 1.1 0 1.1 0
0
+0 0 0 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 0 1.1 1.1 1.1 0 1.1 0 1.1 0
0
+1.1 1.1 1.1 1.1 0 1.1 1.1 1.1 1.1 0 0 0 0 0 1.1 0 0 0 0 0 0 0 0
0
+1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 1.1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0
.ENDDATA

**.PRINT TRAN POWER
**.MEASURE TRAN avgpwr AVG POWER FROM 0 TO 800e-12
**.MEASURE TRAN maxpwr MAX POWER FROM 0 TO 800e-12
**.MEASURE TRAN avg_vdd AVG P(v0) FROM 0 TO 800e-12

.OP

.TEMP 25.0
.OPTION

```

```

+     ARTIST=2
+     INGOLD=2
+     PARHIER=LOCAL
+     PSF=2
+     POST
.INCLUDE "/apps/FreePDK45/ncsu_basekit/models/hspice/hspice_nom.include"

** Library name: my
** Cell name: inv
** View name: schematic
.subckt inv in out
m0 out in vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m1 out in 0 0 NMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
.ends inv
** End of subcircuit definition.

** Library name: my
** Cell name: NAND2
** View name: schematic
.subckt NAND2 a b y
m0 y a vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m1 y b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m3 net11 b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
m2 y a net11 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
PS=390e-9 M=1
.ends NAND2
** End of subcircuit definition.

** Library name: my
** Cell name: AND2
** View name: schematic
.subckt AND2 a b y
x10 a b net7 NAND2
x11 net7 y inv
.ends AND2
** End of subcircuit definition.

** Library name: my
** Cell name: SPD3L_C3_1b
** View name: schematic
.subckt SPD3L_C3_1b a b ci ci_b co co_b pc s
m33 s1 s vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m32 s1 a_ vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m38 s2 co_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1
m41 s2 s vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
PS=300e-9 M=1
m17 c4 b_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
PD=390e-9 PS=390e-9 M=1

```

m14 c3 a_b vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
 PD=390e-9 PS=390e-9 M=1
 m31 c2 co vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
 PS=300e-9 M=1
 m16 c4 co_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
 PD=300e-9 PS=300e-9 M=1
 m27 c1 co vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15 PD=300e-9
 PS=300e-9 M=1
 m30 c2 b_ vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
 PD=390e-9 PS=390e-9 M=1
 m25 c1 a_ vdd! vdd! PMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
 PD=390e-9 PS=390e-9 M=1
 m15 c3 co_b vdd! vdd! PMOS_VTL L=50e-9 W=90e-9 AD=9.45e-15 AS=9.45e-15
 PD=300e-9 PS=300e-9 M=1
 m34 s1 a_ net086 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
 PD=480e-9 PS=480e-9 M=1
 m36 net021 ci 0 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
 PD=480e-9 PS=480e-9 M=1
 m42 net046 ci 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
 PS=390e-9 M=1
 m19 net08 b_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
 PS=390e-9 M=1
 m22 net061 ci_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
 PD=390e-9 PS=390e-9 M=1
 m18 c3 a_b net08 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
 PS=390e-9 M=1
 m26 net044 ci 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
 PS=390e-9 M=1
 m21 c4 b_b net061 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
 PD=390e-9 PS=390e-9 M=1
 m20 net08 ci_b 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
 PS=390e-9 M=1
 m37 net046 a_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
 PS=390e-9 M=1
 m40 s2 co_b net046 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15
 PD=390e-9 PS=390e-9 M=1
 m39 net046 b_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
 PS=390e-9 M=1
 m35 net086 b_ net021 0 NMOS_VTL L=50e-9 W=270e-9 AD=28.35e-15 AS=28.35e-15
 PD=480e-9 PS=480e-9 M=1
 m24 c1 a_ net044 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
 PS=390e-9 M=1
 m29 net075 ci 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
 PS=390e-9 M=1
 m28 c2 b_ net075 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
 PS=390e-9 M=1
 m23 net044 b_ 0 0 NMOS_VTL L=50e-9 W=180e-9 AD=18.9e-15 AS=18.9e-15 PD=390e-9
 PS=390e-9 M=1
 xi20 b net015 inv
 xi19 a net016 inv
 xi42 s1 s2 s NAND2
 xi36 c2 c1 co NAND2
 xi35 c4 c3 co_b NAND2
 xi21 net016 pc a_b AND2
 xi18 pc b_b AND2
 xi17 a pc a_ AND2
 xi22 pc net015 b_b AND2

```

.ends SPD3L_C3_1b
** End of subcircuit definition.

** Library name: my
** Cell name: SPD3L_C3_4b_test
** View name: schematic
xi30 a3 b3 net27 net26 co co_b pc s3 SPD3L_C3_1b
xi29 a2 b2 net29 net28 net27 net26 pc s2 SPD3L_C3_1b
xi28 a1 b1 net31 net30 net29 net28 pc s1 SPD3L_C3_1b
xi27 a0 b0 ci ci_b net31 net30 pc s0 SPD3L_C3_1b
v0 vdd! 0 DC=1.1

v4 pc 0 PULSE 0 1.1 0 10e-12 10e-12 200e-12 400e-12

v17 a3 0 PULSE !A3_ A3_ 0 10e-12 10e-12 240e-12 400e-12
v14 a2 0 PULSE !A2_ A2_ 0 10e-12 10e-12 240e-12 400e-12
v7 a1 0 PULSE !A1_ A1_ 0 10e-12 10e-12 240e-12 400e-12
v13 a0 0 PULSE !A0_ A0_ 0 10e-12 10e-12 240e-12 400e-12

v16 b3 0 PULSE !B3_ B3_ 0 10e-12 10e-12 240e-12 400e-12
v15 b2 0 PULSE !B2_ B2_ 0 10e-12 10e-12 240e-12 400e-12
v6 b1 0 PULSE !B1_ B1_ 0 10e-12 10e-12 240e-12 400e-12
v12 b0 0 PULSE !B0_ B0_ 0 10e-12 10e-12 240e-12 400e-12

v5 ci 0 PULSE !Ci_ Ci_ 0 10e-12 10e-12 240e-12 400e-12
v18 ci_b 0 PULSE Ci_ !Ci_ 0 10e-12 10e-12 240e-12 400e-12
**For nanosim testing
*****
**Test1
***v17 a3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v14 a2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v7 a1 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v13 a0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

***v16 b3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v6 b1 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

***v5 ci 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v18 ci_b 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
*****
```

**Test2

```

***v17 a3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v14 a2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v7 a1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v13 a0 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12

***v16 b3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v15 b2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
***v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

***v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
***v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****
```

```

**Test3
**v17 a3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v14 a2 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v7 a1 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v13 a0 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12

**v16 b3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****
```

```

**Test4
**v17 a3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v14 a2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v7 a1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v13 a0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v16 b3 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****
```

```

**Test5
**v17 a3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v14 a2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v7 a1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v13 a0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v16 b3 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v15 b2 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v6 b1 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v12 b0 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12

**v5 ci 0 PULSE 0 1.1 0 10e-12 10e-12 240e-12 400e-12
**v18 ci_b 0 PULSE 1.1 0 0 10e-12 10e-12 240e-12 400e-12
*****
```

```

c7 co 0 1e-15
c6 co_b 0 1e-15
c5 s3 0 1e-15
c4 s2 0 1e-15
c3 s1 0 1e-15
c0 s0 0 1e-15
.END
```

Appendix 4: Performance Results

Average Power

Circuit 1 D3L 1-Bit

<i>A</i>	<i>B</i>	<i>Ci</i>	<i>Hspice (uW)</i>		
			Avg	Max	Av_Vdd
0	0	0	53.984	414.7	-51.598
0	0	1	73.205	410.16	-70.683
0	1	0	75.396	577.6	-73.092
0	1	1	61.1	573	-58.951
1	0	0	74.017	533.68	-71.428
1	0	1	55.689	531.84	-53.453
1	1	0	58.57	692.47	-56.55
1	1	1	72.58	688.85	-70.464

Circuit 1 D3L 4-Bit

<i>A</i>	<i>B</i>	<i>Ci</i>	<i>Hspice (uW)</i>		
			Avg	Max	Av_Vdd
0001	0101	0	241.56	1639	-234.52
1010	0011	1	262.08	1758.6	-254.75
0000	1111	1	217.46	1853.4	-211.65
1111	0111	1	253.72	2149.7	-246.56
1111	1111	1	273.35	2329.2	-266.73

Circuit 1 SPD3L 1-Bit

<i>A</i>	<i>B</i>	<i>Ci</i>	<i>Hspice (uW)</i>		
			Avg	Max	Av_Vdd
0	0	0	59.014	414.77	-56.621
0	0	1	71.533	410.24	-69.032
0	1	0	73.834	577.7	-71.299
0	1	1	56.68	573.3	-54.646
1	0	0	70.144	533.87	-67.525
1	0	1	55.294	531.79	-53.129
1	1	0	57.765	691.13	-55.454
1	1	1	77.701	692.89	-75.399

Circuit 1 SPD3L 4-Bit

<i>A</i>	<i>B</i>	<i>Ci</i>	<i>Hspice (uW)</i>		
			Avg	Max	Av_Vdd
0001	0101	0	242.48	1639.7	-235.27
1010	0011	1	256.97	1756.3	-249.29
0000	1111	1	200.17	1853.8	-194.48
1111	0111	1	268.82	2165.9	-262.36
1111	1111	1	293.2	2327.5	-286

Circuit 2 D3L 1-Bit

<i>A</i>	<i>B</i>	<i>Ci</i>	<i>Hspice (uW)</i>		
			Avg	Max	Av_Vdd
0	0	0	78.275	471.52	-75.447
0	0	1	96.374	547.04	-93.343
0	1	0	94.007	589.92	-92.221
0	1	1	81.347	514.42	-80.016
1	0	0	92.865	554.95	-89.783
1	0	1	80.975	490.21	-78.262
1	1	0	74.585	548.68	-73.186
1	1	1	91.936	589.75	-90.22

Circuit 2 D3L 4-Bit

<i>A</i>	<i>B</i>	<i>Ci</i>	<i>Hspice (uW)</i>		
			Avg	Max	Av_Vdd
0001	0101	0	320.14	1660	-313.15
1010	0011	1	340.92	1785.3	-333.3
0000	1111	1	298.73	1459.3	-295.13
1111	0111	1	333.9	1859.2	-327.94
1111	1111	1	346.11	2024.2	-341.69

Circuit 2 SPD3L 1-Bit

<i>A</i>	<i>B</i>	<i>Ci</i>	<i>Hspice (uW)</i>		
			Avg	Max	Av_Vdd
0	0	0	80.155	451.12	-77.226
0	0	1	96.03	533.94	-93.124
0	1	0	87.391	538.32	-85.525
0	1	1	75.727	494.82	-74.181
1	0	0	93.994	532.99	-90.864
1	0	1	82.44	483.81	-79.56
1	1	0	68.455	548.16	-66.996
1	1	1	83.427	565.27	-81.725

Circuit 2 SPD3L 4-Bit

A	B	Ci	Hspice (uW)		
			Avg	Max	Av_Vdd
0001	0101	0	309.67	1567.5	-302.26
1010	0011	1	326.88	1682.7	-319.39
0000	1111	1	277.2	1362.2	-273.35
1111	0111	1	309.17	1765.8	-303.28
1111	1111	1	313.03	1908.7	-308.68

Circuit 3 D3L 1-Bit

A	B	Ci	Hspice (uW)		
			Avg	Max	Av_Vdd
0	0	0	50.59	383.7	-47.958
0	0	1	66.05	419.06	-63.458
0	1	0	69.548	546	-67.13
0	1	1	55.451	552.12	-53.471
1	0	0	75.043	510.57	-72.569
1	0	1	51.279	512.74	-49.295
1	1	0	56.505	666.66	-54.399
1	1	1	73.513	670.62	-71.421

Circuit 3 D3L 4-Bit

A	B	Ci	Hspice (uW)		
			Avg	Max	Av_Vdd
0001	0101	0	223.13	1639.5	-215.62
1010	0011	1	254.21	1758.3	-246.82
0000	1111	1	205.19	1852.9	-199.32
1111	0111	1	259.35	2171.9	-252.36
1111	1111	1	283.57	2312.9	-276.43

Circuit 3 SPD3L 1-Bit

A	B	Ci	Hspice (uW)		
			Avg	Max	Av_Vdd
0	0	0	55.469	383.77	-52.971
0	0	1	67.124	418.94	-45.584
0	1	0	71.286	546.09	-68.745
0	1	1	51.81	552.19	-49.686
1	0	0	69.264	509.54	-66.73
1	0	1	50.867	512.49	-48.849
1	1	0	55.549	667.63	-53.419
1	1	1	76.381	672.03	-74.171

Circuit 3 SPD3L 4-Bit

A	B	Ci	Hspice (uW)		
			Avg	Max	Av_Vdd
0001	0101	0	228.62	1641.5	-221.33
1010	0011	1	247.17	1758.5	-240.37
0000	1111	1	190.96	1853.1	-184.57
1111	0111	1	267.27	2155.7	-259.42
1111	1111	1	292.75	2335.1	-285.73

NanoSim Outputs

Circuit 1 D3L 1-Bit

A	B	Ci	Nano Sim (u)							
			Avg S C	Avg C C	Avg W C	Avg SWC	Avg DWC	WC %	Avg Blk Pwr	Av Vdd
0	0	0	-49.08	-54.63	-1.53957	-2.06E-04	-1.5393	2.74	53.99	-49.08
0	0	1	-66.69	-67.92	-7.025	-1.97E-04	-7.025	9.37	73.36	-66.69
0	1	0	-68.57	-69.53	-7.112713	-1.97E-04	-7.1125	9.279	75.427	-68.57
0	1	1	-55.82	-60.7	-3.35	-1.89E-04	-3.35	5.2355	61.403	-55.82
1	0	0	-67.122	-68.30565	-7.2742	-1.97E-04	-7.27	9.62	73.834	-67.12268
1	0	1	-50.57	-55.18	-2.776	1.89E-04	-2.77	4.79	55.63	-50.57
1	1	0	-53.504	-56.86	-3.46	1.89E-04	-3.46	5.743	58.85	-53.5
1	1	1	-66.23	-67.15	-5.93	1.81E-04	-5.94	8.12	72.86	-66.23

Circuit 1 D3L 4-Bit

A	B	Ci	Nano Sim (u)							
			Avg S C	Avg C C	Avg W C	Avg SWC	Avg DWC	WC %	Avg Blk Pwr	Av Vdd
0001	0101	0	-221.16	-229.802	-20.054	-6.64E-04	-20.054	8.02	243.277	-221.16
1010	0011	1	-239.52	-245.83	-23.8	-6.56E-04	-23.8	8.28	263.48	-239.52
0000	1111	1	-200.13	-215.8	-16.32	-6.56E-04	-16.32	7.03	220.14	-200.13
1111	0111	1	-231.98	-237.36	-21.202	-6.31E-04	-21.2	8.2	255.18	-231.98
1111	1111	1	-250.05	-251.21	-24.9	-6.23E-04	-24.905	9.02	275.06	-250.05

Circuit 1 SPD3L 1-Bit

A	B	Ci	Nano Sim (u)							
0	0	0	Avg S C	Avg C C	Avg W C	Avg SWC	Avg DWC	WC %	Avg Blk Pwr	Av Vdd
0	0	1	-53.49	-56.01	-4.075	2.49E-04	-4.075	6.78	58.84	-53.49
0	0	1	-64.6534	-64.83	-7.006	-2.41E-04	-7.005	9.75	71.118	-64.65
0	1	0	-66.92	-67.32	-7.32	-2.41E-04	-7.32	9.8	73.62	-66.92
0	1	1	-51.54	-55.306	-3.02	-2.33E-04	-3.023	5.18	56.7	-51.54
1	0	0	-63.47	-63.87	-7.0993	-2.41E-04	-7.09	10.14	69.81	-63.47
1	0	1	-50.23	-53.59	-3.227	-2.33E-04	-3.22706	5.67	55.25	-50.24
1	1	0	-52.51	-54.68	-3.7	-2.33E-04	-3.7	6.34	57.76	-52.51
1	1	1	-71.08	-68.6	-8.55	-2.55E-04	-8.55	11.09	78.19	-71.08

Circuit 1 SPD3L 4-Bit

A	B	Ci	Nano Sim (u)							
0001	0101	0	Avg S C	Avg C C	Avg W C	Avg SWC	Avg DWC	WC %	Avg Blk Pwr	Av Vdd
1010	0011	1	-221.48	-225.29	-21.72	-8.38E-04	-21.72	8.7955	243.63	-221.48
0000	1111	1	-234.39	-234.29	-24.47	-8.30E-04	-24.47	9.458	257.83	-234.39
1111	0111	1	-183.65	-193.33	-14.93	-8.30E-04	-14.93	7.17	202.02	-183.65
1111	1111	1	-246.32	-242.02	-26.65	-8.06E-04	-26.65	9.921	270.95	-246.32
1111	1111	1	-268.37	-259.97	-30.37	-7.97E-04	-30.377	10.46	295.212	-268.37

Circuit 2 D3L 1-Bit

A	B	Ci	Nano Sim (u)							
0	0	0	Avg S C	Avg C C	Avg W C	Avg SWC	Avg DWC	WC %	Avg Blk Pwr	Av Vdd
0	0	1	-71.004	-69.52	-7.87	-2.91E-04	-7.87	10.17	78.108	-71.0045
0	0	1	-87.53	-83.32	-11.89	-2.82E-04	-11.89	12.49	96.29	-87.53
0	1	0	-85.68	-78.99	-14.69	-2.57E-04	-14.68	15.68	94.28	-85.71
0	1	1	-74.77	-71.27	-11.39	-2.48E-04	-11.39	13.779	82.256	-74.77
1	0	0	-83.64	-80.12	-11.16	-2.83E-04	-11.16	12.22	92.0092	-83.644
1	0	1	-73.1	-72.49	-8.13	-2.74E-04	-8.139	10.09	80.41	-73.1
1	1	0	-68.62	-64.1	-10.94	-2.49E-04	-10.94	14.58	75.489	-68.362
1	1	1	-84.36	-76.64	-15.43	-2.40E-04	-15.43	16.746	92.8	-84.36

Circuit 2 D3L 4-Bit

A	B	Ci	Nano Sim (u)							
0001	0101	0	Avg S C	Avg C C	Avg W C	Avg SWC	Avg DWC	WC %	Avg Blk Pwr	Av Vdd
1010	0011	1	-293.6	-280.53	-42.03	-9.57E-04	-42.03	13.03	322.96	-293.6
0000	1111	1	-311.66	-297.25	-45.73	-9.48E-04	-45.73	13.334	342.83	-311.6
1111	0111	1	-276.28	-264.22	-45.34	-8.96E-04	-45.34	14.64	303.9	-276.28
1111	1111	1	-306.29	-285.8	-51.27	-8.98E-04	-51.27	15.2	336.92	-300.2
1111	1111	1	-319.21	-291.13	-58.26	-8.64E-04	-58.26	16.67	351.13	-319.21

Circuit 2 SPD3L 1-Bit

A	B	Ci	Nano Sim (u)							
			Avg S C	Avg C C	Avg W C	Avg SWC	Avg DWC	WC %	Avg Blk Pwr	Av Vdd
0	0	0	-72.455	-68.23	-9.65	-3.64E-04	-9.6153	12.39	79.7	-72.45
0	0	1	-87.13	-79.11	-13.75	-3.55E-04	-13.78	14.839	95.845	-87.13
0	1	0	-79.843	-72.32	-13.69	-3.30E-04	-13.69	15.92	87.82	-79.84
0	1	1	-69.335	-64.87	-10.35	-3.21E-04	-10.35	13.76	76.26	-69.335
1	0	0	-85.04	-78.12	-12.9	-3.56E-04	-12.9	14.17	93.55	-85.04
1	0	1	-74.69	-70.78	-9.71	-3.47E-04	-9.7	12.06	82.16	-74.69
1	1	0	-62.75	-57.47	-9.53	-3.22E-04	-9.529	14.22	69.03	-62.75
1	1	1	-76.48	-67.83	-13.322	-3.12E-04	-13.322589	16.4	84.13	-76.48

Circuit 2 SPD3L 4-Bit

A	B	Ci	Nano Sim (u)							
			Avg S C	Avg C C	Avg W C	Avg SWC	Avg DWC	WC %	Avg Blk Pwr	Av Vdd
0001	0101	0	-283.54	-261.24	-43.48	-1.25E-03	-43.47	14.26	311.9	-283.54
1010	0011	1	-299.08	-275.009	-45.93	1.24E-03	-45.92	14.311	328.99	-299.08
0000	1111	1	-330	-239.27	-40.37	1.19E-03	-40.37	14.437	281.33	-255.75
1111	0111	1	-284.31	-257.11	-46.59	1.19E-03	-46.593	15.34	312.74	-284.31
1111	1111	1	-287.64	-255.45	-50.2	1.15E-03	-50.204	16.425	316.4	-287.64

Circuit 3 D3L 1-Bit

A	B	Ci	Nano Sim (u)							
			Avg S C	Avg C C	Avg W C	Avg SWC	Avg DWC	WC %	Avg Blk Pwr	Av Vdd
0	0	0	-45.57	-49.61	-2.1	-2.16E-04	-2.1	4.06	50.129	-45.57
0	0	1	-59.8	-58.76	-6.67	-1.96E-04	-6.67	10.199	65.78	-59.8
0	1	0	-62.9	-62.16	-6.63	-2.07E-04	-6.63	9.64	69.19	-62.9
0	1	1	-50.46	-53.54	-4.32	-1.88E-04	-4.32	7.48	55.51	-50.467
1	0	0	-68.19	-67.46	-7.55	-2.07E-04	-7.557	10.07	75.01	-68.19
1	0	1	-46.87	-48.65	-3.27	-1.88E-04	-3.27	6.31	51.56	-46.87
1	1	0	-51.76	-52.88	-3.57	-1.99E-04	-3.57	6.33	56.93	-51.76
1	1	1	-67.466	-67.52	-7.003	-1.80E-04	-7	9.39	74.21	-67.466

Circuit 3 D3L 4-Bit

A	B	Ci	Nano Sim (u)							
			Avg S C	Avg C C	Avg W C	Avg SWC	Avg DWC	WC %	Avg Blk Pwr	Av Vdd
0001	0101	0	-203.84	-206.54	-18.95	-6.75E-04	-18.95	8.4	224.22	-203.84
1010	0011	1	-232.49	-233.77	-25.24	-6.56E-04	-25.24	9.74	255.73	-232.488
0000	1111	1	-187.68	-199.83	-17.56	-6.56E-04	-17.56	8.08	206.45	-187.68
1111	0111	1	-238.5	-241.42	-23.62	-6.31E-04	-23.62	8.91	262.35	-238.5
1111	1111	1	-260.61	-260.99	-27.91	-6.23E-04	-27.91	9.66	286.68	-260.68

Circuit 3 SPD3L 1-Bit

A	B	Ci	<i>Nano Sim (u)</i>							
			Avg S C	Avg C C	Avg W C	Avg SWC	Avg DWC	WC %	Avg Blk Pwr	Av Vdd
0	0	0	-49.94	-50.63	-4.24	-2.59E-04	-4.24	7.72	54.94	-49.94
0	0	1	-60.69	-58.36	-7.68	-2.40E-04	-7.68	11.63	66.75	-60.69
0	1	0	-64.47	-62.5	-8.08	-2.51E-04	-8.08	11.45	70.92	-64.47
0	1	1	-46.93	-48.92	-3.83	-2.32E-04	-3.83	7.27	51.62	-46.93
1	0	0	-62.84	-60.74	-7.42	-2.51E-04	-7.42	10.89	69.13	-62.84
1	0	1	-46.32	-47.58	-3.76	-2.32E-04	-3.76	7.334	50.95	-46.32
1	1	0	-50.5	-51.21	-3.91	-2.43E-04	-3.91	7.1	55.56	-50.5
1	1	1	-69.75	-66.53	-8.97	-2.44E-04	-8.97	11.88	76.735	-69.75

Circuit 3 SPD3L 4-Bit

A	B	Ci	<i>Nano Sim (u)</i>							
			Avg S C	Avg C C	Avg W C	Avg SWC	Avg DWC	WC %	Avg Blk Pwr	Av Vdd
0001	0101	0	-208.74	-206.26	-22.2	-8.49E-04	-22.2	9.71	229.61	-209.74
1010	0011	1	-225.73	-221.05	-116	-8.29E-04	-25.9	10.49	248.31	-225.73
0000	1111	1	-174.33	-180.95	-15.94	-8.29E-04	-15.94	8.1	191.76	-174.33
1111	0111	1	-244.73	-239.166	-27.24	-8.05E-04	-27.24	10.22	269.2	-244.73
1111	1111	1	-268.34	-259.73	-21.012	-7.97E-04	-31.01	10.66	295.28	-268.44

Delay Results

Circuit 1 D3L 1-Bit

A	B	Ci	Evaluation Delay(p)			Precharge Delay		
			PC->Co	PC->Co_b	PC->S	PC->Co	PC->Co_b	PC->S
0	0	0	-	36.947	-	-	39.436	-
0	0	1	-	47.435	52.045	-	39.19	36.171
0	1	0	-	46.104	51.362	-	37.295	39.918
0	1	1	47.582	-	-	32.863	-	-
1	0	0	-	51.952	44.837	-	37.927	34.091
1	0	1	41.35	-	-	32.346	-	-
1	1	0	42.79	-	-	35.137	-	-
1	1	1	32.912	-	43.307	37.145	-	34.556

Circuit 1 D3L 4-Bit

A	B	Ci	Evaluation Delay(<i>p</i>)							PreCharge Delay(<i>p</i>)						
			PC-> Co	PC-> Co_b	PC-> S3	PC-> S2	PC-> S1	PC-> S0	PC-> Co	PC-> Co_b	PC-> S3	PC-> S2	PC-> S1	PC-> S0		
0001	0101	0	-	47.064	-	76.347	71.732	-	-	40.045	-	42.249	41.764	-		
1010	0011	1	-	76.533	71.249	72.059	72.231	-	-	39.457	39.946	41.68	40.119	-		
0000	1111	1	136.64	-	-	-	-	-	38.967	-	-	-	-	-	-	-
1111	0111	1	66.146	-	-	64.342	56.13	43.129	38.01	-	-	40.338	40.339	40.341		
1111	1111	1	43.227	-	66.696	64.454	56.259	43.157	41.225	-	40.212	40.214	40.216	40.222		

Circuit 1 SPD3L 1-Bit

A	B	Ci	Evaluation Delay(<i>p</i>)				Precharge Delay(<i>p</i>)			
			PC->Co	PC->Co_b	PC->S	PC->Co	PC->Co_b	PC->S		
0	0	0	-	36.976	-	-	36.374	-		
0	0	1	-	46.929	47.088	-	35.638	37.089		
0	1	0	-	45.908	45.903	-	35.799	37.635		
0	1	1	41.028	-	-	31.897	-	-		
1	0	0	-	45.201	44.181	-	35.787	31.582		
1	0	1	41.102	-	-	30.936	-	-		
1	1	0	42.246	-	-	31.486	-	-		
1	1	1	33.253	-	40.963	34.646	-	33.663		

Circuit 1 SPD3L 4-Bit

A	B	Ci	Evaluation Delay(<i>p</i>)							PreCharge Delay(<i>p</i>)						
			PC->Co	PC->Co_b	PC->S3	PC->S2	PC->S1	PC->S0	PC->Co	PC->Co_b	PC->S3	PC->S2	PC->S1	PC->S0		
0001	0101	0	-	46.137	-	74.215	69.638	-	-	38.187	-	38.972	38.957	-		
1010	0011	1	-	71.115	71.783	69.64	66.382	-	-	36.621	37.067	39.013	38.01	-		
0000	1111	1	115.92	-	-	-	-	-	35.966	-	-	-	-	-	-	-
1111	0111	1	69.6	-	-	66.511	57.877	40.779	36.449	-	-	38.061	38.059	38.07		
1111	1111	1	42.335	-	67.537	66.516	57.887	40.787	38.948	-	38.009	38.006	38.007	38.011		

Circuit 2 D3L 1-Bit

A	B	Ci	Evaluation Delay(<i>p</i>)				Precharge Delay			
			PC->Co	PC->Co_b	PC->S	PC->Co	PC->Co_b	PC->S		
0	0	0	-	54.405	-	-	54.045	-		
0	0	1	-	74.995	84.593	-	54.156	62.711		
0	1	0	-	77.499	82.13	-	55.784	62.291		
0	1	1	81.681	-	-	62.131	-	-		
1	0	0	-	61.643	70.525	-	49.942	59.285		
1	0	1	70.117	-	-	59.172	-	-		
1	1	0	73.477	-	-	56.891	-	-		
1	1	1	73.363	-	73.292	57.737	-	61.472		

Circuit 2 D3L 4-Bit

A	B	Ci	Evaluation Delay(p)							PreCharge Delay(p)						
			PC-> Co	PC-> Co_b	PC-> S3	PC-> S2	PC-> S1	PC-> S0	PC-> Co	PC-> Co_b	PC-> S3	PC-> S2	PC-> S1	PC-> S0		
0001	0101	0	-	74.507	-	93.064	97.965	-	-	53.976	-	62.619	62.307	-		
1010	0011	1	-	91.711	93.552	98.106	106.68	-	-	45.878	59.438	62.213	60.816	-		
0000	1111	1	137.66	-	-	-	-	-	62.234	-	-	-	-	-		
1111	0111	1	92.534	-	-	98.795	98.585	-	59.047	-	-	60.84	60.842			
1111	1111	1	74.073	-	98.384	98.4	98.197	73.385	57.321	-	61.013	61.011	61.01	61.215		

Circuit 2 SPD3L 1-Bit

A	B	Ci	Evaluation Delay(p)				Precharge Delay									
			PC->Co	PC->Co_b	PC->S	PC->Co	PC->Co_b	PC->S								
0	0	0	-	55.693	-	-	-	51.518	-							
0	0	1	-	68.141	71.053	-	-	51.63	55.818							
0	1	0	-	69.054	71.467	-	-	52.378	55.623							
0	1	1	71.499	-	-	56.001	-	-								
1	0	0	-	62.235	71.263	-	-	45.739	56.861							
1	0	1	71.174	-	-	57.136	-	-								
1	1	0	60.47	-	-	50.646	-	-								
1	1	1	60.712	-	71.263	50.512	-	-	56.861							

Circuit 2 SPD3L 4-Bit

A	B	Ci	Evaluation Delay(p)							PreCharge Delay(p)						
			PC-> Co	PC-> Co_b	PC-> S3	PC-> S2	PC-> S1	PC-> S0	PC-> Co	PC-> Co_b	PC-> S3	PC-> S2	PC-> S1	PC-> S0		
0001	0101	0	-	64.801	-	86.967	81.005	-	-	51.554	-	55.731	55.561	-		
1010	0011	1	-	81.667	87.073	81.029	92.373	-	-	45.678	56.919	55.469	55.047	-		
0000	1111	1	142.17	-	-	-	-	-	55.838	-	-	-	-	-		
1111	0111	1	83.016	-	-	80.954	80.953	64.397	56.92	-	-	55.113	55.113	55.36		
1111	1111	1	60.703	-	81.391	81.391	81.391	64.57	50.717	-	55.336	55.336	55.336	55.583		

Circuit 3 D3L 1-Bit

A	B	Ci	Evaluation Delay(<i>p</i>)			Precharge Delay		
			PC->Co	PC->Co_b	PC->S	PC->Co	PC->Co_b	PC->S
0	0	0	-	36.23	-	-	38.471	-
0	0	1	-	46.439	81.557	-	39.46	59.272
0	1	0	-	44.739	70.77	-	37.192	56.994
0	1	1	47.826	-	-	39.475	-	-
1	0	0	-	52.353	81.557	-	38.862	59.272
1	0	1	42.383	-	-	39.742	-	-
1	1	0	43.936	-	-	41.464	-	-
1	1	1	33.446	-	49.507	42.647	-	42.996

Circuit 3 D3L 4-Bit

A	B	Ci	Evaluation Delay(<i>p</i>)						PreCharge Delay(<i>p</i>)					
			PC-> Co	PC-> Co_b	PC-> S3	PC-> S2	PC-> S1	PC-> S0	PC-> Co	PC-> Co_b	PC-> S3	PC-> S2	PC-> S1	PC-> S0
0001	0101	0	-	46.55	-	92.992	70.095	-	-	38.41	-	54.305	56.095	-
1010	0011	1	-	76.273	105.19	70.021	76.096	-	-	38.766	59.653	56.083	42.931	-
0000	1111	1	135.44	-	-	-	-	-	39.409	-	-	-	-	-
1111	0111	1	66.411	-	-	69.086	61.047	49.546	39.739	-	-	43.11	43.128	43.141
1111	1111	1	43.995	-	71.895	69.023	61.21	49.567	42.623	-	43.015	43.061	43.064	43.081

Circuit 3 SPD3L 1-Bit

A	B	Ci	Evaluation Delay(<i>p</i>)			Precharge Delay		
			PC->Co	PC->Co_b	PC->S	PC->Co	PC->Co_b	PC->S
0	0	0	-	35.209	-	-	35.187	-
0	0	1	-	45.182	76.622	-	35.87	56.075
0	1	0	-	44.376	73.957	-	35.514	55.937
0	1	1	41.02	-	-	36.326	-	-
1	0	0	-	43.867	72.362	-	34.03	54.62
1	0	1	42.107	-	-	38.037	-	-
1	1	0	42.671	-	-	38.197	-	-
1	1	1	33.758	-	41.823	39.064	-	39.664

Circuit 3 SPD3L 4-Bit

A	B	Ci	Evaluation Delay(p)							PreCharge Delay(p)						
			PC-> Co	PC-> Co_b	PC-> S3	PC-> S2	PC-> S1	PC-> S0	PC-> Co	PC-> Co_b	PC-> S3	PC-> S2	PC-> S1	PC-> S0		
0001	0101	0	-	45.283	-	97.921	72.591	-	-	36.307	-	53.567	53.535	-		
1010	0011	1	-	69.119	97.749	72.255	65.313	-	-	34.01	54.66	53.61	39.634	-		
0000	1111	1	114.29	-	-	-	-	-	36.306	-	-	-	-	-	-	-
1111	0111	1	70.007	-	-	66.276	57.472	41.812	38.099	-	-	39.619	39.622	39.631		
1111	1111	1	43.384	-	67.528	66.155	57.519	41.813	39.817	-	39.737	39.739	39.738	39.749		