Jeff Grindel

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Objective: To obtain a full time electrical engineering position. I will be a valued team member through my education and experience in digital circuit design, computer architecture design, and HDL programming. I will also bring excellent communication skills, hard work, and self-motivation to projects that I work on.

Education:

Master of Science in Electrical Engineering GPA: 4.0/4.0 • Graduation Date : May 2014

Illinois Institute of Technology , Chicago, IL

- Advanced VLSI Design
- Fault Detection in Digital Circuits
- Advanced Computer Architecture
- CAD Techniques for VLSI Design

Bachelor of Science in Electrical Engineering GPA: 3.8/4.0 • Graduation Date: May 2014

Illinois Institute of Technology, Chicago, IL

- Advanced Logic Design
- Microcomputers

Work Experience:

BAE Systems • Electronic Hardware Intern Manassas, VA [May 2013 – Present]

- Designed Verilog sync pulse generator logic and negative sync pulse generator logic for divide by 1, 2, 3 and 4
- Coded test bench for sync pulse generators in VHDL and verified functionality in Questa
- Reverse engineered an AC scan engine and designed and coded a testbench for functional and regression testing

Bechtel OG&C • Electrical Engineering Intern Houston, TX [June 2012 – August 2012]

- Designed and developed a full layout of an electrical substation including equipment sizing, rating, and layout to meet NEC codes and standards
- Modeled a power system utilizing ETAP and performed power flow, short-circuit, and motor acceleration studies

Bechtel National • Electrical Engineering Intern Richland, WA [May 2011 – August 2011]

- Developed systematic procedure to verify and modify lighting circuit loads utilizing Excel
- Incorporated field engineering sketches of as-built embedded conduit into section cut drawings

Class Projects:

Design and Synthesis of Multi-Operand Adders Chicago, IL [December 2012]

- VLSI design including datapath circuit design, standard cell based design flow, and design validation and verification through construction of fast-multi-operand adder architectures in Verilog
- Utilized commercial EDA tools and software from Synopsys, Cadence Design Systems and Mentor Graphics to perform design, synthesis, power analysis, and timing analysis

Design and Implementation of a MIPS CPU Chicago, IL [December 2012]

- Developed, designed, and implemented a custom 32-bit MIPS processor based on a custom instruction set utilizing VHDL for programming, and ModelSim for testing
- Created multiple test benches to ensure and verify proper operation of the processor

Technical Skills:

Programming:

- VHDL, Verilog, Assembly
- Java, C/C++
- HTML, CSS

Applications:

- Cadence Virtuoso, DRV, Synopsys ICC
- Questa, ModelSim, HSPICE, Calibre DRC/LVS
- Eclipse, Microsoft Visual C++ 2010

Organizations:

- Eta Kappa Nu, President
- BSA, Eagle Scout
- IEEE
- Tau Beta Pi