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|  | |  | |  | | **Jeff Grindel** | | | | | | | | | |  |  |  | | |
| 4710 N. Racine Apt. 2W, Chicago, IL 60640 • (509) 554-1593 • [jeff.grindel@gmail.com](mailto:jeff.grindel@gmail.com) • [jeffgrindel.com](http://jeffgrindel.com/?utm_source=Website&utm_medium=jeffgrindel.com&utm_campaign=Website) | | | | | | | | | | | | | | | | | | | | |
|  |  | | |  | |  | |  | | |  | | | |  |  |  |  | | |
| Objective: | To obtain a full time electrical engineering position. I will be a valued team member through my education and experience in digital circuit design, computer architecture design, and HDL programming. I will also bring excellent communication skills, hard work, and self-motivation to projects that I work on. | | | | | | | | | | | | | | | | | | | |
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| Education: | **Master of Science in Electrical Engineering** | | | | | | | | | | | GPA: 4.0/4.0 • Graduation Date : May 2014 | | | | | | | | |
|  |  | | *Illinois Institute of Technology* , Chicago, IL | | | | | | | | | | | | | | | | | |
|  | | Advanced VLSI Design | | | | | | |  | | | Advanced Computer Architecture | | | | | |  | |
|  | | Fault Detection in Digital Circuits | | | | | | |  | | | CAD Techniques for VLSI Design | | | | | |  | |
|  |  | |  | | | | | | |  | | |  | | | | | |  | |
|  | **Bachelor of Science in Electrical Engineering** | | | | | | | | | | | GPA: 3.8/4.0 • Graduation Date: May 2014 | | | | | | | | |
|  |  | | *Illinois Institute of Technology*, Chicago, IL | | | | | | | | | | | | | | | | | |
|  |  | | Advanced Logic Design | | | | | | |  | | | Microcomputers | | | | |  | | |
|  |  | |  | | | | | | |  | | |  | | | | |  | | |
| Work | **BAE Systems** • **Electronic Hardware Intern** | | | | | | | | | | | | | Manassas, VA [May 2013 – Present] | | | | | | |
| Experience: |  | | Designed Verilog sync pulse generator logic and negative sync pulse generator logic for divide by 1, 2, 3 and 4 | | | | | | | | | | | | | | | | | |
|  |  | | Coded test bench for sync pulse generators in VHDL and verified functionality in Questa | | | | | | | | | | | | | | | | | |
|  |  | | Reverse engineered an AC scan engine and designed and coded a testbench for functional and regression testing | | | | | | | | | | | | | | | | | |
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|  | **Bechtel OG&C** • **Electrical Engineering Intern** | | | | | | | | | | | | | Houston, TX [June 2012 – August 2012] | | | | | | |
|  |  | | Designed and developed a full layout of an electrical substation including equipment sizing, rating, and layout to meet NEC codes and standards | | | | | | | | | | | | | | | | | |
|  |  | | Modeled a power system utilizing ETAP and performed power flow, short-circuit, and motor acceleration studies | | | | | | | | | | | | | | | | | |
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|  | **Bechtel National** • **Electrical Engineering Intern** | | | | | | | | | | | | | Richland, WA [May 2011 – August 2011] | | | | | | |
|  |  | | Developed systematic procedure to verify and modify lighting circuit loads utilizing Excel | | | | | | | | | | | | | | | | | |
|  |  | | Incorporated field engineering sketches of as-built embedded conduit into section cut drawings | | | | | | | | | | | | | | | | | |
|  |  | |  | | |  | |  | | |  | | |  | |  |  |  | | |
| Class | **Design and Synthesis of Multi-Operand Adders** | | | | | | | | | | | | | Chicago, IL [December 2012] | | | | | | |
| Projects: |  | | VLSI design including datapath circuit design, standard cell based design flow, and design validation and verification through construction of fast-multi-operand adder architectures in Verilog | | | | | | | | | | | | | | | | | |
|  |  | | Utilized commercial EDA tools and software from Synopsys, Cadence Design Systems and Mentor Graphics to perform design, synthesis, power analysis, and timing analysis | | | | | | | | | | | | | | | | | |
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|  | **Design and Implementation of a MIPS CPU** | | | | | | | | | | | | | Chicago, IL [December 2012] | | | | | | |
|  |  | | Developed, designed, and implemented a custom 32-bit MIPS processor based on a custom instruction set utilizing VHDL for programming, and ModelSim for testing | | | | | | | | | | | | | | | | | |
|  |  | | Created multiple test benches to ensure and verify proper operation of the processor | | | | | | | | | | | | | | | | | |
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| Technical | **Programming:** | | | |  | | | **Applications:** | | | | | | | |  |  |  | | |
| Skills: |  | | VHDL, Verilog, Assembly | | | | |  | Cadence Virtuoso, DRV, Synopsys ICC | | | | | | | | | | |  |
|  |  | | Java, C/C++ | | | | |  | Questa, ModelSim, HSPICE, Calibre DRC/LVS | | | | | | | | | | |  |
|  |  | | HTML, CSS | | | | |  | Eclipse, Microsoft Visual C++ 2010 | | | | | | | | | | |  |
|  | | | | | | | | | | | | | | | | | | | |  |
| Organizations: |  | | Eta Kappa Nu, President | | | | |  | IEEE | | | | | | | | | | |  |
|  |  | | BSA, Eagle Scout | | | |  |  | Tau Beta Pi | | | | | | | | | | |  |