Self-paced : 電子所 碩一 r09943113 董濟昀

Fp_accum

1. Introduction

2. Csim / syn / co-sim

Csim：

hls_fp_accumulator_csim.log

```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../../fp_accum.cpp in debug mode
   Generating csim.exe

3670058.0000    3670058.5000    00000.5000
TEST OK!
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************

```

Syn：

Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	2.50 ns	3.359 ns	0.31 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
245	245	0.823 us	0.823 us	64	64	function

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	4	-
FIFO	-	-	-	-	-
Instance	-	4	788	486	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	1573	-
Register	-	-	3844	-	-
Total	0	4	4632	2063	0
Available	890	840	407600	203800	0
Utilization (%)	0	~0	1	1	0

Interface

Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_clk	in	1	ap_ctrl_hs	hls_fp_accumulator	return value
ap_rst	in	1	ap_ctrl_hs	hls_fp_accumulator	return value
ap_start	in	1	ap_ctrl_hs	hls_fp_accumulator	return value
ap_done	out	1	ap_ctrl_hs	hls_fp_accumulator	return value
ap_idle	out	1	ap_ctrl_hs	hls_fp_accumulator	return value
ap_ready	out	1	ap_ctrl_hs	hls_fp_accumulator	return value
ap_return	out	32	ap_ctrl_hs	hls_fp_accumulator	return value
window0_address0	out	7	ap_memory	window0	array
window0_ce0	out	1	ap_memory	window0	array
window0_q0	in	32	ap_memory	window0	array
window0_address1	out	7	ap_memory	window0	array
window0_ce1	out	1	ap_memory	window0	array
window0_q1	in	32	ap_memory	window0	array

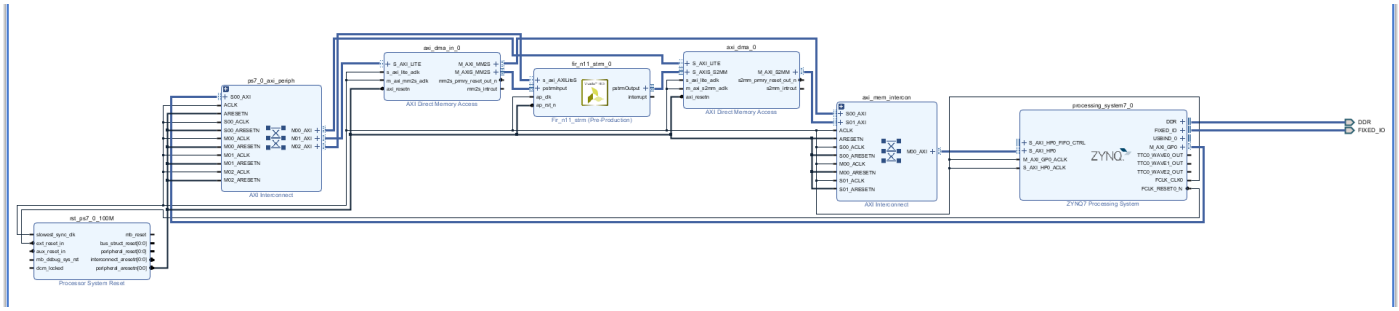
Co-sim：

cosim.log

```
INFO: [COSIM-47] Using XSIM for RTL simulation.
INFO: [COSIM-14] Instrumenting C test bench ...
   Build using "C:/Xilinx/Vivado/2019.2/tps/win64/msys64/mingw64/bin/g++"
   Compiling apatb_hls_fp_accumulator.cpp
   Compiling fp_accum.cpp_pre.cpp.tb.cpp
   Generating cosim.tv.exe
INFO: [COSIM-302] Starting C TB testing ...
INFO: [COSIM-333] Generating C post check test bench ...
INFO: [COSIM-12] Generating RTL test bench ...
INFO: [COSIM-1] *** C/RTL co-simulation file generation completed. ***
INFO: [COSIM-323] Starting verilog simulation.
INFO: [COSIM-15] Starting XSIM ...

```

3. Implement



4. Optimize
5. Github

   https://github.com/jeff-tong/MSOC---Application-Acceleration-with-High-Level-Synthesis-
6. Reference