

# Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:2/4/2021

Name: OP Joy Jefferson	SRN:PES2UG19CS270	Section:E
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Week# \_\_\_\_9\_\_\_\_

Program Number: \_\_\_\_1\_\_\_\_

Consider a direct mapped cache of size 16 bytes with block size 4 bytes. The size of main memory is 256 bytes. Find Number of bits in tag, index and offset. The processor generates requests as follows

1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11.

Find hit rate and miss rate.

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

ParaCache

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2) 16

Memory Size (power of 2) 256

Offset Bits 2

DIRECT MAPPED CACHE

Instruction Breakdown

TAG	INDEX	OFFSET
4 bit	2 bit	2 bit

Memory Block

B.1.W.0	B.1.W.1	B.1.W.2	B.1.W.3
B.2.W.0	B.2.W.1	B.2.W.2	B.2.W.3
B.3.W.0	B.3.W.1	B.3.W.2	B.3.W.3
B.4.W.0	B.4.W.1	B.4.W.2	B.4.W.3
B.5.W.0	B.5.W.1	B.5.W.2	B.5.W.3

b) Screenshot showing the Cache Table

NTU Direct Mapped Cache Simulator

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2) 16

Memory Size (power of 2) 256

Offset Bits 2

Reset Submit

Instruction

Load (in hex) #

List of next 10 Instructions

Run Simulation Submit

### DIRECT MAPPED CACHE

#### Instruction Breakdown

0001	00	01
4 bit	2 bit	2 bit

#### Memory Block

B. 4 W. 0	B. 4 W. 1	B. 4 W. 2	B. 4 W. 3
B. 5 W. 0	B. 5 W. 1	B. 5 W. 2	B. 5 W. 3
B. 6 W. 0	B. 6 W. 1	B. 6 W. 2	B. 6 W. 3
B. 7 W. 0	B. 7 W. 1	B. 7 W. 2	B. 7 W. 3
B. 8 W. 0	B. 8 W. 1	B. 8 W. 2	B. 8 W. 3
B. 9 W. 0	B. 9 W. 1	B. 9 W. 2	B. 9 W. 3

#### Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0001	BLOCK 4 WORD 0 - 3	0
1	1	0000	BLOCK 1 WORD 0 - 3	0
2	1	0000	BLOCK 2 WORD 0 - 3	0
3	0	-	0	0

c) Screenshot showing hit and miss rates

### Statistics

Hit Rate : 38%

Miss Rate : 63%

#### List of Previous Instructions :

- Load 1 [Miss]
- Load 4 [Miss]
- Load 8 [Miss]
- Load 5 [Hit]
- Load 14 [Miss]
- Load 11 [Miss]
- Load 13 [Hit]
- Load 38 [Miss]
- Load 9 [Miss]
- Load 8 [Hit]
- Load 4 [Miss]
- Load 28 [Miss]
- Load 5 [Hit]
- Load 6 [Hit]
- Load 9 [Miss]
- Load 11 [Hit]

# Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:2/2/2021

Name: OP JOY JEFFERSON	SRN:PES2UG19CS270	Section:E
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Week# \_\_\_\_9\_\_\_\_

Program Number: \_\_\_\_2\_\_\_\_

Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Randomly generate 10 addresses and find hit rate and miss rate.

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

ParaCache

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2) 16384

Memory Size (power of 2) 131072

Offset Bits 8

**DIRECT MAPPED CACHE**

Instruction Breakdown

TAG	INDEX	OFFSET
3 bit	6 bit	8 bit

Memory Block

B.0W.0	B.0W.1	B.0W.2	B.0W.3	B.0W.4	B.0W.5	B.0W.6	B.0W.7	B.0W.8	B.0W.9
B.1W.0	B.1W.1	B.1W.2	B.1W.3	B.1W.4	B.1W.5	B.1W.6	B.1W.7	B.1W.8	B.1W.9
B.2W.0	B.2W.1	B.2W.2	B.2W.3	B.2W.4	B.2W.5	B.2W.6	B.2W.7	B.2W.8	B.2W.9
B.3W.0	B.3W.1	B.3W.2	B.3W.3	B.3W.4	B.3W.5	B.3W.6	B.3W.7	B.3W.8	B.3W.9

b) Screenshot showing the Cache Table

Index	Value	Tag	Data
0	0	0	Miss
1	0	0	Miss
2	0	0	Miss
3	0	0	Miss
4	0	0	Miss
5	0	0	Miss
6	0	0	Miss
7	0	0	Miss
8	0	0	Miss
9	0	0	Miss
10	0	0	Miss
11	0	0	Miss
12	0	0	Miss
13	0	0	Miss
14	0	0	Miss
15	0	0	Miss
16	0	0	Miss
17	0	0	Miss
18	0	0	Miss
19	0	0	Miss
20	0	0	Miss
21	0	0	Miss
22	0	0	Miss
23	0	0	Miss
24	0	0	Miss
25	0	0	Miss
26	0	0	Miss
27	0	0	Miss
28	0	0	Miss
29	0	0	Miss
30	0	0	Miss
31	0	0	Miss
32	0	0	Miss
33	0	0	Miss
34	0	0	Miss
35	0	0	Miss
36	0	0	Miss
37	0	0	Miss
38	0	0	Miss
39	0	0	Miss
40	0	0	Miss
41	0	0	Miss
42	0	0	Miss
43	0	0	Miss
44	0	0	Miss
45	0	0	Miss
46	0	0	Miss
47	0	0	Miss
48	0	0	Miss
49	0	0	Miss
50	0	0	Miss
51	0	0	Miss
52	0	0	Miss
53	0	0	Miss
54	0	0	Miss
55	0	0	Miss
56	0	0	Miss
57	0	0	Miss
58	0	0	Miss
59	0	0	Miss
60	0	0	Miss
61	0	0	Miss
62	0	0	Miss
63	0	0	Miss

c) Screenshot showing hit and miss rates

### Statistics

Hit Rate

:

0%

Miss Rate

:

100%

### List of Previous Instructions :

- Load 352C [Miss]
- Load 2EA3 [Miss]
- Load 1AC97 [Miss]
- Load B7C7 [Miss]
- Load E457 [Miss]
- Load C370 [Miss]
- Load EF13 [Miss]
- Load 48C3 [Miss]
- Load 6828 [Miss]
- Load 1626C [Miss]

# Microprocessor and Computer Architecture Laboratory

**UE19CS256**

**4th Semester, Academic Year 2020-21**

Date:2/3/2021

Name: OP JOY JEFFERSON	SRN:PES2UG19CS270	Section:E
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Week#   9  

Program Number:   3  

A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.

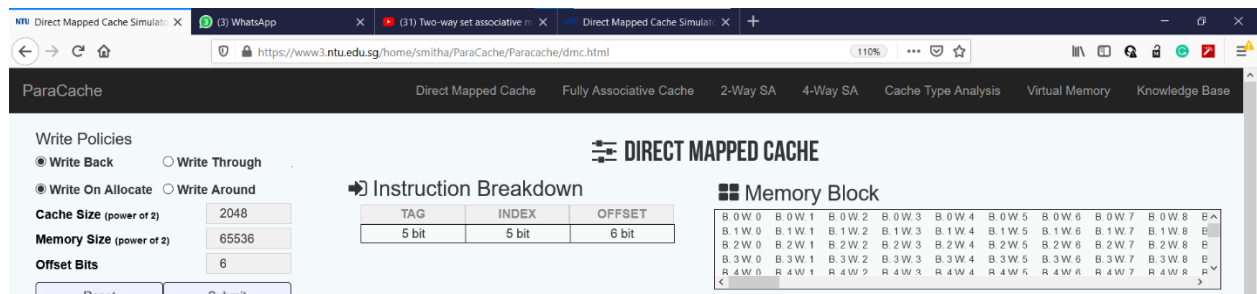
a) Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.

(b) When a program is executed, the processor reads data sequentially from the following word addresses:

1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11.

All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor



b) Screenshot showing the Cache Table

**Cache Table**

Index	Value	Tag	Data Index	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	1	00000	BLOCKED WORD 0 - 31	0
10	1	00001	BLOCKED WORD 0 - 31	0
11	0	00100	BLOCKED WORD 0 - 31	0
12	0	00101	BLOCKED WORD 0 - 31	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0

c) Screenshot showing hit and miss rates

**Statistics**

**Hit Rate : 56%**

**Miss Rate : 44%**

**List of Previous Instructions :**

- Load 1 [Miss]
- Load 4 [Miss]
- Load 8 [Miss]
- Load 5 [Hit]
- Load 14 [Miss]
- Load 11 [Miss]
- Load 13 [Hit]
- Load 38 [Miss]
- Load 9 [Hit]
- Load B [Hit]
- Load 4 [Hit]
- Load 2B [Miss]
- Load 5 [Hit]
- Load 6 [Hit]
- Load 9 [Hit]
- Load 11 [Hit]

# Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:2/3/2021

Name: OP JOY JEFFERSON	SRN:PES2UG19CS270	Section:E
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Week#\_\_\_9\_\_\_\_\_ Program Number: \_\_\_4\_\_

Consider a 2-way set associative cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Randomly generate 10 addresses and find hit rate and miss rate.

- a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

➡ Instruction Breakdown

TAG	INDEX	OFFSET
4 bit	5 bit	8 bit

- b) Screenshot showing the Cache Table

 Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	B. 0 W. 0 - 255	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0

c) Screenshot showing hit and miss rates



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**Statistics**

**Hit Rate : 94%**

**Miss Rate : 6%**

**List of Previous Instructions :**

- Load 1 [Miss]
- Load 4 [Hit]
- Load 8 [Hit]
- Load 5 [Hit]
- Load 14 [Hit]
- Load 11 [Hit]
- Load 13 [Hit]
- Load 38 [Hit]
- Load 9 [Hit]
- Load B [Hit]
- Load 4 [Hit]
- Load 2B [Hit]
- Load 5 [Hit]
- Load 6 [Hit]
- Load 9 [Hit]
- Load 11 [Hit]

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4th Semester, Academic Year 2020-21

Date:2/3/2021

Name: OP JOY JEFFERSON	SRN:PES2UG19CS270	Section:E
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Week# 9

Program Number: 5

Consider a main memory having 64 byte capacity and cache memory of 8 bytes initially empty .The following addresses are generated by the CPU. All values in hexadecimal. Clearly label data that is replaced in cache lines

Show the cache memory table and filled data in the cache lines of block size 1 byte. LRU Policy is used.

- Cache Address Table showing the splitup of the address fields for the requests generated by the processor
- Screenshot showing the Cache Table
- Screenshot showing hit and miss rates

The cache is mapped as

- Direct Mapped

### ➡ Instruction Breakdown

000	01	0
3 bit	2 bit	1 bit

### ☐ Memory Block

B. 1 W. 0	B. 1 W. 1
B. 2 W. 0	B. 2 W. 1
B. 3 W. 0	B. 3 W. 1
B. 4 W. 0	B. 4 W. 1
B. 5 W. 0	B. 5 W. 1
B. 6 W. 0	B. 6 W. 1

### ☐ Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	010	BLOCK 8 WORD 0 - 1	0
1	1	000	BLOCK 1 WORD 0 - 1	0
2	1	101	BLOCK 16 WORD 0 - 1	0
3	1	000	BLOCK 3 WORD 0 - 1	0

### Statistics

Hit Rate : 20%

Miss Rate : 80%

### List of Previous Instructions :

- Load B [Miss]
- Load 2F [Miss]
- Load 31 [Miss]
- Load F [Miss]
- Load A [Hit]
- Load 7 [Miss]
- Load 2C [Miss]
- Load 11 [Miss]
- Load B [Hit]
- Load 2 [Miss]

## b) Two way set Associative

### ☐ 2-WAY SET ASSOCIATIVE CACHE

### ➡ Instruction Breakdown

0000	1	0
4 bit	1 bit	1 bit

### ☐ Memory Block

B. 8 W. 0	B. 8 W. 1
B. 9 W. 0	B. 9 W. 1
B. A W. 0	B. A W. 1
B. B W. 0	B. B W. 1
B. C W. 0	B. C W. 1
B. D W. 0	B. D W. 1

### ☐ Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	4	BLOCK 8 WORD 0 - 1	0
1	1	1	BLOCK 3 WORD 0 - 1	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	b	BLOCK 16 WORD 0 - 1	0
1	1	2	BLOCK 5 WORD 0 - 1	0

**Statistics**

Hit Rate : 10%

Miss Rate : 90%

**List of Previous Instructions :**

- Load B [Miss]
- Load 2F [Miss]
- Load 31 [Miss]
- Load F [Miss]
- Load A [Miss]
- Load 7 [Miss]
- Load 2C [Miss]
- Load 11 [Miss]
- Load B [Hit]
- Load 2 [Miss]

### c) Four Way Set associative

**4-WAY SET ASSOCIATIVE CACHE**

**Instruction Breakdown**

00001	0	0
5 bit	0 bit	1 bit

**Memory Block**

B. 1 W. 0	B. 1 W. 1
B. 2 W. 0	B. 2 W. 1
B. 3 W. 0	B. 3 W. 1
B. 4 W. 0	B. 4 W. 1
B. 5 W. 0	B. 5 W. 1
B. 6 W. 0	B. 6 W. 1

**Cache Table**

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	5	B. 5 W. 0 - 1	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	B. 1 W. 0 - 1	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	16	B. 16 W. 0 - 1	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	8	B. 8 W. 0 - 1	0

**Statistics**

Hit Rate : 20%

Miss Rate : 80%

**List of Previous Instructions :**

- Load B [Miss]
- Load 2F [Miss]
- Load 31 [Miss]
- Load F [Miss]
- Load A [Hit]
- Load 7 [Miss]
- Load 2C [Miss]
- Load 11 [Miss]
- Load B [Hit]
- Load 2 [Miss]

### d) Fully Associative

## FULLY ASSOCIATIVE CACHE

### ➡ Instruction Breakdown

00001	0
5 bit	1 bit

### 🗄 Memory Block

B. 1 W. 0	B. 1 W. 1
B. 2 W. 0	B. 2 W. 1
B. 3 W. 0	B. 3 W. 1
B. 4 W. 0	B. 4 W. 1
B. 5 W. 0	B. 5 W. 1
B. 6 W. 0	B. 6 W. 1

### 🗃 Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	00001	BLOCK 1 WORD 0 - 1	0
1	1	10110	BLOCK 16 WORD 0 - 1	0
2	1	01000	BLOCK 8 WORD 0 - 1	0
3	1	00101	BLOCK 5 WORD 0 - 1	0

### Statistics

Hit Rate : 10%

Miss Rate : 90%

### List of Previous Instructions :

- Load B [Miss]
- Load 2F [Miss]
- Load 31 [Miss]
- Load F [Miss]
- Load A [Hit]
- Load 7 [Miss]
- Load 2C [Miss]
- Load 11 [Miss]
- Load B [Miss]
- Load 2 [Miss]

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### **Disclaimer:**

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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