Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:

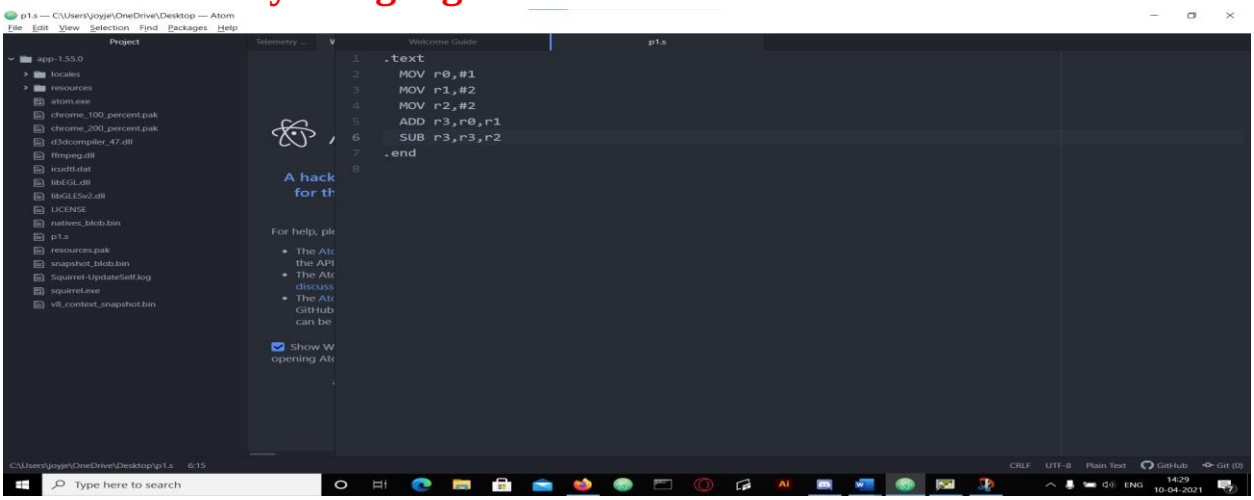
Name: OP JOY JEFFERSON	SRN:PES2UG19CS270	Section:E

Week#____10_____ Program Number: ____1__

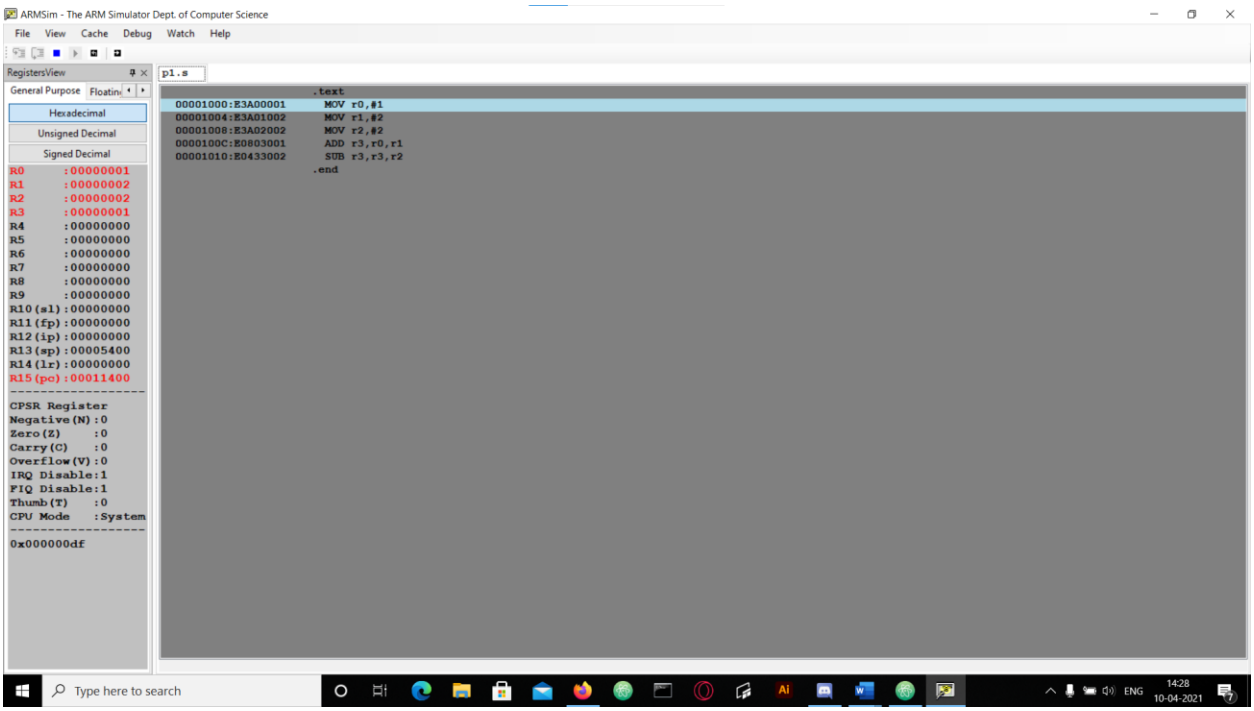
Given a C- Code convert it in its equivalent ARM Code.
These programs need to be executed on ARMSIM Simulator

1) x = (a + b) - c;

ARM Assembly Language Code

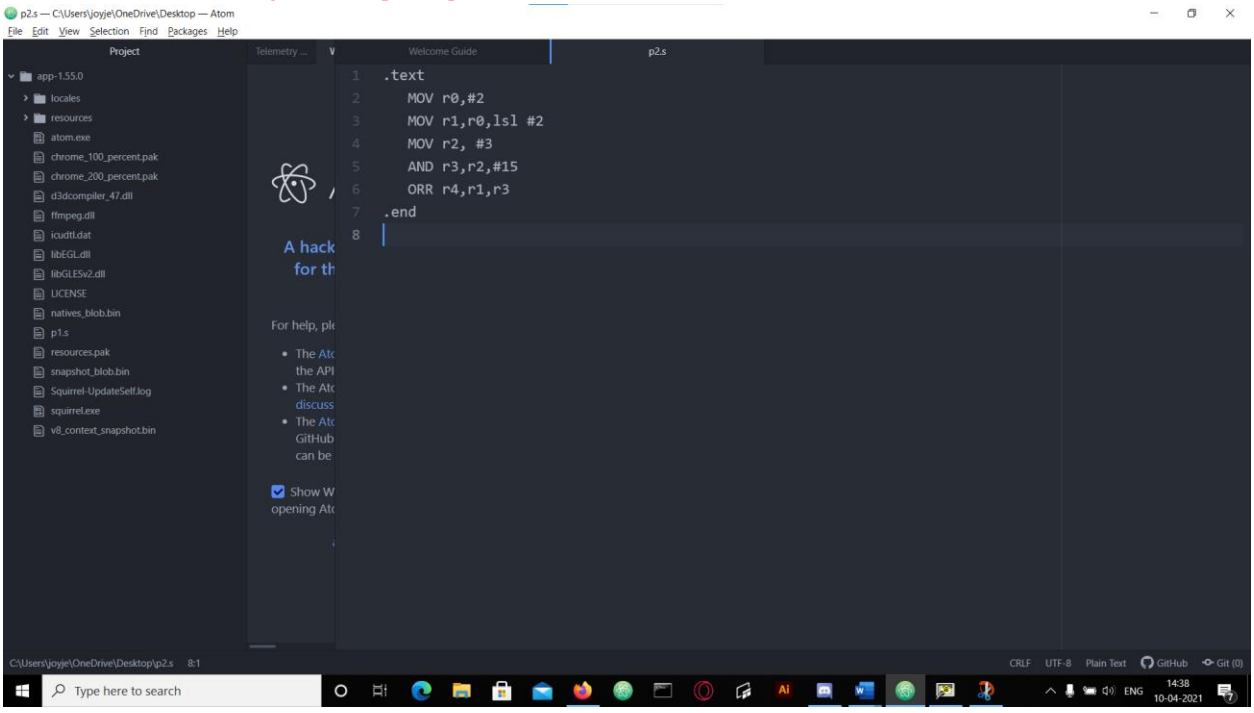


Screenshot showing the value of x, a, b, c in the register window.

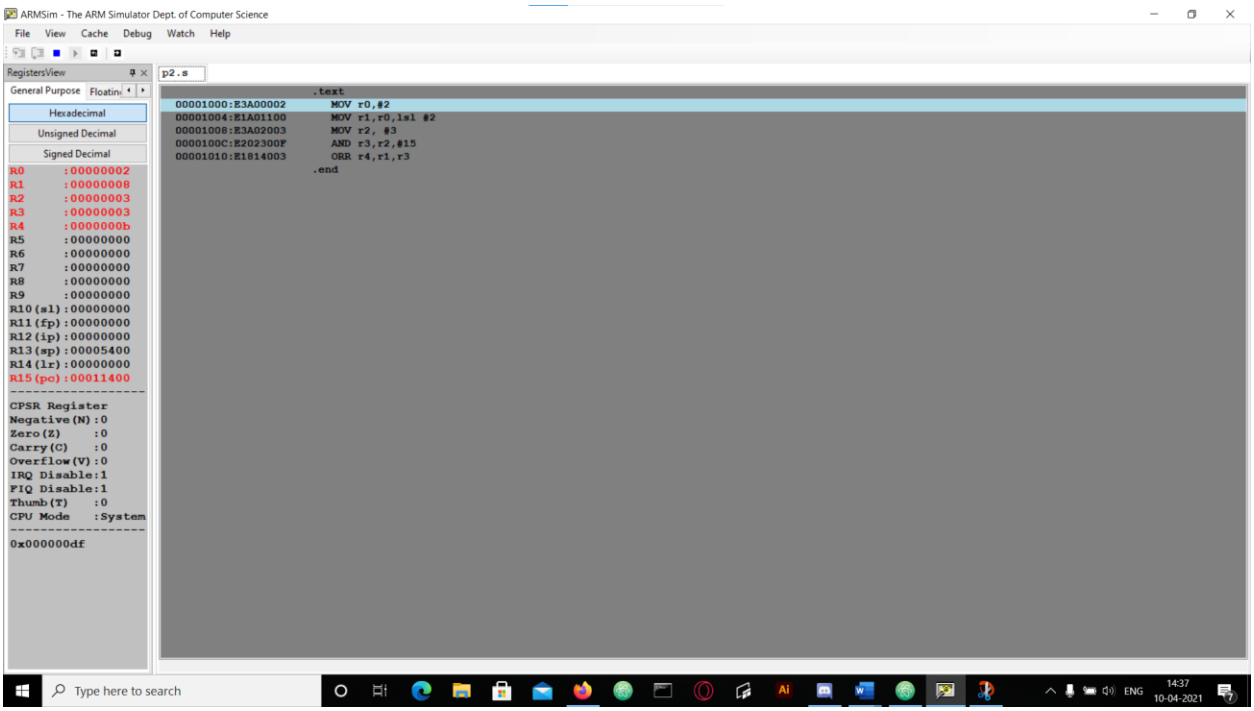


2) z = (a << 2) | (b & 15);

ARM Assembly Language Code



Screenshot showing the value of a, b, z in the register window.



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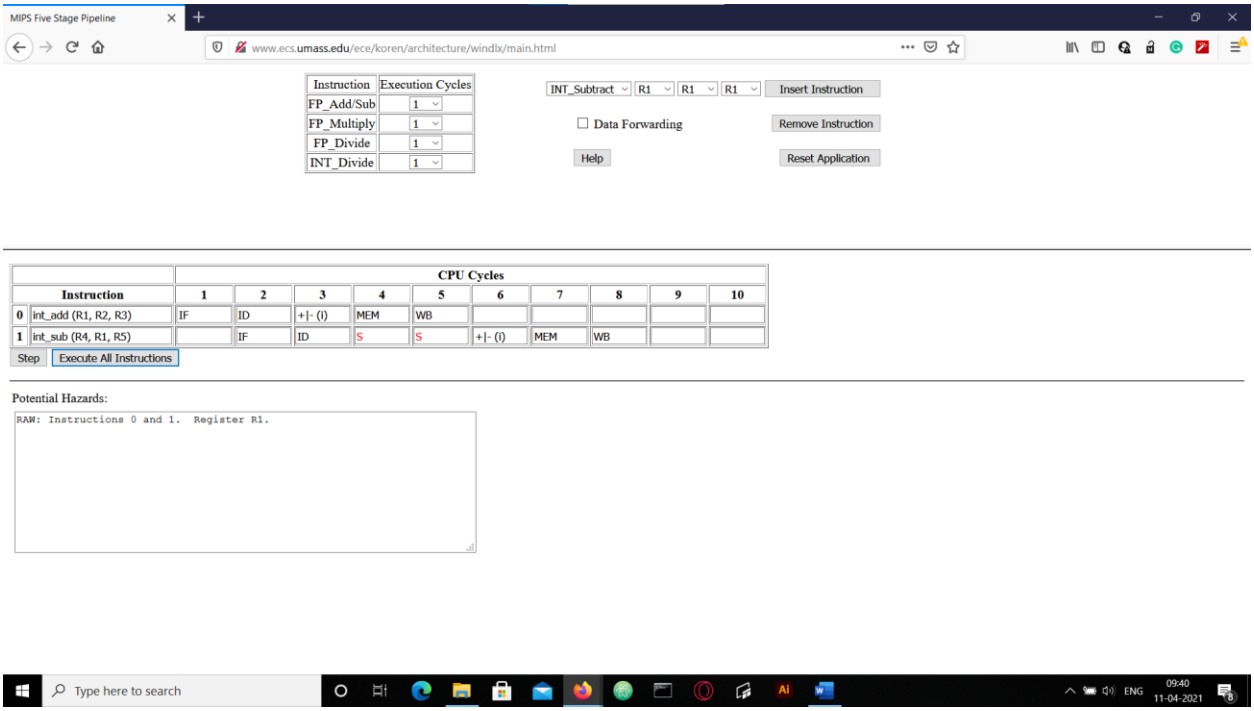
Week#____10_____ Program Number: ____2__

1) Consider the following instructions. Execute these instructions using simulator of 5 stage pipeline of MIPS architecture.

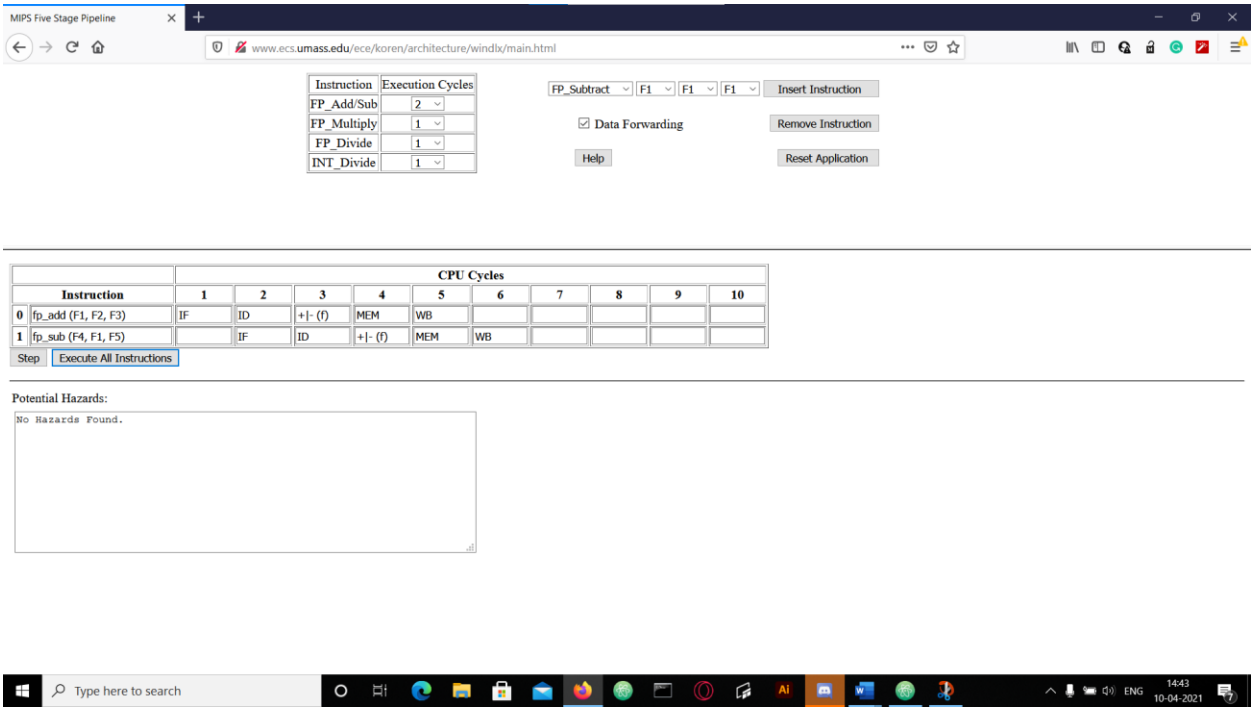
ADD R0, R1, R2
SUB R3, R0, R4.



Observe the following and note down the results.

a) Check whether there is data dependency for the second instruction?
   Yes, there is data dependency(RAW) for the second screenshot.
   Related Screenshot
   (inserted above).
b) If yes, then, how many stall states have been introduced?
   2 stalls
   Related Screenshot
   (inserted above).
c) If data forwarding is applied how many stall states have been reduced?
   Zero.

Related Screenshot



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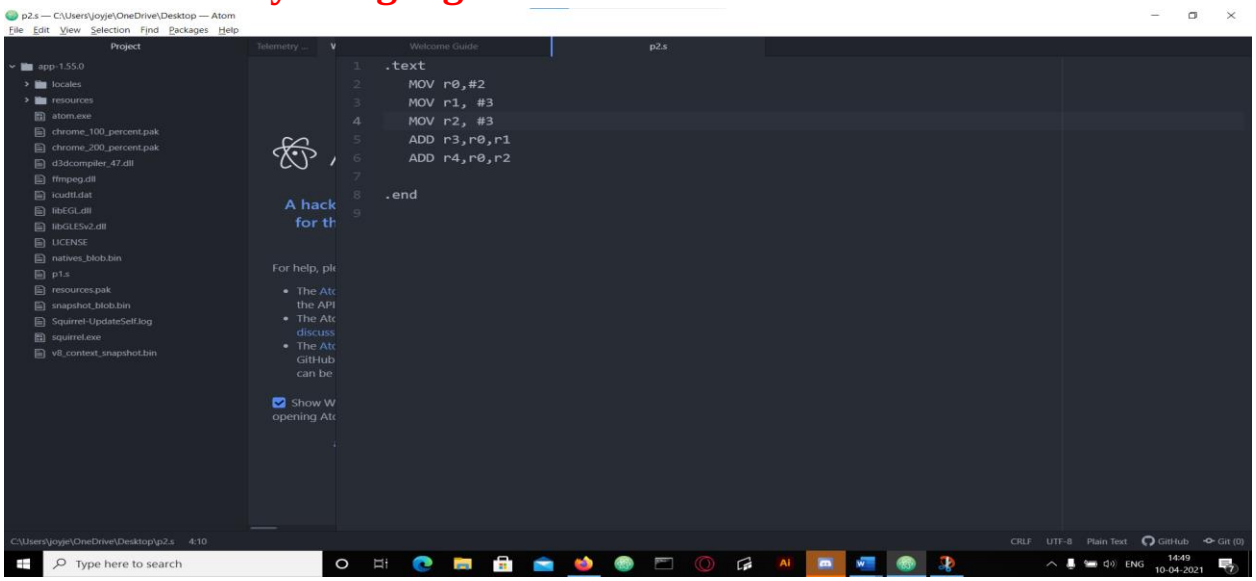
Week#____10_____ Program Number: ____3__

Consider the following code segment in C.

A = B + E;
C = B + F;

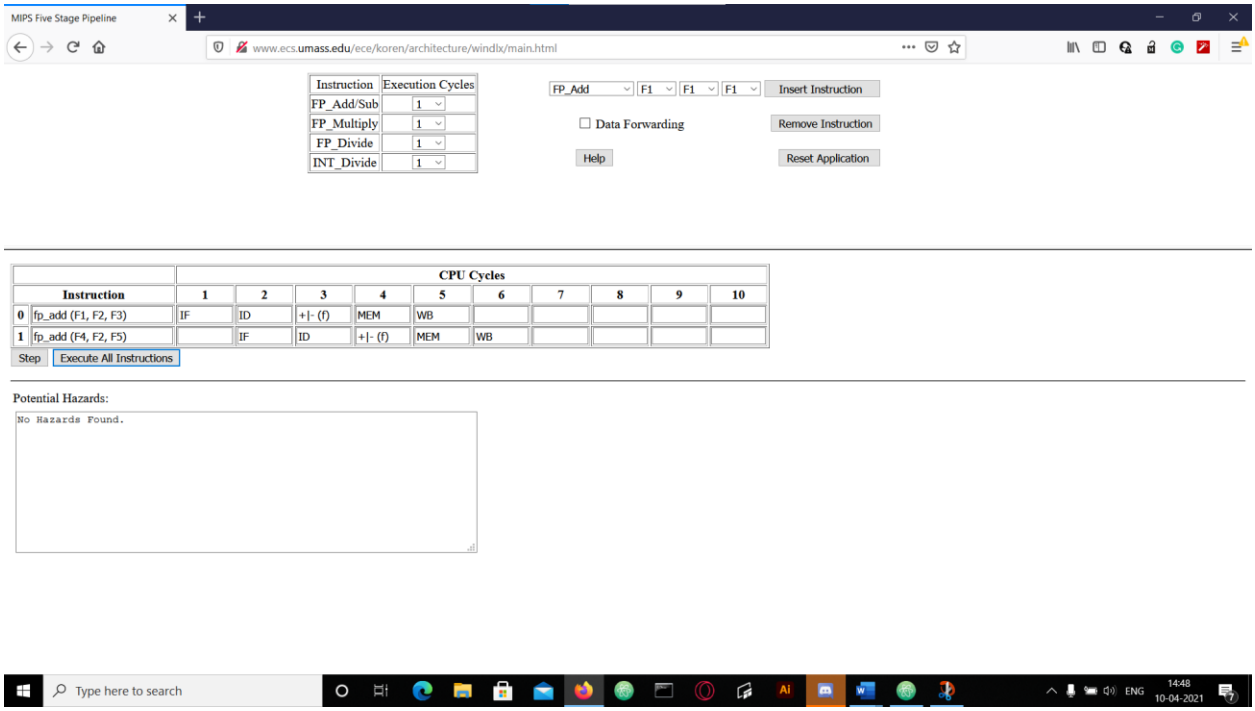
a) Write the code using MIPS 5 STAGE pipeline architecture.

ARM Assembly Language Code



b) Find the hazards;

Related Screenshot



c) Reorder the instructions to avoid pipeline stalls.

Related Screenshot

No reordering required.

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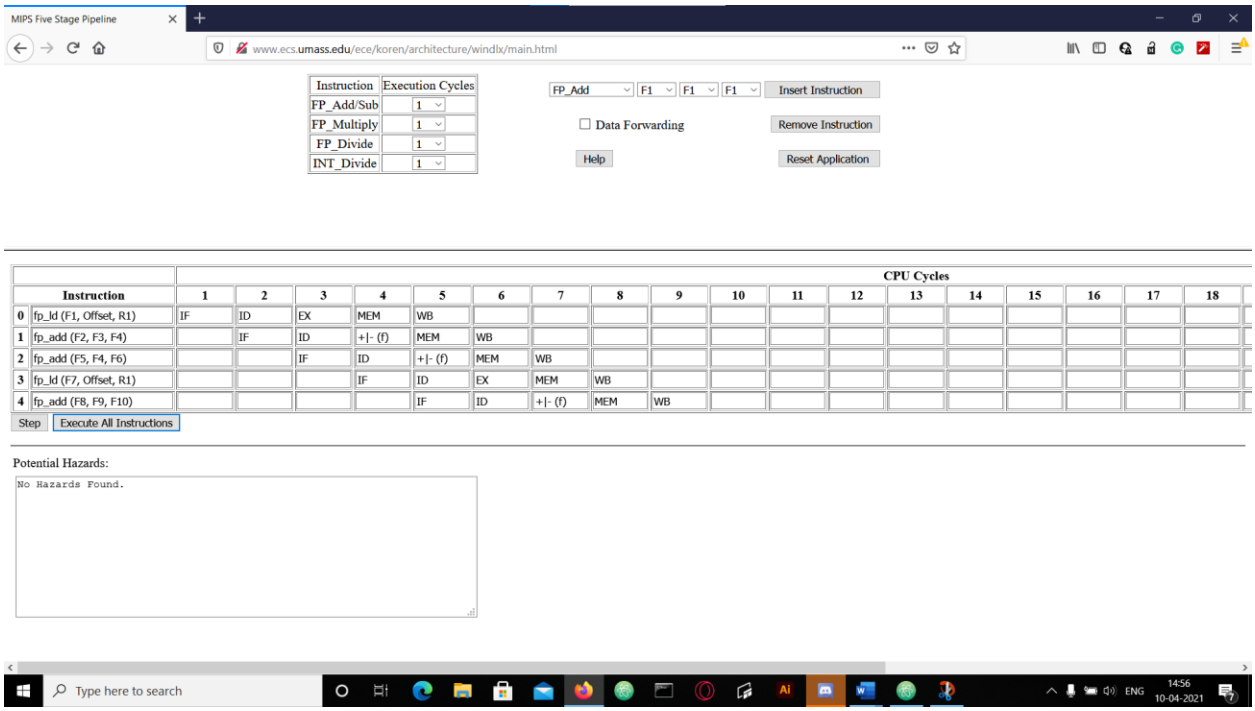
Week#____10_____ Program Number: ___4__

Using MIPS 5 stage pipeline architecture, execute the following instructions and avoid stall states if any.

```
LW    $10, 20($1)
SUB   $11, $2, $3
ADD   $12, $3, $4
LW    $13, 24($1)
ADD   $14, $5, $6
```

a)Related Screenshot with stalls
No stalls.

b) Related Screenshot without stalls


MIPS Five Stage Pipeline
www.ecs.umass.edu/ece/koren/architecture/windlx/main.html
Instruction
Execution Cycles
FP_Add/Sub
FP_Multiply
FP_Divide
INT_Divide
FP_Add
F1
Insert Instruction
Data Forwarding
Remove Instruction
Help
Reset Application
CPU Cycles
Instruction
0 fp_ld (F1, Offset, R1)
1 fp_add (F2, F3, F4)
2 fp_add (F5, F4, F6)
3 fp_ld (F7, Offset, R1)
4 fp_add (F8, F9, F10)
Step
Execute All Instructions
Potential Hazards:
No Hazards Found.
Type here to search
ENG
14:56
10-04-2021

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Week#____10_____ Program Number: ___5__

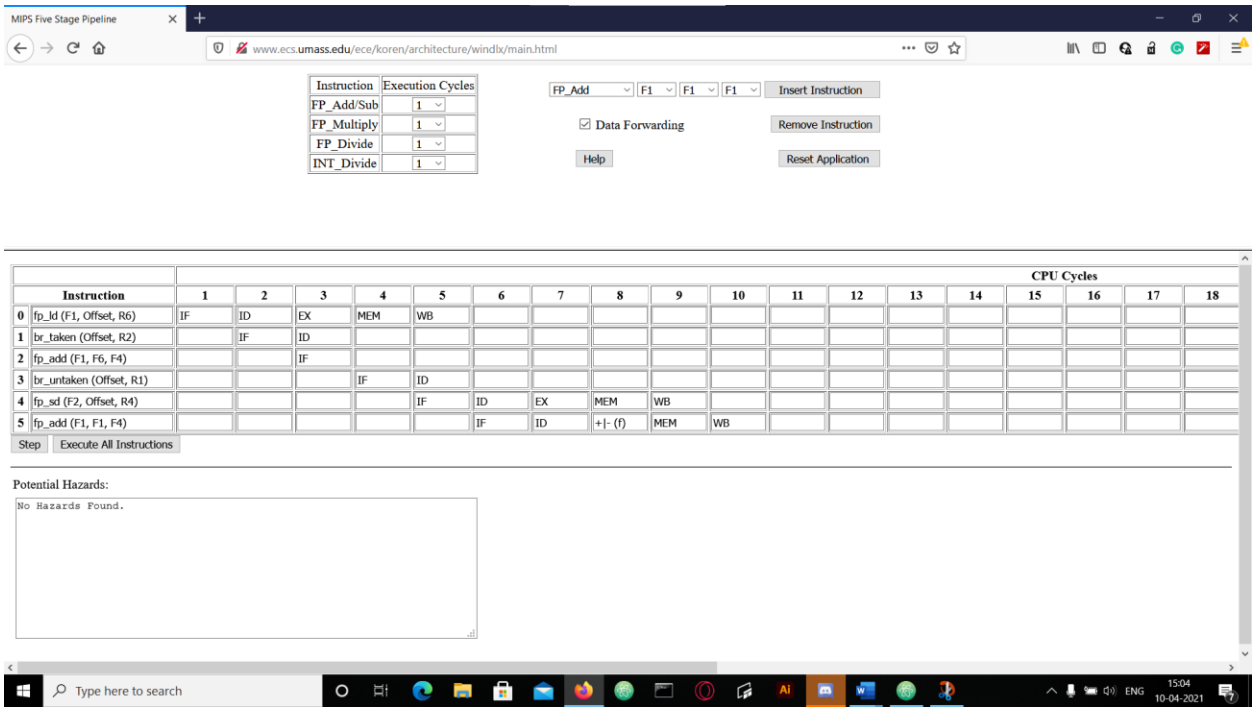
This exercise is to understand the relationship between delay slots, control hazards and branch execution in a 5 stage MIPS pipelined processor.

```
Label 1:    LW    $1, 40($6)
            BEQ   $2, $3, Label2    : branch taken
            ADD   $1, $6, $4
Label2:     BEQ   $1, $2, Label1    : branch not taken
            SW    $2, 20($4)
            ADD   $1, $1, $4
```

Assume full data forwarding and predict- taken branch prediction.

Note the observations.

Related Screenshot


MIPS Five Stage Pipeline
www.ecs.umass.edu/ece/koren/architecture/windlx/main.html
Instruction
Execution Cycles
FP_Add/Sub
FP_Multiply
FP_Divide
INT_Divide
FP_Add
F1
F1
F1
Insert Instruction
Data Forwarding
Remove Instruction
Help
Reset Application
CPU Cycles
Instruction
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
0 fp_ld (F1, Offset, R6) IF ID EX MEM WB
1 br_taken (Offset, R2) IF ID
2 fp_add (F1, F6, F4) IF
3 br_untaken (Offset, R1) IF ID
4 fp_sd (F2, Offset, R4) IF ID EX MEM WB
5 fp_add (F1, F1, F4) IF ID +|- (f) MEM WB
Step
Execute All Instructions
Potential Hazards:
No Hazards Found.
Type here to search
ENG
15:04
10-04-2021

Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature: joy
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SRN: PES2UG19CS270
Section: E
Date: 10/04/2021