Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:22/01/2021

Name: O P Joy Jefferson	SRN:PES2UG19CS270	Section:E

Week#____1_____ Program Number: ____1___

Title of the Program

Write an ALP using ARM instruction set to add and subtract two 32 bit numbers .Both numbers are in registers.

I. ARM Assembly Code for each program

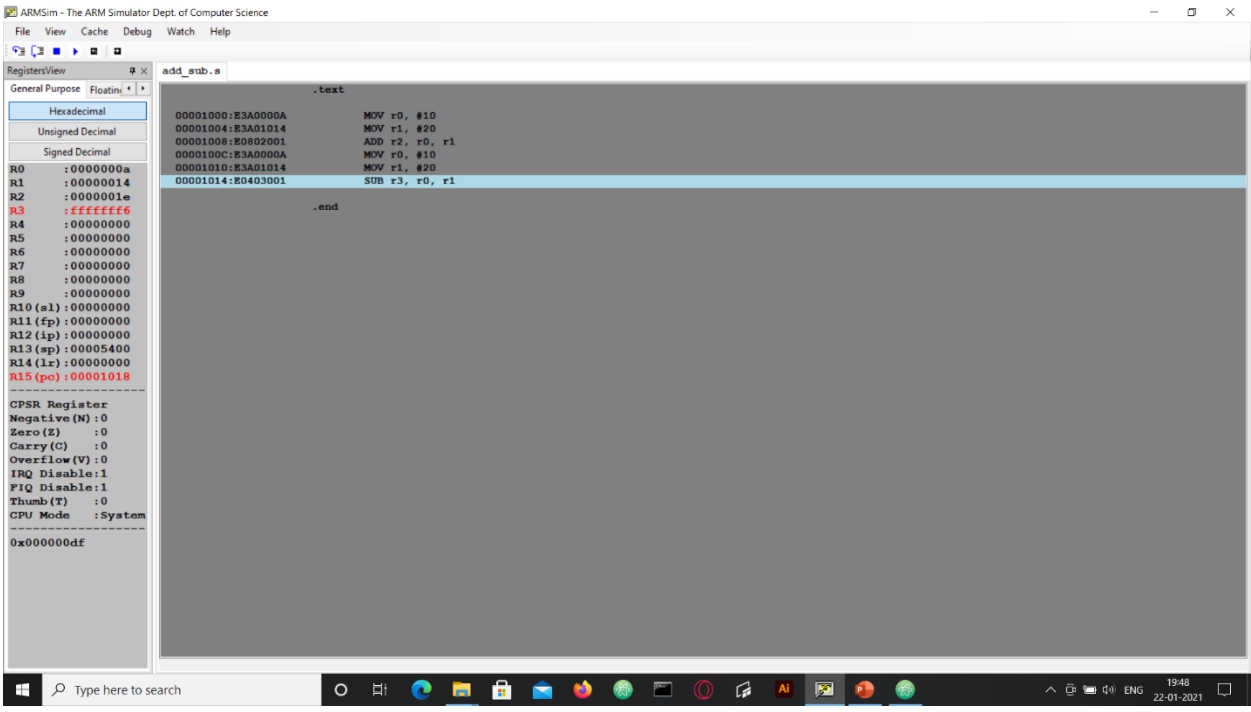
```
.text
        MOV r0, #10
        MOV r1, #20
        ADD r2, r0, r1
        MOV r0, #10
        MOV r1, #20
```

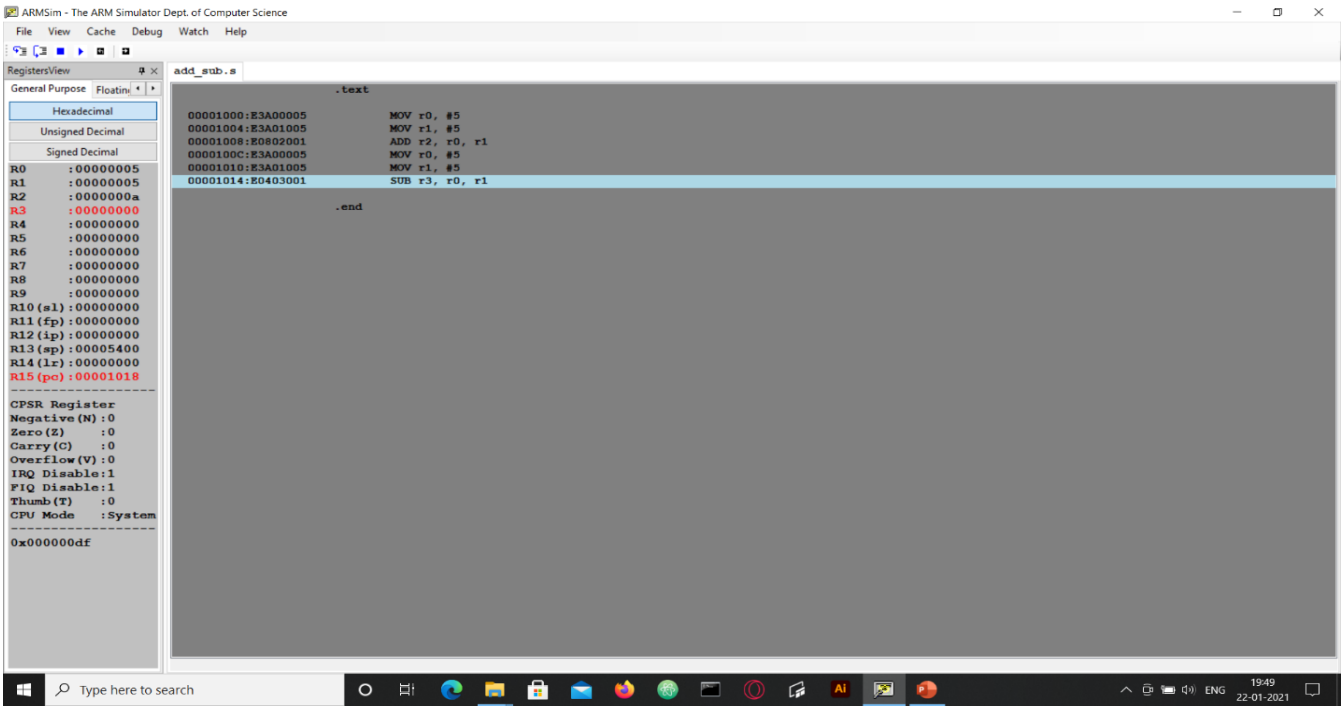
SUB r3, r0, r1

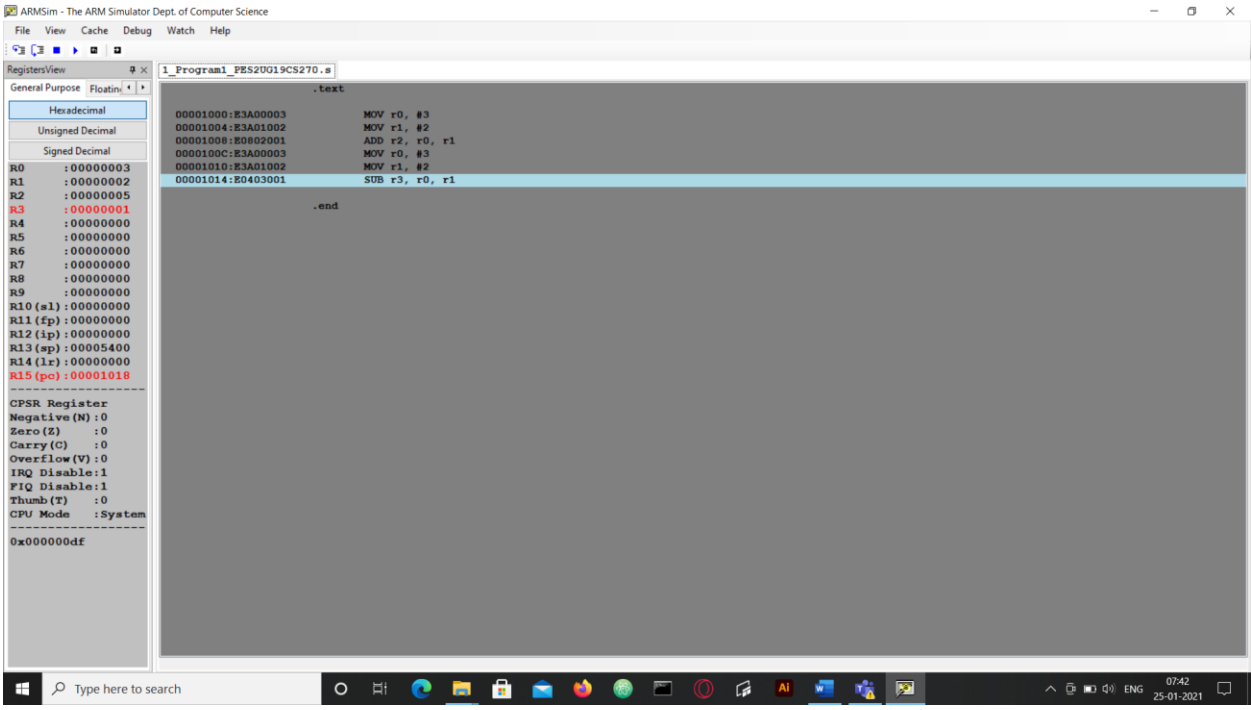
.end

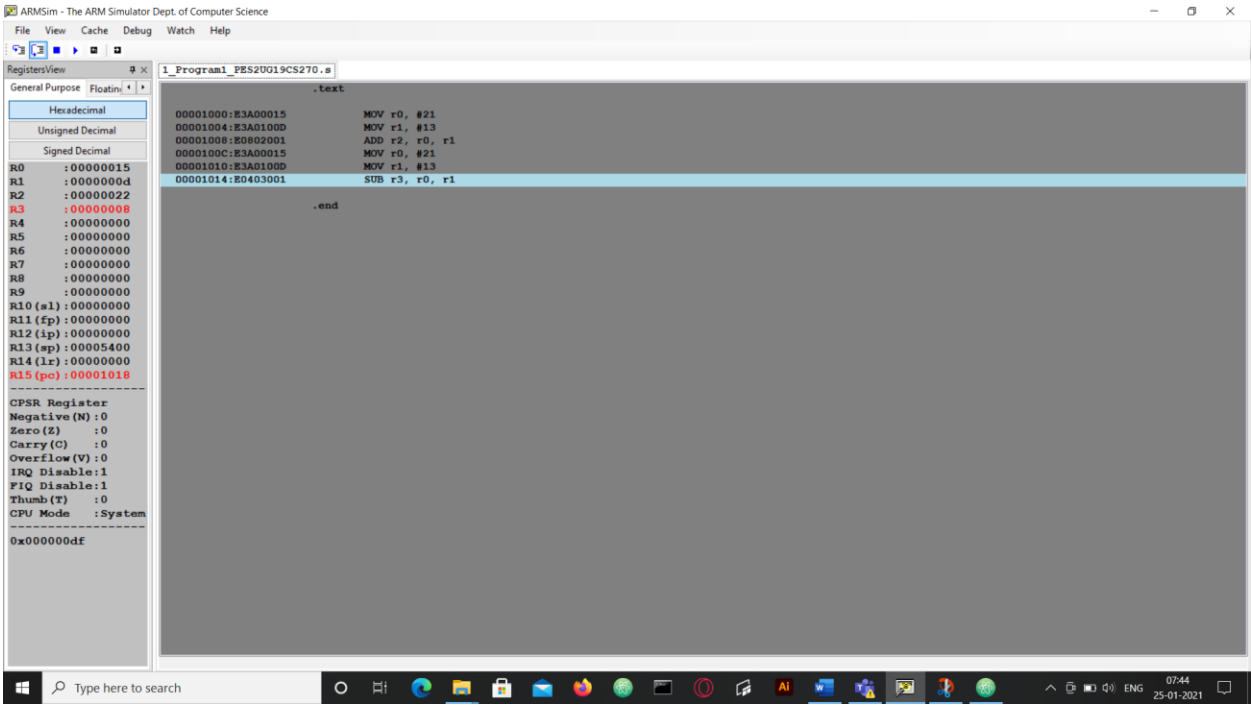
II. Output Screen Shot (Register Window, Output window)

The output should be verified with 2 test cases (one example shown in class, one example of own choice)




ARMSim - The ARM Simulator Dept. of Computer Science
File View Cache Debug Watch Help
RegistersView
General Purpose Floatin
Hexadecimal
Unsigned Decimal
Signed Decimal
R0 :00000005
R1 :00000005
R2 :0000000a
R3 :00000000
R4 :00000000
R5 :00000000
R6 :00000000
R7 :00000000
R8 :00000000
R9 :00000000
R10(sl):00000000
R11(fp):00000000
R12(ip):00000000
R13(sp):00005400
R14(lr):00000000
R15(pc):00001018
CPSR Register
Negative(N):0
Zero(Z) :0
Carry(C) :0
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T) :0
CPU Mode :System
0x000000df
add_sub.s
.text
00001000:E3A00005 MOV r0, #5
00001004:E3A01005 MOV r1, #5
00001008:E0802001 ADD r2, r0, r1
0000100C:E3A00005 MOV r0, #5
00001010:E3A01005 MOV r1, #5
00001014:E0403001 SUB r3, r0, r1
.end
Type here to search
ENG
19:49
22-01-2021


ARMSim - The ARM Simulator Dept. of Computer Science
File View Cache Debug Watch Help
RegistersView
General Purpose Floatin
Hexadecimal
Unsigned Decimal
Signed Decimal
R0 :00000003
R1 :00000002
R2 :00000005
R3 :00000001
R4 :00000000
R5 :00000000
R6 :00000000
R7 :00000000
R8 :00000000
R9 :00000000
R10(sl):00000000
R11(fp):00000000
R12(ip):00000000
R13(sp):00005400
R14(lr):00000000
R15(pc):00001018
CPSR Register
Negative(N):0
Zero(Z) :0
Carry(C) :0
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T) :0
CPU Mode :System
0x000000df
1_Program1_PES2UG19CS270.s
.text
00001000:E3A00003 MOV r0, #3
00001004:E3A01002 MOV r1, #2
00001008:E0802001 ADD r2, r0, r1
0000100C:E3A00003 MOV r0, #3
00001010:E3A01002 MOV r1, #2
00001014:E0403001 SUB r3, r0, r1
.end
Type here to search
ENG
07:42
25-01-2021



III. Output table for each program

Example
R0=10=Hex 0A
R1=20=Hex 14
After Addition R2=30=Hex 1E
After Subtraction R3 = -10 = -Hex 0A

R0	R1	Arithmetic Operation	Result
0x0A	0x14	ADD	R2 =0x1E
0x0A	0x14	SUBTRACT	R3=-0x0A

Example
R0=5=Hex 5
R1=5=Hex 5
After Addition R2=10=Hex 0a
After Subtraction R3 = 0 = Hex 0

R0	R1	Arithmetic Operation	Result
0x05	0x05	ADD	R2 =0x0a
0x05	0x05	SUBTRACT	R3=0x00

Example
R0=5=Hex 3
R1=5=Hex 2
After Addition R2=5=Hex 5
After Subtraction R3 = 1 = Hex 1

R0	R1	Arithmetic Operation	Result
0x03	0x03	ADD	R2 =0x05
0x02	0x02	SUBTRACT	R3=0x01

Example R0=21=Hex 15 R1=13=Hex 0d After Addition R2=34=Hex 22 After Subtraction R3 = 8 = Hex 8			
R0	R1	Arithmetic Operation	Result
0x15	0x0d	ADD	R2 =0x22
0x15	0x0d	SUBTRACT	R3=0x08

Microprocessor and Computer Architecture Laboratory

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4th Semester, Academic Year 2020-21

Date:22/01/2021

Name: O P JOY JEFFERSON	SRN: PES2UG19CS270	Section:E

Week#____1_____ Program Number: ____2___

Title of the Program

Write an ALP to demonstrate logical operations. All operands are in registers.

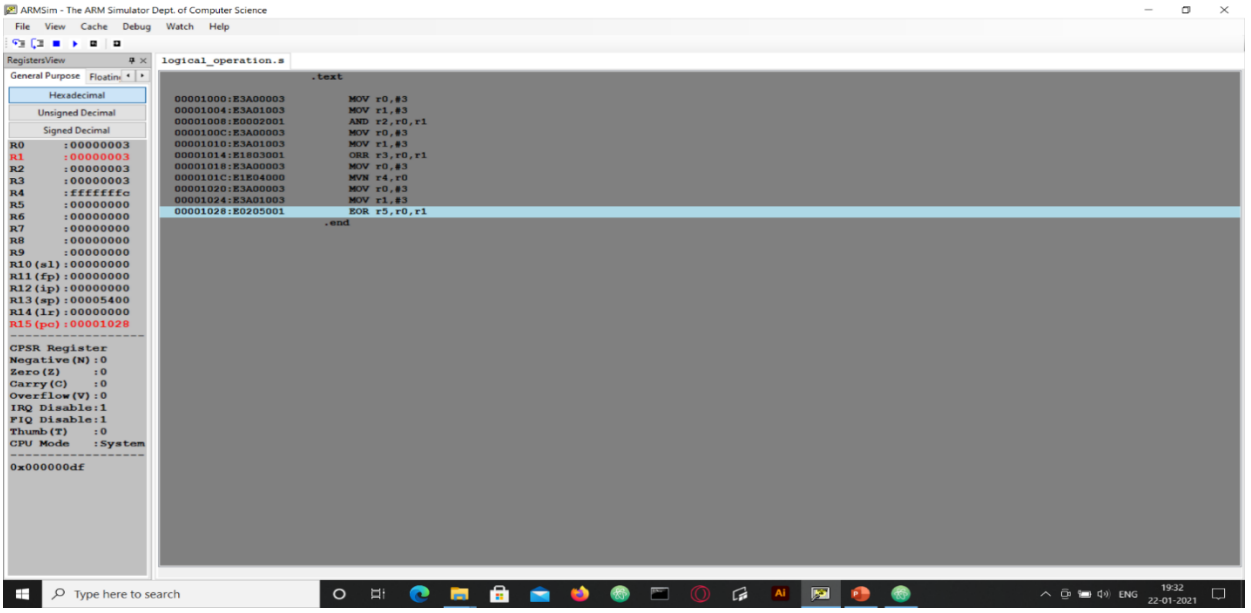
I. ARM Assembly Code for each program

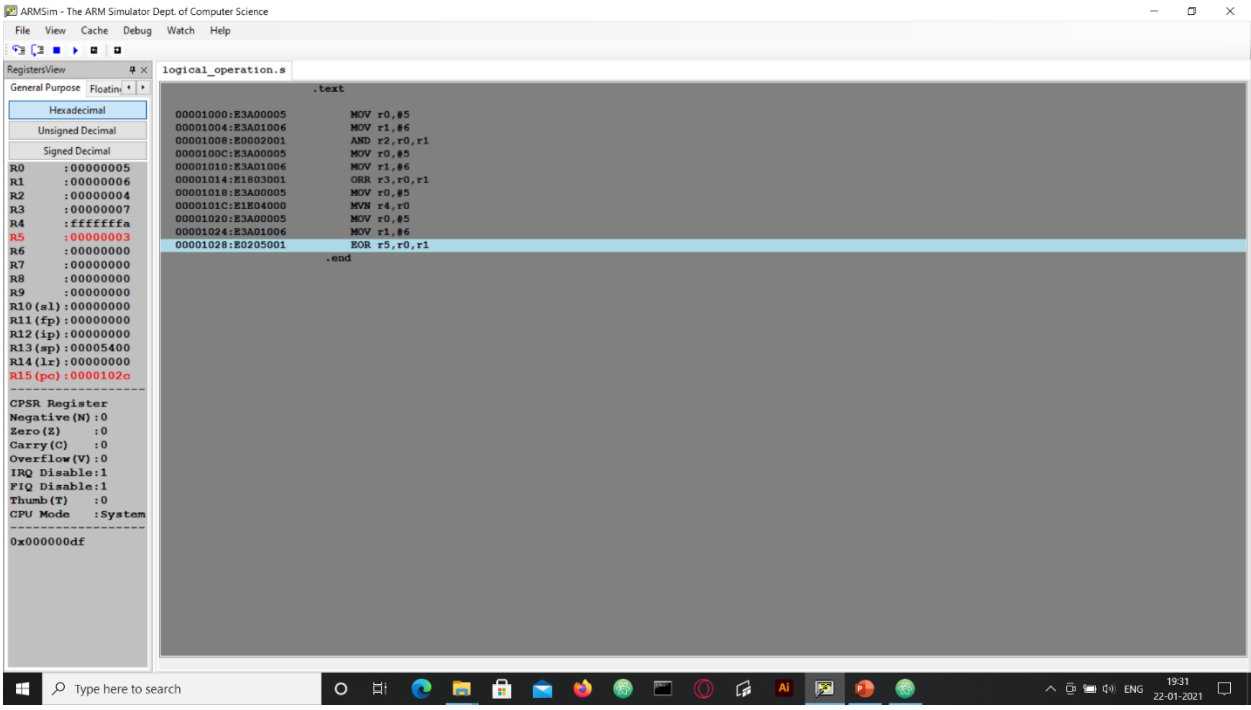
```
.text
    MOV r0,#5
    MOV r1,#6
    AND r2,r0,r1
    MOV r0,#5
    MOV r1,#6
    ORR r3,r0,r1
    MOV r0,#5
    MVN r4,r0
    MOV r0,#5
    MOV r1,#6
    EOR r5,r0,r1
.end
```

II. Output Screen Shot (Register Window, Output window)

The output should be verified with 2 test cases

(one example shown in class, one example of own choice)





III. Output table for each program

1).

R0	R1	Logical Operation	Instruction	Result
0x03	0x03	AND	AND	R0 =0x03
0x05	0x06	OR	ORR	R0 =0x03
0x05	0x06	EX-OR	EOR	R0 =0x03
0x05		NOT	MVN	R0 =0xfffffffc

2).

R0	R1	Logical Operation	Instruction	Result

0x05	0x06	AND	AND	R0 =0x04
0x05	0x06	OR	ORR	R0 =0x07
0x05	0x06	EX-OR	EOR	R0 =0x03
0x05		NOT	MVN	R0 =0xfffffffa

Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:

Name: O P JOY JEFFERSON	SRN:PES2UG19CS270	Section:E

Week#____1_____ Program Number: ____3___

Title of the Program

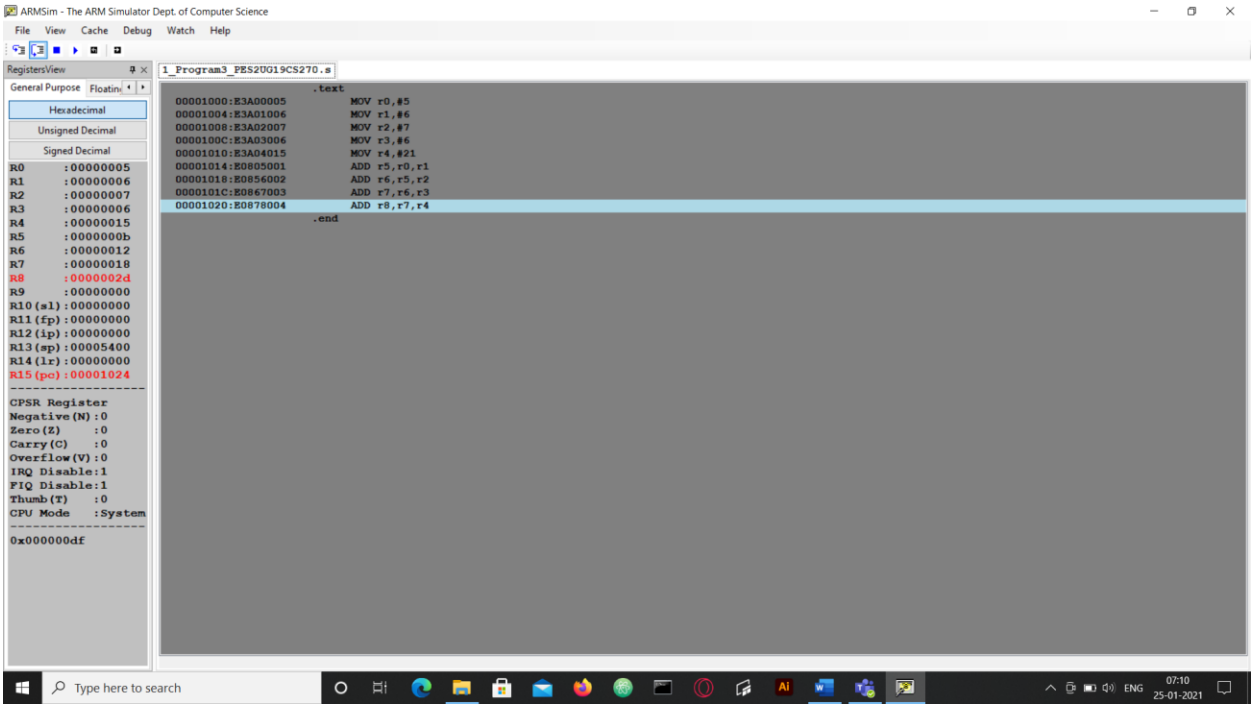
Write an ALP to add 5 numbers where values are present in registers.

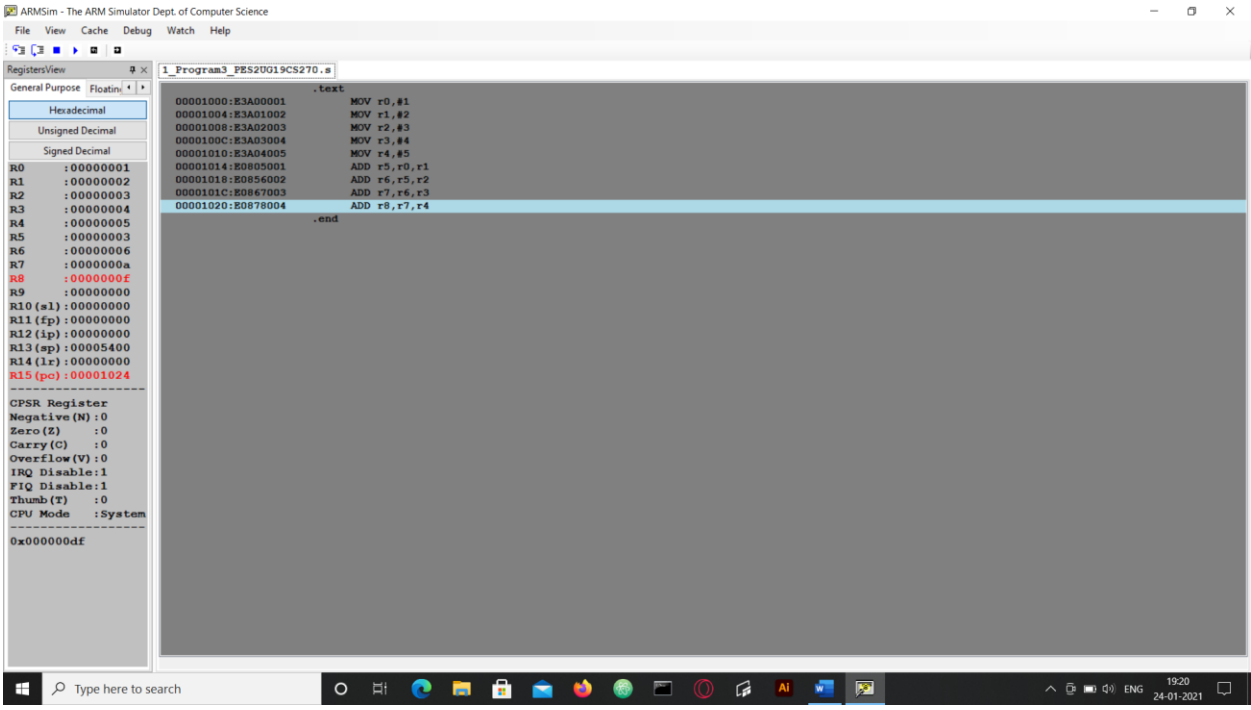
I. ARM Assembly Code for each program

```
.text
    MOV r0,#5
    MOV r1,#6
    MOV r2,#7
    MOV r3,#6
    MOV r4,#21
    ADD r5,r0,r1
    ADD r6,r5,r2
    ADD r7,r6,r3
    ADD r8,r7,r4
.end
```

II. Output Screen Shot (Register Window, Output window)

The output should be verified with 2 test cases (one example shown in class, one example of own choice)





III. Output table for each program

1).

R0		0x05
R1		0x06
R2		0x07
R3		0x06
R4		0x0f
R5	R0+R1	0x0b
R6	R5+R2	0x12
R7	R6+R3	0x18
R8	R7+R4	0x2d

2).

R0		0x01
R1		0x02

R2		0x03
R3		0x04
R4		0x05
R5	R0+R1	0x03
R6	R5+R2	0x06
R7	R6+R3	0x0a
R8	R7+R4	0x0f

Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:

Name: OP Joy Jefferson	SRN:PES2UG19CS270	Section:E

Week#____1_____ Program Number: ____4___

Title of the Program

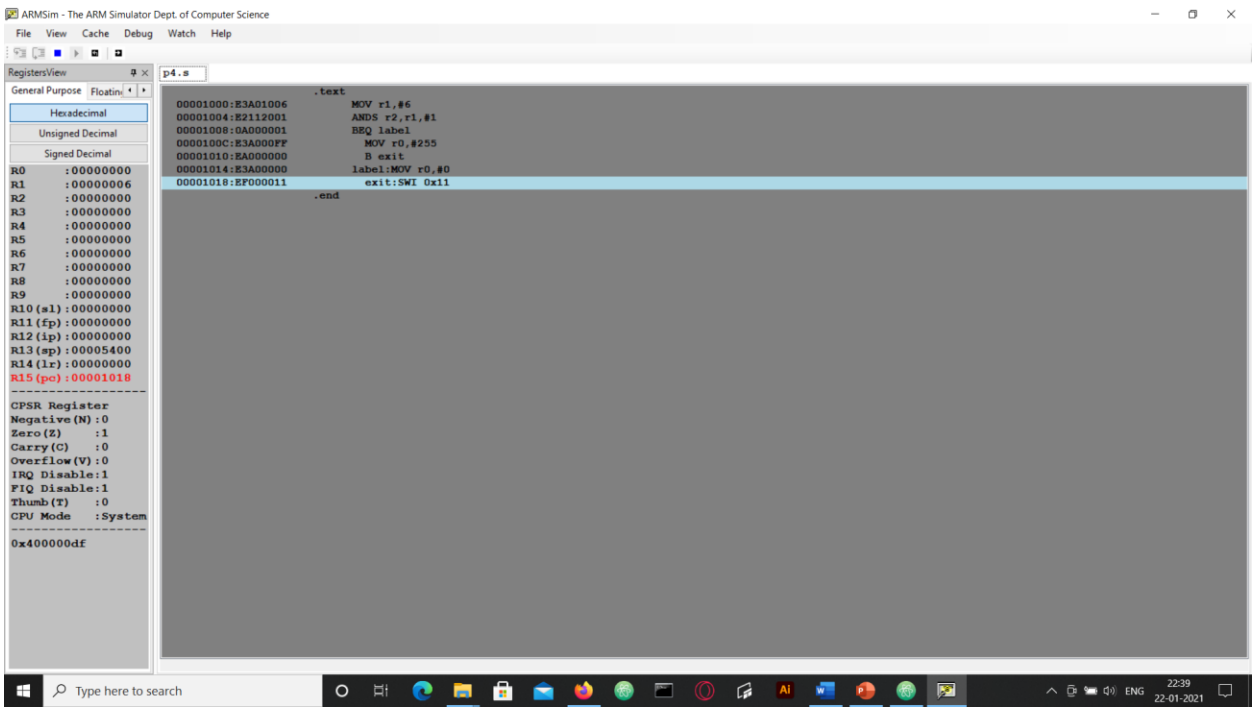
Write an ALP using ARM instruction set to check if a number stored in a register is even or odd. If even, store 00 in R0, else store FF in R0

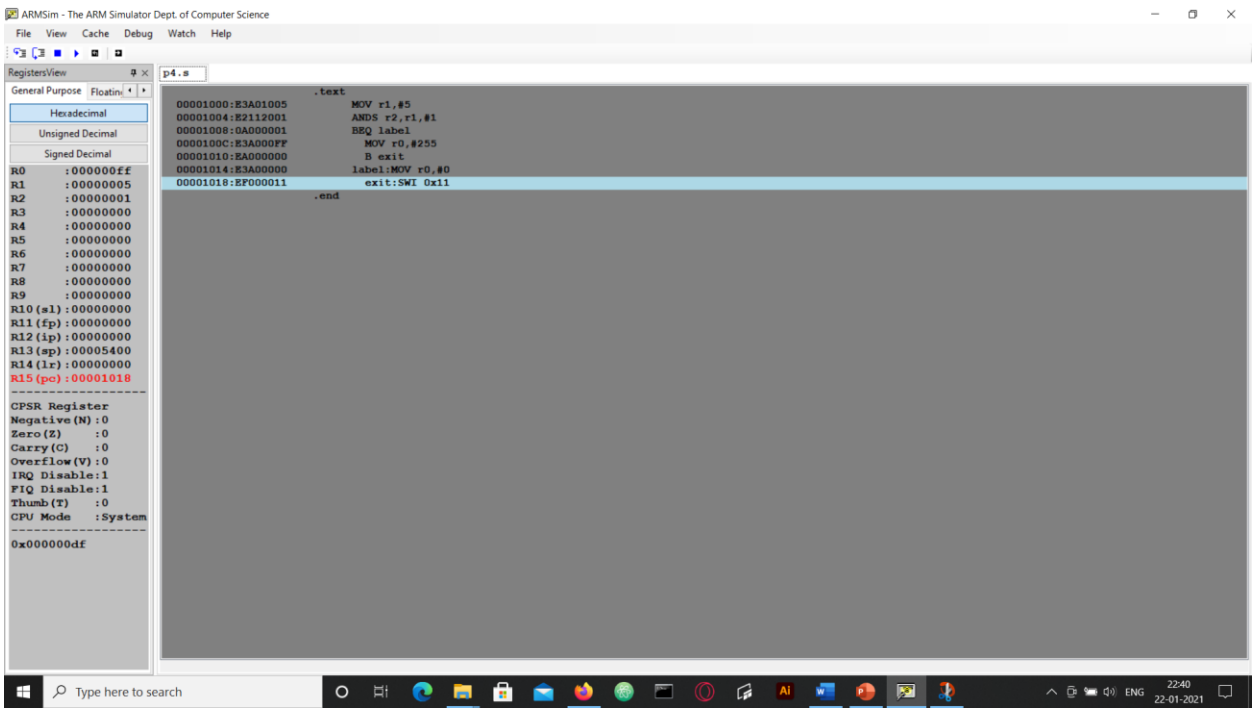
I. ARM Assembly Code for each program

```
.text
        MOV r0, #6
        ANDs r0, r0, #1
        BEQ condition
                MOV r1, #255
                B exit
        condition:
                MOV r2, #0
        exit:
                SWI 0x011
.end
```

II. Output Screen Shot (Register Window, Output window)

The output should be verified with 2 test cases (one example shown in class, one example of own choice)





III. Output table for each program

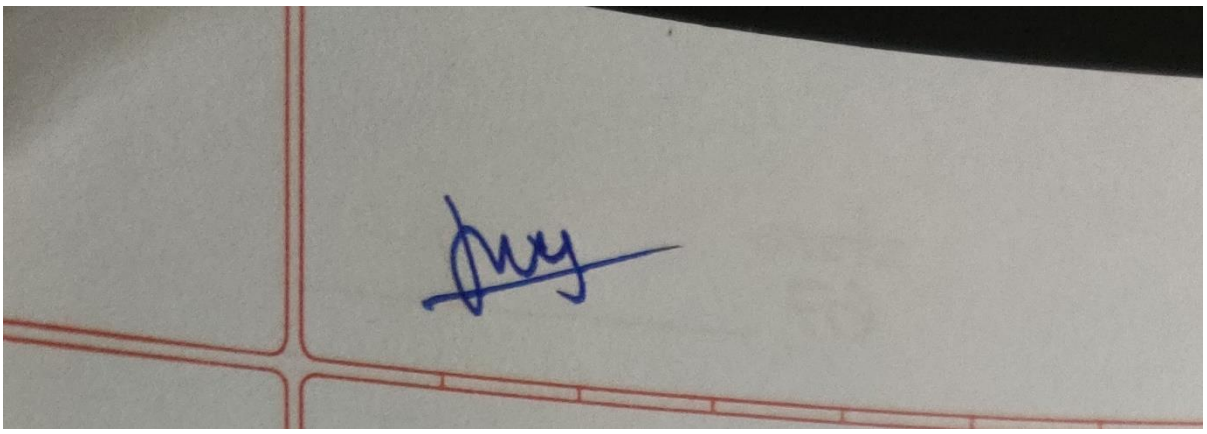
CASE 1	R1		0x06
	R2	After AND operation	0x00
	R0	(EVEN)	0x00
CASE 2	R1		0x05
	R2	After AND operation	0x01
	R0	(ODD)	0xFF

Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.

- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature:



Name:O P JOY JEFFERSON

SRN:PES2UG19CS270

Section: E

Date:22/01/2021