**CVSD HW6 101403021 郭鈞哲**

## Basic

## 1.

下方圖片是 CLE_DC.sdc 的內容

```
# You can only modify clock period

set cycle  10        ;#clock period defined by designer

#don't modify the following part
create_clock -period $cycle [get_ports  clk]
set_dont_touch_network      [all_clocks]
set_fix_hold                [all_clocks]
set_clock_uncertainty  0.1  [all_clocks]
set_clock_latency      0.5  [all_clocks]
set_ideal_network           [get_ports clk]

#Don't touch the basic env setting as below
set_input_delay  1     -clock clk [remove_from_collection [all_inputs] [get_ports clk]]
set_output_delay 1     -clock clk [all_outputs]
set_load         1     [all_outputs]
set_drive        1     [all_inputs]

set_operating_conditions -max_library slow -max slow
set_wire_load_model -name tsmc13_wl10 -library slow

set_max_fanout 6 [all_inputs]
```

我的 clock cycle 設定為 10 ns

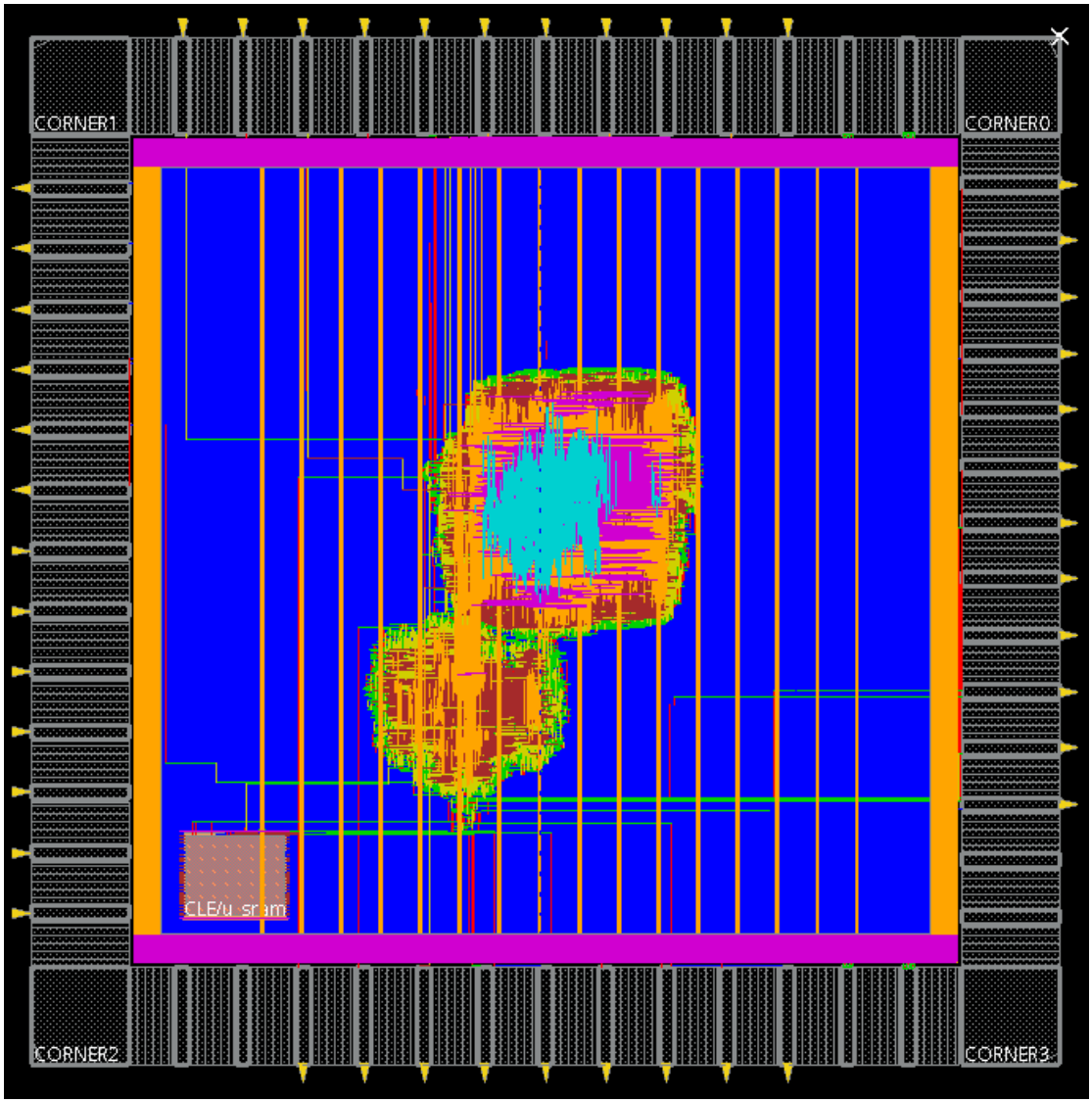
## 2.

| Area before Dft insertion | Area after Dft insertion |
|---|---|
| From CLE_syn.area_rpt | From CLE_syn.timing_rpt |
| Number of ports: 157<br>Number of nets: 28419<br>Number of cells: 28189<br>Number of combinational cells: 25468<br>Number of sequential cells: 2713<br>Number of macros/black boxes: 1<br>Number of buf/inv: 3910<br>Number of references: 179<br><br>Combinational area: 229238.965358<br>Buf/Inv area: 28616.466352<br>Noncombinational area: 92869.844521<br>Macro/Black Box area: 69557.296875<br>Net Interconnect area: 4445395.778900<br><br>Total cell area: 391666.106754<br>Total area: 4837061.885654<br>1 | Number of ports: 214<br>Number of nets: 31085<br>Number of cells: 28194<br>Number of combinational cells: 25473<br>Number of sequential cells: 2713<br>Number of macros/black boxes: 1<br>Number of buf/inv: 3915<br>Number of references: 185<br><br>Combinational area: 231136.658407<br>Buf/Inv area: 29869.147595<br>Noncombinational area: 115986.733829<br>Macro/Black Box area: 69557.296875<br>Net Interconnect area: 4699963.965973<br><br>Total cell area: 416680.689111<br>Total area: 5116644.655084<br>1 |

| Timing before Dft insertion | Timing after Dft insertion |
|---|---|
| From CLE_syn_dft.area_rpt | From CLE_syn_dft.timing_rpt |
| clock clk (rise edge) 10.00 10.00<br>clock network delay (ideal) 0.50 10.50<br>clock uncertainty -0.10 10.40<br>ROM_MEM_reg_2__0_/CK (DFFRX2) 0.00 10.40 r<br>library setup time -0.16 10.24<br>data required time 10.24<br>---<br>data required time 10.24<br>data arrival time -10.24<br>---<br>slack (MET) 0.00<br><br>1 | clock clk (rise edge) 10.00 10.00<br>clock network delay (ideal) 0.50 10.50<br>clock uncertainty -0.10 10.40<br>ROM_MEM_reg_103__3_/CK (SDFFRX2) 0.00 10.40 r<br>library setup time -0.33 10.07<br>data required time 10.07<br>---<br>data required time 10.07<br>data arrival time -10.07<br>---<br>slack (MET) 0.00<br><br>1 |

可以看到插完 scan chain 之後 area 變大， timing 也不同

## 3.
## Final chip layout figure



**Chip size**

```
innovus 12> analyzeFloorplan
**WARN: (IMPAFPU-9006): Command 'analyzeFloorplan' is obsolete. Please use commands 'placeDesi
gn + trialRoute + create_ps_per_micron_model + timeDesign -proto + load_timing_debug_report -p
roto' to analyze congestion and timing for the floorplan.
Start to collect the design information.
Build netlist information for Cell CHIP.
Finished collecting the design information.
Average module density = 1.000.
Density for the design = 1.000.
       = stdcell_area 2158947 sites (3664597 um^2) / alloc_area 2158947 sites (3664597 um^2).
Pin Density = 0.05378.
            = total # of pins 118791 / total area 2208660.
************************ Analyze Floorplan *************************
    Die Area(um^2)            : 6701258.38
    Core Area(um^2)           : 3748979.48
    Chip Density (Counting Std Cells and MACROs and IOs): 89.869%
    Core Density (Counting Std Cells and MACROs): 99.150%
    Average utilization       : 100.000%
    Number of instance(s)     : 102873
    Number of Macro(s)        : 1
    Number of IO Pin(s)       : 45
    Number of Power Domain(s) : 0
************************ Estimation Results ************************
********************************************************************
```

**4. 10.3~10.5 都沒有 violation**

**Verify Geometry**

```
VG: elapsed time: 26.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
 *** verify geometry (CPU: 0:00:25.8  MEM: 155.9M)
```

**Verify Antenna**

```
innovus 12>
******* START VERIFY ANTENNA *********
Report File: CHIP.antenna.rpt
LEF Macro File: CHIP.antenna.lef
5000 nets processed: 0 violations
10000 nets processed: 0 violations
15000 nets processed: 0 violations
20000 nets processed: 0 violations
25000 nets processed: 0 violations
Verification Complete: 0 Violations
******* DONE VERIFY ANTENNA *********
(CPU Time: 0:00:04.0  MEM: 0.453M)
```

**Verify Connectivity**

```
******** Start: VERIFY CONNECTIVITY ********
Start Time: Sun Dec 23 22:14:32 2018

Design Name: CHIP
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (2591.0800, 2586.2800)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 22:14:33 **** Processed 5000 nets.
**** 22:14:33 **** Processed 10000 nets.
**** 22:14:33 **** Processed 15000 nets.
**** 22:14:34 **** Processed 20000 nets.
**** 22:14:34 **** Processed 25000 nets.

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Sun Dec 23 22:14:35 2018
Time Elapsed: 0:00:03.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:03.3  MEM: 62.012M)
```

## 5.

## Pre-layout

**testfixture_a**

```
                Simulation Summary

-----------------------------------------------------

Congratulations! All data have been generated successfully!

-------------------------PASS------------------------

err=   0
Simulation complete via $finish(1) at time 11861236 PS + 0
./testfixture_a.v:201       #(`CYCLE/2); $finish;
```

**testfixture_b**

```
                Simulation Summary

--------------------------------------------------

Congratulations! All data have been generated successfully!

------------------------PASS----------------------

err=   0
Simulation complete via $finish(1) at time 11861236 PS + 0
./testfixture_b.v:201       #(`CYCLE/2); $finish;
```

**testfixture_c**

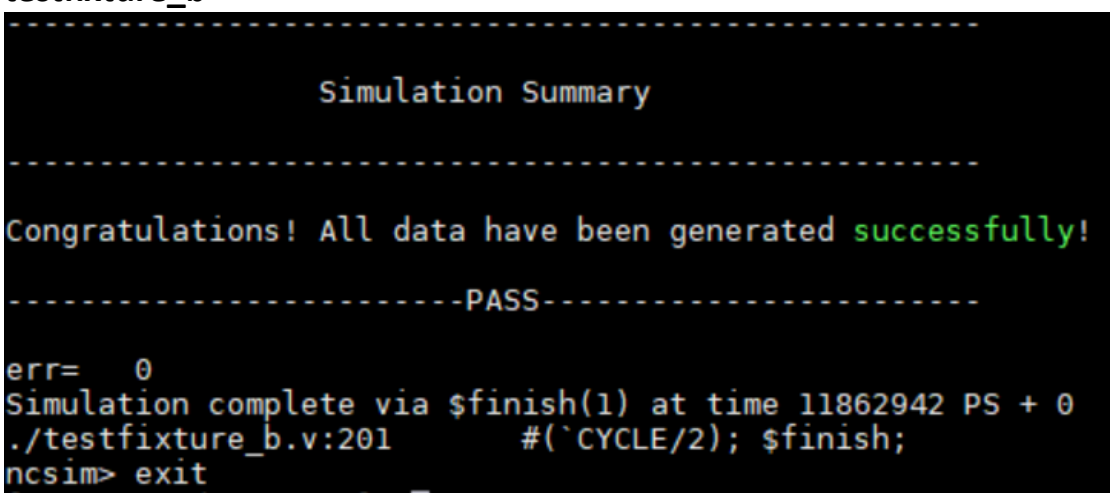
```
                Simulation Summary

--------------------------------------------------

Congratulations! All data have been generated successfully!

------------------------PASS----------------------

err=   0
Simulation complete via $finish(1) at time 11861236 PS + 0
./testfixture_c.v:201       #(`CYCLE/2); $finish;
ncsim> exit
```

## Post-layout

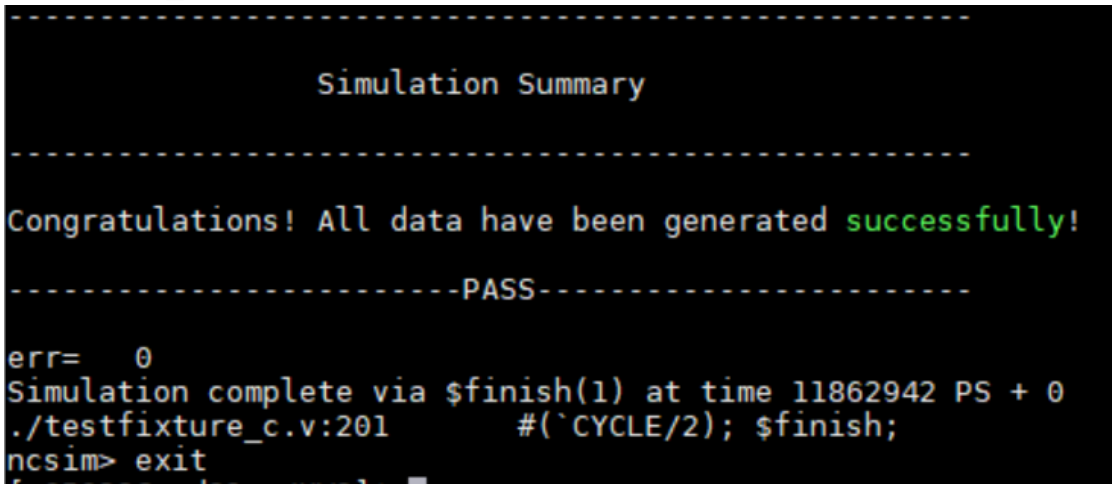
**testfixture_a**

```
--------------------------------------------------

                Simulation Summary

--------------------------------------------------

Congratulations! All data have been generated successfully!

------------------------PASS----------------------

err=   0
Simulation complete via $finish(1) at time 11862942 PS + 0
./testfixture_a.v:201       #(`CYCLE/2); $finish;
ncsim> exit
```

**testfixture_b**



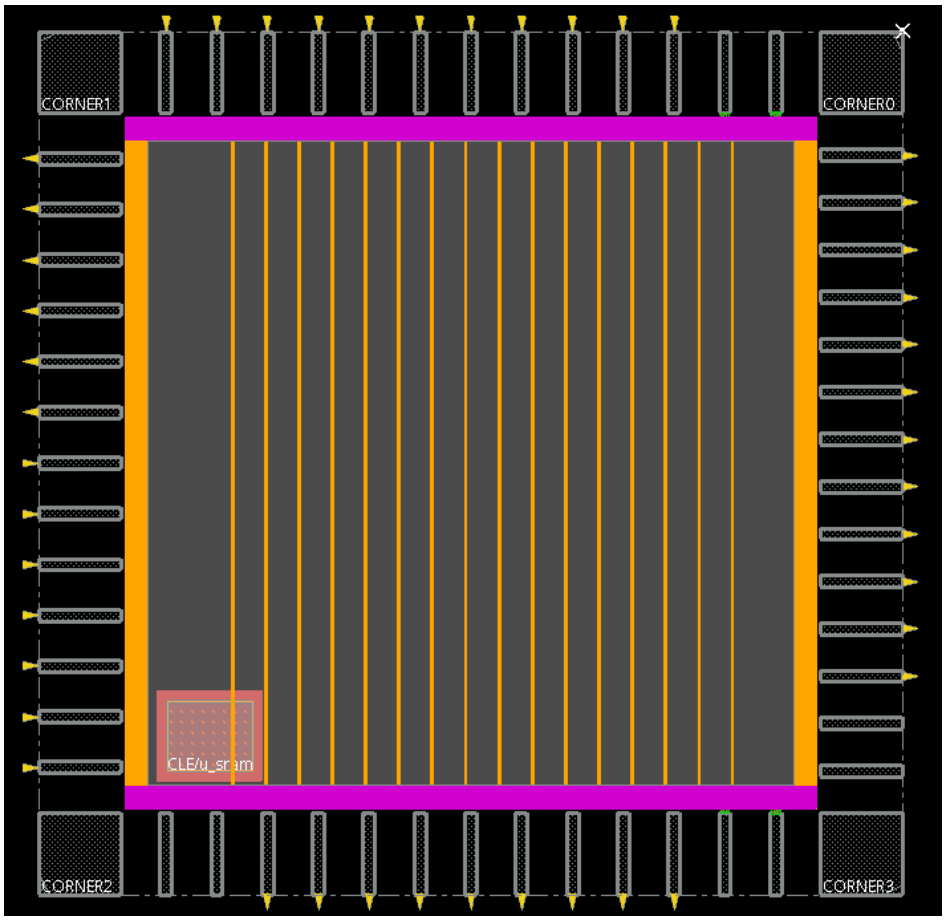

**testfixture_c**



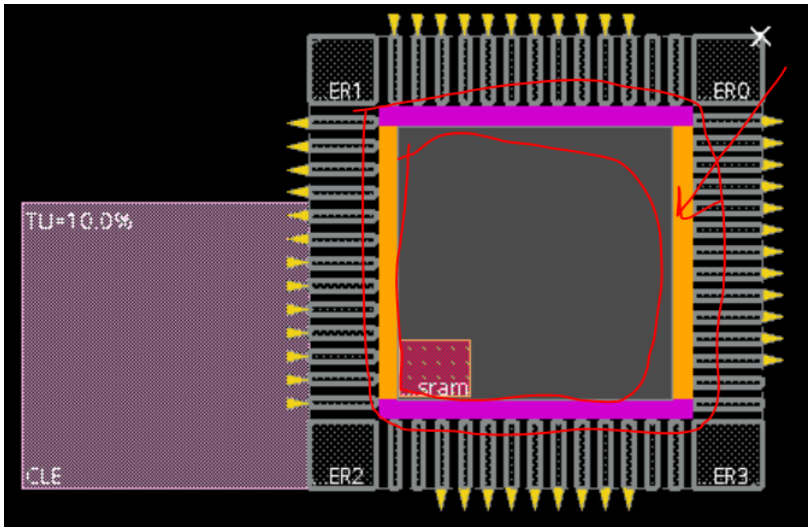

pre-sim 和 post-sim 只有些微的差異，我想這可能是因為 wire load model 的 delay 和實際拉出來的線不一樣，而如果萃取出寄生電容和寄生電阻的話，應該結果會差更多

**6.**

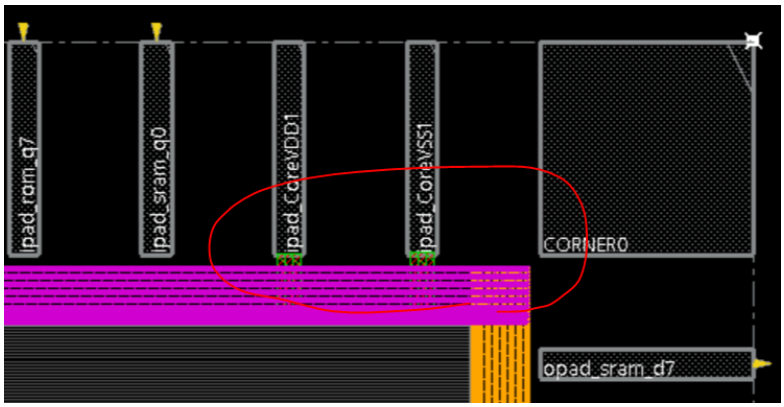
這是整體的 **power plan** 圖，下方會一一做說明

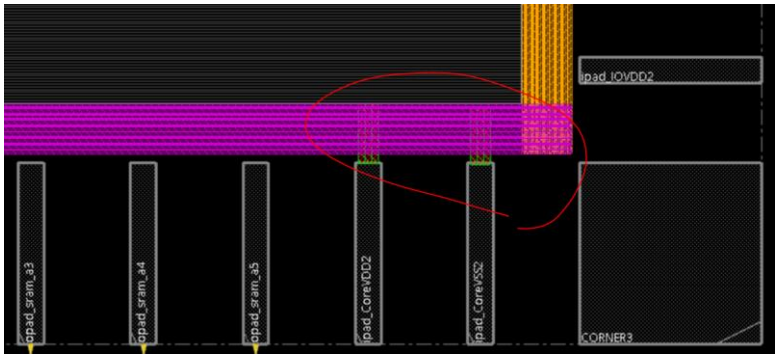



在 Core 跟 I/O pad 之間，有很多 VDD、VSS 交錯，這就是 **Power ring** ，這是為了讓晶片內部供應電壓均勻，避免 IR drop



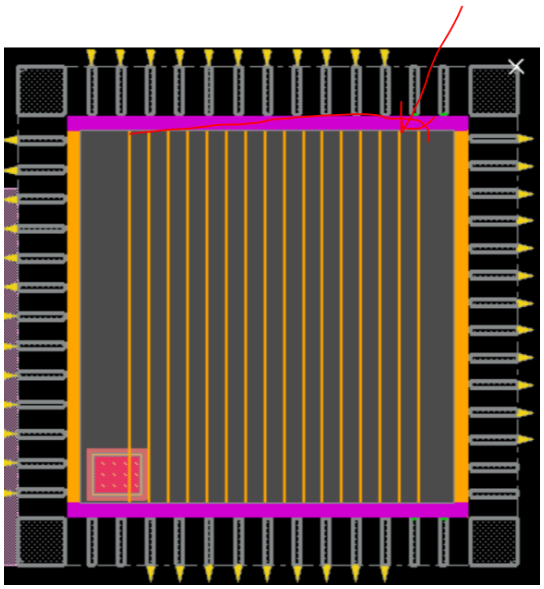
圖中有四條 **Power pad** (右上和右下的綠色處) 接到 Power ring ，這是為了讓 Core pin 接到 VDD 、 VSS




**Power-stripe**

這是為了讓 core 內部的供電電壓均勻



如同中縱向橘色的那幾條

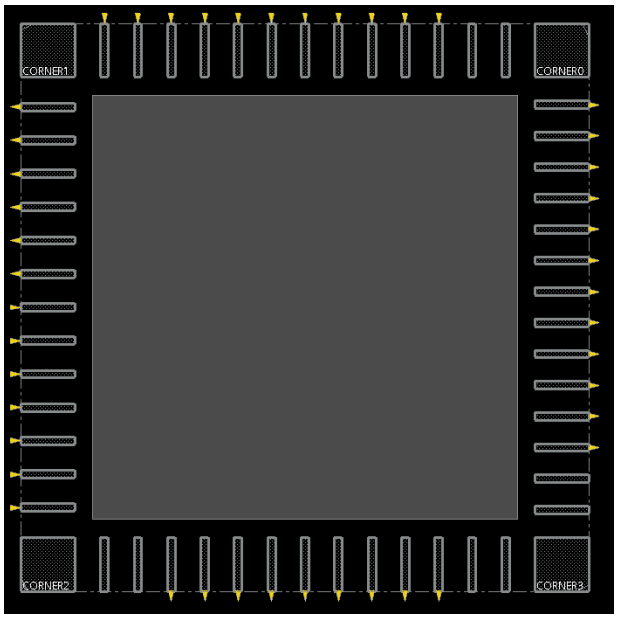
**7.**

VSS 做好放在 clk 和 reset 旁邊，這樣可以做 noise shielding

同一組的 input 最好放在一起，這樣大家的 noise 會比較接近

四個角落的 PAD 是為了要對稱，以及讓外圍 PAD 可以連起來

PAD 是為了要穩壓，而 PAD 也要吃電壓，所以也需要一組或多組 VDD 和 VSS




**8.**

由於為了繞線方便， core utilization 的條件設很寬鬆，所以可以看到繞線其實有很多空間是被浪費掉的，下次或許會盡力找到可以繞線以及不浪費空間的平衡點，我想這是可以改進的地方，另外由於 gate-synthesis 的面積過大，在繞線時花了很久的時間，下次在設計 gate-level 的時候，會在 area 這邊多留意，盡量把面積往下壓