Computer-Aided VLSI System Design
HW4 - DFT/ATPG
Due in 12:00 11/27/2018 (Tue)

TA:
葉日豐 r06921074@ntu.edu.tw

Purpose

In this homework, you have to perform DFT insertion to the synthesized *Frequency Analysis System* gate-level netlist. You also have to generate test patterns by using TetraMAX® ATPG.

Goal

Learn how to insert scan chain which is based on the design and generate the test patterns

Download Files from CEIBA website

1. Create a work directory and copy the files into it.
2. Check if you have these files:

Filename	Description
FAS_syn.v	Synthesized gate level Verilog netlist (no scan chain yet)
.synopsys_dc.setup	Synopsys Design Compiler setup file, which defines search paths, library name, etc.
FAS_syn.sdc	The constraints that are used in this homework.

Note: in the lab, you used the file "constraints.tcl". But here we use "FAS_syn.sdc" instead of it.

Problem 1:   Perform DFT insertion

1. Perform DFT insertion with **X scan chains** and fix any DRC violation.
2. Save the DFT insertion results.
3. Modify the testbench and verify the DFT inserted design. Make sure your DFT inserted design still work in functional mode.

Hint:

*Scan chain number is <u>based on the design's DFF number</u>. We usually link 100 DFF with one scan chain.

*You can follow the step on Lab4 but sometimes you may need to modify some parameters (that's all based on the design).

Problem 2:   Generate stuck-at fault test patterns

4. Generate stuck-at fault test patterns for the scan-ready design.

5. Save the ATPG results.

6. Verify the Verilog format test patterns (optional).

Hint:

In this homework, all you need is to make sure that your test coverage will over than 98%. You can do some experiments to find the minimum pattern count.

Online Submission (FTP):

FTP:

Deadline	12:00 11/27/2018 (Tue)
IP	140.112.175.174
Account	1071cvsd
Password	cvsd2018

Please submit a zipped file named *StudentID_HW4_vk.zip* (k is the number of version, k =1,2,…). This zip file has to contain the 11 files below.

Script Files:
1. "dft.tcl" : dft insertion script
2. "atpg.tcl" : atpg script

Synthesis Results:
3. "report_FAS_syn.txt" : pre-scan report summarizing timing, power, and area

DFT Insertion Results:
4. FAS_dft.v" : gate level netlist (scan-ready)
5. "FAS_dft.sdf" : post-scan (scan-ready) sdf file
6. "report_dft.txt" : post-scan report summarizing timing, power, and area
7. "FAS_dft.spf" : test protocol file
8. "FAS_dft.scan_path" : scan path report
9. "FAS_dft.scan_cell" : scan cell report

ATPG Results:

10. "FAS_atpg.stil" : STIL format test patterns

Questions:

11. "Answers.txt": answer the following questions by **your results**. All answers must base on your own result. There is no golden answer for all students.

   (A)

       A-1. How many flip-flops are chained?

       A-2. How many scan cells in every scan chain, respectively?

       A-3. What are the inputs and outputs of these scan chains?

       A-4. What is the name of the scan enable pin for your scan chain?

   (B)

       B-1. What is the area before scan chain insertion?

       B-2. What is the area after scan chain insertion?

       B-3. How much is the area overhead percentage of scan chain?

       B-4. Try to explain why scan chain introduces area overhead.

   (C) Ignore the input external and output external delay.

       C-1. How long (ns) is the critical path delay before scan chain insertion?

       C-2. How long the critical path after scan chain insertion?

       C-3. How many percent is the path delay overhead?

       C-4. Sometimes, the individual gate delay changes in the critical path. Try to explain why?

   (D)

       D-1. How many total faults (uncollapsed) are there in the circuit?

       D-2. How many patterns do we have?

       D-3. What is the test coverage (%)?

       D-4. What is the fault coverage (%)?

Revised by Bing-Chuan Bai, 2011

Revised by Kuan-Yu Liao, 2012

Revised by Chieh-Fu Chu, 2013

Revised by Guo-Yu Lin, 2014

Revised by Kuan-Yen Huang, 2015

Revised by Po-Wei Chen, 2018

Revised by Rih-Fong Yeh, 2018