**邏輯合成與驗證 HW1 學號:R05943029 修課學生:郭鈞哲**

**Part1**

1.BLIF file

.model 4bitadder

.inputs A3 A2 A1 A0 B3 B2 B1 B0 CIN

.outputs COUT S3 S2 S1 S0

.subckt fulladder a=A0 b=B0 cin=CIN s=S0 cout=CARRY1

.subckt fulladder a=A1 b=B1 cin=CARRY1 s=S1 cout=CARRY2

.subckt fulladder a=A2 b=B2 cin=CARRY2 s=S2 cout=CARRY3

.subckt fulladder a=A3 b=B3 cin=CARRY3 s=S3 cout=COUT

.end

.model fulladder

.inputs a b cin

.outputs s cout

.names a b cin s

100 1

010 1

001 1

111 1

.names a b cin cout

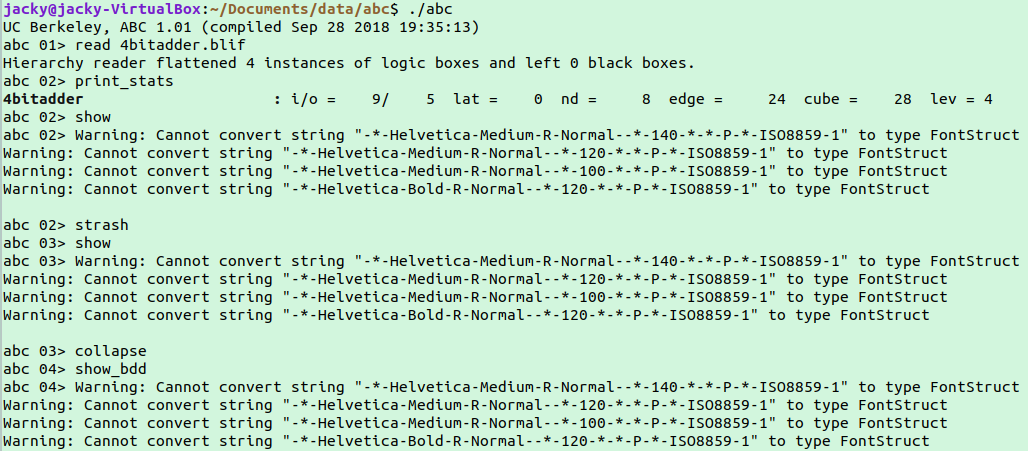
11- 1

1-1 1

-11 1

.end

2.Screenshot of your ABC execution steps



3.

result of “show” command

|  |  |
| --- | --- |
| Logic Network  C:\Users\張道寬\AppData\Local\Microsoft\Windows\INetCache\Content.Word\LN.PNG | Structurally Hashed Aig |

result of “show\_bdd”

|  |  |
| --- | --- |
| Result of COUT’s BDD  C:\Users\張道寬\AppData\Local\Microsoft\Windows\INetCache\Content.Word\COUT's bdd.png | Result of S3’s BDD  C:\Users\張道寬\AppData\Local\Microsoft\Windows\INetCache\Content.Word\S3's bdd.png |
| Result of S2’s BDD  C:\Users\張道寬\AppData\Local\Microsoft\Windows\INetCache\Content.Word\S2's bdd.png | Result of S1’s BDD  C:\Users\張道寬\AppData\Local\Microsoft\Windows\INetCache\Content.Word\S1's bdd.png |
| Result of S0’s BDD  C:\Users\張道寬\AppData\Local\Microsoft\Windows\INetCache\Content.Word\S0's bdd.png | |

**Part2**

(a)

1.

|  |  |
| --- | --- |
| By command “aig” | By command “strash” |
| Unsorted. Converts local functions of the nodes to AIGs | Transforms the current network into an AIG by one-level structural hashing. The resulting AIG is a logic network composed of two-input AND gates and inverters represented as complemented attributes on the edges. Structural hashing is a purely combinational transformation, which does not modify the number and positions of latches. |
|  |  |

2.

|  |  |
| --- | --- |
| By command “bdd” | By command “collapse” |
| Unsorted. Converts local functions of the nodes to BDDs. | Recursively composes the fanin nodes into the fanout nodes resulting in a network, in which each CO is produced by a node, whose fanins are CIs. Collapsing is performed by building global functions using BDDs and is, therefore, limited to relatively small circuits. After collapsing, the node functions are represented using BDDs. |
|  | C:\Users\張道寬\AppData\Local\Microsoft\Windows\INetCache\Content.Word\COUT's bdd.png |

(b)by using command “logic”, Transforms the AIG into a logic network with the SOP representation of the two-input AND-gates.