

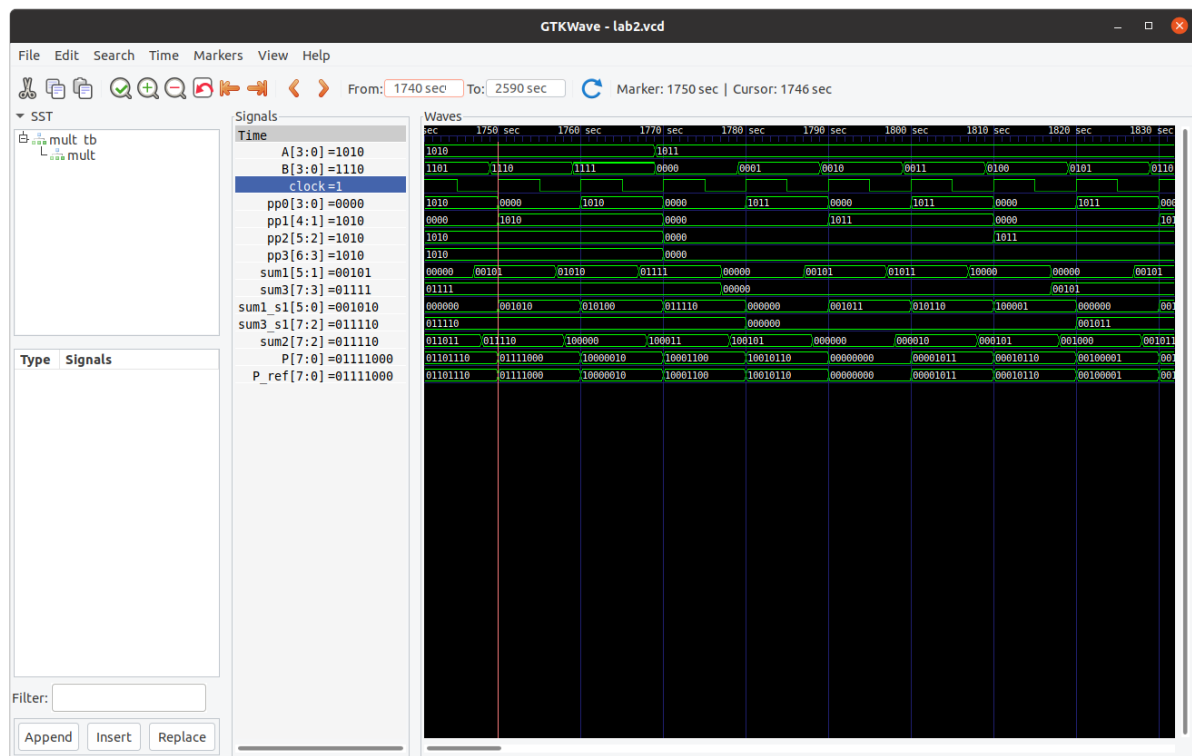
# Lab 2

## Lab 2: Part 1

### 1. `mult_fast` code

```
module mult_fast(
    output reg[7:0] P, // product
    input[3:0] A, B, // multiplicand and multiplier
    input clk // clock (posedge)
);
// stage 0 (input)
reg[3:0] a_s0, b_s0;
always @(posedge clk) begin
    a_s0 <= A;
    b_s0 <= B;
end
// stage 1
wire[3:0] pp0 = a_s0 & {4{b_s0[0]}}; // ignore the delays of AND gates
wire[4:1] pp1 = a_s0 & {4{b_s0[1]}}; // ignore the delays of AND gates
wire[5:2] pp2 = a_s0 & {4{b_s0[2]}}; // ignore the delays of AND gates
wire[6:3] pp3 = a_s0 & {4{b_s0[3]}}; // ignore the delays of AND gates
reg[5:1] sum1;
always @(pp0, pp1)
    sum1[5:1] <= #7 pp0[3:1] + pp1[4:1]; // delay of the 4-bit adder
reg[7:3] sum3;
always @(pp2, pp3)
    sum3[7:3] <= #7 pp2[5:3] + pp3[6:3]; // delay of the 4-bit adder
reg[5:0] sum1_s1;
reg[7:2] sum3_s1;
always @(posedge clk) begin
    sum1_s1 <= {sum1, pp0[0]};
    sum3_s1 <= {sum3, pp2[2]};
end
// stage 2 (output)
reg[7:2] sum2;
always @(sum1_s1, sum3_s1)
    sum2[7:2] <= #8 sum1_s1[5:2] + sum3_s1[7:2]; // delay of the 6-bit adder
always @(posedge clk) begin
    P <= {sum2, sum1_s1[1:0]};
end
endmodule
```

2. Show the waveform with the settings in `lab2.sav`, (should include 1750 to 1800 sec)



3. What is the latency (worst case waiting time from the input becomes steady to the register of the last stage refreshes)?

感覺是20秒(ticks)，觀察 $P = A \times B$ 的結果 (have to wait for the rising or falling edge, hence 20 instead of 21)

## Lab 2: Part 2

Minimize the clock cycle by changing the delays in the module multtb.

1. What is the minimum clock cycle?

8 ticks

2. screenshot

