JMicron Technology Corporation

PCB Layout Guide

JMS578

Document No.: LOG-16009 / Revision: 1.1 / Issue Date: 08-02-2017

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Printed in Taiwan 2017

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Revision History

Revision	Effect Date	Description of Revision		Author
		Reference	Description of the Change	
1.0	06-06-2014	--	Initial release.	Mika
1.1	08-02-2017		1.Add Cin placement rule 2.Add rule for remove area under capacitors	Jason

This document is valid until ☐ the date dd-mm-yyyy ☒ the next revision has been effective.

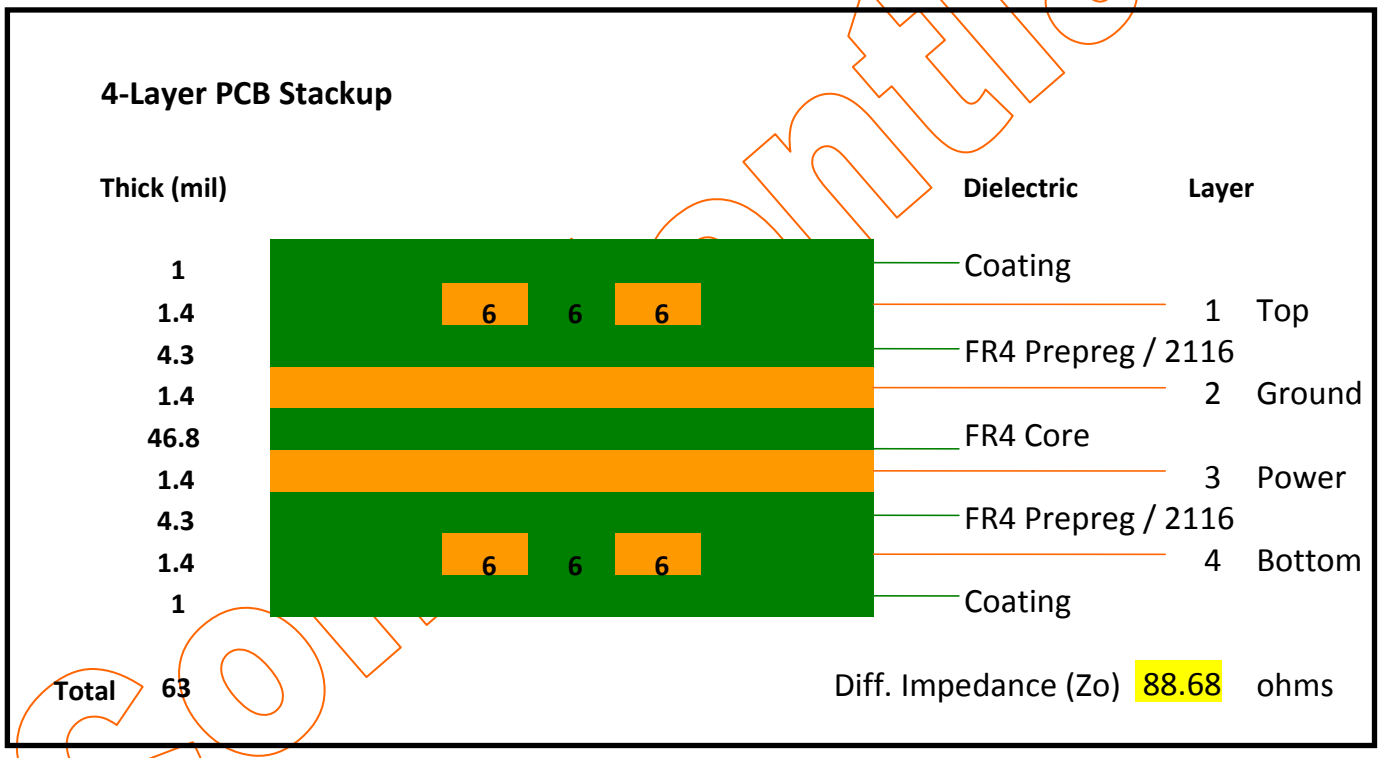
Table of Contents

1 Overviews

1.1 Description

This layout guide include USB3.0, SATA3.0, USB2.0, Power plane , Crystal and Switching Regulator .

1.2 PCB Stack up



2 USB3.0 Layout Guide

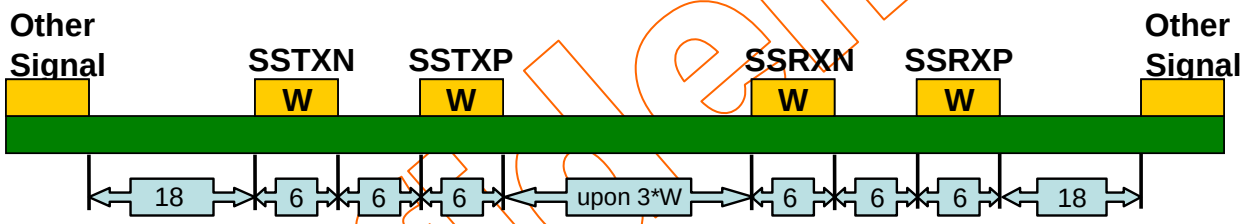
2.1 Relative Net Name & Pairs

USB3.0 have 2 differential signal pair，detailed information is as follows:

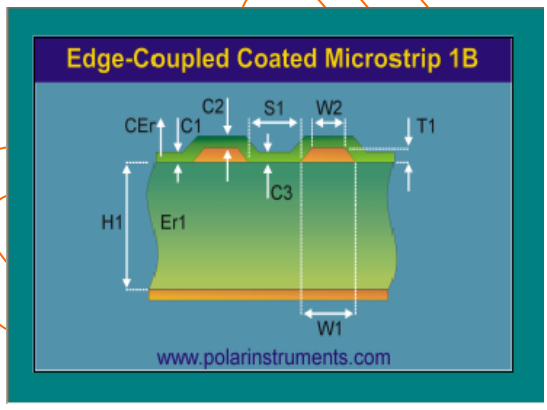
Net Name	Routing Layer	Reference Layer
SSTXP, SSTXN, SSRXN, SSRXP	1st layer	2nd layer (GND)

2.2 Net Spacing & Trace Length Rule

- USB Trace : Trace Width / Trace Separation / Pair Separation ＝ 6 / 6 / 18.0 mil]
  Target differential impedance: 89 Ω



Unit: mil



				Tolerance	Minimum	Maximum
Substrate 1 Height	H1	4.3000	+/-	0.0000	4.3000	4.3000
Substrate 1 Dielectric	Er1	4.3000	+/-	0.0000	4.3000	4.3000
Lower Trace Width	W1	6.0000	+/-	0.0000	6.0000	6.0000
Upper Trace Width	W2	6.0000	+/-	0.0000	6.0000	6.0000
Trace Separation	S1	6.0000	+/-	0.0000	6.0000	6.0000
Trace Thickness	T1	1.4000	+/-	0.0000	1.4000	1.4000
Coating Above Substrate	C1	1.0000	+/-	0.0000	1.0000	1.0000
Coating Above Trace	C2	1.0000	+/-	0.0000	1.0000	1.0000
Coating Between Traces	C3	1.0000	+/-	0.0000	1.0000	1.0000
Coating Dielectric	CEr	3.4000	+/-	0.0000	3.4000	3.4000
Differential Impedance	Zdiff	88.68			88.68	88.68

- USB3.0 trace length mismatch < 5mil.
- Away from the Oscillator , Switching Regulator LC , Power components and Power trace.

- Route all SuperSpeed USB signal traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.
- Do not route SuperSpeed USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

3 SATA3.0 Layout Guide

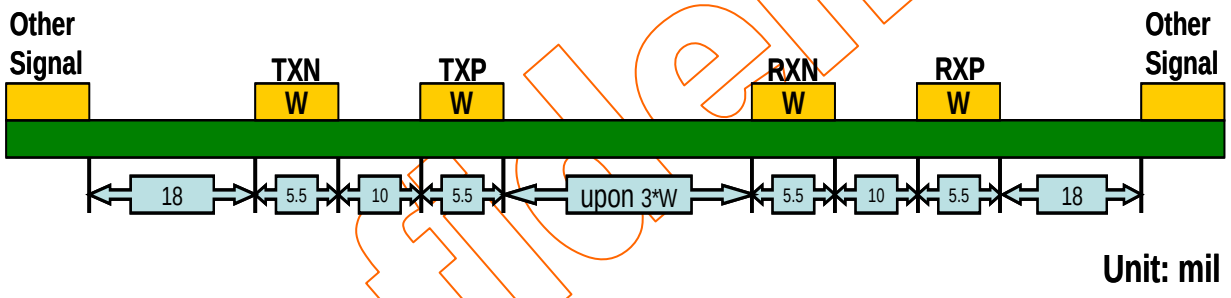
3.1 Relative Net Name & Pairs

SATA3.0 have 2 differential signal pair，detailed information is as follows:

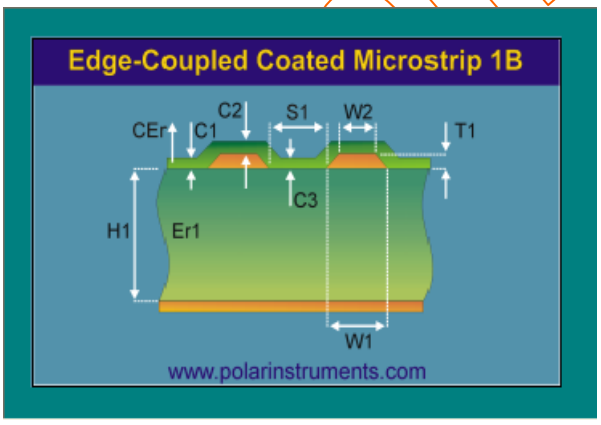
Net Name	Routing Layer	Reference Layer
TXP, TXN, RXN, RXP	1st layer	2nd layer (GND)

3.2 Net Spacing & Trace Length Rule

- SATA Trace : Trace Width / Trace Separation / Pair Separation ＝ 5.5 / 10 / 18.0 mil]
  Target differential impedance: 100 Ω



Unit: mil



				Tolerance	Minimum	Maximum
Substrate 1 Height	H1	4.3000	+/-	0.0000	4.3000	4.3000
Substrate 1 Dielectric	Er1	4.3000	+/-	0.0000	4.3000	4.3000
Lower Trace Width	W1	5.5000	+/-	0.0000	5.5000	5.5000
Upper Trace Width	W2	5.5000	+/-	0.0000	5.5000	5.5000
Trace Separation	S1	10.0000	+/-	0.0000	10.0000	10.0000
Trace Thickness	T1	1.4000	+/-	0.0000	1.4000	1.4000
Coating Above Substrate	C1	1.0000	+/-	0.0000	1.0000	1.0000
Coating Above Trace	C2	1.0000	+/-	0.0000	1.0000	1.0000
Coating Between Traces	C3	1.0000	+/-	0.0000	1.0000	1.0000
Coating Dielectric	CEr	3.4000	+/-	0.0000	3.4000	3.4000
Differential Impedance	Zdiff	100.03			100.03	100.03

- SATA3.0 trace length mismatch < 5mil.
- Away from the Oscillator , Switching Regulator LC , Power components and Power trace.

- Route all SATA signal traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.
- Do not route SATA traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

4 USB2.0 Layout Guide

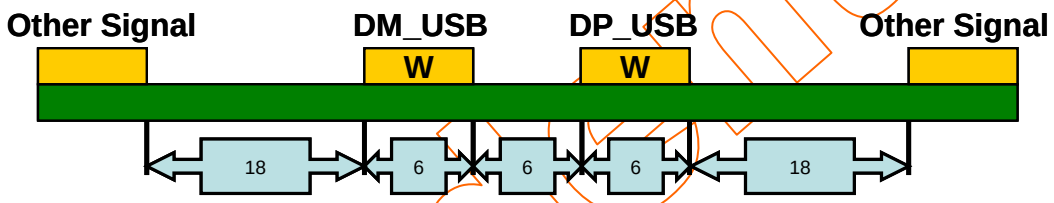
4.1 Relative Net Name & Pairs

USB2.0 have a differential signal pair，detailed information is as follows:

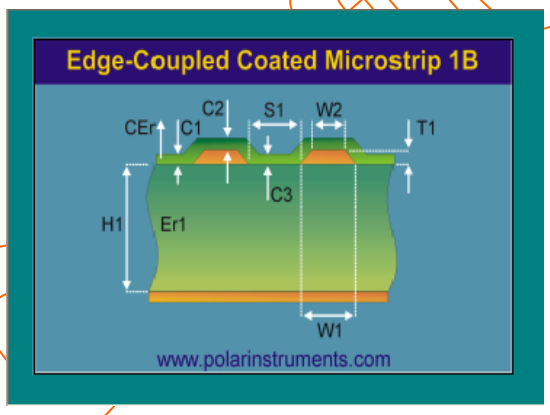
Net Name	Routing Layer	Reference Layer
DP_USB, DM_USB	1st layer	2nd layer (GND)

4.2 Net Spacing & Trace Length Rule

- USB Trace : Trace Width / Trace Separation / Pair Separation ＝ 6 / 6 / 18 mil]
  Target differential impedance: 89 Ω



Unit: mil



				Tolerance	Minimum	Maximum
Substrate 1 Height	H1	4.3000	+/-	0.0000	4.3000	4.3000
Substrate 1 Dielectric	Er1	4.3000	+/-	0.0000	4.3000	4.3000
Lower Trace Width	W1	6.0000	+/-	0.0000	6.0000	6.0000
Upper Trace Width	W2	6.0000	+/-	0.0000	6.0000	6.0000
Trace Separation	S1	6.0000	+/-	0.0000	6.0000	6.0000
Trace Thickness	T1	1.4000	+/-	0.0000	1.4000	1.4000
Coating Above Substrate	C1	1.0000	+/-	0.0000	1.0000	1.0000
Coating Above Trace	C2	1.0000	+/-	0.0000	1.0000	1.0000
Coating Between Traces	C3	1.0000	+/-	0.0000	1.0000	1.0000
Coating Dielectric	CEr	3.4000	+/-	0.0000	3.4000	3.4000
Differential Impedance	Zdiff	88.68			88.68	88.68

- USB2.0 trace length mismatch < 5mil.
- Away from the Oscillator , Switching Regulator LC , Power components and Power trace.
- Route all high-speed USB signal traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.

- Do not route high-speed USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

5 Crystal Layout Guide

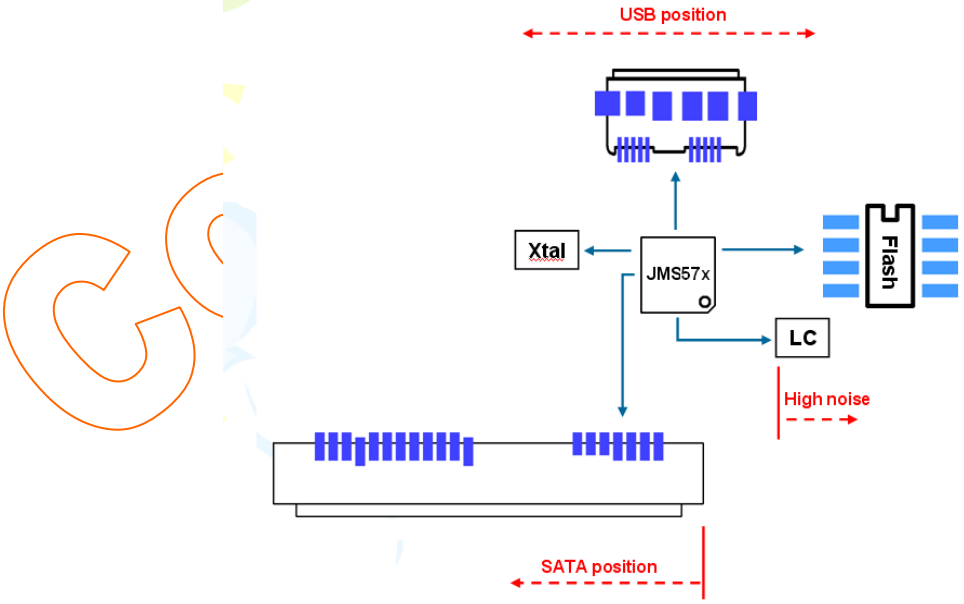
5.1 Relative Net Name & Pairs

The Oscillator/Crystal detailed information is as follows:

Net Name	Routing Layer	Reference Layer
XIN, XOUT	1st layer	2nd layer (GND)

5.2 Layout Rule

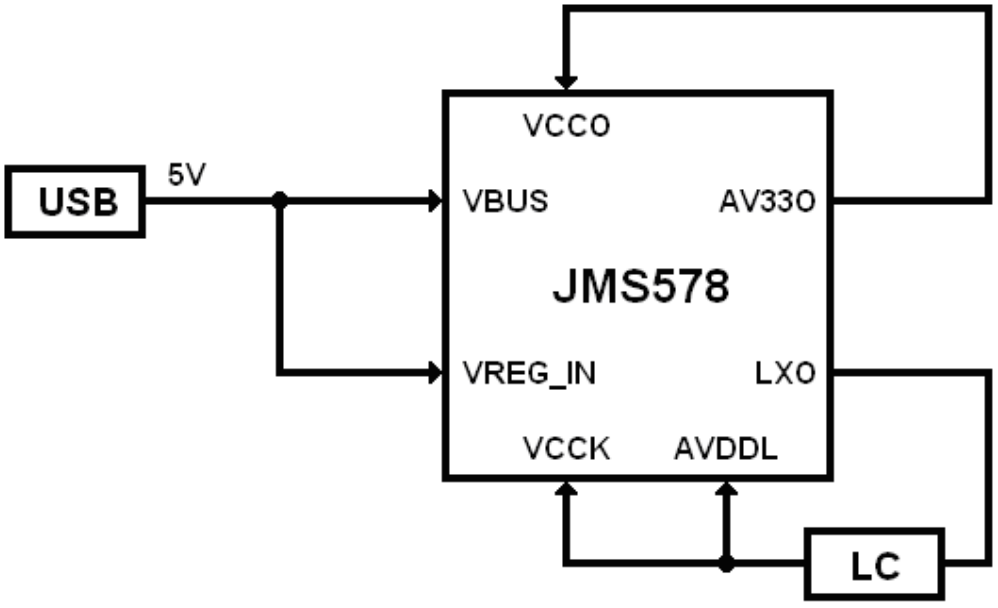
- The crystal unit should then be placed as close as possible to the XIN and XOUT pins to minimize etch lengths.
- Ensure that the ground plane under the IC and its components are of good quality.
- Avoid placing a separate ground under the oscillator and connecting it to the general ground through a single point.
- Avoid long connections to the crystal and to the load capacitor that create a large loop on the PCB.
- Use a short connection between the two crystal load capacitors and route the common connection to the IC ground reference.



6 Power Layout Guide

6.1 Relative Net Name

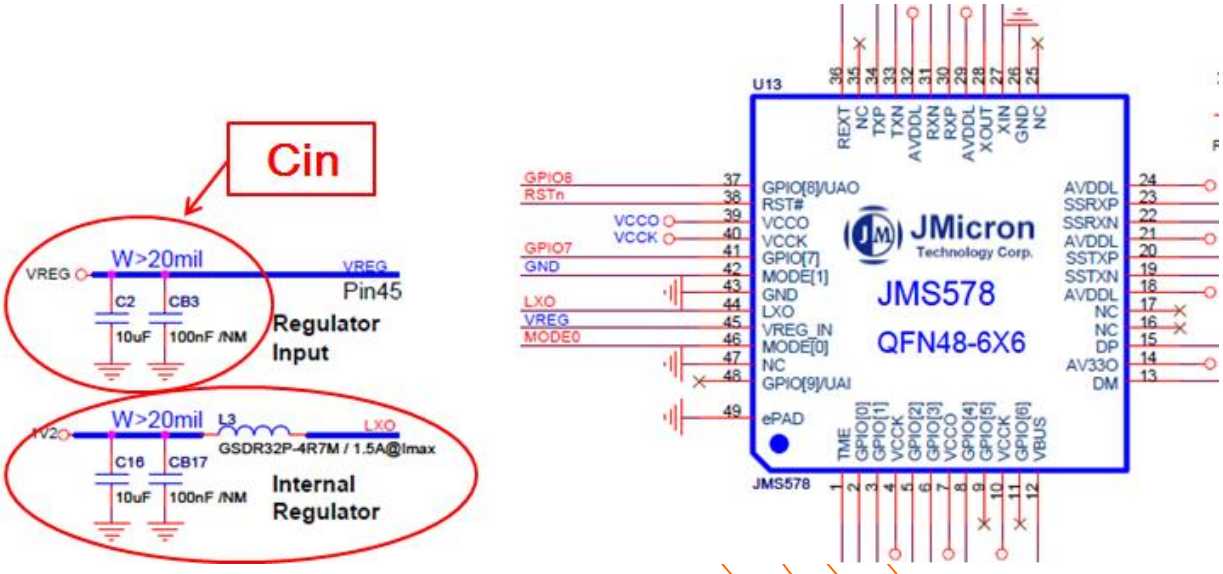
Power detailed information is as follows:



6.2 Layout Rule

- The width of 5V ≧ 60 mil (suggest 80mil)
- The width of AV33O , VCCO ≧ 15 mil (suggest 30 mil)
- The width of VREG_IN , LXO , VCCK , AVDDL ≧ 30 mil (suggest 40 mil)

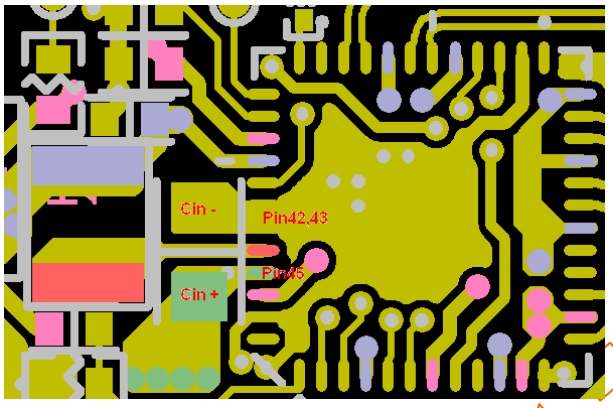
7 Switching Regulator LC Layout Guide



7.1 LC Layout Rule

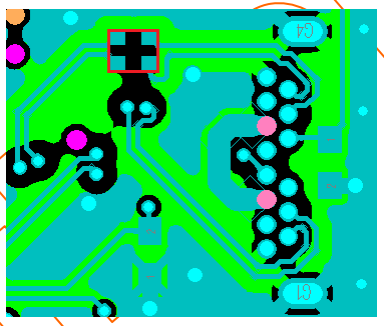
- Place the Cin as close as possible to Pin45 and Pin43.
- C16,CB17,L3 Away from the JMS578.
- C2, CB3, C16, CB17, L3 Away from USB signal and SATA signal.

Layout example for Cin



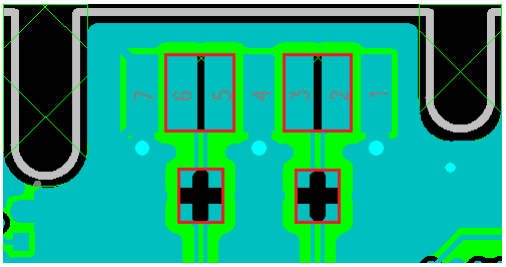
Note: 1. Cin- as close as possible to Pin43
2. Cin+ as close as possible to Pin45

Layout example for SATA connector



Note: Remove area under capacitors and SATA signals pins

Layout example for SATA connector



Note: Remove area under capacitors and SATA signals pins

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