

PCB Layout Guide

JMS578

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Revision History

| Revision | Effect Date | Description of Revision | | Author | |
|----------|-------------|-------------------------|--|--------|--|
| Revision | | Reference | Description of the Change | Author | |
| 1.0 | 06-06-2014 | | Initial release. | Mika | |
| 1.1 | 08-02-2017 | | 1.Add Cin placement rule 2.Add rule for remove area under capacitors | Jason | |
| | | | | | |
| | | | | | |
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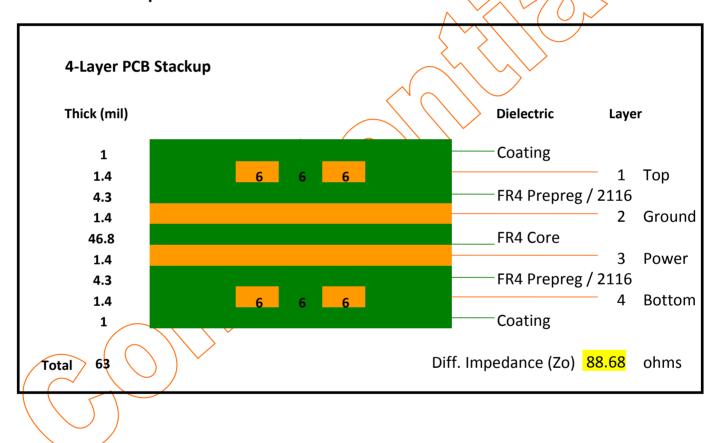


1 Overviews

1.1 Description

This layout guide include USB3.0, SATA3.0, USB2.0, Power plane, Crystal and Switching Regulator.

1.2 PCB Stack up



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2 USB3.0 Layout Guide

2.1 Relative Net Name & Pairs

USB3.0 have 2 differential signal pair, detailed information is as follows:

| Net Name | Routing I | _ayer | Reference Layer | | |
|---|---|-----------------------------|--|--|--|
| SSTXP, SSTXN, SSRXN, SSRXP | 1st laye | er | 2nd layer (GND) | | |
| 2.2 Net Spacing & Trace Length Rule | | | | | |
| ● USB Trace : Trace Width / Trace Separation / Pair Separation ← 6√6 18.0 mil] | | | | | |
| Target differential impedar | nce: 89 Ω / | \sim | $\overline{}$ | | |
| · | \sim | \sim / / | | | |
| | (| | | | |
| Other | | | Other | | |
| Signal SSTXN SSTXP | SSR | XN SSF | | | |
| W W | \\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ | V | | | |
| 18 - × 6 × 6 × 6 × 6 | ipon 3*W 6 | J-ж 6 J-ж 6 | Unit: mil | | |
| | Substrate 1 Height | H1 4.3000 +/- | Tolerance Minimum Maximum 0.0000 | | |
| Edge-Coupled Coated Microstrip 1B | Substrate 1 Dielectric | Er1 4.3000 +/- | 0.0000 4.3000 4.3000 | | |
| C2 S1 W2 | Lower Trace Width | W1 6.0000 +/- | 0.0000 6.0000 | | |
| CEr C1 T1 | Upper Trace Width | W2 6.0000 +/- | 0.0000 6.0000 | | |
| 1 1 1 1 1 1 1 1 1 | Trace Separation | S1 6.0000 +/- | 0.0000 6.0000 | | |
| C3 | Trace Thickness | T1 1.4000 +/- | 0.0000 1.4000 1.4000 | | |
| H1 Er1 | Coating Above Substrate | C1 1.0000 +/- | 0.0000 1.0000 1.0000 | | |
| | Coating Above Trace Coating Between Traces | C2 1.0000 +/- C3 1.0000 +/- | 0.0000 1.0000 1.0000 0.0000 1.0000 1.0000 | | |
| WI | Coating Dielectric | CEr 3.4000 +/- | 0.0000 3.4000 3.4000 | | |
| www.polarinstruments.com | | 3.1000 | | | |
| | Differential Impedance | Zdiff 88.68 | 88.68 88.68 | | |

- USB3.0 trace length mismatch < 5mil.
- Away from the Oscillator, Switching Regulator LC, Power components and Power trace.

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 Route all SuperSpeed USB signal traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.

 Do not route SuperSpeed USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.





3 SATA3.0 Layout Guide

3.1 Relative Net Name & Pairs

SATA3.0 have 2 differential signal pair, detailed information is as follows:

| Net Name | Routing I | _ayer | Reference Layer |
|---|--|---|---|
| TXP, TXN, RXN, RXP | 1st laye | er | 2nd layer (GND) |
| Net Spacing & Trace Length Rule | • | $\langle \rangle$ | |
| SATA Trace: Trace Width / Trace Se | paration / Pair Se | paration = | 5.5 / 10 / 18.0 mil] |
| Target differential impe | edance: 100 O | $^{\prime}$ | \wedge |
| . a. gat aa. ap. | | \sim | |
| | (| | |
| ther | | | Other |
| gnal <u>TXN</u> <u>TXP</u> | RX | N R | χP Signal |
| W W | W | V | |
| | | | _ |
| | | | |
| 18 5.5 7 10 5.5 | upon 3*W 5.5 | 10 - 10 5 | 5 18 5 Unit: mil |
| 18 5.5 7 10 5.5 |)) | | Unit: mil |
| | Substrate 1 Height | H1 4.3000 + | Unit: mil Tolerance Minimum Maximum 4.3000 4.3000 |
| Edge-Coupled Coated Microstrip 1B | Substrate 1 Height Substrate 1 Dielectric | H1 4.3000 +. Er1 4.3000 + | Tolerance Minimum Maximum /- 0.0000 4.3000 4.3000 /- 0.0000 4.3000 4.3000 |
| | Substrate 1 Height | H1 4.3000 + Er1 4.3000 + W1 5.5000 + | Unit: mil Tolerance Minimum Maximum 7- 0.0000 4.3000 4.3000 7- 0.0000 5.5000 5.5000 |
| Edge-Coupled Coated Microstrip 1B | Substrate 1 Height Substrate 1 Dielectric Lower Trace Width | H1 4.3000 + Er1 4.3000 + W1 5.5000 + | Unit: mil Tolerance Minimum Maximum -0.0000 4.3000 4.3000 -0.0000 5.5000 5.5000 -0.0000 5.5000 5.5000 |
| Edge-Coupled Coated Microstrip 1B CET C1 S1 W2 T1 C3 T1 | Substrate 1 Height Substrate 1 Dielectric Lower Trace Width Upper Trace Width | H1 4.3000 + Er1 4.3000 + W1 5.5000 + W2 5.5000 + | Tolerance Minimum Maximum 7- 0.0000 4.3000 4.3000 7- 0.0000 5.5000 5.5000 7- 0.0000 5.5000 5.5000 7- 0.0000 10.0000 10.0000 |
| Edge-Coupled Coated Microstrip 1B | Substrate 1 Height Substrate 1 Dielectric Lower Trace Width Upper Trace Width Trace Separation | H1 4.3000 + Er1 4.3000 + W1 5.5000 + W2 5.5000 + S1 10.0000 + | Tolerance Minimum Maximum 7- 0.0000 4.3000 4.3000 7- 0.0000 5.5000 5.5000 7- 0.0000 5.5000 5.5000 7- 0.0000 10.0000 10.0000 7- 0.0000 11.0000 11.4000 |
| Edge-Coupled Coated Microstrip 1B CET C1 S1 W2 T1 C3 T1 | Substrate 1 Height Substrate 1 Dielectric Lower Trace Width Upper Trace Width Trace Separation Trace Thickness | H1 | Unit: mil Tolerance Minimum Maximum 1. 0.0000 4.3000 4.3000 1. 0.0000 5.5000 5.5000 1. 0.0000 1.0000 1.0000 1. 0.0000 1.0000 1.0000 1. 0.0000 1.0000 1.0000 |
| Edge-Coupled Coated Microstrip 1B | Substrate 1 Height Substrate 1 Dielectric Lower Trace Width Upper Trace Width Trace Separation Trace Thickness Coating Above Substrate | H1 | Unit: mil Tolerance Minimum Maximum 7. 0.0000 4.3000 4.3000 7. 0.0000 5.5000 5.5000 7. 0.0000 1.0000 10.0000 7. 0.0000 1.4000 1.4000 7. 0.0000 1.0000 1.0000 7. 0.0000 1.0000 1.0000 |
| Edge-Coupled Coated Microstrip 1B | Substrate 1 Height Substrate 1 Dielectric Lower Trace Width Upper Trace Width Trace Separation Trace Thickness Coating Above Substrate Coating Above Trace | H1 | Unit: mil Tolerance Minimum Maximum 0.0000 4.3000 4.3000 0.0000 5.5000 5.5000 0.0000 10.0000 10.0000 0.0000 1.4000 1.4000 0.0000 1.0000 1.0000 0.0000 1.0000 1.0000 |

- SATA3.0 trace length mismatch < 5mil.
- Away from the Oscillator, Switching Regulator LC, Power components and Power trace.

Differential Impedance

Zdiff 100.03

100.03

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- Route all SATA signal traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.
- Do not route SATA traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.



6 / 6 / 18 mil

Unit: mil



4 USB2.0 Layout Guide

4.1 Relative Net Name & Pairs

USB2.0 have a differential signal pair, detailed information is as follows:

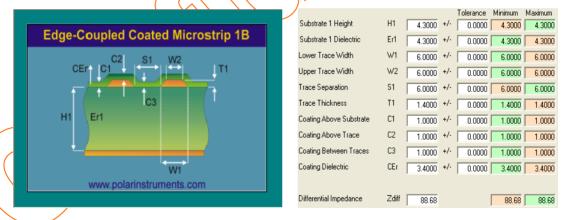
| | Net Name | Routing Layer | Reference Layer |
|-----|---------------------------------|---------------|-----------------|
| | DP_USB, DM_USB | 1st layer | 2nd layer (GND) |
| 4.2 | Net Spacing & Trace Length Rule | | |

Other Signal

W

W

Other Signal



- USB2.0 trace length mismatch < 5mil.
- Away from the Oscillator, Switching Regulator LC, Power components and Power trace.
- Route all high-speed USB signal traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.

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 Do not route high-speed USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.





5 Crystal Layout Guide

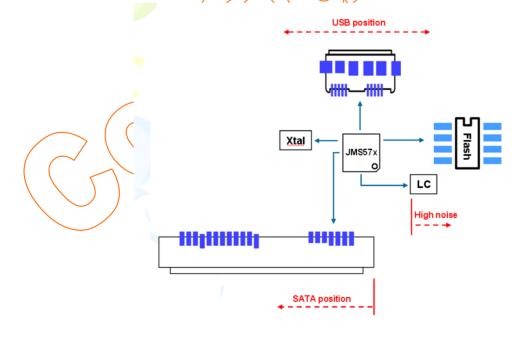
5.1 Relative Net Name & Pairs

The Oscillator/Crystal detailed information is as follows:

| Net Name | Routing Layer | Reference Layer |
|-----------|---------------|-----------------|
| XIN, XOUT | 1st layer | 2nd layer (GND) |

5.2 Layout Rule

- The crystal unit should then be placed as close as possible to the XIN and XOUT pins to minimize etch lengths.
- Ensure that the ground plane under the IC and its components are of good quality.
- Avoid placing a separate ground under the oscillator and connecting it to the general ground through a single point.
- Avoid long connections to the crystal and to the load capacitor that create a large loop on the PCB.
- Use a short connection between the two crystal load capacitors and route the common connection to the IC ground reference.

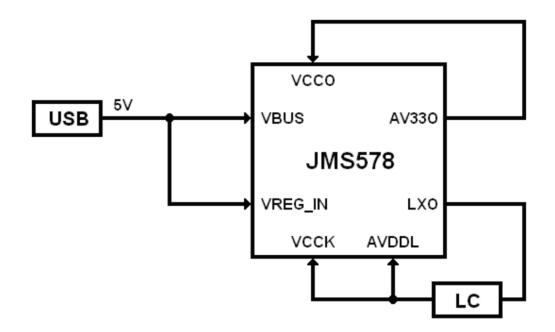


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6 Power Layout Guide

6.1 Relative Net Name

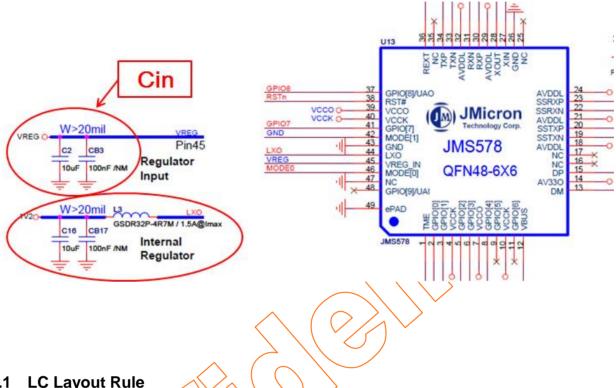
Power detailed information is as follows:



6.2 Layout Rule

- The width of 5√ ≥ 60 mil (suggest 80mil)
- The width of AV33O , $VCCO \ge 15$ mil (suggest 30 mil)
- The width of VREG_IN, LXO, VCCK, AVDDL ≥ 30 mil (suggest 40 mil)

7 Switching Regulator LC Layout Guide

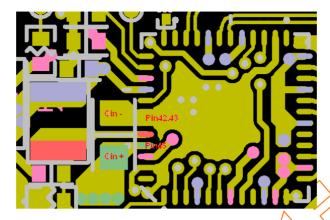


7.1 LC Layout Rule

- Place the Cin as close as possible to Pin45 and Pin43.
- C16,CB17,L3 Away from the JMS578.
- C2, CB3, C16, CB17, L3 Away from USB signal and SATA signal.



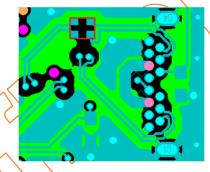
Layout example for Cin



Note: 1. Cin- as close as possible to Pin43

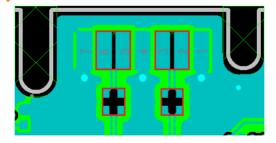
2. Cin+ as close as possible to Pin45

Layout example for SATA connector



Note: Remove area under capacitors and SATA signals pins

Layout example for SATA connector



Note: Remove area under capacitors and SATA signals pins

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