JMicron Technology Corporation

DATASHEET

JMS578
SuperSpeed USB to SATA 6.0Gb/s Bridge Controller

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Revision History

Revision number	Effective date	Description of revision		Author
		Reference	Description of change	
1.00	1/13/2015	--	Initial release.	Mika Cheng
1.01	9/2/2016		Removed the SPI list and performance benchmark: to individual documents due to frequent update.	Mika Cheng
1.02	1/20/2017		Revised Crystal pin assign	Mika Cheng
1.03	6/7/2017		1. Revised 26, 47 pin assign 2. Removed 4.6 Vbus detector	Mika Cheng
1.04	8/23/2017		1. Added the outline drawing of LQFP 2. Added package pin-out information of LQFP 3. Added the statement of product naming rule for LQFP	Mika Cheng
1.05	9/18/2017		Added the reason for removing SPI list and performance benchmark to the description of change of revision 1.01.	Larry Chien

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1 Introduction

JMS578 is a SuperSpeed USB to SATA 6Gb/s bridge controller with high performance and low power consumption. It can support external SPI NVRAM for Vendor VID/PID of USB2.0/USB3.0 device controller. It has 10 GPIOs to do customization for various applications. It supports software utilities for downloading the upgraded firmware code under USB2.0/USB3.0. It complies with both the USB Mass Storage Class Bulk-Only Transport (BOT) Specification and USB Attached SCSI Protocol (UASP) Specification.

2 Features

- Complies with Gen2i/Gen2m of Serial ATA II Electrical Specification 2.6
- Complies with Gen3 of Serial ATA III Electrical Specification 3.2
- Complies with USB 3.0 Specification, USB Mass Storage Class, Bulk-Only Transport Specification
- Complies with USB Attached SCSI Protocol (UASP) Specification
- Supports USB Super-Speed/High-Speed/Full-Speed Operation
- Supports USB2.0/USB3.0 power saving mode
- Supports SHA-1/SHA-256 for IEEE-1667 digest calculation
- Supports external SPI NVRAM for Vendor VID/PID of USB2.0/USB3.0 device controller
- Supports ATA/ATAPI PACKET command set
- 10 GPIOs for customization
- Provides hardware control PWM
- Provides software utilities for downloading the upgraded firmware code under USB2.0/USB3.0
- Design for Windows 7, Windows 10 and MAC 10.9.5 or later version.
- Supports 30MHz external crystal
- Embedded 5V to 1.2V voltage regulator
- Embedded 5V to 3.3V linear voltage regulator (LDO)
- QFN48 package (6x6) and LQFP48 package (7x7)

3 Block diagram

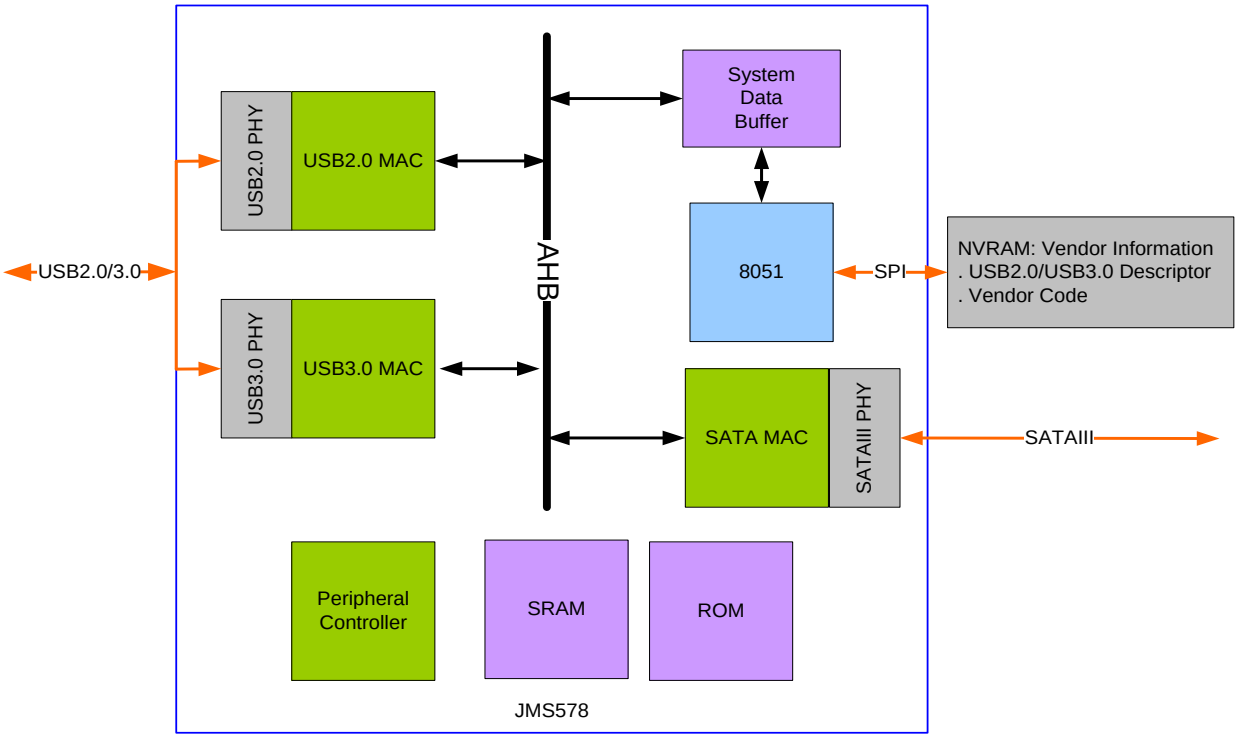
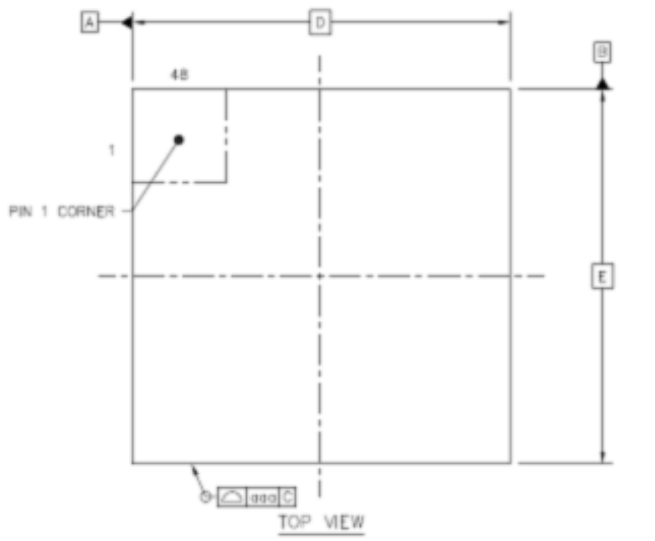
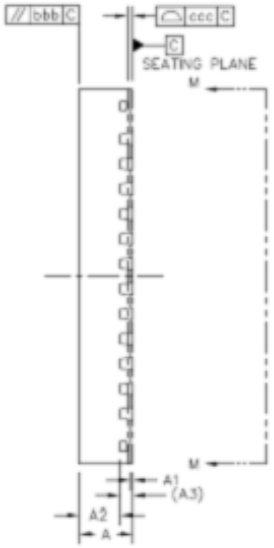


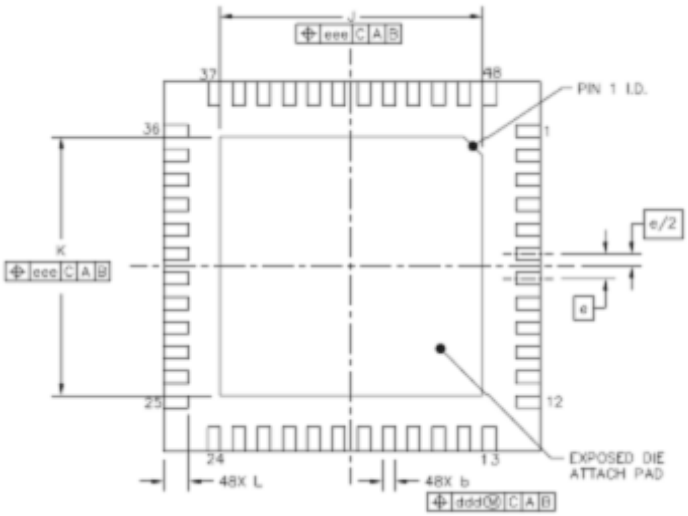
Figure 1 Block diagram

4 Package dimension

4.1 QFN48 6x6







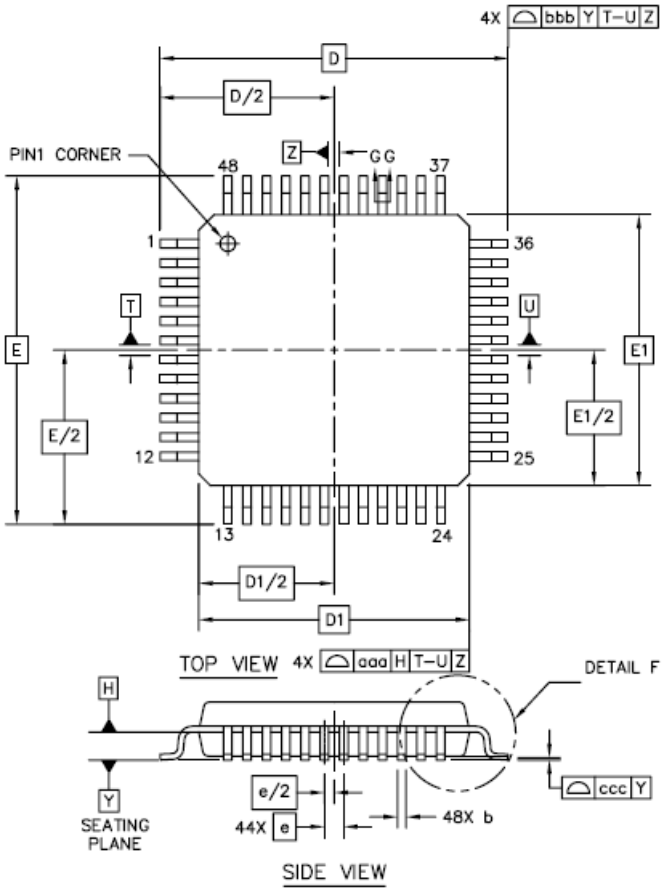
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	4.1	4.2	4.3
	Y	K	4.1	4.2	4.3
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Unit: mm

Note: The ground pad size is (J * K)

Figure 2 Package dimension of QFN48 6x6

4.2 LQFP48 7x7



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	---	1.45
LEAD WIDTH(PLATING)		b	0.17	---	0.27
LEAD WIDTH		b1	0.17	---	0.23
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.5 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.08		
MOLD FLATNESS		eee	0.05		

Unit: mm

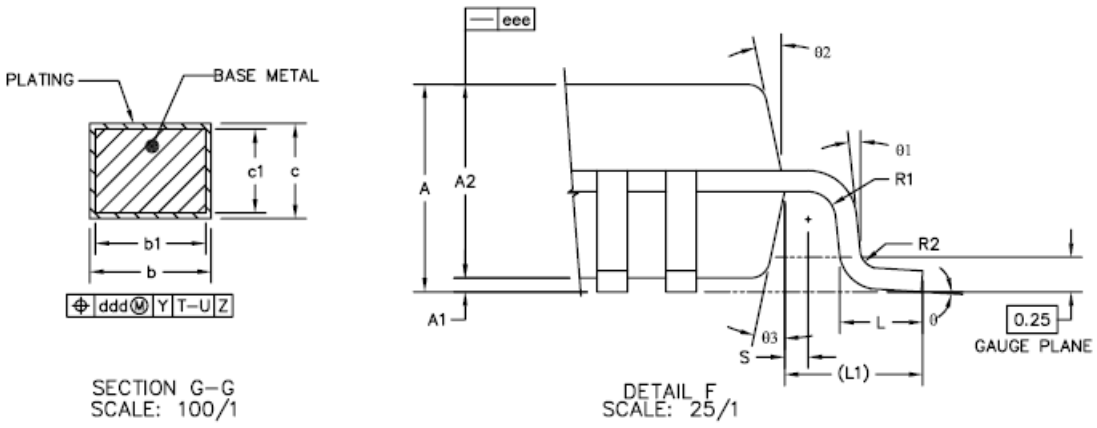


Figure 3 Package dimension of LQFP48 7x7

5 Package pin-out

5.1 Pin assignment

5.1.1 QFN48

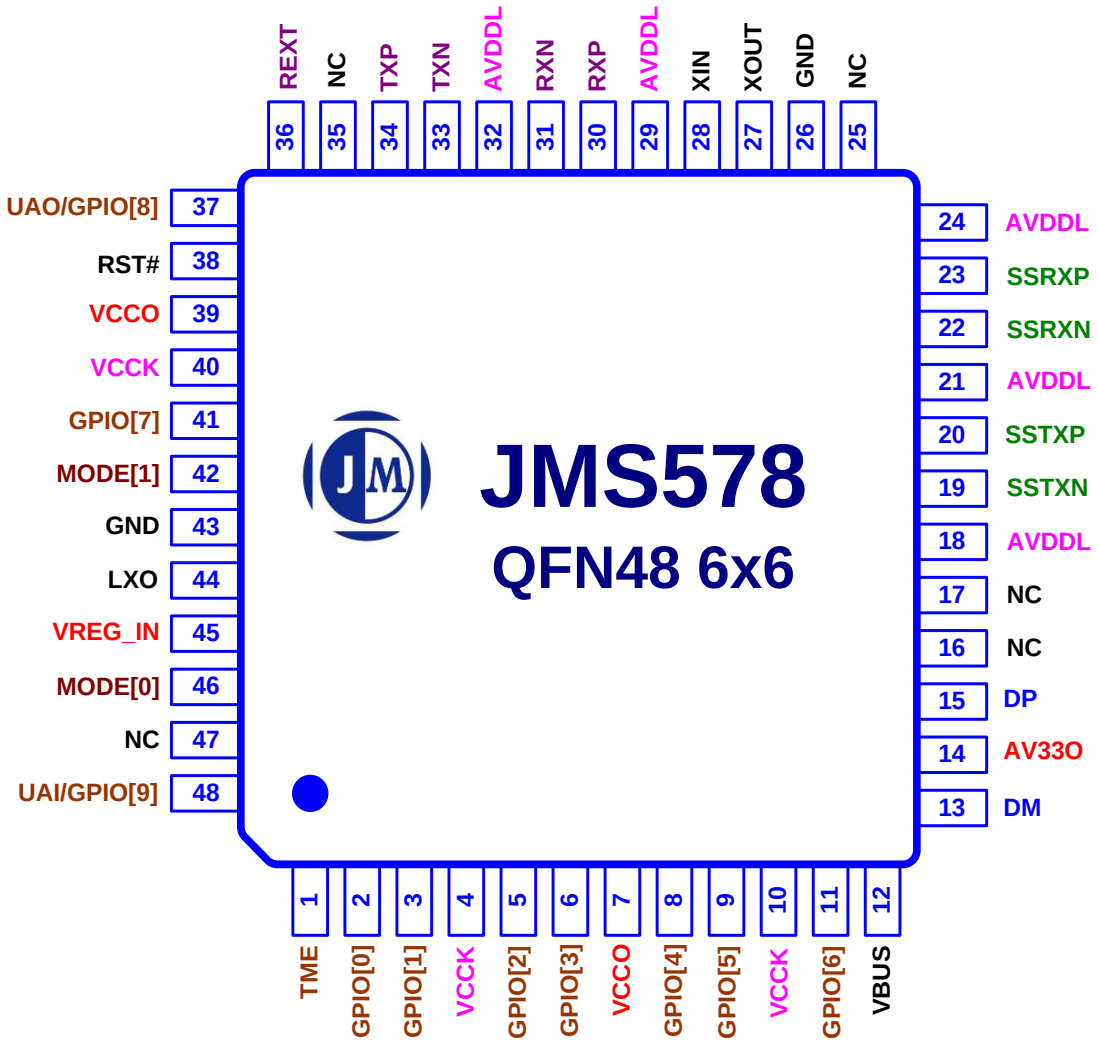


Figure 4 Pin assignment of QFN48

5.1.2 LQFP48

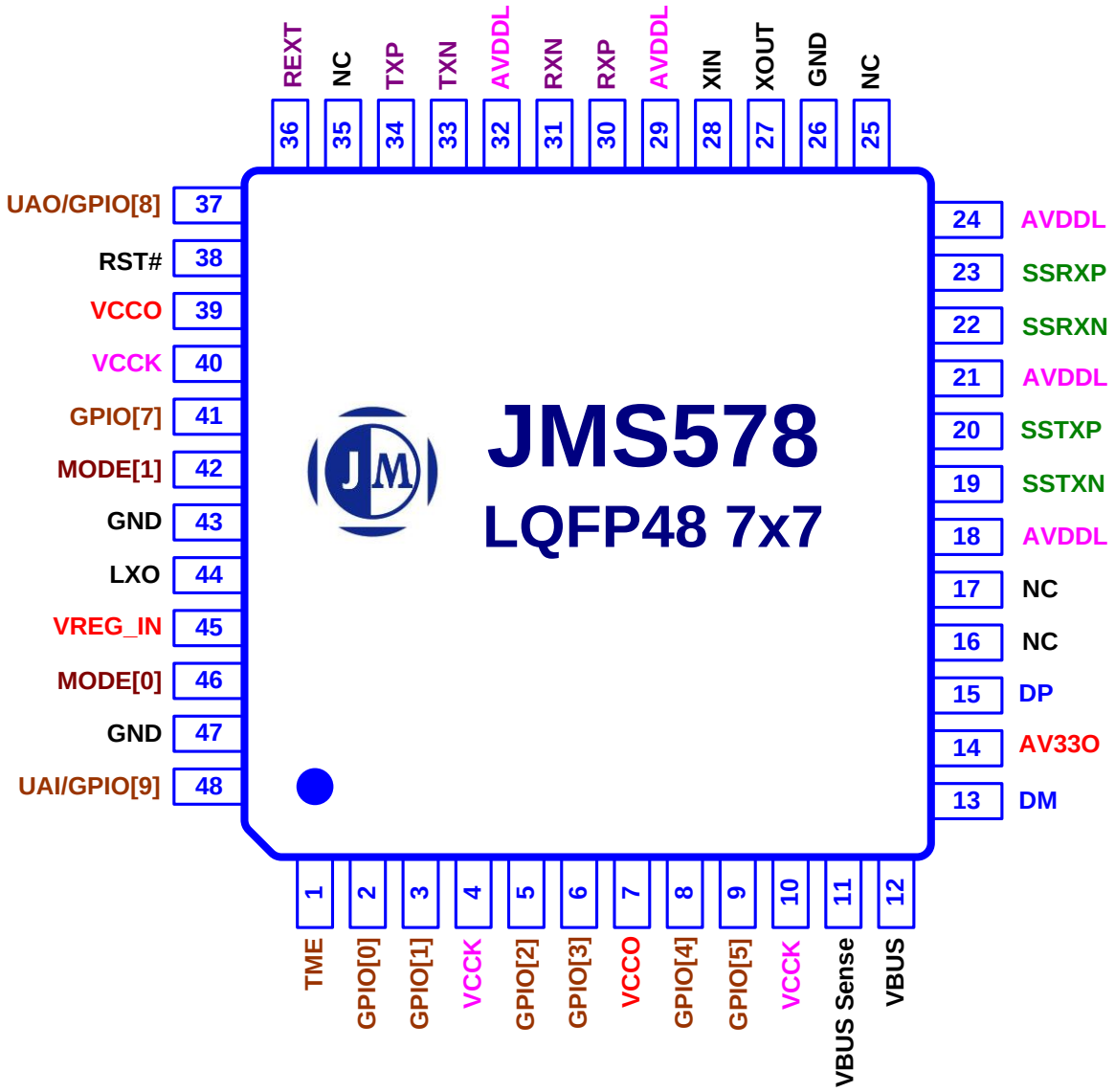


Figure 5 Pin assignment of LQFP48

5.2 Pin type definition

Table 1 Pin type definition

Pin Type	Definition
A	Analog
D	Digital
I	Input
O	Output
IO	Bi-directional
L	Internal weak pull-low (Max. 164KΩ, Typical 96 KΩ, Min. 61KΩ)
H	Internal weak pull-high (Max. 141KΩ, Typical 93 KΩ, Min. 66KΩ)

5.3 Pin description

5.3.1 Serial ATA interface

Table 2 Description of Serial ATA interface pins

Signal Name	Pin No.		Type	Description
	QFN	LQFP		
RXP	30	30	AI	**Serial ATA Port RX+ signal.** A 10nF CAP should be connected between this pin and SATA connector.
RXN	31	31	AI	**Serial ATA Port RX- signal.** A 10nF CAP should be connected between this pin and SATA connector.
TXP	34	34	AO	**Serial ATA Port TX+ signal.** A 10nF CAP should be connected between this pin and SATA connector.
TXN	33	33	AO	**Serial ATA Port TX- signal.** A 10nF CAP should be connected between this pin and SATA connector.
NC	35	35	AI	**Non Connect** Don't Care on the connectivity
AVDDL	32	32	AI	**SATA Analog 1.2V Power Supply.**
REXT	36	36	AI	**External Reference Resistance.** A 12KΩ±1% external resistor should be connected to this pin.

5.3.2 USB3.0 interface

Table 3 Description of USB3.0 interface pins

Signal Name	Pin No.		Type	Description
	QFN	LQFP		
SSRXP	23	23	AI	**Super Speed RX+ signal.**
SSRXN	22	22	AI	**Super Speed RX- signal.**
SSTXP	20	20	AO	**Super Speed TX+ signal.** A 100nF CAP should be connected between this pin and USB connector.
SSTXN	19	19	AO	**Super Speed TX- signal.** A 100nF CAP should be connected between this pin and USB connector.
NC	16	16	N/A	**Non Connect** Don't Care on the connectivity
NC	17	17	N/A	**Non Connect** Don't Care on the connectivity
AVDDL	18,21,24	18,21,24	AI	**USB3.0 Analog 1.2V Power Supply.**

5.3.3 USB2.0 interface

Table 4 Description of USB2.0 interface pins

Signal Name	Pin No.		Type	Description
	QFN	LQFP		
DM	13	13	AIO	**USB2.0 Bus D- Signal.**
DP	15	15	AIO	**USB2.0 Bus D+ Signal.**
VBUS	12	12	AI	**USB2.0/3.0 Cable Power Input.**
AV33O	14	14	AO	**USB2.0 Analog 3.3V Output.** A capacitance to ground is recommended on this pin. The value should be 1uF. The output voltage range is 3.3V±10%. Note: 1. This PIN provides power less than 100mA @ 3.3V. 2. This pin can afford chip internal power usage only.

5.3.4 Crystal interface

Table 5 Description of crystal interface pins

Signal Name	Pin No.		Type	Description
	QFN	LQFP		
XIN	28	28	AI	**Crystal Input/Oscillator Input.** It is connected to a 30MHz crystal or crystal oscillator. The variation range should be ±30ppm. And the input voltage should range in 1.2V±5%.
XOUT	27	27	AO	**Crystal Output.** It is connected to a crystal. While crystal oscillator is applied, this pin should be reserved as No Connection (NC). The output variation range is around ±30ppm (input dependent). And the output voltage range is 1.2V±5% (input dependent).
NC	25	25	N/A	**Non Connect** Don't Care on the connectivity
AVDDL	29	29	AI	**1.2V Analog Power Supply**

5.3.5 Voltage regulation

Table 6 Description of voltage regulation interface pins

Signal Name	Pin No.		Type	Description
	QFN	LQFP		
VREG_IN	45	45	AI	**Voltage Regulator Power Supply**
GND	43	43	AI	**Voltage Regulator Ground**
LXO	44	44	AO	**Voltage Regulator Output** Switch node. Connect with external power inductor with a value of 4.7uH.

5.3.6 Digital power and system control interface

Table 7 Description of digital power and system control interface pins

Signal Name	Pin No.		Type	Description
	QFN	LQFP		
VCCO	7, 39	7, 39	P	**3.3V I/O Power Supply.**
VCCK	4, 10, 40	4, 10, 40	P	**1.2V Core Power Supply.**
GND	E-PAD, 26	26, 47	P	**Ground.**
RST#	38	38	DI	**System Global Reset Input.** Schmitt trigger input pin. Active-low to reset the entire chip. An external RC should be connected to this pin.
TME	1	1	DI	**MP Test Mode Enable.** Schmitt trigger input pin. This pin is reserved for IC mass production testing. Keep this pin to logic “0” in normal operation.
MODE[1:0]	42, 46	42, 46	DIL	**Chip Operation Mode Selection.** Value MODE[1:0] = 2’b01 is recommended in normal operation. For the others, they are using in IC mass production testing.
GPIO[0]	2	2	DIOH	**Serial Flash (SO)** After power on status detecting, this pin becomes Data Output of serial flash. This pin is by default set to input.
GPIO[1]	3	3	DIOH	**Serial Flash (SCK)** This pin is Serial Flash Data Clock (SCK) of serial flash. This pin is by default set to output.
GPIO[2]	5	5	DIOH	**Serial Flash(SI)** Serial Flash Data Input (SI) of serial flash. This pin is by default set to output.
GPIO[3]	6	6	DIOH	**Serial Flash(CE0#**) This pin functions as Chip Enable (CE0#) of Serial Flash
GPIO[4]	8	8	DIOH	**GPIO[4]** Can be configured by customer firmware.
GPIO[5]	9	9	DIOH	**GPIO[5]** Can be configured by customer firmware.
GPIO[6]	11	11	DIOH	**GPIO[6]** Can be configured by customer firmware.
GPIO[7]	41	41	DIOH	**GPIO[7]** Can be configured by customer firmware.
UAO/GPIO[8]	37	37	DIOH	**8051 UART interface/GPIO[8]** Can be configured by customer firmware.
UAI/GPIO[9]	48	48	DIOH	**8051 UART interface/GPIO[9]** Can be configured by customer firmware.
NC	47	-	N/A	**Non Connect** Don’t Care on the connectivity or connect to ground

LED indicator

By default, GPIO[4] is used as HDD access indicator. If user has different application for LED function, please contact JMicron's AE before PCB layout.

GPIO initial value

All GPIOs are set as input mode and their internal pull-up function is enabled during reset.

After reset, the firmware code programs all of GPIOs as input mode, and then the initial values of GPIOs are read and stored in the system RAM for future usage.

6 Clock and reset

6.1 Crystal input

Table 8 Crystal input

Parameter	Symbol	Min	Typical	Max	Unit
Crystal start up time vs. AVDDL	$\mathbf{T}_{Crystal}$			150	mS
Crystal frequency	f_{clk}		30		MHz
Long term stability (crystal only)	$\Delta\mathbf{f}_{MAX\_Crystal}$	-30		30	ppm
Long term stability (on board)	$\Delta\mathbf{f}_{MAX\_OnBoard}$	-150		150	ppm
Equivalent series resistance	**ESR**			55	OHM
Drive level	**DL**		50		uW

6.2 Reset input

All functions will be initialized by reset except the Analog Power-On Reset Circuit depending on the Power on-off.

The reset input pin is the Schmitt trigger input pin. VT+ Schmitt Trigger Low to High Threshold Point is 1.31V and VT- Schmitt Trigger High to Low Threshold Point is 0.96V.

7 Electrical characteristics

7.1 Absolute maximum rating

Table 9 Absolute maximum rating

Parameter	Symbol	Min	Max	Unit
Digital 3.3V power supply	$VCCO_{(ABS)}$	-0.3	3.6	V
Digital 1.2V power supply	$VCCK_{(ABS)}$	-0.3	1.32	V
Analog 1.2V power supply	$AVDDL_{(ABS)}$	-0.3	1.32	V
Digital I/O input voltage	$V_{I(D)}$	-0.3	3.6	V
USB VBUS power supply	VBUS	4.0	5.5	V
Storage Temperature	$T_{STORAGE}$	-40	150	^{o}C

7.2 Recommended power supply operation conditions

Table 10 Recommended power supply operation conditions

Parameter	Symbol	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO	3.0	3.3	3.6	V
Digital 1.2V power supply	VCCK	1.08	1.2	1.32	V
Analog 1.2V power supply	AVDDL	1.08	1.2	1.32	V
Digital I/O input voltage	$V_{I(D)}$	0	3.3	3.6	V
Ambient operation temperature	T_A	0		70	^{o}C
Case operation temperature	T_C	0		90	^{o}C
Junction Temperature	T_J			125	^{o}C

7.3 Recommended external clock source conditions

Table 11 Recommended external clock source conditions

Parameter	Symbol	Min	Typical	Max	Unit
External reference clock			30		MHz
Clock Duty Cycle		45	50	55	%

7.4 Power supply DC characteristics

7.4.1 Power on (no USB connected)

Table 12 Power supply DC characteristics – Power on (no USB connected)

USB2.0 PHY, USB3.0 PHY and SATA PHY are OFF.

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO	Operate @3.3V	0.01	0.1	0.3	mA
Digital 1.2V power supply	VCCK	Operate @1.2V	22	26.5	35	mA
Analog 1.2V power supply	AVDDL	Operate @1.2V	20	22	30	mA

7.4.2 USB2.0 to SATA mode

Table 13 Power supply DC characteristics – USB2.0 to SATA mode

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO	Operate @3.3V	0.1	0.2	0.5	mA
Digital 1.2V power supply	VCCK	Operate @1.2V	50	55	65	mA
Analog 1.2V power supply	AVDDL	Operate @1.2V	110	117	130	mA

7.4.3 USB3.0 to SATA mode

Table 14 Power supply DC characteristics – USB3.0 to SATA mode @ U0 state

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO	Operate @3.3V	0.1	0.2	0.5	mA
Digital 1.2V power supply	VCCK	Operate @1.2V	75	82	90	mA
Analog 1.2V power supply	AVDDL	Operate @1.2V	160	175	185	mA

Table 15 Power supply DC characteristics – USB3.0 to SATA mode @ U3 state (suspend @S4)

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO	Operate @3.3V	0.1	0.2	0.5	mA
Digital 1.2V power supply	VCCK	Operate @1.2V	1	2	4	mA
Analog 1.2V power supply	AVDDL	Operate @1.2V	2	3	6	mA

Table 16 Power supply DC characteristics – USB3.0 to SATA mode @ U1/U2 state

No pending commands, SATA OFF, USB2 OFF.

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO	Operate @3.3V	0.1	0.2	0.3	mA
Digital 1.2V power supply	VCCK	Operate @1.2V	19	24	29	mA
Analog 1.2V power supply	AVDDL	Operate @1.2V	15	20	25	mA

7.5 I/O DC characteristics

Table 17 I/O DC characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Input low voltage	V_{IL}			0.7	V
Input high voltage	V_{IH}	1.5			V
Output low voltage	V_{OL}			0.3	V
Output high voltage	V_{OH}	1.9			V
Output Current	I_O		10	12	mA

7.6 Switching power efficiency (VREG_IN)

Efficiency = $Vout \times Iout / Vin \times Iin$, Vin = 5V, Vout = 1.2V

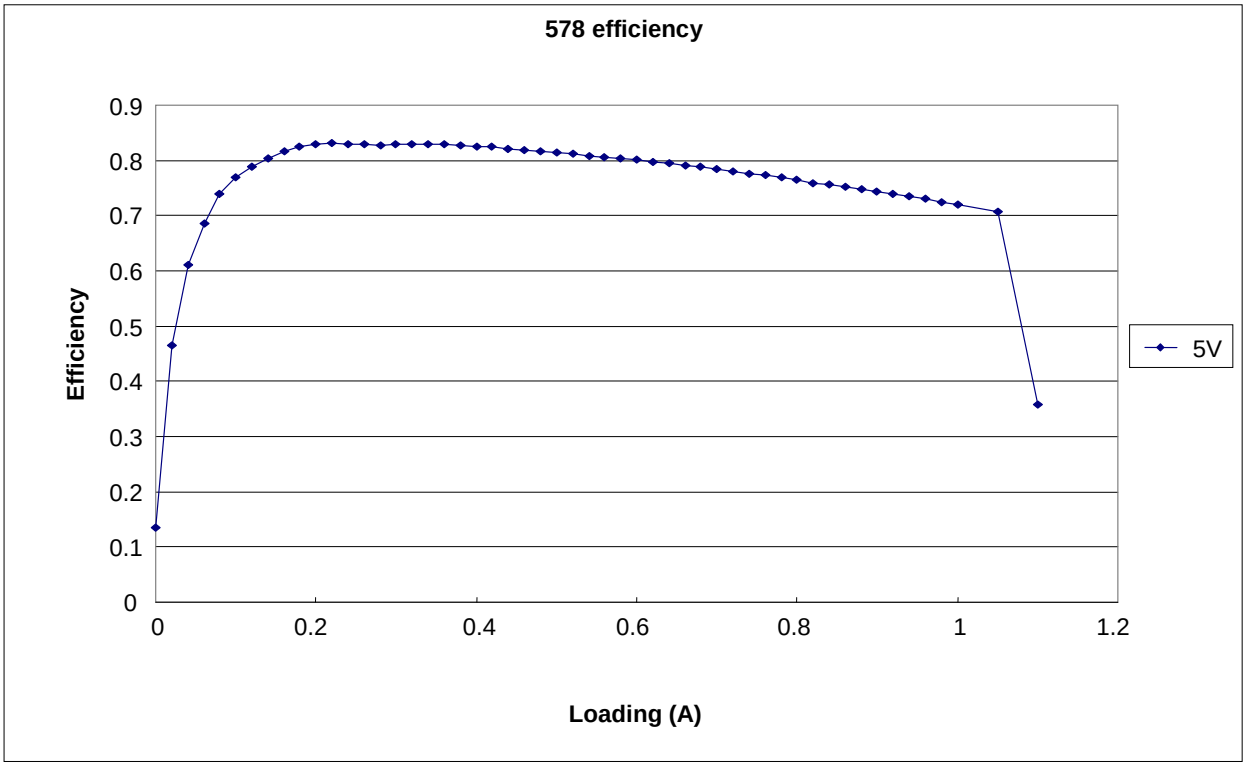


Figure 6 Switching power efficiency

7.7 Internal linear regulator

Table 18 Internal liner regulator

Parameter	Symbol	Min	Typical	Max	Unit
Input voltage range	V_{IN_LINEAR}	4	5	5.5	V
Output voltage range	V_{OUT_LINEAR}	3.10	3.3	3.45	V
Max output current	I_{MAX}	-	-	100	mA

7.8 Power ripple

Table 19 Power ripple

Parameter	Symbol	Condition	Min	Typical	Max	Unit
5V Power Supply [1]	P_{5V}	Operate @ USB3.0	-	80	150	mV
3.3V Power Supply [2]	P_{3V3}	Operate @ USB3.0	-	80	150	mV
1.2V Power Supply [3]	P_{1V2}	Operate @ USB3.0	-	80	100	mV

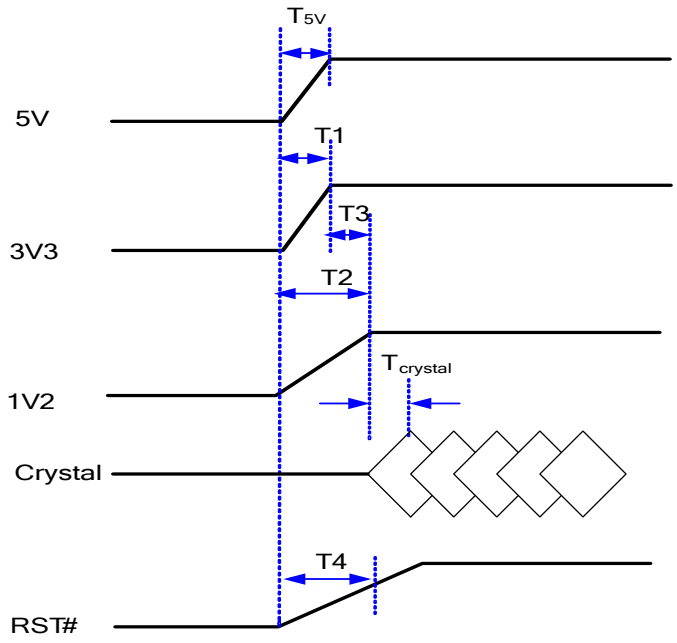
Notes: 1. Test point near Vbus capacitor.

2. Test point at LDO output capacitor.

3. Test point at AVDDL bypass capacitor.

7.9 Power-on sequence

The power-on sequence rules are defined in this section. Designers should follow all the rules for external power designs.



T_{5V}: Rise time for 5V power rail from 10% to 90%

T1: Rise time for 3V3 power rail from 10% to 90%

T2: Rise time for 1V2 power rail from 10% to 90%

T3: Time interval between 3.3V power and 1.2V power

T4: Rise time for RST# signal from 0.0V to 2.2V

$T_{Crystal}$: Time interval between 1.2V and 90% clock swing

Note: Clock must meet 30MHz +/-30ppm in the mean time.

Figure 7 Illustration of power-on sequence

The recommended power sequence and timing requirements are listed as below.

Table 20 Recommended power sequence and timing requirements

Time	Minimum	Maximum
T_{5V}	-	20 ms
T1	0.0 ms	10 ms
T2	0.0 ms	10 ms
T3	-10 ms	10 ms
T4	100 ms	500 ms
Tcrystal	-	150.0 ms

The RESET timing constrain is based on the external RC reset circuits. In order to control the charge and discharge time for RC circuits, minimum and maximum requirements are listed. If designers apply timing control chip to control the reset signal, the only requirement will be minimum value. In other words, the maximum value can be skipped without problems.

8 Internal switch regulator

- Input voltage range: 2.25V ~ 5.50V
- Output voltage range: 1.05V ~ 1.32V (programmable)
- Output voltage accuracy : I_{LOAD}= 700 mA, V_{OUT}±10%
- Max. output current : 700 mA
- Over-current protection (OCP): Yes (1,500mA)
- Input capacitor: 10uF
- Output capacitor: 10uF ~ 20uF
- Output inductor: 4.7uH
- Start-up time : < 500us
- Thermal shutdown: No
- Faster shutdown: No

9 Product naming rule and ordering information

9.1 Format of the part number

The part number covers the information of the provider, product category, device number, package type, material type, product grade (based on operating temperature), mask ROM version and device version. The format of the part number is illustrated in **Figure 8** below.

Figure 8 Format of the part number

9.2 Definition of the part number

Table 21 defines each section of the part number illustrated in **Figure 8**.

Table 21 Explanation of the part number

Section	Length	Designation	Code(s)	Definition
a	2 digits	Brand name	JM	**JM**icron
b	1 digit	Product category	S	**S**uper**S**peed USB
c	3 digits	Device number	578	The serial number assigned randomly to form the device name "**JMS578**" in conjunction with brand name and product category.
d	1 digit	Package type	L Q	L = **L**QFP Q = **Q**FN
e	1 digit	Material & grade	G U	G = RoHS compliant **G**reen product with JEDEC MSL 3 and commercial grade operating temperature ranging from 0 to 70°C. U = "G" product encapsulated using the **U**ltra low alpha particle mold compound required by the specific customer.
f	1 digit	Internal bonding type	A	Wire bonding option **A**
g	2 digit	Version of mask ROM	A1	Version **A1**
h	1 digit	Version of the IC	A	Version **A**