UNIVERSIDADE FEDERAL DE SANTA CATARINA
DEPARTAMENTO DE ENGENHARIA ELÉTRICA
EEL - 7020 SISTEMAS DIGITAIS

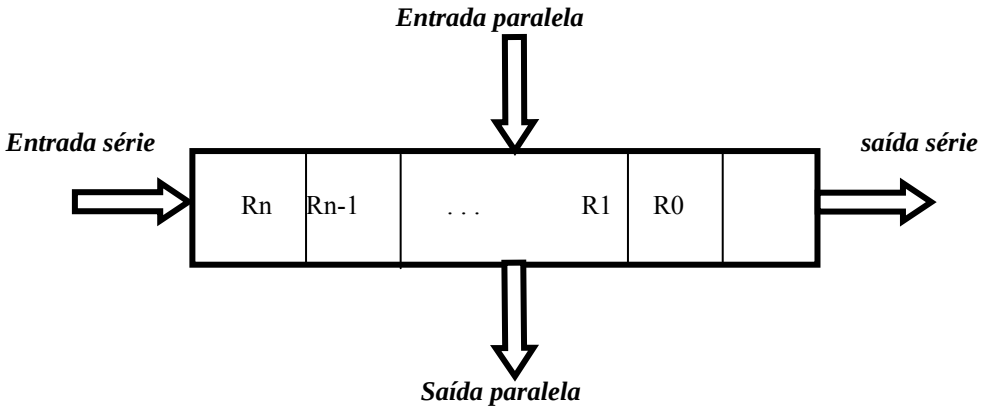
EXP. 9: REGISTRADOR DE DESLOCAMENTO

1. Introdução:

Os registradores de deslocamento são circuitos utilizados na prática quando se requer manipular bits ou palavras binárias.

Os registradores podem ser implementados a partir de flip-flops, sendo que a conexão entre eles determinará o seu comportamento.

Na figura abaixo estão representados os tipos de movimentação de dados num registro de deslocamentos.



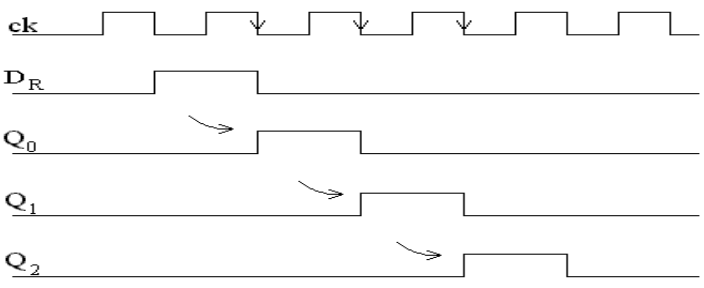
Os registros de deslocamento podem ser utilizados na conversão de dados do formato paralelo/série ou vice-versa. Podem também ser utilizados simplesmente como registros temporários de dados ou ainda realizar operações aritméticas de multiplicação ou divisão através de deslocamentos para a esquerda ou direita dependendo do caso.

2. Parte Experimental

Estudo do registrador de deslocamento CI 7495, utilizando a bancada experimental e o manual TTL:

- Analisar o funcionamento do CI 7495:
- Estudar a tabela de Função
- Efetuar deslocamentos **SERIE (DIR/ESQ ; ESQ/DIR) ; PARLELO/PARALELO**
- Contador em **ANEL** com deslocamento para **DIR** com início em qualquer valor
- Desenvolva no simulador CIRCUIT MAKER uma unidade de contagem composta por um contador decimal, um conversor de código BCD/7 seg. e um display de 7 segmentos. Utilize o CI 7495 para operar de forma que ao se apertar um comando, o display fique estático no último valor da contagem, porém o contador deve continuar a contagem. Ao se apertar pela segunda vez o comando, o display passa a mostrar o valor da contagem atual e as mudanças ocorridas a cada instante. Utilize outros componentes (por exe. flip-flops), se necessário.

Observe a movimentação de um bit (1) dentro do registro



National Semiconductor

June 1989

5495A/DM7495
4-Bit Parallel Access Shift Registers

General Description

These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation.

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied simultaneously to clock 1 and clock 2 if both modes can be clocked from the same source.

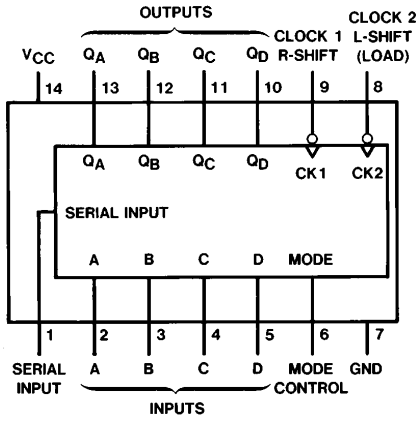
Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the truth table will also ensure that register contents are protected.

Features

- Typical maximum clock frequency 36 MHz
- Typical power dissipation 250 mW

Connection Diagram

Dual-In-Line Package



TL/F/6534–1

Order Number 5495ADMQB, 5495AFMQB or DM7495N
See NS Package Number J14A, N14A or W14B

RRD-B30M105/Printed in U. S. A.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		25		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		35	ns

Function Table

Inputs								Outputs			
Mode Control	Clocks		Serial	Parallel				Q_A	Q_B	Q_C	Q_D
	2(L)	1(R)		A	B	C	D				
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_{B}†	Q_{C}†	Q_{D}†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

†Shifting left requires external connection of Q_B to A, Q_C to B, Q_D to C. Serial data is entered at input D.

H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care (Any input, including transitions)

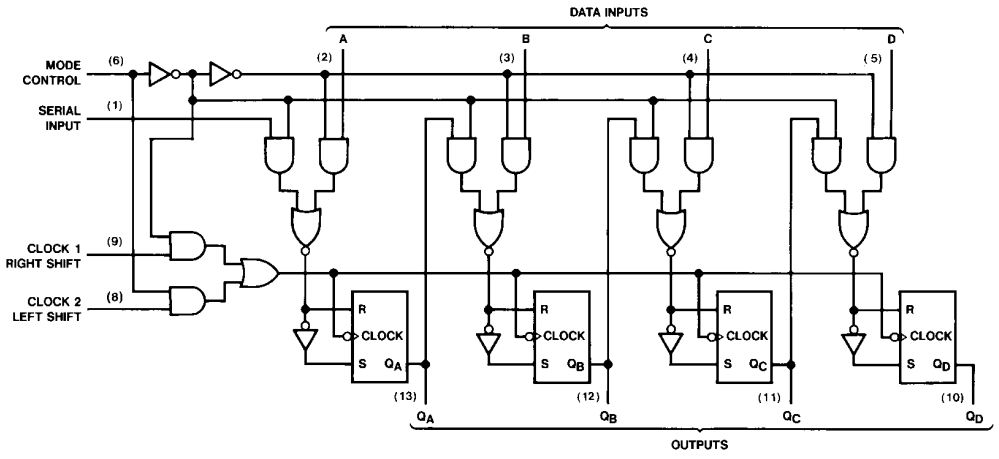
↓ = Transition from high to low level, ↑ = Transition from low to high level

a, b, c, d = The level of steady, state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, Q_D, respectively, before the most recent ↓ transition of the clock.

Logic Diagram



TL/F/6534–2