

1. (6 points) Draw symbols for the gates named, and write a number in the gate symbol to indicate how many transistors are used by the gate.

+4
2NAND:

~~3NOR:~~

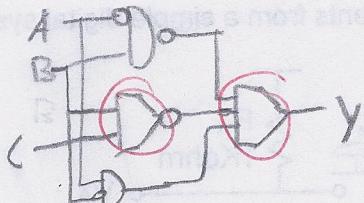
~~4AND:~~

~~INV:~~

2. (8 points) Sketch logic circuits for the Verilog description below. First sketch the circuit as described without attempting to minimize, and then sketch a minimized version of the same circuit.

assign Y = $\sim(\sim A \& B) \mid \sim(B \mid C) \mid (A \& \sim B);$

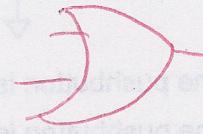
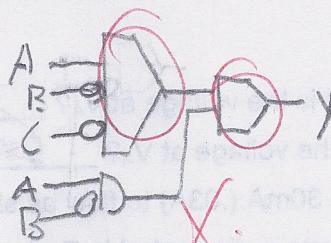
Not minimized (3 points):



$$\bar{A}\bar{B} + \bar{B}+C + A\bar{B}$$

$$A+\bar{B} + \bar{B}+C + A\bar{B}$$

Minimized (5 points):



That's OR gate.

NOT

3. (6 points) Place an N or P in the blanks below to indicate the proper type of FET to correctly complete each sentence.

~~N~~ FETs show a bubble on their gate symbols to indicate they are turned ON with a logic 0.

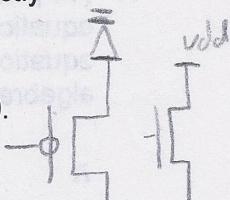
P FETs form a channel full of positive charge carriers when they are ON.

N FETs form a channel full of negative charge carriers when they are ON.

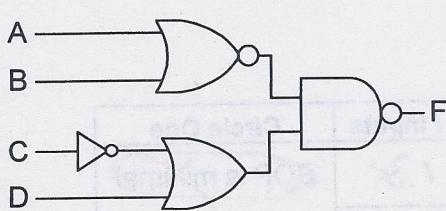
N FETs conduct low voltage (or '0') signals well.

P FET sources are always connected to Vdd when used in a logic circuit.

~~X~~ FETs turn ON when high voltage (or '1') is applied to their gate.



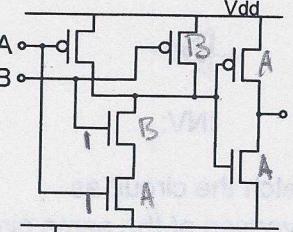
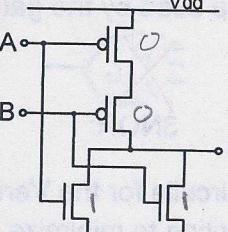
4. (6 points) Provide a Verilog-syntax assignment statement that describes the circuit below.



$$F = (A+B)(\bar{C}+D)$$

+6
assign F = $\sim(\sim(A \mid B) \& (\sim C \mid D));$

5. (12 points) Provide a gate name and circuit symbol, and complete the truth table for the circuits below.

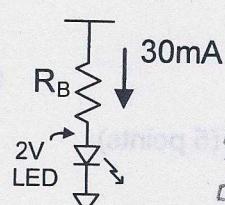
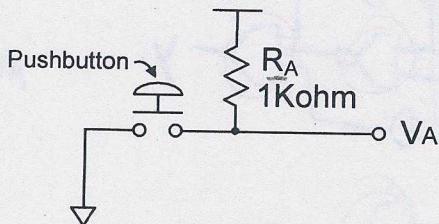
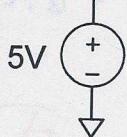
Gate Name: Not	Symbol	Gate Name: Nand	Symbol																					
	<table border="1" style="border-collapse: collapse; width: 50px;"> <tr><td>A</td><td>0</td><td>1</td></tr> <tr><td>B</td><td>1</td><td>0</td></tr> <tr><td>F</td><td>1</td><td>0</td></tr> </table>	A	0	1	B	1	0	F	1	0		<table border="1" style="border-collapse: collapse; width: 50px;"> <tr><td>A</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>B</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>F</td><td>1</td><td>0</td><td>0</td></tr> </table>	A	0	0	1	B	0	1	0	F	1	0	0
A	0	1																						
B	1	0																						
F	1	0																						
A	0	0	1																					
B	0	1	0																					
F	1	0	0																					

6. (4 points) Below are some circuit elements from a simple digital system.

$$V = IR$$

$$P = VI$$

$$I^2R$$



$$5V = 0.03A \cdot R$$

$$\frac{5V}{0.03A} = R$$

$$\frac{5}{\frac{3}{100}} = \frac{500}{3}$$

$$\frac{25}{1000} = \frac{5}{200}$$

$$\frac{1}{40}$$

When the pushbutton is not pressed, what is the voltage at V_A ? ~~5V~~

When the pushbutton is pressed, what is the voltage at V_A ? ~~5V~~

What resistance (in Ohms) must R_B be for 30mA (.03A) to flow as shown? ~~5 / 0.03 Ω (Ohms)~~

When the pushbutton is pressed, what power is dissipated in R_A (recall $P = VI$)? ~~1/4 Watts~~

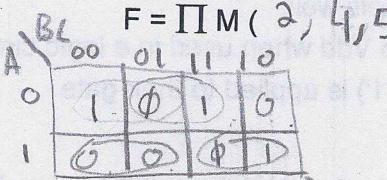
$$V = IR \quad 5V = I \cdot 1000 \quad \frac{5}{1000} = I \cdot \frac{5}{1000}$$

7. (14 points) Complete the following minterm/maxterm equations and write minimum SOP and POS equations for the logic system shown in the truth table. Show the gate/input count for each equation, indicate which equation (POS or SOP) is the most minimal, and whether they are algebraically equal (i.e., whether you could perform Boolean algebra on one to get the other).

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

$$F = \sum m(0, 3, 6) + \phi(7)$$

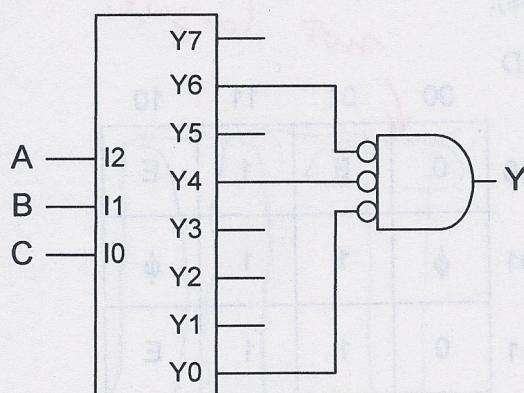
$$\cdot \phi(7)$$



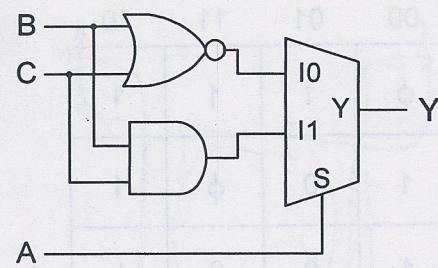
F = $\prod M(2, 4, 5)$

Equations	Gates / Inputs	Circle One
$F_{SOP} = \bar{A}\bar{B} + \bar{A}C + AB = \bar{A}C$	2 / 3	SOP is minimal
$F_{POS} = (\bar{A}B) \cdot (\bar{A}C) \cdot (B'C)$	4 / 3	POS is minimal

8. (10 points) Complete the truth table to document the behavior of the circuit below.

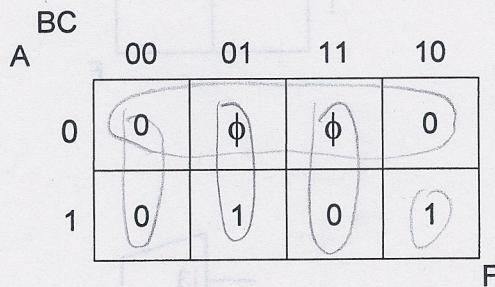


A	B	C	Y
0	0	0	0
1	0	1	1
2	0	1	1
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	0



A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

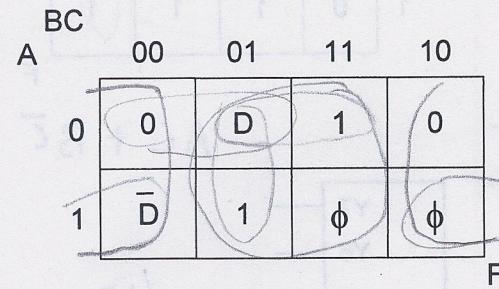
9. (12 points) Loop the K-maps in both SOP and POS forms, finding the most minimal cover in each case (do not consider XOR patterns). Indicate whether the equations are algebraically equal.



$$F_{SOP} = (\bar{B}C) + (A\bar{B}\bar{C})$$

$$F_{POS} = A \oplus (B+\bar{C}) \wedge (\bar{B}+\bar{C})$$

Equations are algebraically equal: T / F

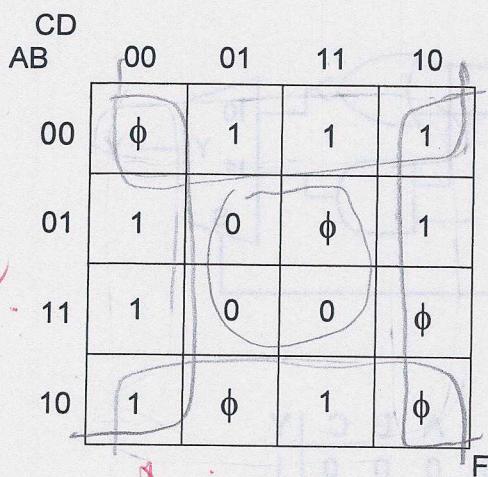


$$F_{SOP} = (\bar{A}C\bar{D}) + (\bar{A}\bar{C}D) + (A\bar{C}\bar{D}) + (ACD)$$

$$F_{POS} = ((\bar{C}+D)) \wedge (A+B+\bar{D})$$

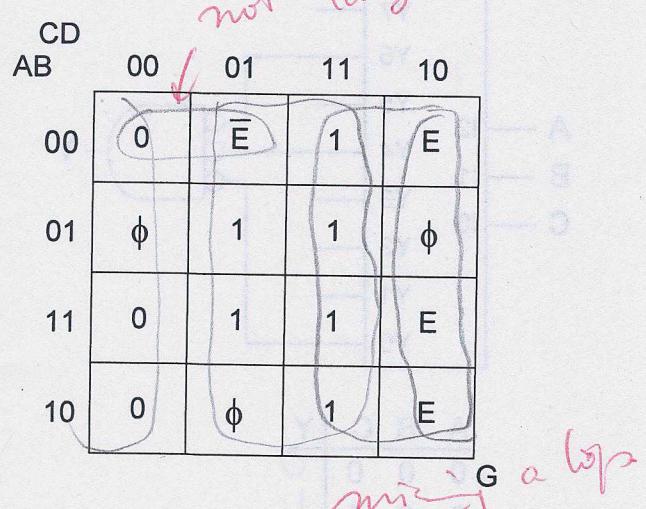
Equations are algebraically equal: T / F X

10. (10 points) Loop the K-maps in POS form (lower left) and SOP form (lower right), finding the most minimal cover in each case (do not consider XOR patterns).



$$F_{SOP} = \overline{C} + \overline{B}$$

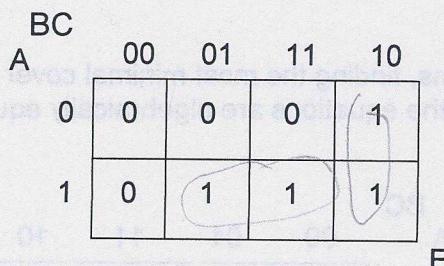
$$G = \overline{D+E} \cdot \overline{B+C+E}$$



$$F_{POS} = \overline{B} \cdot \overline{D}$$

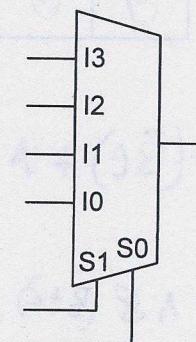
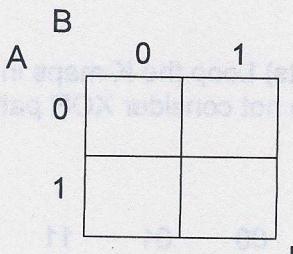
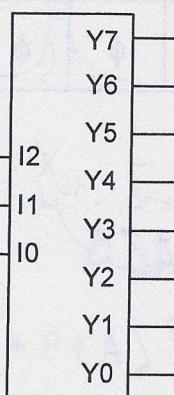
$$G = \overline{D+E} \cdot \overline{B+C+E}$$

12. (12 points) The K-map below specifies a given circuit. **Neatly** sketch two versions of a circuit that can each implement the system, one using a 3:8 decoder and the other using a 4:1 mux. (Hint: For the mux circuit you will need to compress the K-map from a 3-variable map into a 2-variable K-map). Be sure to label all input signals.



$$AC + BC$$

42



ABC

001
000
011
010
101
006
111
110

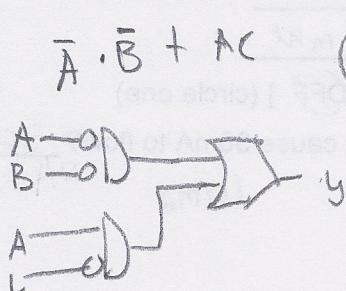
- +5.*
13. (Extra 5 points) A parity circuit uses a circuit based on Xor gates to generate a parity bit, and the same circuit can be used to check parity (circle one): True False



1. A logic circuit is specified by the following Verilog description:

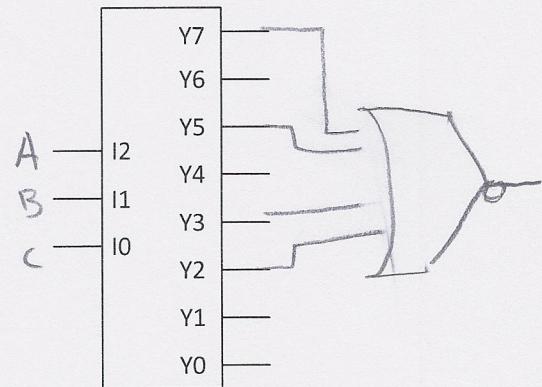
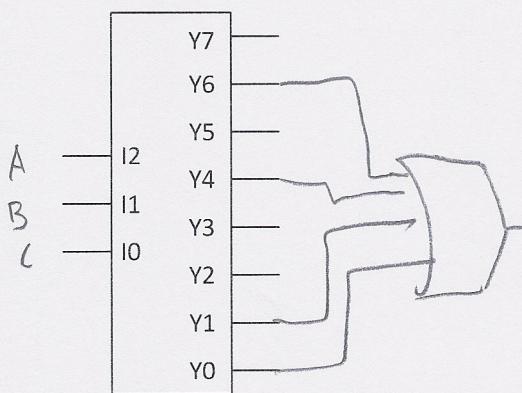
$$\text{assign } Y = \sim(A \mid B) \mid (\sim A \And \sim B \And C) \mid (A \And \sim C) \mid \sim(B \Mid C);$$

- a. (5 points) Sketch a minimized version of the same circuit.



A	BC	00	01	11	10
0		1	1	0	0
1		1	0	0	1

- b. (5 points) **Neatly** sketch a circuit using a 3:8 binary decoder to implement the equation above. If you can sketch two different circuits using 3:8 binary decoders, you can get 5 extra points.



2. (12 points) Loop the K-maps in both SOP and POS forms, finding the most minimal cover in each case (do not consider XOR patterns). Indicate whether the equations are algebraically equal.

		BC		F
		00	01	
A	0	1	1	(\ominus)
	1	0	1	0

$$F_{SOP} = \bar{A} + \bar{B}C + \bar{B}\bar{C}$$

$$F_{POS} = (\bar{A} \mid B \mid C)(\bar{B} + \bar{C})$$

		BC		F
		00	01	
A	0	0	1	\bar{D}
	1	D	1	ϕ

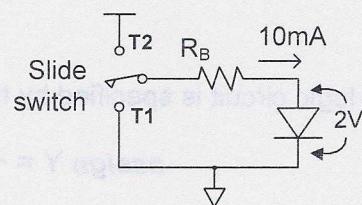
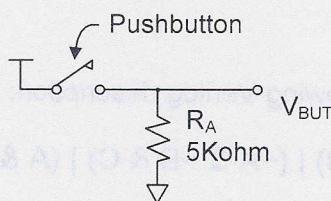
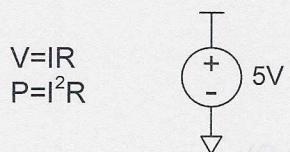
$$F_{SOP} = AD + (\bar{D} \mid \bar{B} \mid \bar{C})$$

$$F_{POS} = ((1D)(\bar{B} \mid \bar{D}))(\bar{A} + C)$$

Equations are algebraically equal: T /

Equations are algebraically equal: T /

3. (4 points) Below are some circuit elements from a simple digital system.



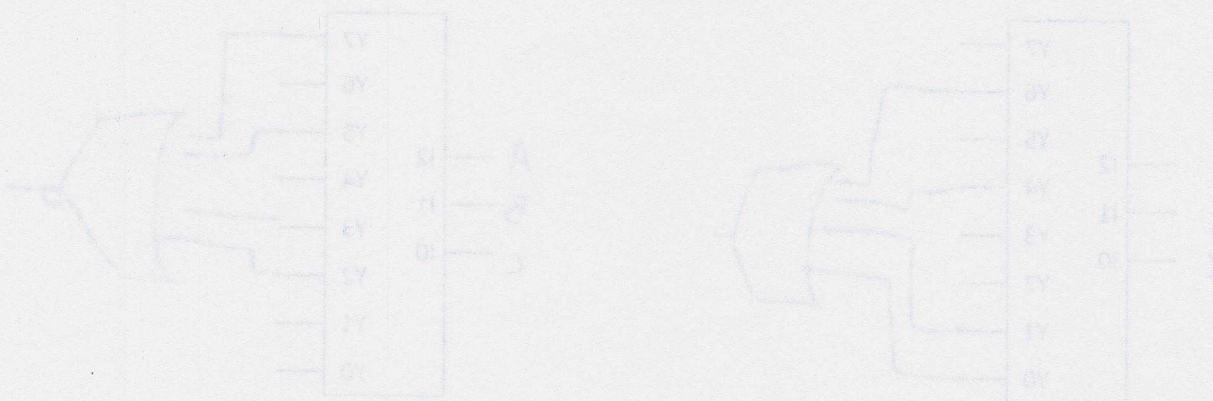
When the pushbutton is not pressed, what is the voltage at V_{BUT} ? 0

When the pushbutton is pressed, what power is dissipated in R_A ? 5 mW

When the slide switch is connected to Ground (T1), the LED is [ON / OFF] (circle one)

When the slide switch is connected to Vdd (T2), what resistance R_B will cause 30mA to flow? 300 Ω
10mA

avoids noise and thermal noise is caused by noise in the logic circuit (analog IC) and noise in the power supply. The noise in the logic circuit is due to the switching of transistors and noise in the power supply is due to the switching of transistors.



These are known as minimum width pulses, which are 20ns long. These pulses are used to control the switches in the circuit.

00	11	10	00	A	00	11	10	00	A
0	0	1	0	0	1	0	1	0	0
0	1	0	1	1	0	1	0	1	1

$$0 \oplus 0 = 0$$

$$0 \oplus 1 = 1$$

$$0 \oplus 0 = 0$$

$$0 \oplus 1 = 1$$

What is the output of the AND gate?

What is the output of the OR gate?

1. A logic circuit is specified by the following Verilog description:

$$\text{assign } Y = \overline{(A \mid B)} \mid (\overline{A} \wedge \overline{B} \wedge C) \mid (A \wedge \overline{C}) \mid \overline{(B \mid C)};$$

- a. (5 points) Sketch a minimized version of the same circuit.

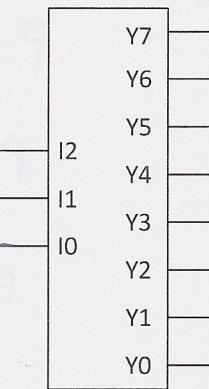
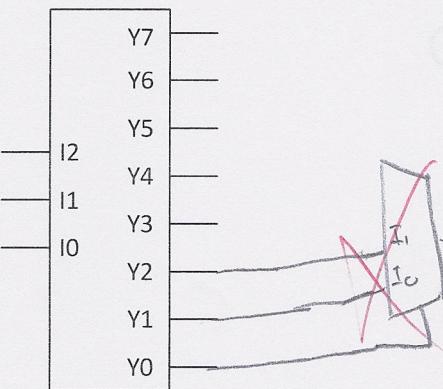
$$(\neg A \mid B) \mid (\neg A \cdot \neg B \cdot C) \mid (A \cdot \neg C) \mid \neg (B \mid C)$$

A	B	C	y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

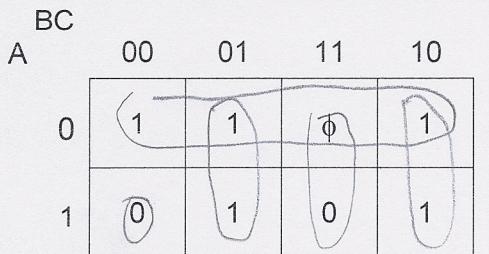
$$(\neg A \cdot \neg B) \mid (A \cdot B \cdot \neg C)$$

		BC	
		A	00 01 11 10
A	B	00	1 1 0 0
		01	0 0 0 1
1	0	11	0 0 0 0
		10	0 1 0 1

- b. (5 points) **Neatly** sketch a circuit using a 3:8 binary decoder to implement the equation above. If you can sketch two different circuits using 3:8 binary decoders, you can get 5 extra points.



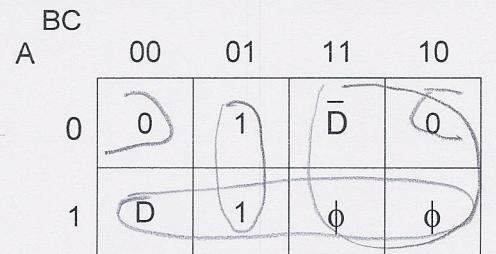
2. (12 points) Loop the K-maps in both SOP and POS forms, finding the most minimal cover in each case (do not consider XOR patterns). Indicate whether the equations are algebraically equal.



$$F_{SOP} = \overline{A} \mid (\overline{B} \cdot C) \mid (B \cdot \overline{C})$$

$$F_{POS} = (\overline{B} \mid \overline{C}) \cdot (\overline{A} \mid B \mid C)$$

Equations are algebraically equal: T / F



$$F_{SOP} = A \mid (\overline{B} \cdot C)$$

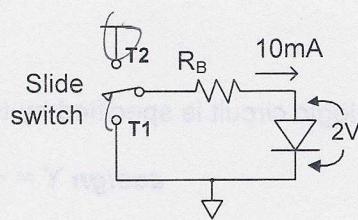
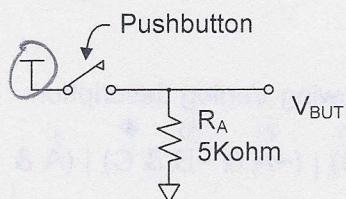
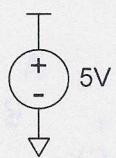
$$F_{POS} = (\overline{B}) \cdot (\overline{A} \mid C) \cdot$$

Equations are algebraically equal: T / F

3. (4 points) Below are some circuit elements from a simple digital system.

$$V=IR$$

$$P=I^2R$$



+3. When the pushbutton is not pressed, what is the voltage at V_{BUT} ? 0V

When the pushbutton is pressed, what power is dissipated in R_A ? $\frac{5}{1000}$ Watts

When the slide switch is connected to Ground (T1), the LED is [ON / OFF] (circle one) OFF No Voltage

When the slide switch is connected to V_{dd} (T2), what resistance R_B will cause $30mA$ to flow? $5/3 \times 10^2 \Omega$

$$V=IR$$

$$P=I^2R$$

$$5V = I(5000)$$

$$\frac{5}{5000} = I$$

$$5000$$

$$\frac{1}{1000} = I$$

$$P = \left(\frac{1}{1000}\right)^2 (5000)$$

$$P = \frac{1}{1000000} (5000)$$

$$P = \frac{5}{1000000}$$

$$P = \frac{5}{1000} \text{ Watts}$$

$$V=IR$$

$$5V = 30 \times 10^{-3} R$$

$$\frac{5}{3 \times 10^{-2}} = R$$

01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20
01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20
01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20
01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20
01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20

EE 214

Exam #2

Name: Justin Harper

ID #: 10696738

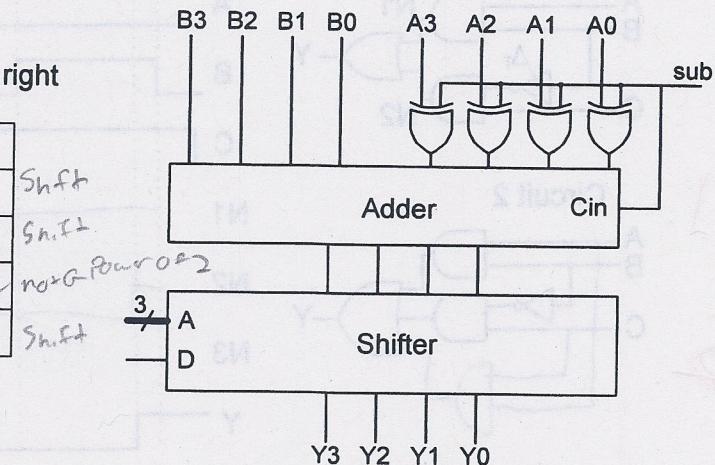
Spring 2014

Cats... Cats everywhere :)

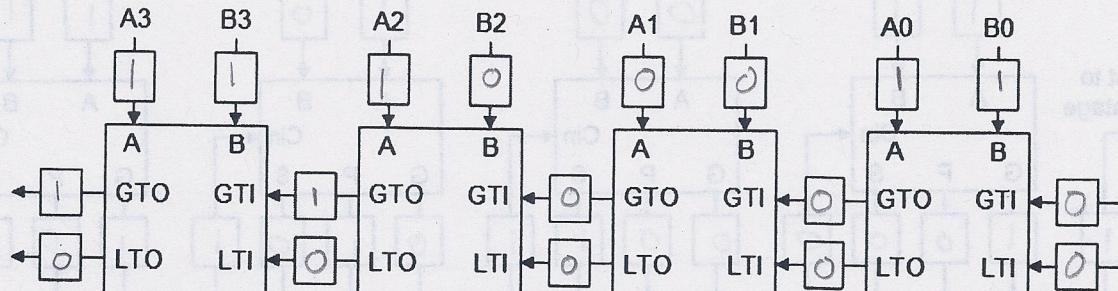
1. (16 points) In the table below, provide entries for the A bus and D and sub signals to configure the circuit to perform the indicated operation. If it is not possible to configure the circuit to perform the indicated operation, draw a line through the row in the table.

A: number of bits D: direction, '1' for right

A2	A1	A0	D	sub	Y
1	0	1	1	0	$(B + A) / 2$
0	1	0	0	1	$(B - A) * 16$
1	1	1	1	1	$(A + B) * 6$
1	1	1	1	1	$(A - B) / 4$



2. (12 points) The figure below shows the structure of a bit-slice magnitude comparator. Fill in 1's and 0's in the boxes to illustrate comparing $A = 13$ to $B = 9$. Then add a single logic gate to the figure to create an $A=B$ output for the four-bit comparator (GTO means $A \text{ GT } B$).



3. (4 points) In the boxes below, show the 8-bit 2's complement numbers that would be input to, and output from, an adder circuit performing the operation $33 - 47$. Show the signed decimal result as well as the binary number.

$$+4$$

47

0 0 1 0 1 1 1
2 6 5 4 3 2 1
2 2 2 2 2 2 2

06101111
11010000

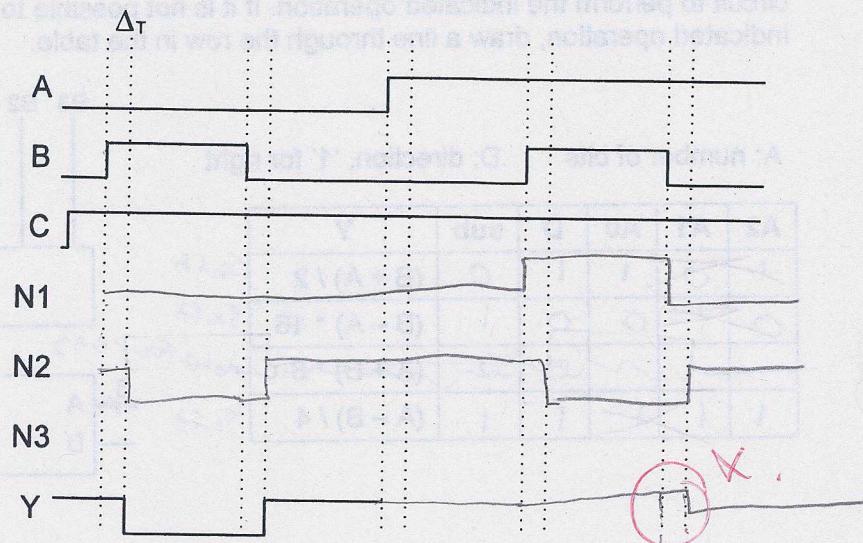
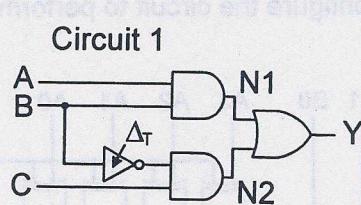
0000100 1110011
4322218 11110100

0	0	1	0	0	0	0	1		
+	1	1	0	1	0	0	0	1	
	1	1	1	1	0	0	1	0	

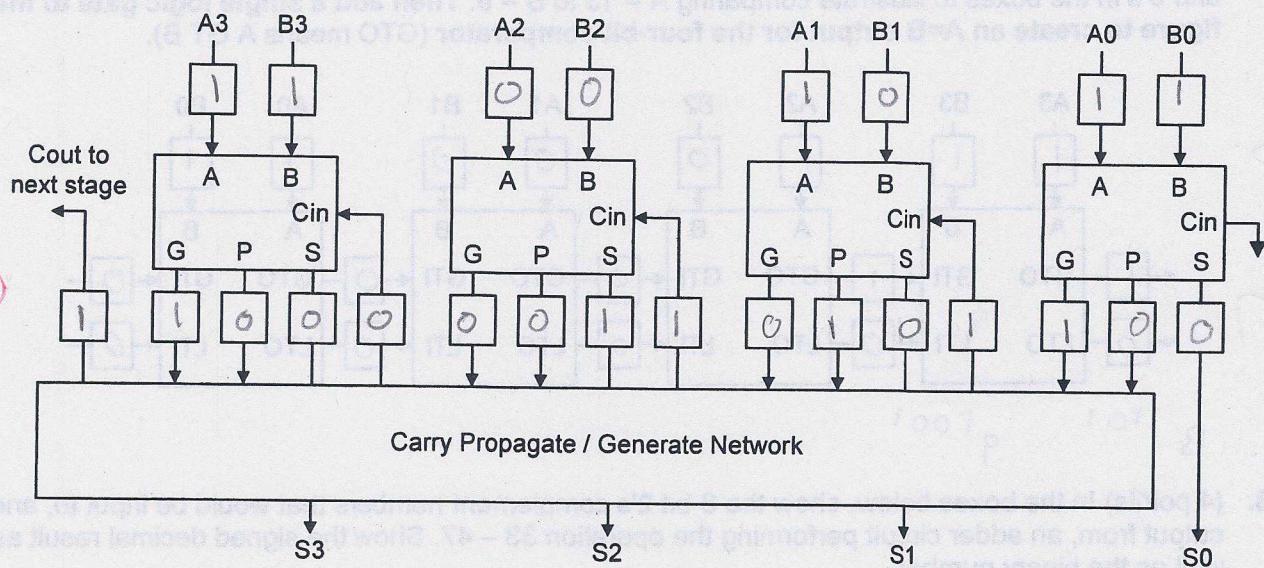
33

-47

4. (13 points) The timing diagram for Circuit 1 below has been partially completed. Assuming the inverter has delay Δ_T and the other gates have no delay, complete the sketch to document any possible glitches. Then modify circuit 2 to create a circuit that performs the same logic as circuit 1, but which cannot form a glitch.



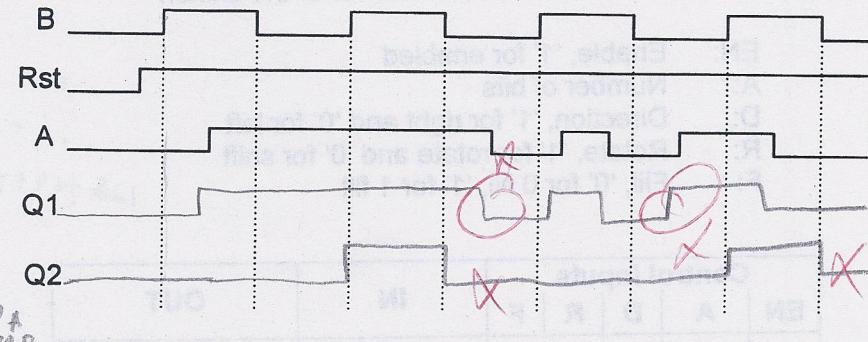
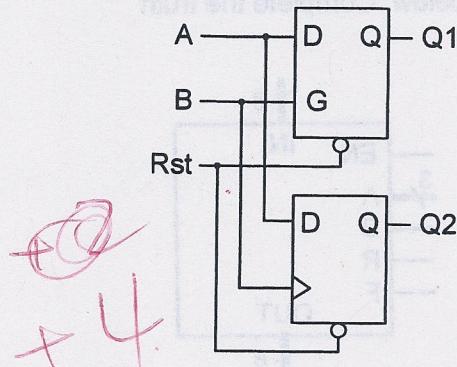
5. (10 points) A figure showing the structure of a CLA is provided below. Fill in 1's and 0's in the boxes to illustrate adding $A=11$ to $B=9$.



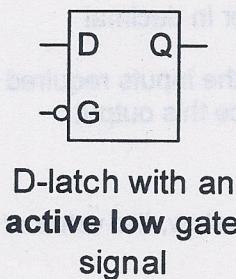
$\begin{array}{r} 1 \\ 0 \\ 1 \\ 1 \\ \hline 3 \\ 2 \\ 1 \\ 0 \\ \hline 2 \\ 2 \\ 2 \\ 2 \end{array}$

$\begin{array}{r} 1 \\ 0 \\ 0 \\ 1 \\ \hline 3 \\ 2 \\ 1 \\ 0 \\ \hline 2 \\ 3 \\ 2 \\ 2 \end{array}$

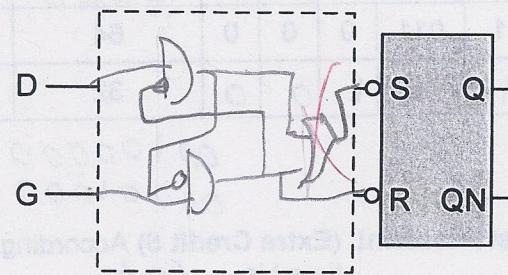
6. (10 points) Complete the timing diagram below:



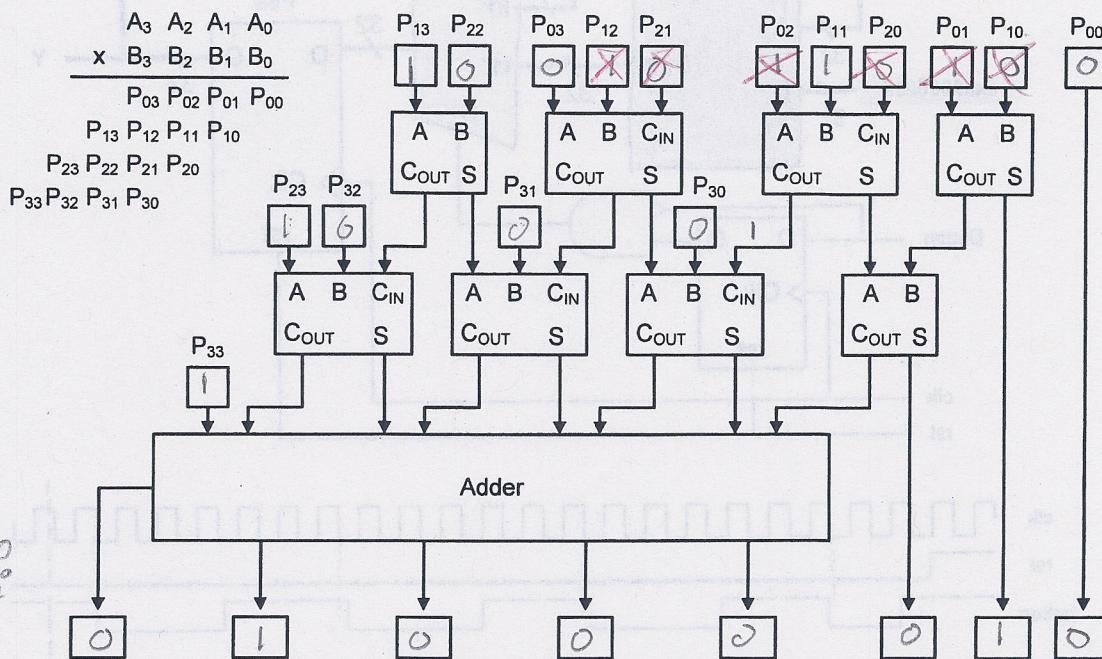
7. (12 points) A D-latch with an **active low** gate signal is shown below (i.e. the latch is transparent when gate is '0'). Sketch a logic circuit in the box below that can work with a NAND SR-Latch to implement a D-latch with **active low** gate signal.



D	G	S	R
0	0	0	0
0	1	0	0
1	0	1	1
1	1	0	0

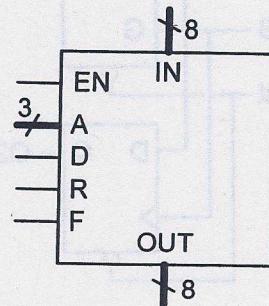


8. (10 points) A figure showing the structure of a multiplier is provided below. Place 1's and 0's in the boxes to illustrate multiplying $A=11$ and $B=6$.



9. (13 points) The figure shows a shifter with the signal definitions listed below. Complete the truth table below to document the behavior of the shifter.

EN: Enable, '1' for enabled
 A: Number of bits
 D: Direction, '1' for right and '0' for left
 R: Rotate, '1' for rotate and '0' for shift
 F: Fill, '0' for 0 fill, '1' for 1 fill



Control Inputs					IN	OUT
EN	A	D	R	F		
0	101	0	1	1	01011010	00000000
1	011	1	0	1	00111000	11100111
1	010	0	1	0	10110000	11000010
1	011	0	0	0	64	8
1	010	1	0	0	32	8

EN=0

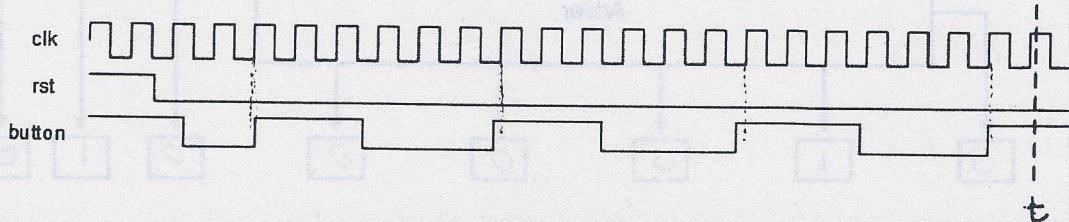
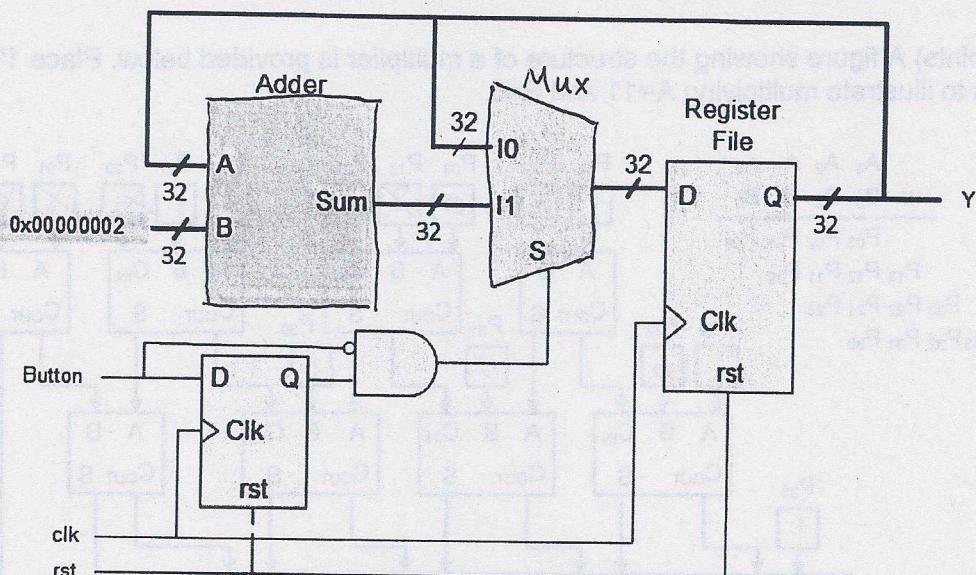
Shift 3 bits R fill with 1
 Shift 2 bits L fill with 0 Rotate

← Answer in decimal

← Show the inputs required to produce this output

00100000
 00001000

Secret Problem! (Extra Credit 5) According to the circuit and waveform below, the value of Y at the time t is cat



Did all the things

U

