Preface

This document describes a custom Application initially built around semiconductor yield analysis workflows. The tool was quite popular and evolved to service many additional user personas, both technical and non-technical. Daily users included production workers all the way up to the General Manager.

This custom application took advantage of an existing data pipeline that was created for other use case specific, “expert user” software platforms. The pipeline was enriched and API's were implemented that leveraged the embedded capabilities of these expert systems to implement machine learning results wrapped in a context that fit the natural workflows of users. This proved to be immensely popular as users no longer needed to learn very complicated expert systems to perform sophisticated analyses.

My role in this application's existence:

- I started as the Analyst who drove the requirements and use cases; I defined what data was needed, the transformations required and the analysis/visualizations that were required as well as heavy input on the UX.

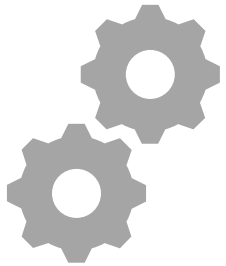
- I was the first user, the evangelist, I became a partner in funding resources and eventually became the Director over the development and data analyst teams who created and used the tools daily . After being acquired, the development team was moved into IT and I became the Global Product Manger for the portfolio of analysis tools.

The capabilities of this tool have been disclosed in more than one publication with the approval of LSI Logic. There is no additional information contained here that has not already been disclosed in the public domain.

Yield Management in High Tech Manufacturing

Mission:

Manage product yields through cost effective use of early detection and corrective action systems.



Key Attributes

Data Pipeline; to be clean and reliable, governance is required

Automate anything that is repetitive (KPI's, Data Mining, etc.)

Deliver information as part of Analysts' natural workflow

Ability to perform Ad Hoc analyses when required

Continuous Iteration

Key to success is the integration of disparate systems and delivery of information in a manner that matches the natural workflows of Analysts.

Commercially Purchased Tools

WIP Management

Tool maintenance management

Process Control/Alarm management

Positional Correlation

Defect database

Yield Management Software (YMS)

In-House Developed Tools

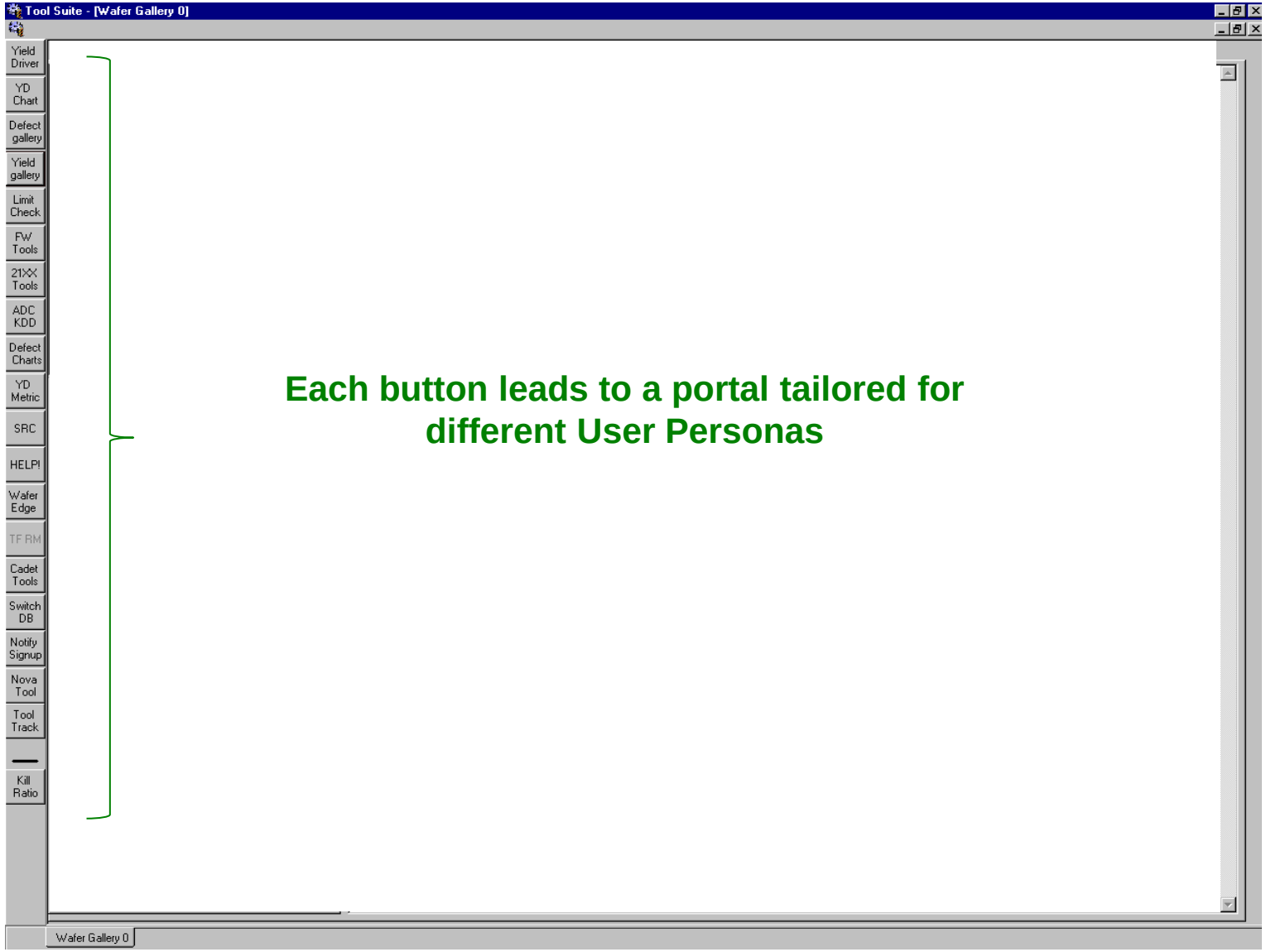
Tool Suite – Engineering Information Portal

CADET – Corrective Action Defect Event Tracking

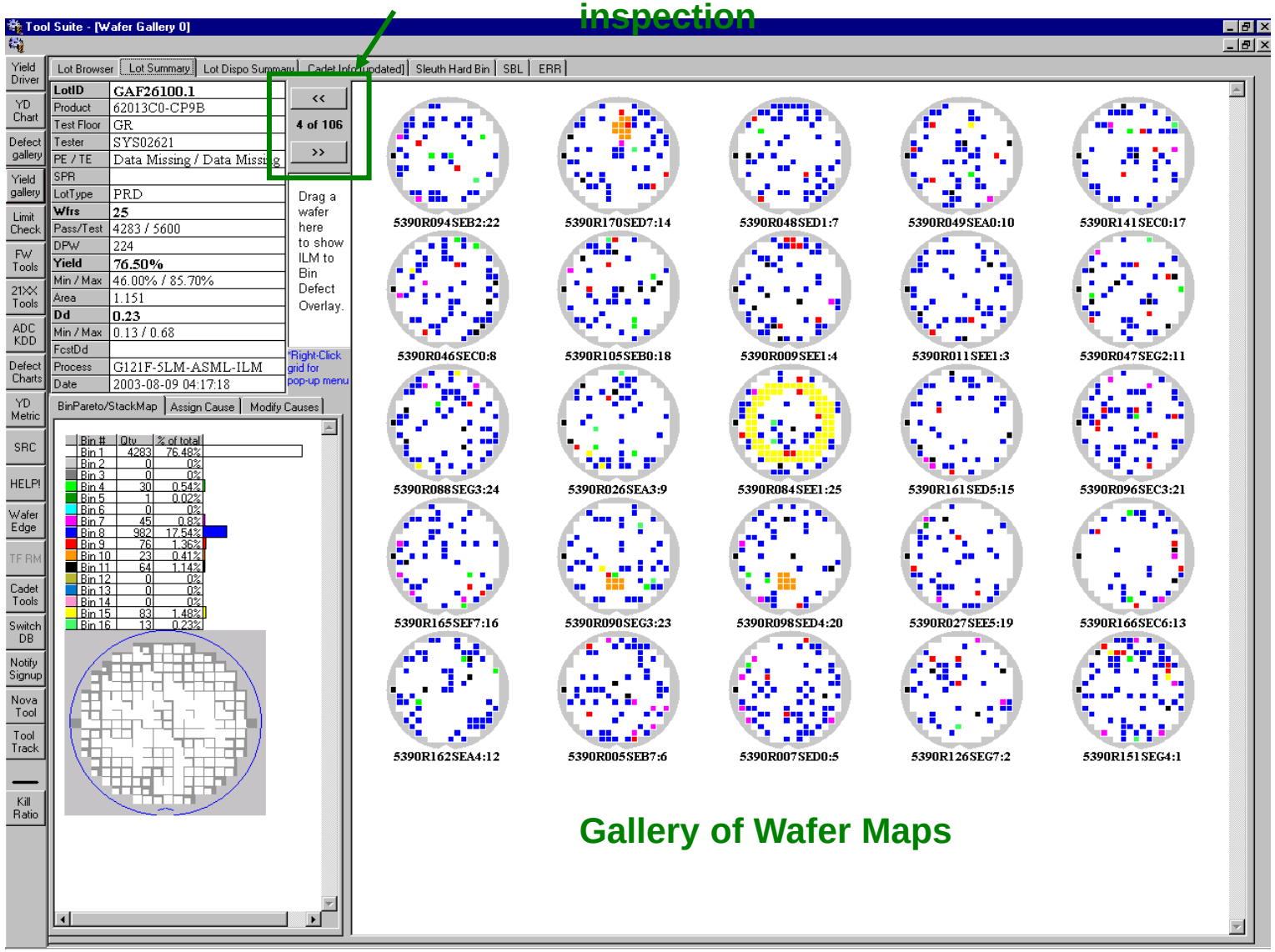
SBL – Statistical Bin Limits

ERR – Engineering Run Requests

In House Developed UI that integrates and enhances capabilities of commercially available software tools

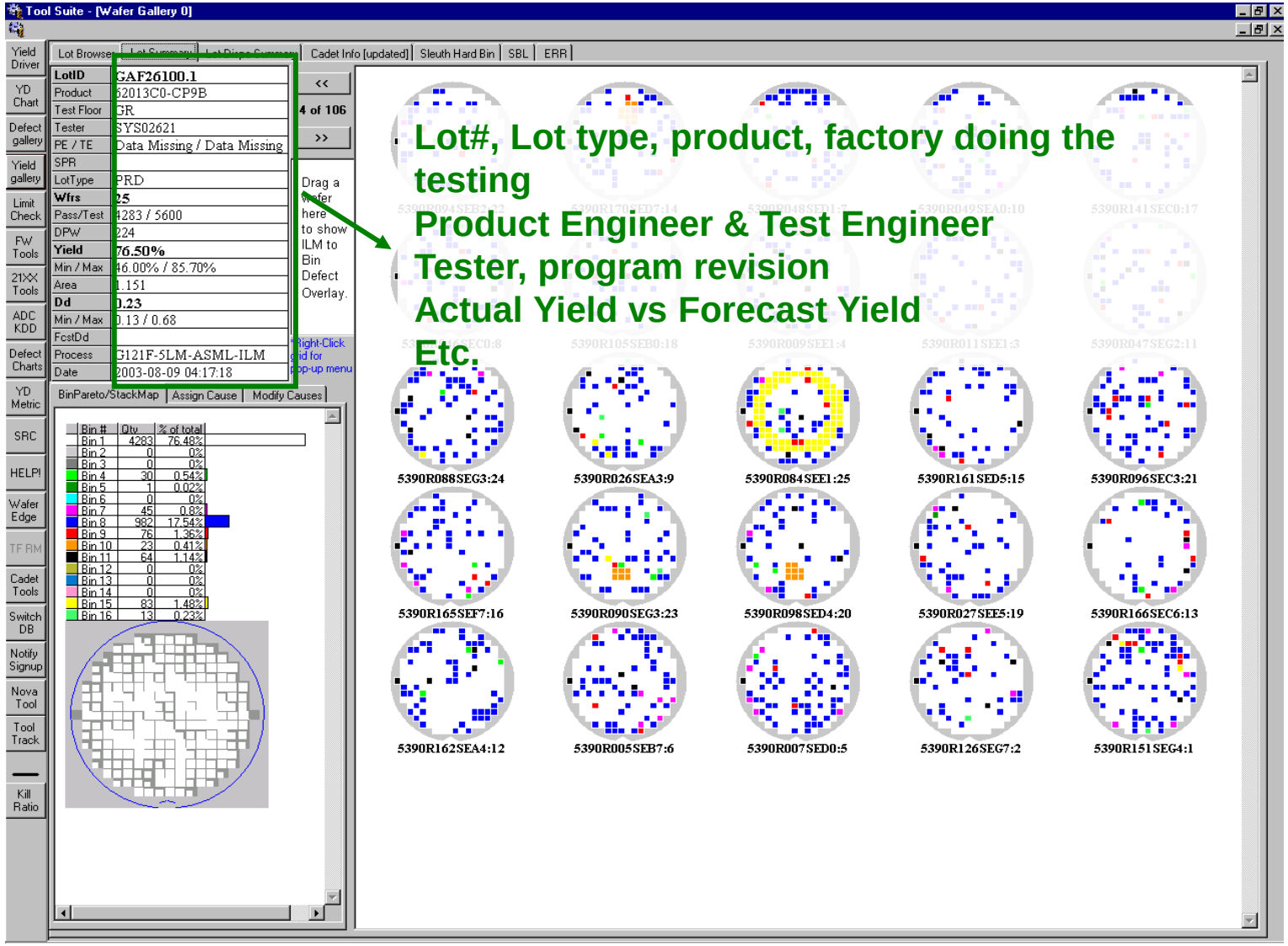


Fast and Easy way to visualize wafer yields



Previously this info needed to be generated by each Analyst

High level contextual information



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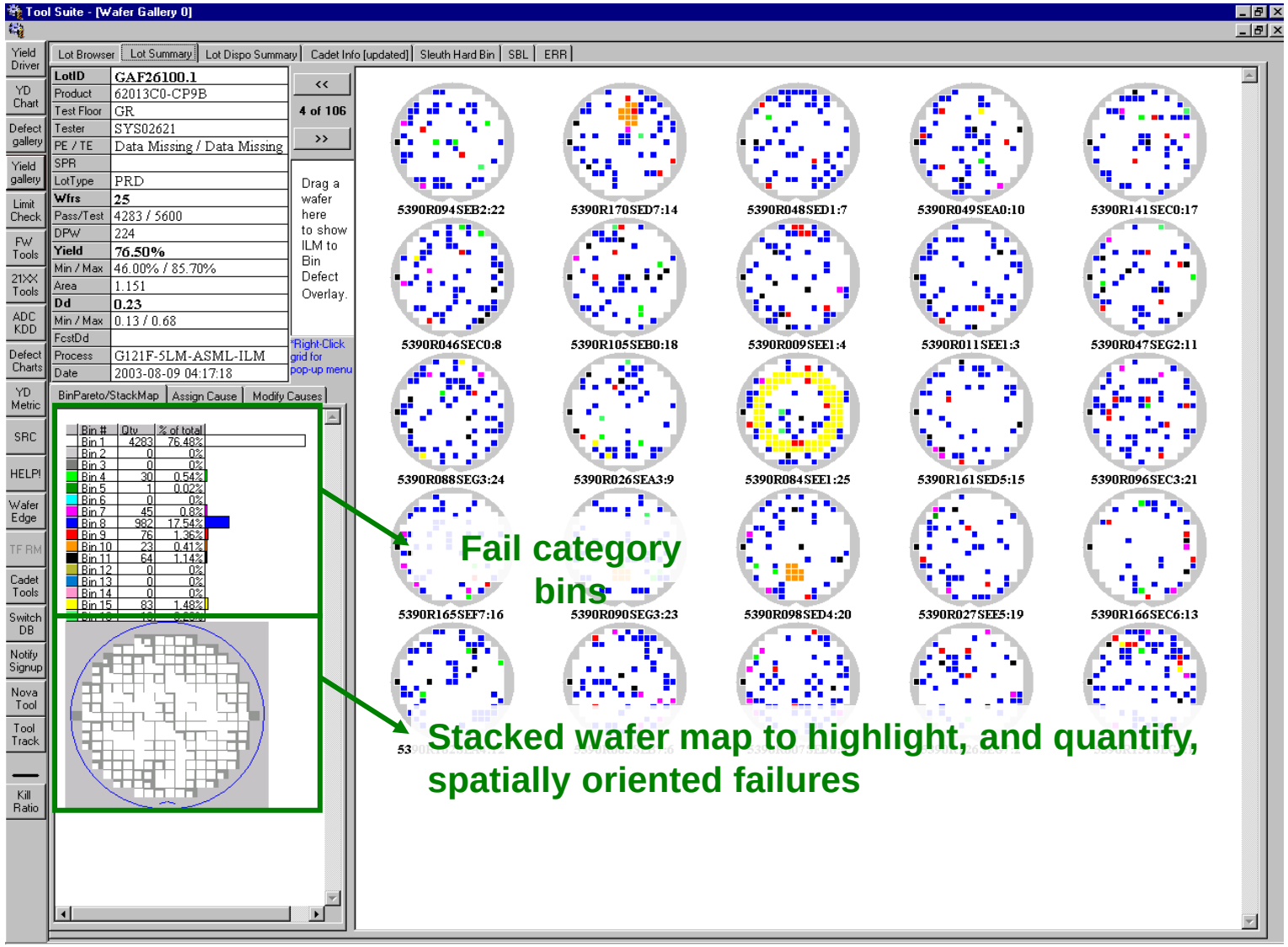
High level assessment of fail categories and spatially dependent yield signatures



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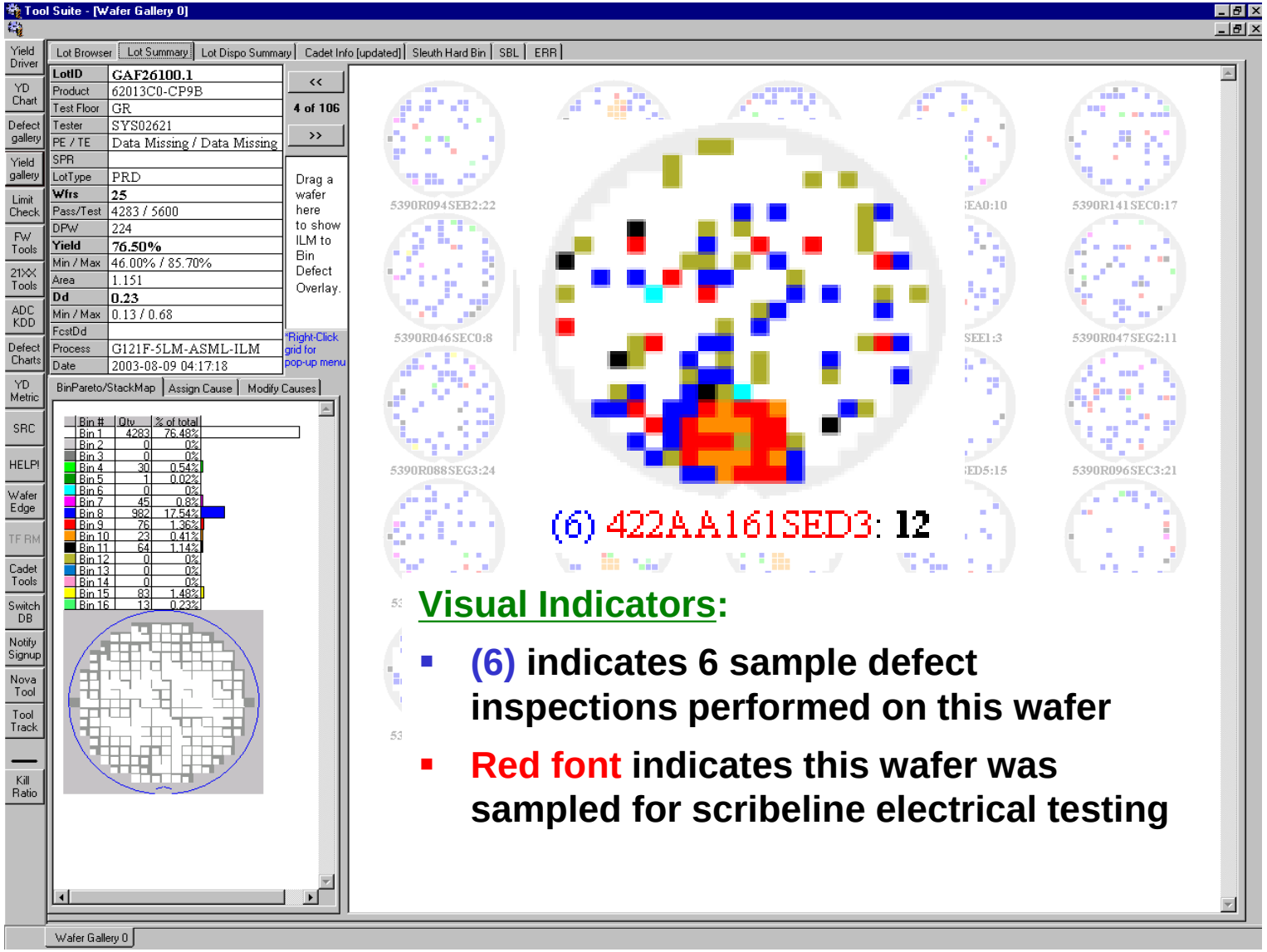
Additional visual indicators that inform Analysts what other data is available for each wafer



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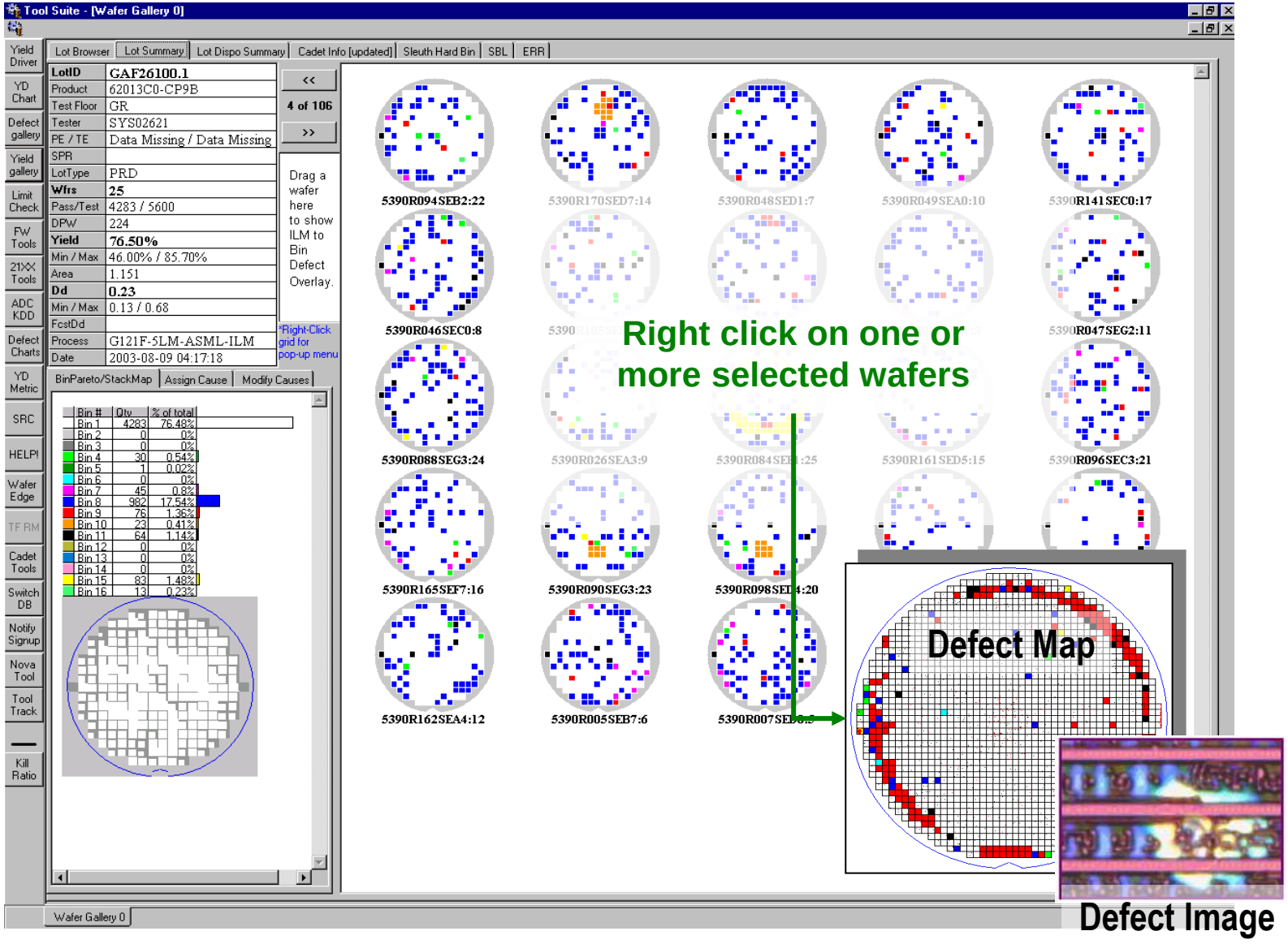
Inter-Operability (API):

Real-time, right-click view of defect maps and images for wafers of interest to Analyst



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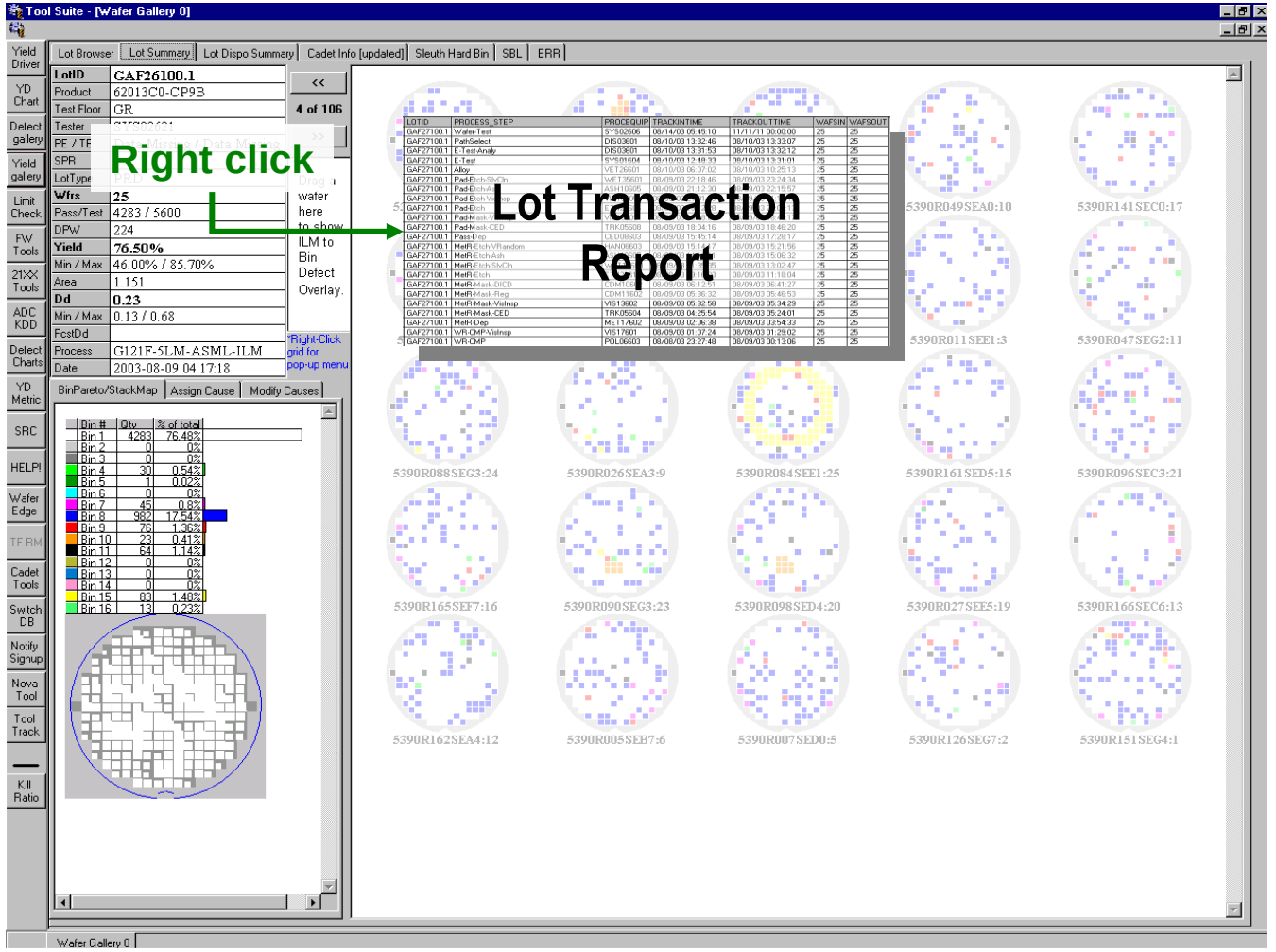
Inter-Operability (API):

Real-time, right-click view of transaction history for lot of interest



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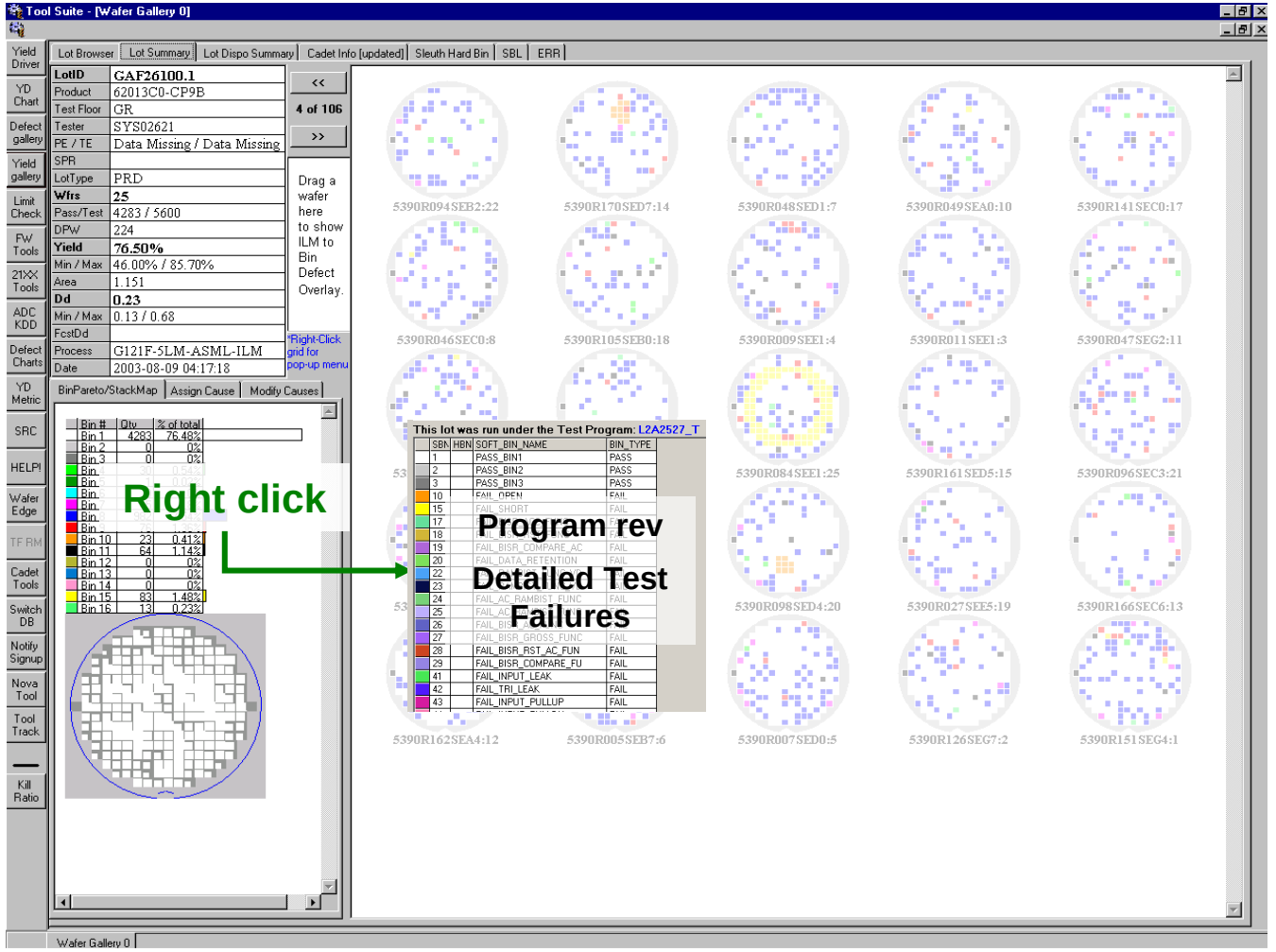
Inter-Operability (API):

Real-time, right-click view of test program revision and detailed test failures



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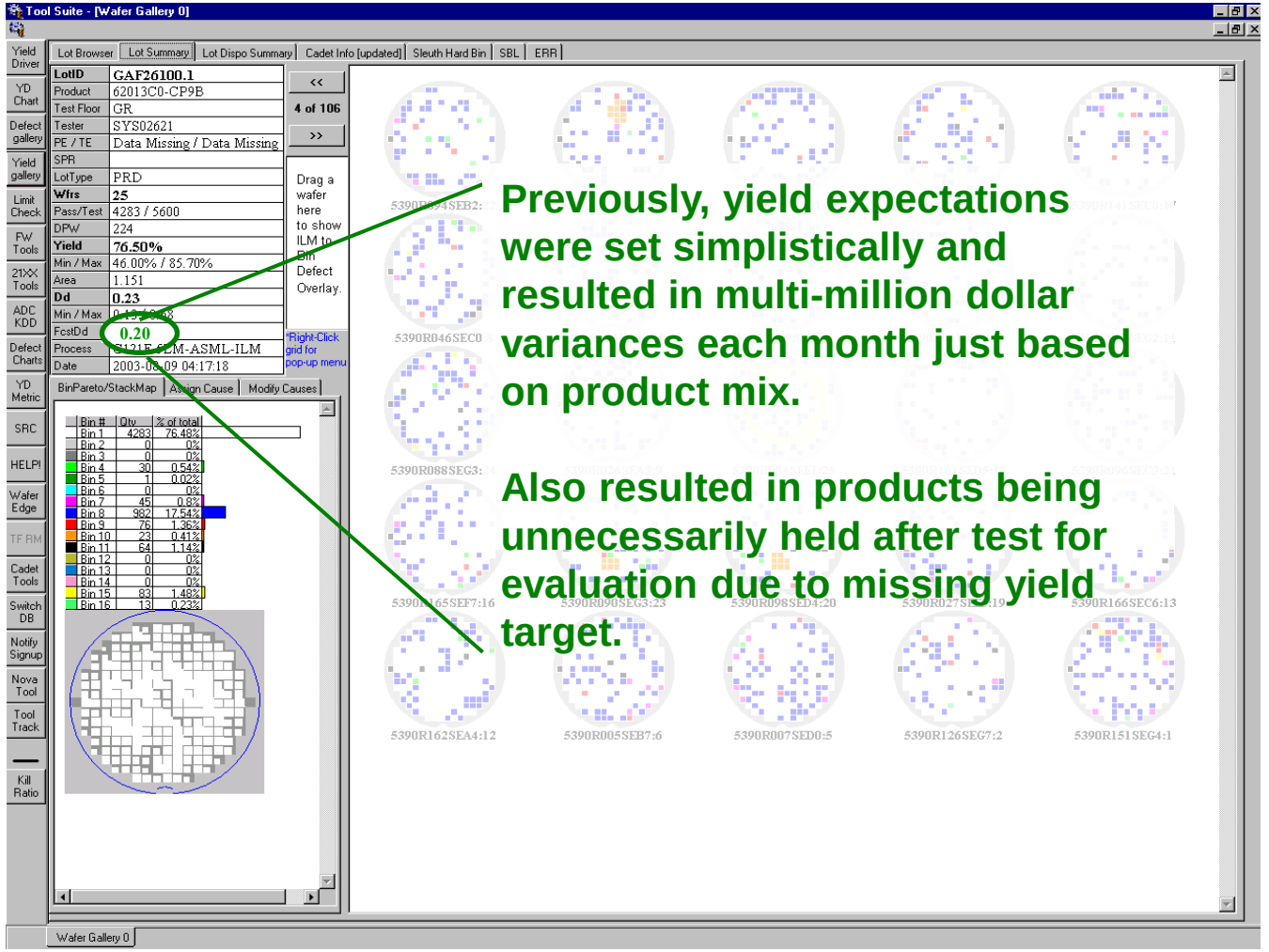
Machine Learning:

Product Specific Yield forecast based on design features and process flow.

Model consisted of Logistic and Linear Regression for important design and process flow attributes and combinations of attributes.

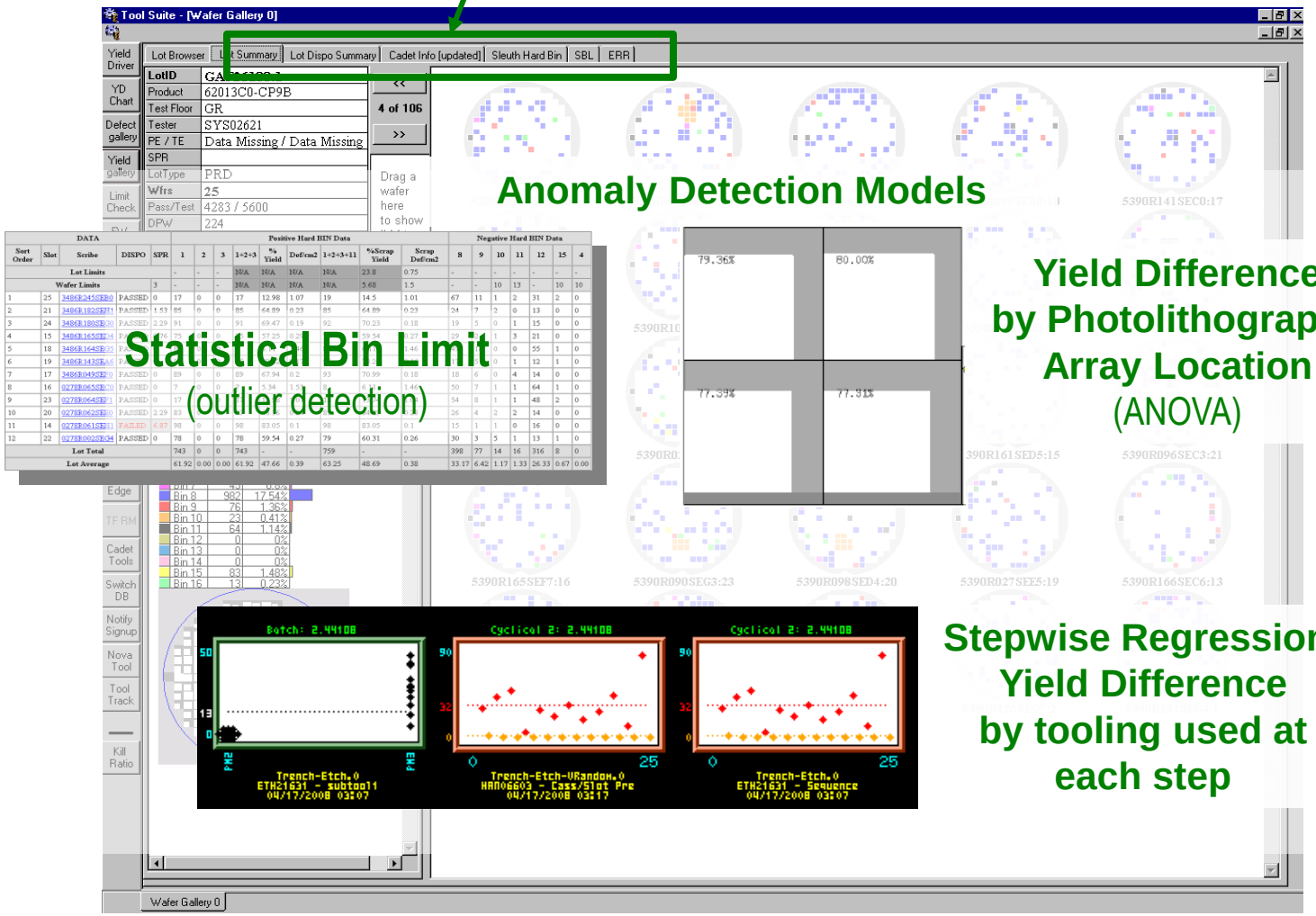


Machine Learning:

Anomaly Detection

- Statistical Bin Limit / CpkN to flag wafers with a-typical fail rates
- ANOVA by Photo Array location to flag repeating failures and across field affects on product performance
- Stepwise Regression to find tooling and sub-tooling that causes yield loss or performance differences

When other model conditions are met, tabs with additional data are presented to Analysts



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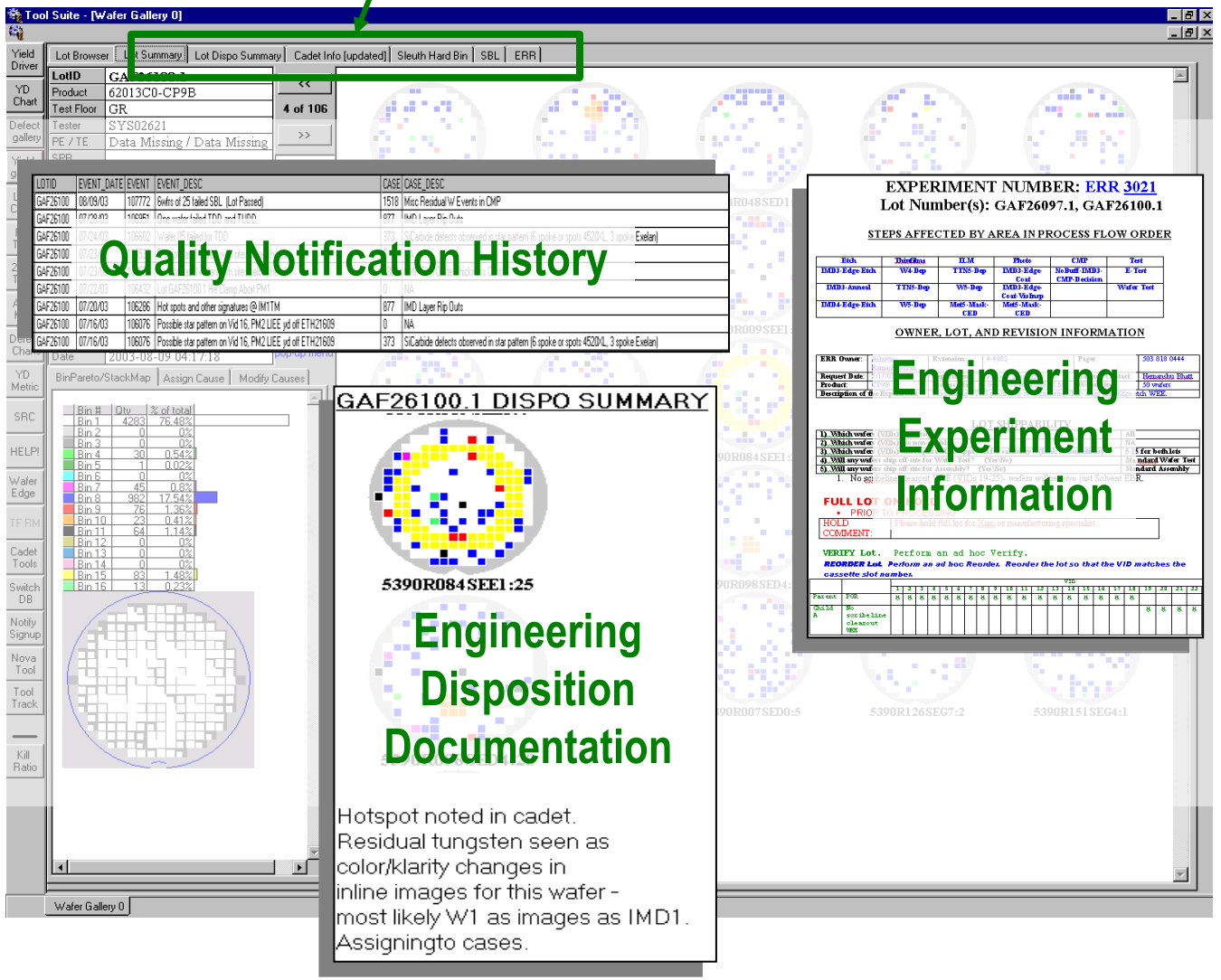
Rule based model conditions

(if these exist, present to Analyst)



Machine Learning:

- Abnormal process events recorded as Quality Notifications
- Non-standard processing performed as part of an experiment (Engineering Experiment)
- Record of Analysis already performed and documented by an Analyst (Disposition Documentation)

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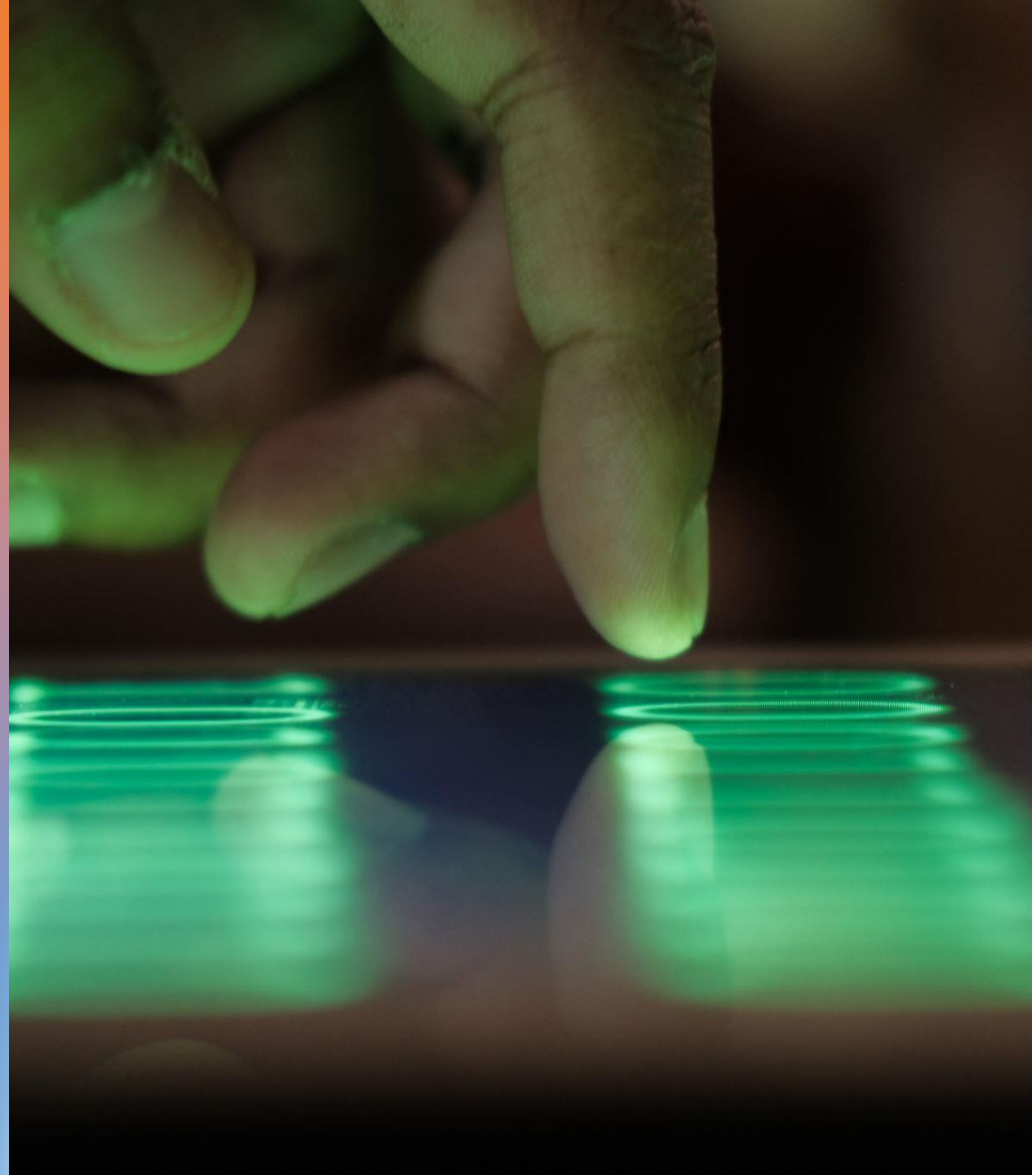

Additional Right-click capabilities…

Side by side comparison of bin maps to defect inspection maps

Lot commonality: Multiple lots with similar fail patterns can be flagged during review of yield maps and run through a “commonality analysis”

Tool maintenance history

Answered with zero effort from Analyst..

- Yield vs Forecast?
- Were there outlier bin failures?
- What do wafer maps look like? Spatial Yield patters?
- Repeating Pattern of Failures?
- Who are Product, Test Engineers?
- Where was the lot tested, on what tester?
- Bin Pareto?
- What tests are in each bin?
- What revision of the test program was used?
- Which wafers were inspected for defects?
- Which wafers were scribeline tested?
- Was there non-standard processing?
- What is documented for analysis that was already done?

More could be answered..

Scribeline Test to Wafer Test auto correlation
(bin and parametric)

Commonality across lots with similar spatial patterns

Auto correlation to In Line measurement / metrology data

Conclusion

This presentation demonstrated capabilities that provided immensely improved efficiencies to data analysts in the semiconductor industry, and which were well before their time.

Replicating, and improving upon, these capabilities with modern software and hardware is feasible.

I hope to share more information on other insightful approaches to semiconductor yield improvement.