

Preface

This document describes a custom Application initially built around semiconductor yield analysis workflows. The tool was quite popular and evolved to service many additional user personas, both technical and non-technical. Daily users included production workers all the way up to the General Manager.

This custom application took advantage of an existing data pipeline that was created for other use case specific, “expert user” software platforms. The pipeline was enriched and API's were implemented that leveraged the embedded capabilities of these expert systems to implement machine learning results wrapped in a context that fit the natural workflows of users. This proved to be immensely popular as users no longer needed to learn very complicated expert systems to perform sophisticated analyses.

My role in this application's existence:

- I started as the Analyst who drove the requirements and use cases; I defined what data was needed, the transformations required and the analysis/visualizations that were required as well as heavy input on the UX.
- I was the first user, the evangelist, I became a partner in funding resources and eventually became the Director over the development and data analyst teams who created and used the tools daily . After being acquired, the development team was moved into IT and I became the Global Product Manger for the portfolio of analysis tools.

The capabilities of this tool have been disclosed in more than one publication with the approval of LSI Logic. There is no additional information contained here that has not already been disclosed in the public domain.

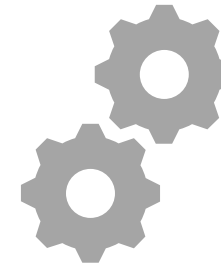


Yield Management in High Tech Manufacturing



Mission:

Manage product yields through cost effective use of early detection and corrective action systems.



Key Attributes

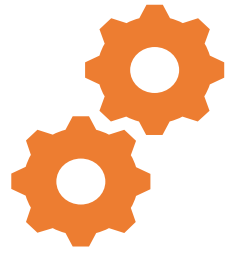
Data Pipeline; to be clean and reliable, governance is required
Automate anything that is repetitive (KPI's, Data Mining, etc.)

Deliver information as part of Analysts' natural workflow

Ability to perform Ad Hoc analyses when required

Continuous Iteration

Key to success is the integration of disparate systems and delivery of information in a manner that matches the natural workflows of Analysts.



Commercially Purchased Tools

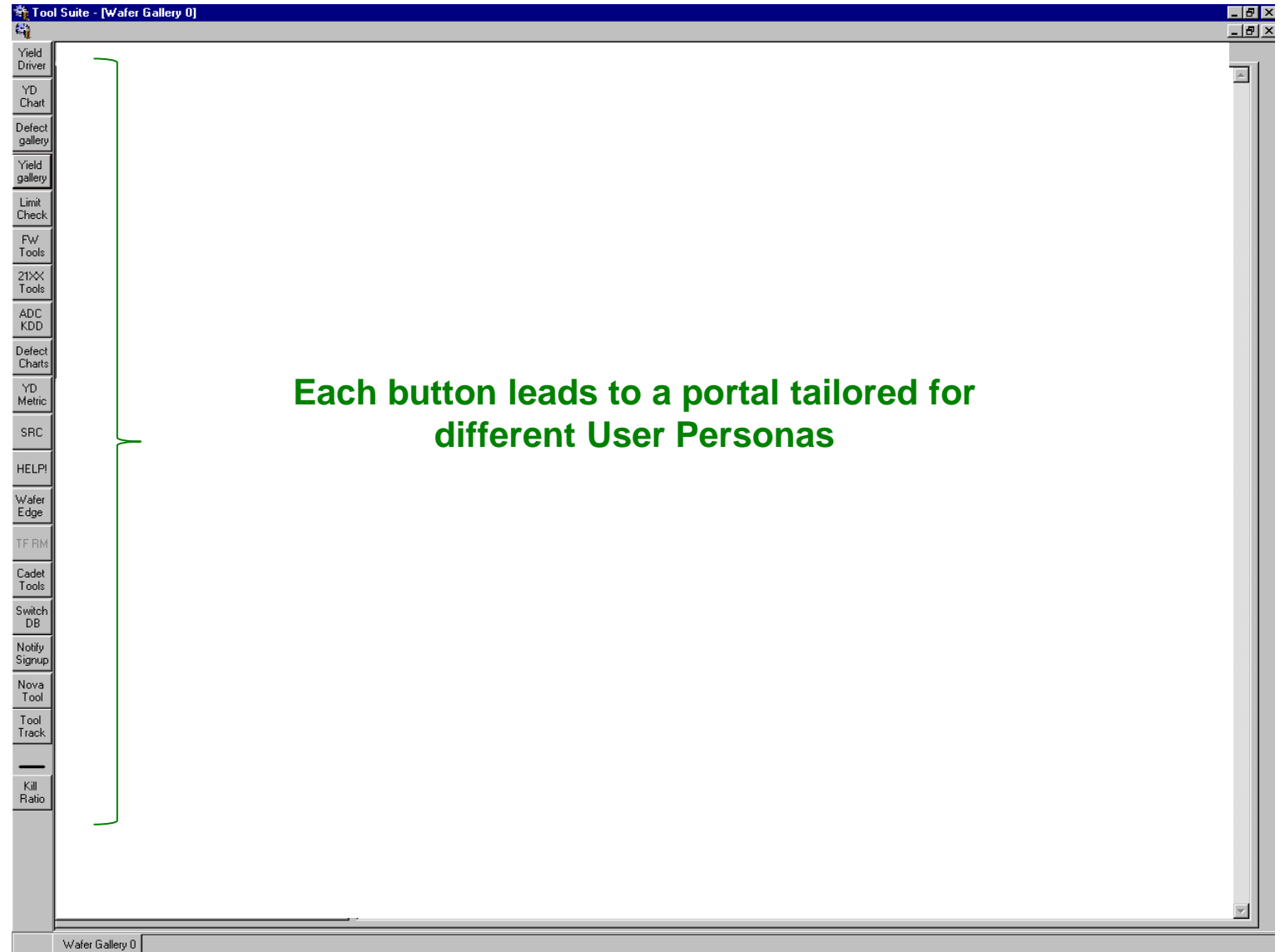
WIP Management
Tool maintenance management
Process Control/Alarm management
Positional Correlation
Defect database
Yield Management Software (YMS)



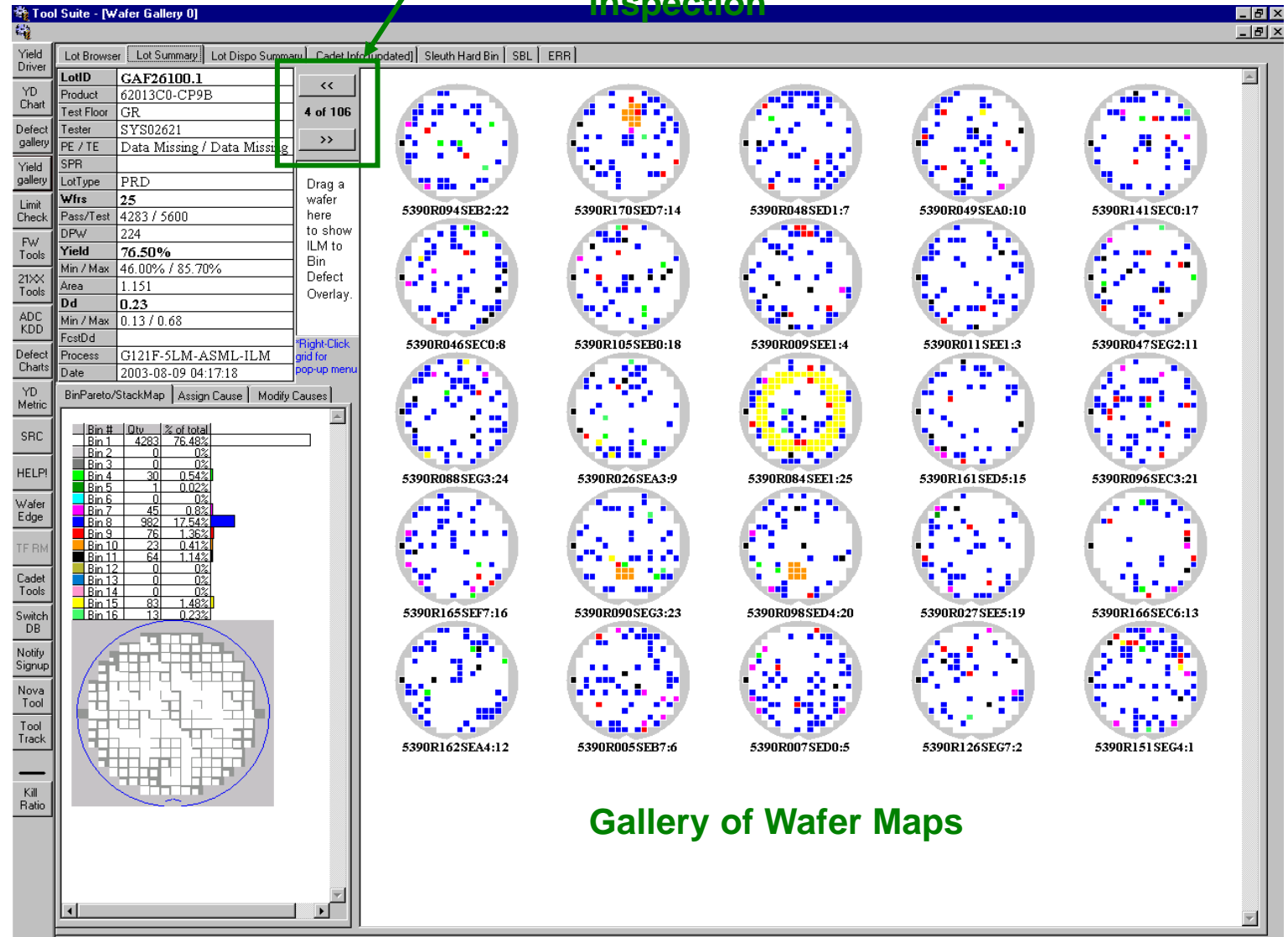
In-House Developed Tools

Tool Suite – Engineering Information Portal
CADET – Corrective Action Defect Event Tracking
SBL – Statistical Bin Limits
ERR – Engineering Run Requests

In House Developed UI
that integrates and
enhances capabilities
of commercially
available software
tools



Fast Scroll to next/previous Lot allows quick visual inspection

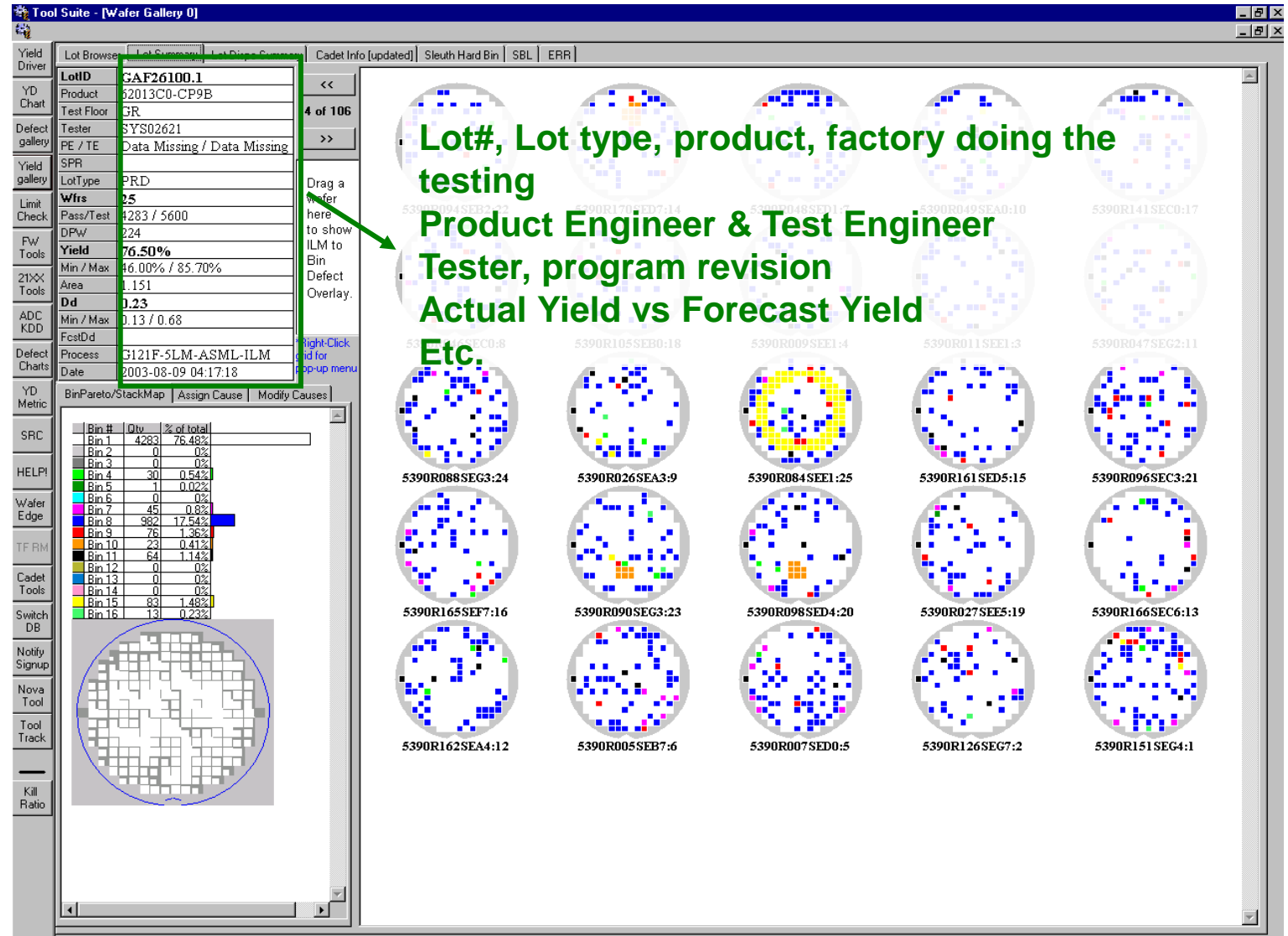


Gallery of Wafer Maps

Previously this info needed to be generated by each Analyst

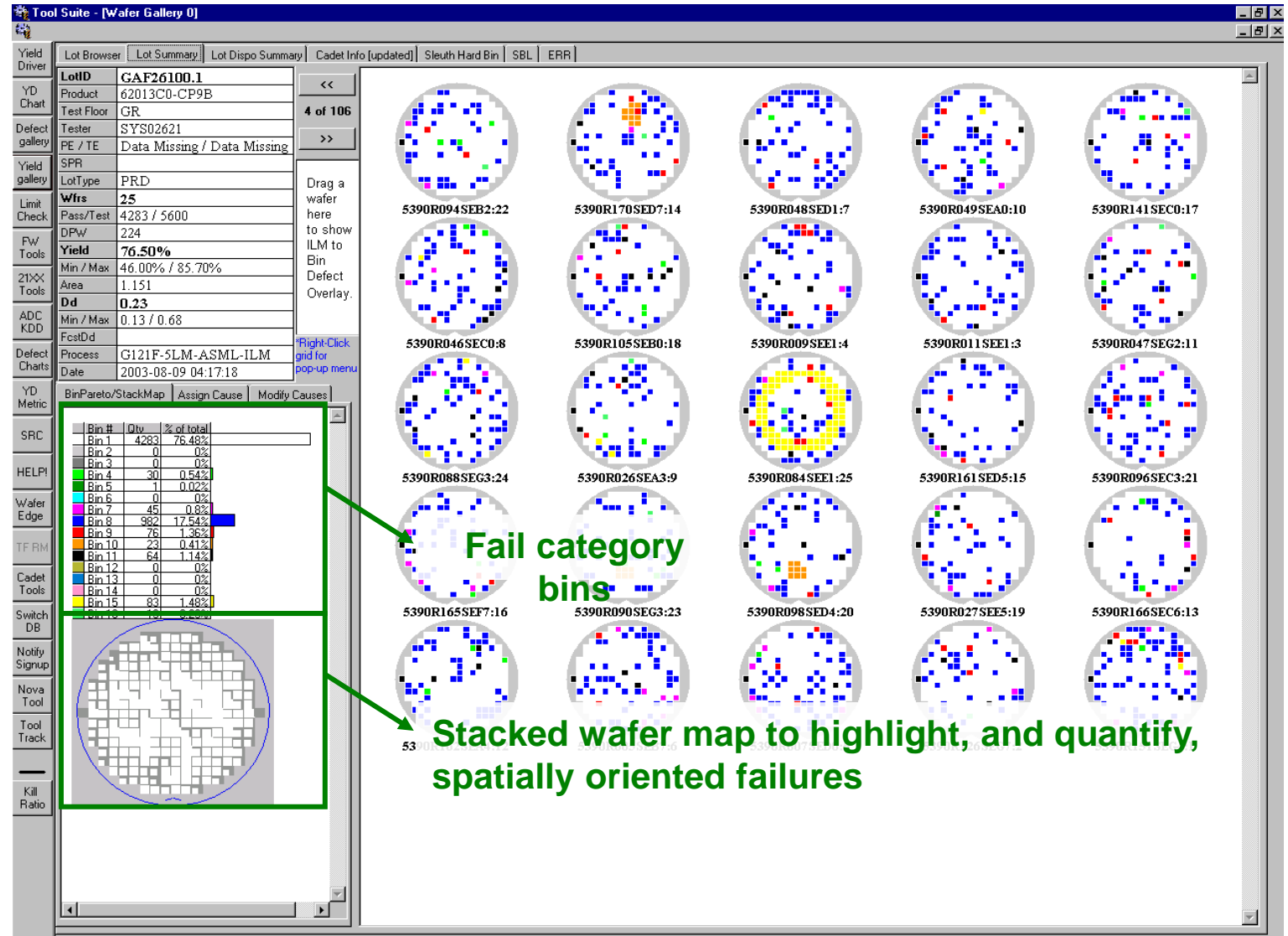
Fast and Easy way to visualize wafer yields

High level contextual
information



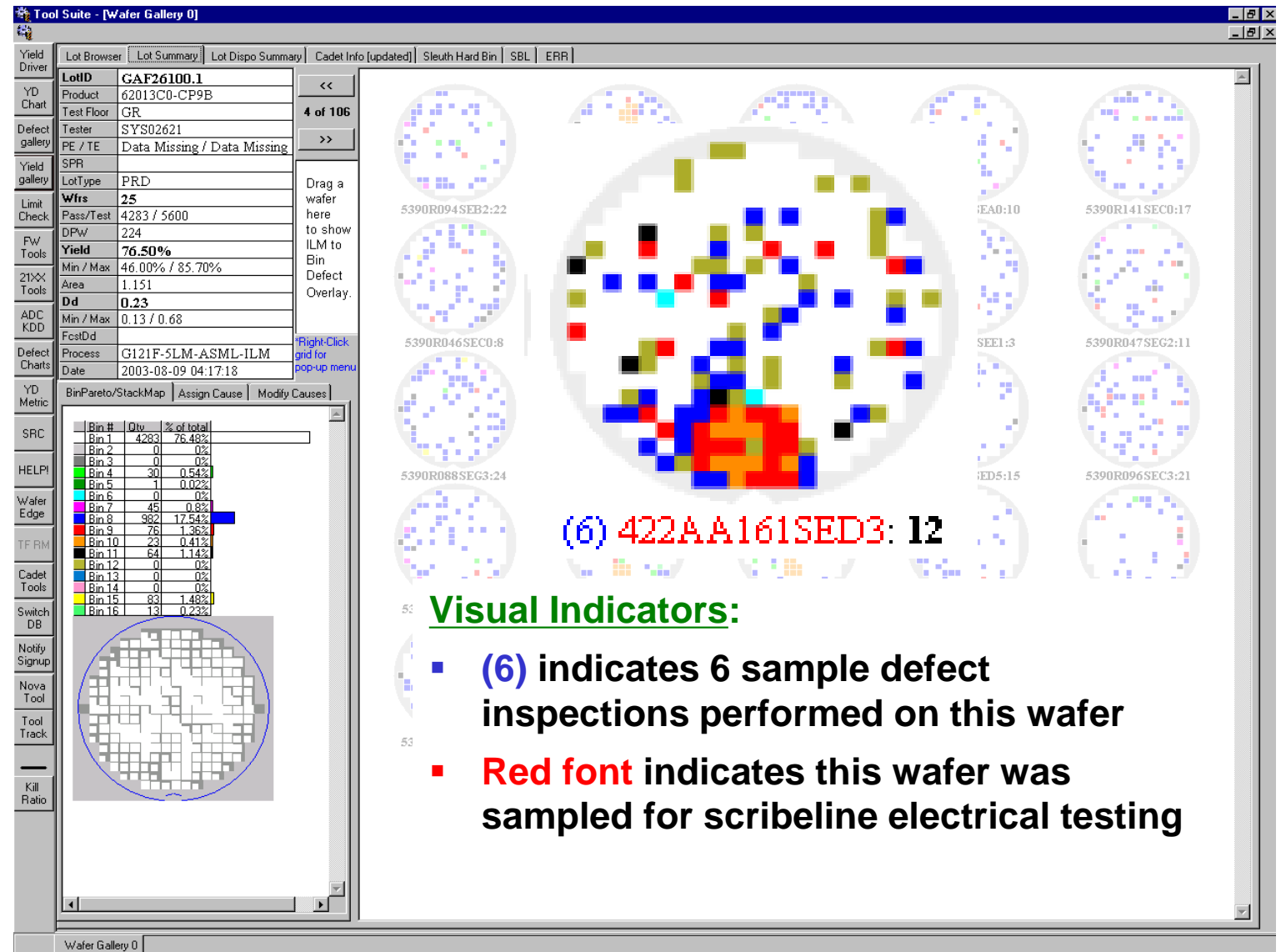
Previously this info needed to be “mined” separately by the Analysts

High level assessment
of fail categories and
spatially dependent
yield signatures



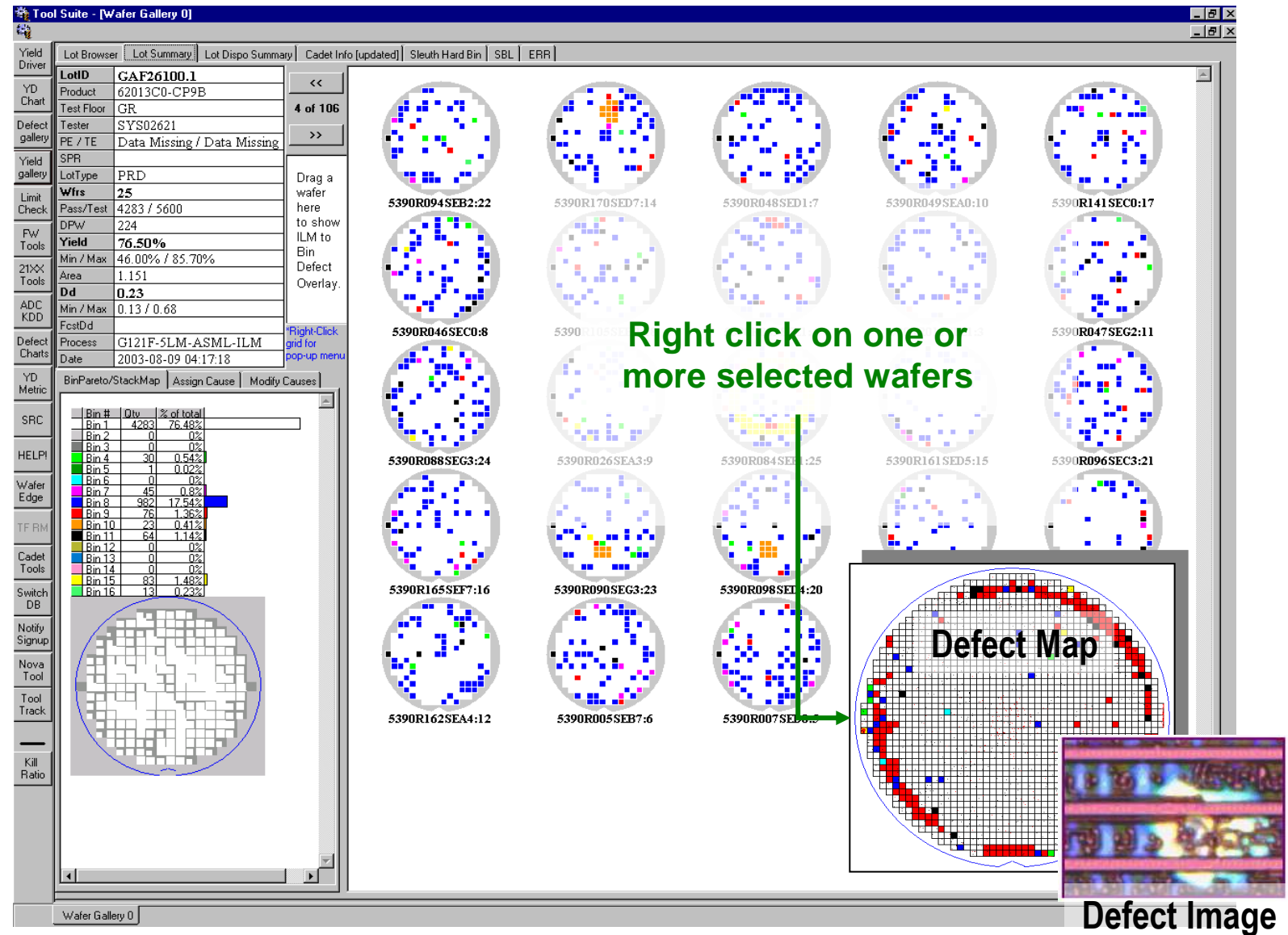
Previously this info needed to be “mined” separately by the Analysts

Additional visual indicators that inform Analysts what other data is available for each wafer



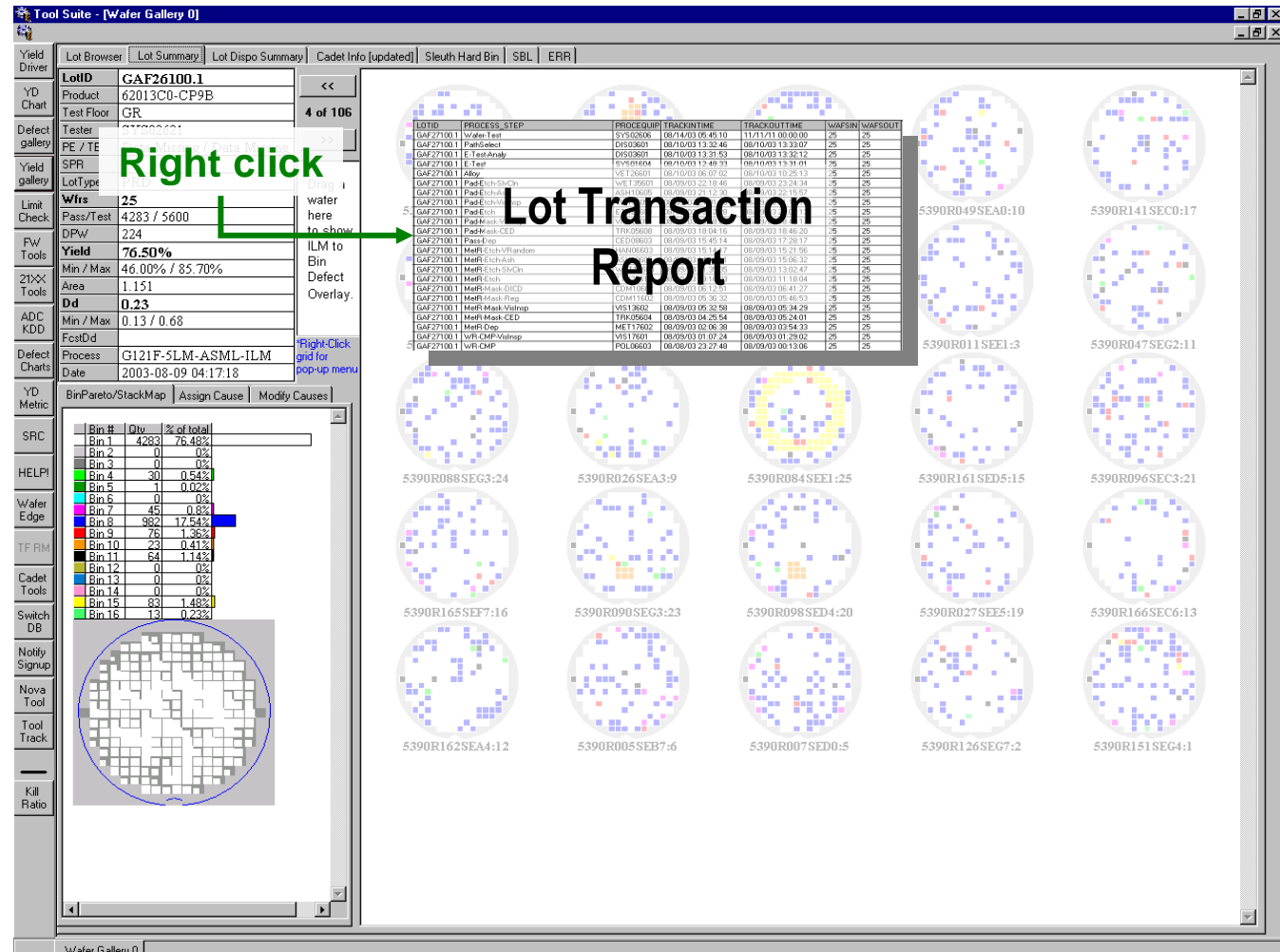
Previously this info needed to be “mined” separately by the Analysts

Inter-Operability (API):
Real-time, right-click
view of defect maps
and images for wafers
of interest to Analyst



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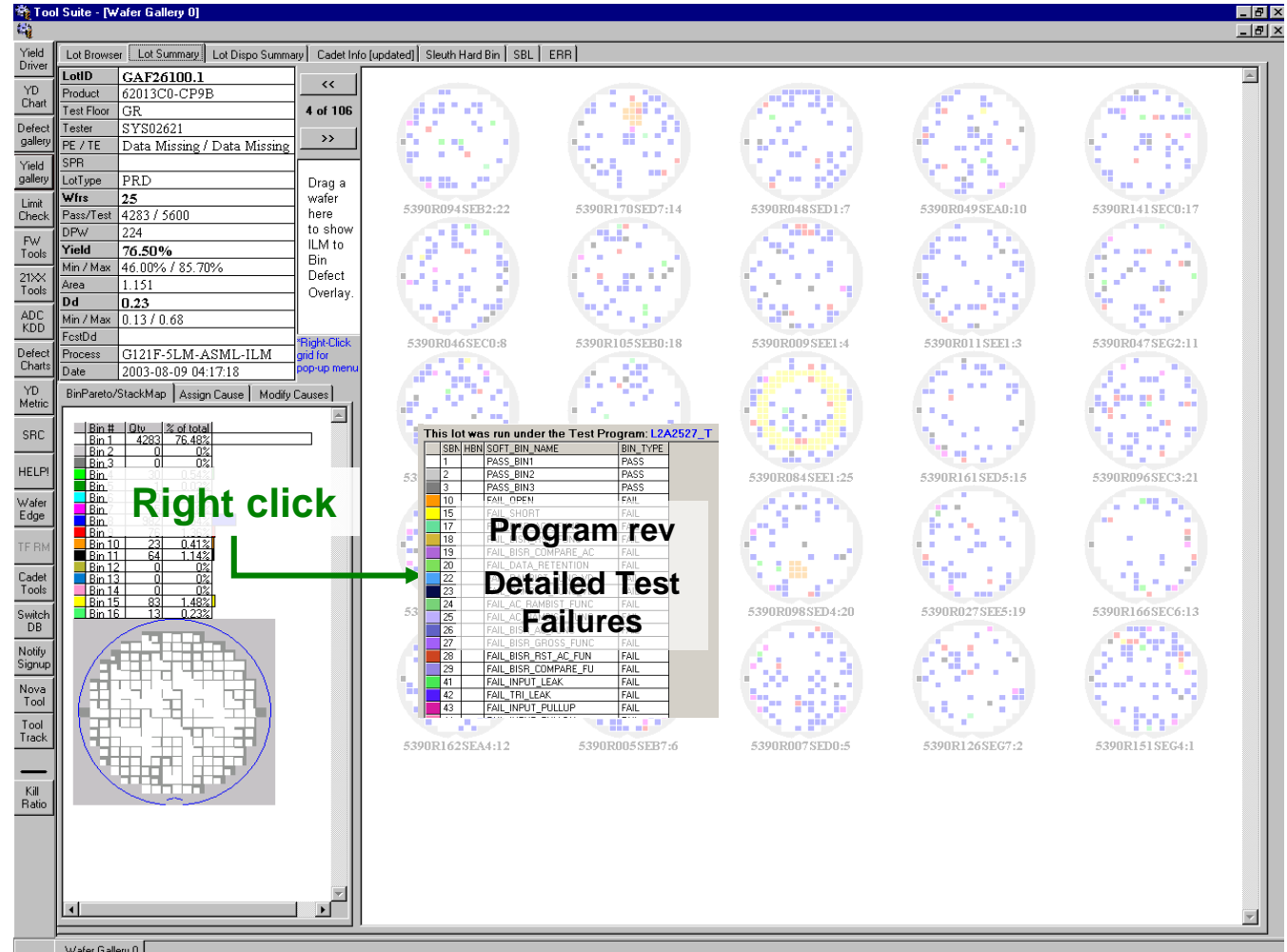
Real-time, right-click
view of transaction
history for lot of
interest



Previously this info needed to be “mined” separately by the Analysts

Inter-Operability (API):

Real-time, right-click
view of test program
revision and detailed
test failures

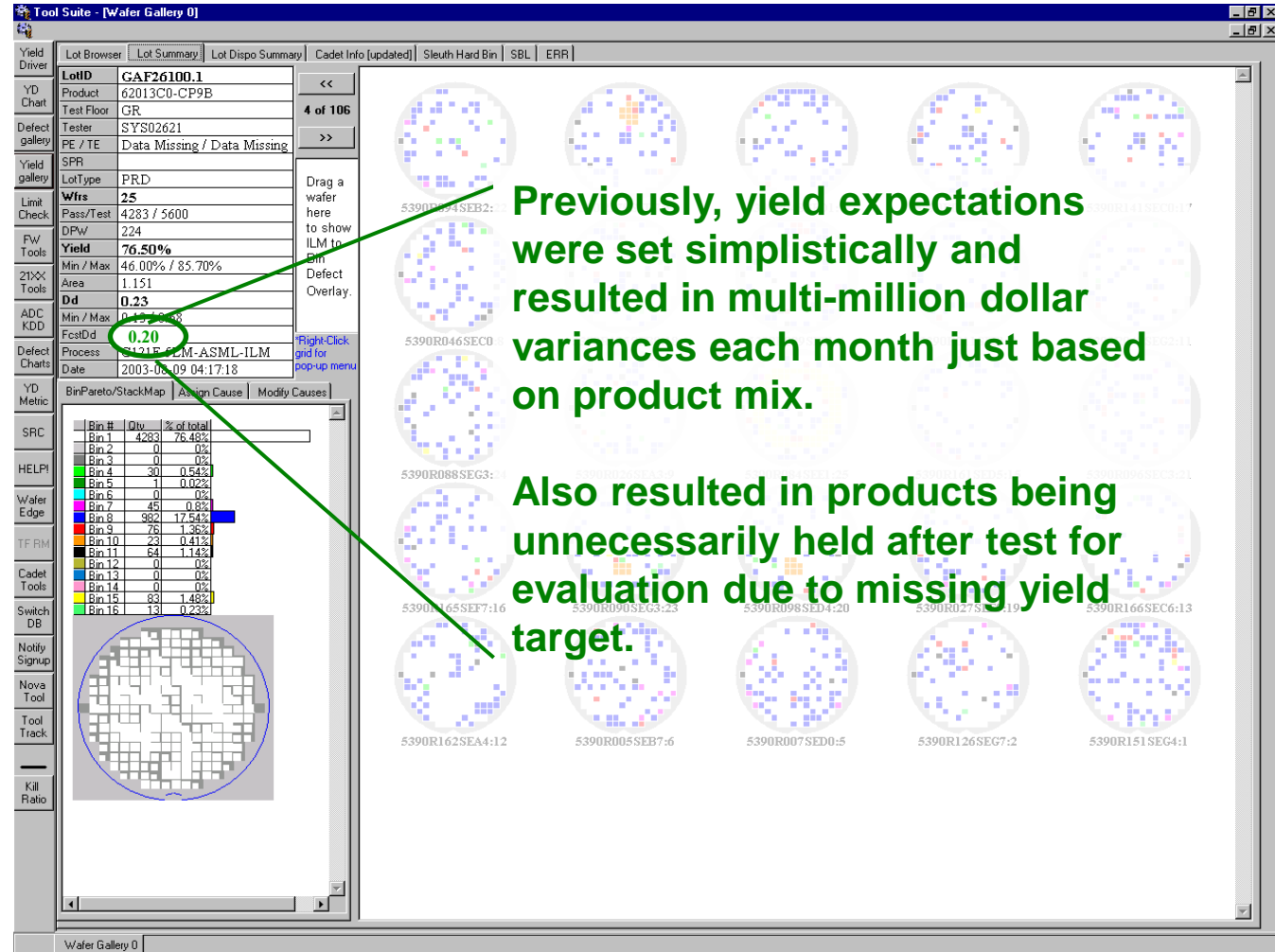


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Machine Learning:

Product Specific Yield forecast based on design features and process flow.

Model consisted of Logistic and Linear Regression for important design and process flow attributes and combinations of attributes.

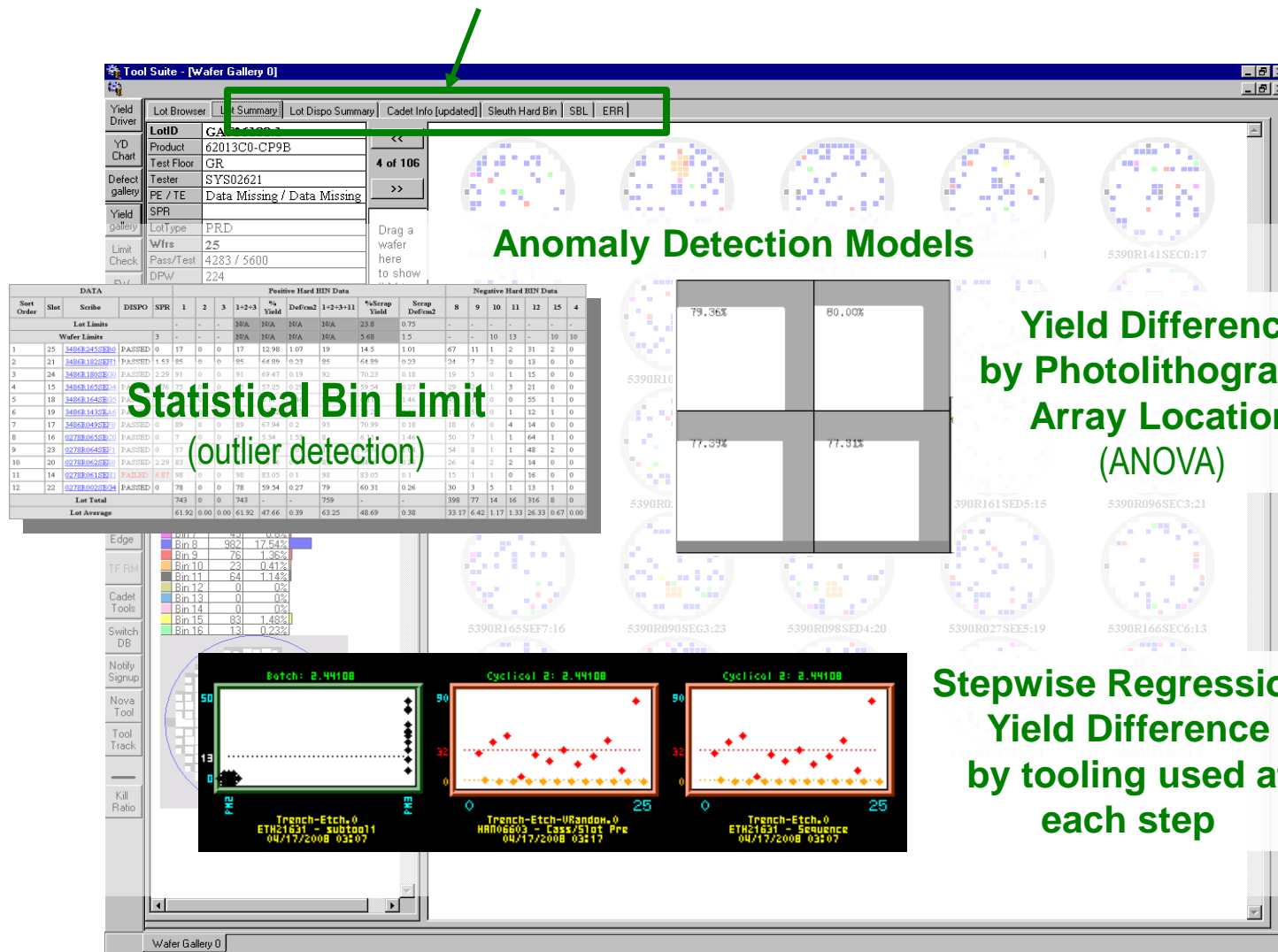


Machine Learning:

Anomaly Detection

- Statistical Bin Limit / CpkN to flag wafers with a-typical fail rates
- ANOVA by Photo Array location to flag repeating failures and across field affects on product performance
- Stepwise Regression to find tooling and sub-tooling that causes yield loss or performance differences

When other model conditions are met, tabs with additional data are presented to Analysts



Previously this info needed to be “mined” separately by the Analyst

Rule based model conditions (if these exist, present to Analyst)

Machine Learning:

- Abnormal process events recorded as Quality Notifications
- Non-standard processing performed as part of an experiment (Engineering Experiment)
- Record of Analysis already performed and documented by an Analyst (Disposition Documentation)

The screenshot displays the 'Tool Suite - [Wafer Gallery 0]' interface. At the top, a navigation bar includes 'Lot Browser', 'Lot Summary', 'Lot Dispo Summary', 'Cadet Info [updated]', 'Sleuth Hard Bin', 'SBL', and 'ERR'. Below this, a table lists wafer details for LOTID GAF26100, including Product (62013C0-CP9B), Test Floor (GR), Tester (SYS02621), and PE / TE (Data Missing / Data Missing). A central panel titled 'Quality Notification History' shows a list of events with columns for LOTID, EVENT DATE, EVENT, EVENT_DESC, and CASE CASE_DESC. To the right, a panel titled 'Engineering Experiment Information' displays 'EXPERIMENT NUMBER: ERR 3021' and 'Lot Number(s): GAF26097.1, GAF26100.1', along with a table of steps affected by area in process flow order. Below this, another panel titled 'Engineering Disposition Documentation' shows a wafer map for '5390R084SEE1:25' with a hotspot noted in cadet. The bottom left panel shows a 'Bin Pareto/StackMap' with a table of bin counts and percentages.

LOTID	EVENT DATE	EVENT	EVENT_DESC	CASE CASE_DESC
GAF26100	08/09/03	107772	Swits of 25 failed SBL (Lot Passed)	1510 Misc Residual W Events in CMP
GAF26100	07/20/03	106065	Hot spots and other signatures @ IM1TM	877 IMD Layer Rip Outs
GAF26100	07/16/03	106076	Possible star pattern on Vid 16, PM2 LUEE yd off ETH21609	0 NA
GAF26100	07/16/03	106076	Possible star pattern on Vid 16, PM2 LUEE yd off ETH21609	373 SICabide defects observed in star pattern (6 spoke or spots 45204L, 3 spoke Eylan)

Bin #	Qty	% of total
Bin 1	4283	76.48%
Bin 2	0	0%
Bin 3	0	0%
Bin 4	30	0.54%
Bin 5	1	0.02%
Bin 6	0	0%
Bin 7	45	0.8%
Bin 8	982	17.54%
Bin 9	76	1.36%
Bin 10	23	0.41%
Bin 11	64	1.14%
Bin 12	0	0%
Bin 13	0	0%
Bin 14	0	0%
Bin 15	83	1.48%
Bin 16	13	0.23%

5390R084SEE1:25

Hotspot noted in cadet. Residual tungsten seen as color/klarity changes in inline images for this wafer - most likely W1 as images as IMD1. Assigning to cases.

Previously this info needed to be “mined” separately by the Analyst

A close-up photograph of a person's hand, with the index finger pointing at a tablet screen. The screen displays a green heatmap or bin map, which is a visualization of data points. The background is dark, and the lighting is focused on the hand and the screen.

Additional Right-click capabilities...

Side by side comparison of bin maps to defect inspection maps

Lot commonality: Multiple lots with similar fail patterns can be flagged during review of yield maps and run through a “commonality analysis”

Tool maintenance history

Answered with zero effort from Analyst..

- Yield vs Forecast?
- Were there outlier bin failures?
- What do wafer maps look like? Spatial Yield patterns?
- Repeating Pattern of Failures?
- Who are Product, Test Engineers?
- Where was the lot tested, on what tester?
- Bin Pareto?
- What tests are in each bin?
- What revision of the test program was used?
- Which wafers were inspected for defects?
- Which wafers were scribeline tested?
- Was there non-standard processing?
- What is documented for analysis that was already done?





More could be answered..

Scribeline Test to Wafer Test auto correlation
(bin and parametric)

Commonality across lots with similar spatial patterns

Auto correlation to In Line measurement / metrology data

Conclusion

This presentation demonstrated capabilities that provided immensely improved efficiencies to data analysts in the semiconductor industry, and which were well before their time.

Replicating, and improving upon, these capabilities with modern software and hardware is feasible.

I hope to share more information on other insightful approaches to semiconductor yield improvement.