SMT Module Integration

Application Note 48

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Technical Documentation

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1 Applicability Table

Table 1: **Applicability table**

Products
Cinterion® TX62-W
Cinterion® TX82-W

2 Introduction

2.1 Scope

The purpose of this document[1] is to aid the integration of Telit Cinterion DIS AIS SMT modules into external applications by discussing module mounting issues as well as application layout issues such as test points for trace, debug and general access purposes or by showing how to enable interfaces for firmware updates. The document also describes additional equipment supporting SMT application development for Telit Cinterion modules.

2.2 Audience

This document is intended for system integrators that are using the Telit Cinterion® TX62-W and TX82-W modules in their products.

2.3 Contact Information, Support

For technical support and general questions, e-mail:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com
- TS-ONEEDGE@telit.com

Alternatively, use: https://www.telit.com/contact-us/

Product information and technical documents are accessible 24/7 on our website: https://www.telit.com

2.4 Conventions

Note: Provide advice and suggestions that may be useful when integrating the module.

Danger: This information MUST be followed, or catastrophic equipment failure or personal injury may occur.

ESD Risk: Notifies the user to take proper grounding precautions before handling the product.

Warning: Alerts the user on important steps about the module integration.

All dates are in ISO 8601 format, that is YYYY-MM-DD.

1. The document is effective only if listed in the appropriate Release Notes as part of the technical documentation delivered with your Telit Cinterion product.

2.5 Related Documents

[1] AT command set related to your Telit Cinterion product
[2] Hardware Interface Description related to your Telit Cinterion product
[3] Application Note 16: Updating Firmware related to your Telit Cinterion product

2.6 Abbreviations

Abbreviation	Description
BGA	Ball Grid Array
BLR	Board Level Reliability
DCE	Data Communication Equipment
DTE	Data Terminal Equipment
ENIG	Electroless Nickel Immersion Gold
LGA	Land Grid Array
PCB	Printed Circuit Board
RF	Radio Frequency
RMA	Return Merchandise Authorization
SMD	Surface Mount Device
SMT	Surface Mount Technology
TC	Thermocouples
TP	Test Point
UART	Universal Asynchronous Receiver-Transmitter

2.7 Terms and Conditions

Refer to https://www.telit.com/hardware-terms-conditions/.

2.8 Disclaimer

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3 SMT Application Layout Issues

3.1 Test Points on Application Board

While developing SMT applications it is necessary to provide test points for certain signals respective lines to and from the module – for debug and/or test purposes during the manufacturing process. In this way it is possible to detect soldering problems. The SMT application needs to allow for easy access to these signals – including but not limited to the ones shown in Figure 1 for TX62 and TX82 with a 1.8V voltage level; for module voltage domains see also [1]). The test points provide for a cost-efficient analysis during end-of-line tests in application production. The more signals and interfaces are available for testing the faster the analysis can be done.

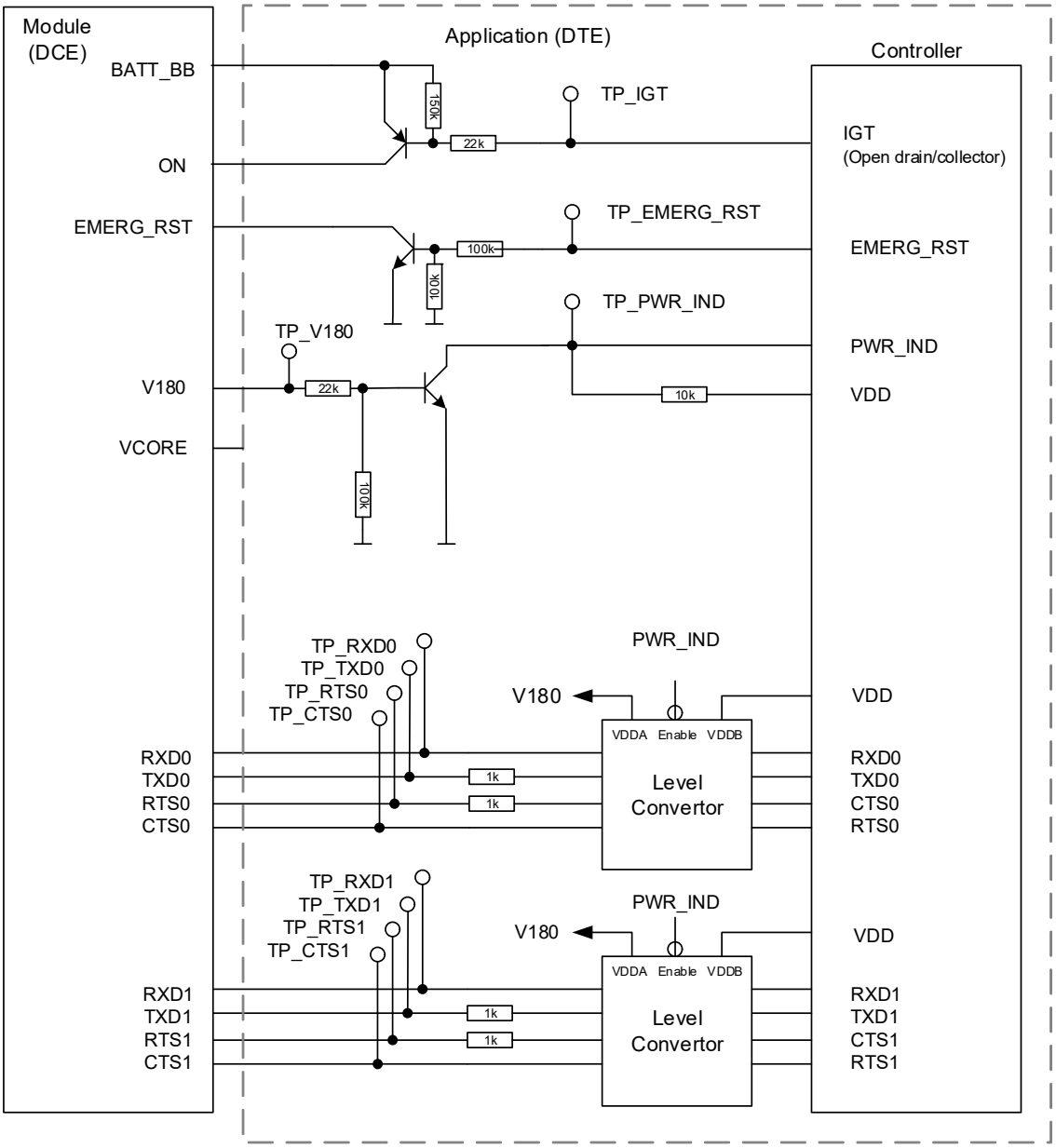

Figure 1: Test points for TX62/TXS82 SMT applications (ASC0 has a 1.8V voltage level)

To reduce the time required to access the module via test points it is recommended to implement a certain layout:

- Generally, test points should be implemented for at least the outgoing signals from the module, while serial resistors should be populated for incoming signals (except for open collector signals such as IGT).
- Test points and serial resistors should be placed as close as possible to the module to minimize RF interference.
- Test points should also be available to provide module access independently of the SMT application in order to check the module's functionality separately. While accessing the module, for example from an external development environment, it should be ensured that the SMT application does not interfere with the test point access. Therefore, all lines together with their location on the SMT application, test points and possibilities for an interruption should be well documented.
- If the test point layout is done in a standardized way, an easy access can be provided.

The following table describes the mandatory signal test points that should be implemented for SMT applications (as far as the module supports the interface lines) as well as some optional test points that might be implemented in case the signals are used.

Table 2: Mandatory and optional test points for SMT applications

Test point	Required	Description
TP_PWR_IND	Yes	Low power indication level signals active state of module.
TP_IGT	Yes	A low IGT state switches the module on.
TP_EMERG_RST	Yes	A high level for more than 10ms sets module to its reset state. After release, the module restarts.
TP_V180	Yes	1.8V external supply voltage.
TP_RXD0	Yes	Asynchronous serial transmit signal of module (ASC0) 1.8V signal level.
TP_TXD0	Yes	Asynchronous serial receive signal of module (ASC0) 1.8V signal level.
TP_RTS0	Yes	Ready to send input of module (ASC0) 1.8V signal level.
TP_CTS0	Yes	Clear to send output of the module (ASC0) 1.8V signal level.
TP_RXD1	Recommended	Asynchronous serial transmit signal of module (ASC1) 1.8V signal level only.
TP_TXD1	Recommended	Asynchronous serial receive signal of module (ASC1) 1.8V signal level only.
TP_RTS1	Recommended	Ready to send input of module (ASC1) 1.8V signal level only.
TP_CTS1	Recommended	Clear to send output of module (ASC1) 1.8V signal level only.
TP_VBATT	Recommended	Measure power consumption at V_{BATT+}

3.1.1 Measuring Power Consumption

To be able to measure power consumption or to use an external power supply (disconnection from application power) during the development phase of an SMT application, it is possible to set up an additional measuring point on the SMT application's PCB. Figure 2 shows how to arrange for such a simple measuring point (recommended as optional TP_VBATT in Table 2) by implementing a 0-Ohm-bridge on the BATT+ line. By cutting this bridge and populating a 0.1Ohm resistor instead, it is possible to measure power consumption. Note: At high power consumption the 0.1Ohm resistor leads to a higher voltage drop in transmit mode. It is therefore recommended to apply an operating voltage V_{BATT+} > 3.8V.

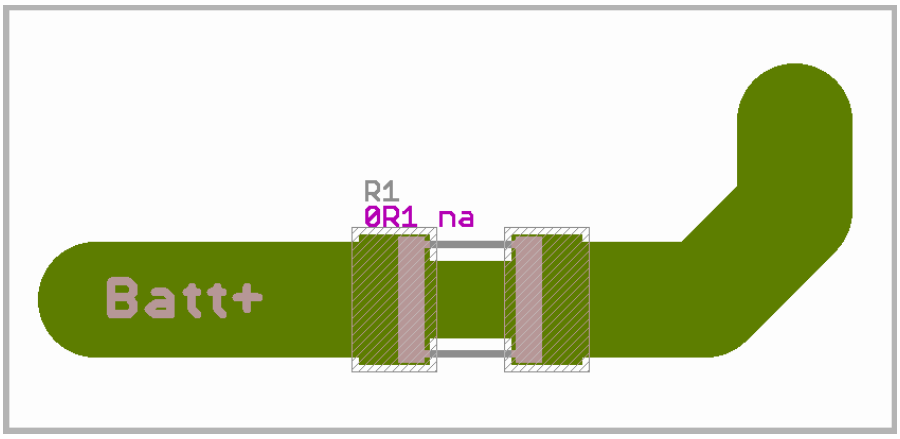

Figure 2: Measuring power consumption

3.1.2 Module Footprint

If the module footprint on the SMT application's PCB is modelled on the BGS2/AGS2 evaluation module's footprint (see Figure 3), some of the test points mentioned in Section 3.1 are directly available at the overlapping solder pads. These test points are: TP_V180, TP_VCORE TP_RXD0, TP_TXD0, TP_RTS0, TP_CTS0, TP_RXD1, TP_TXD1, TP_RTS1 and TP_CTS1. For the other test points additional components will have to be populated on the SMT application's PCB. See also Figure 3.

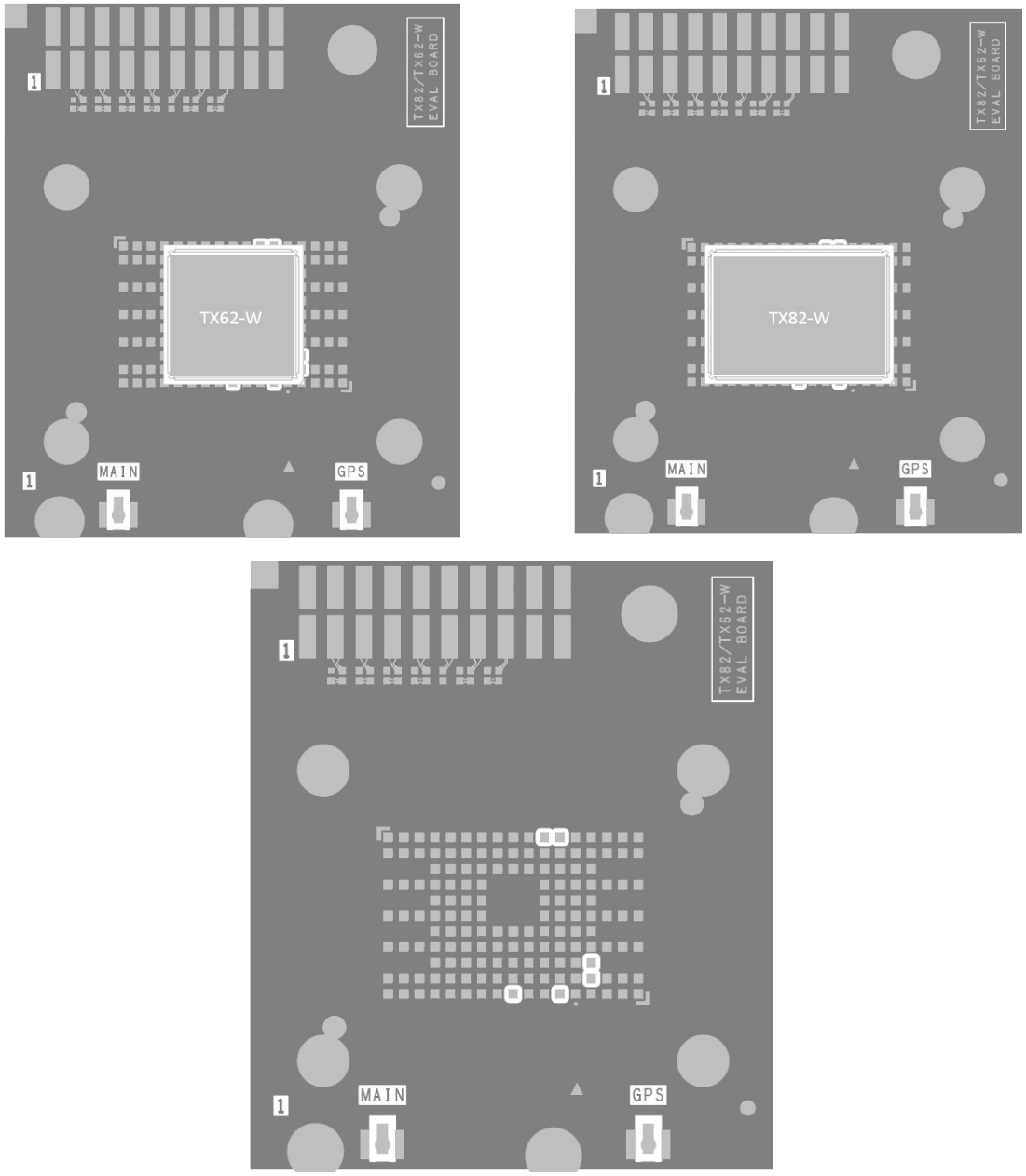

Figure 3: Evaluation module and evaluation board footprint (BGS2 sample)

Please note that the dimensions of the SMT application's module footprint correspond to the land pattern dimensions given in [2].

3.2 Examples for Debug Connections

This section describes how to connect the module via its test points to either the serial interface of a PC (see Section 3.2.1) or to Telit Cinterion DSB75 evaluation board (see Section 3.3). After connecting the module to a PC or the DSB75 the module has to be activated before the debug connection is switched on.

3.2.1 Connection to the Serial Interface of a PC

Figure 4 shows sample circuits to connect the module via serial interface test points to the serial interface of a PC. Depending on the given voltage level the sample circuit has to be slightly adapted and can then be used for either ASC0 and ASC1 in case the voltage level is 1.8V.

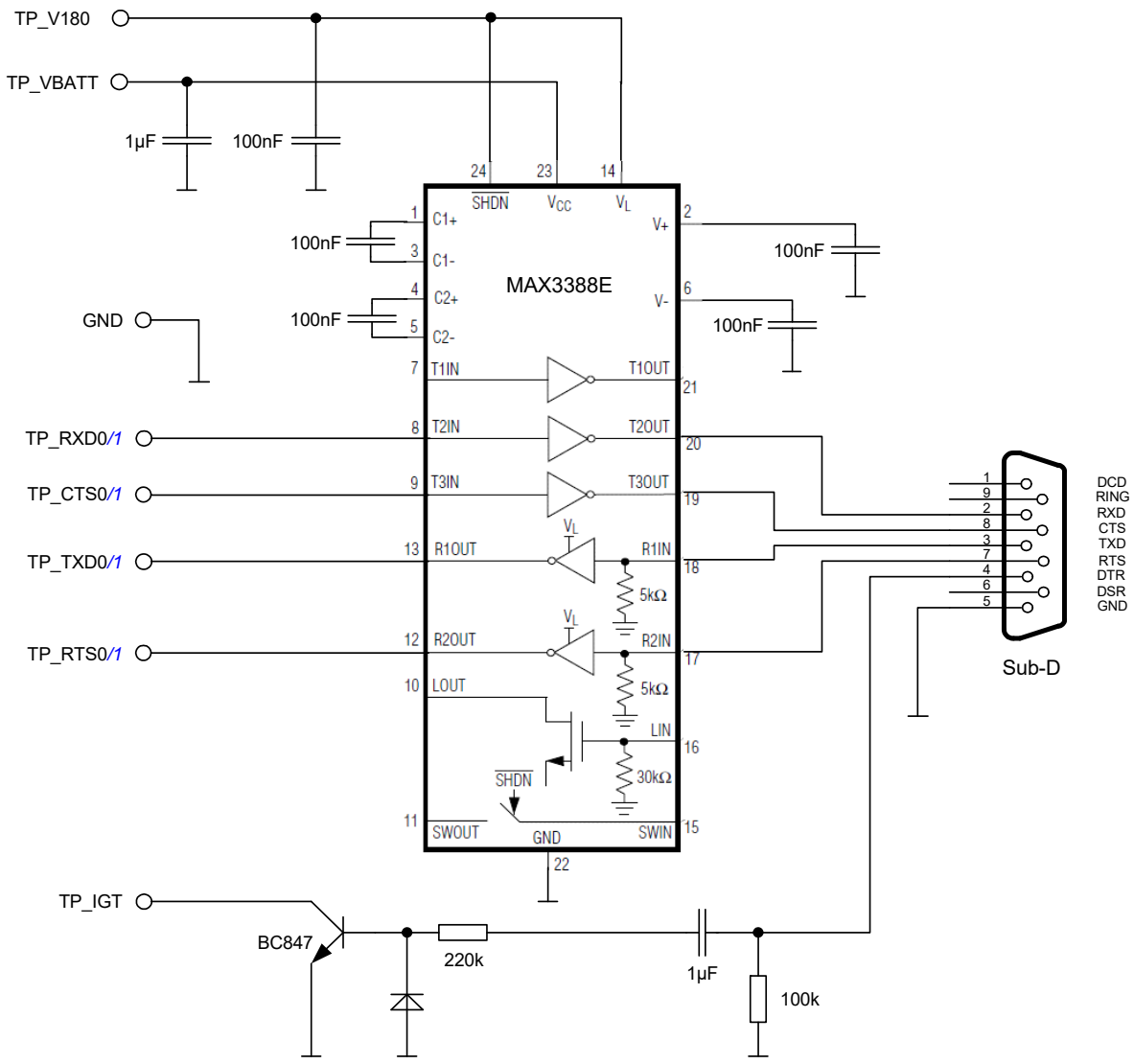

Figure 4: Schematic for a debug connection for serial interface ASC0 and ASC1 (voltage level of 1.8V)

3.3 Update Interface

To support module firmware updates, an update interface to the module via the application needs to be available. This way the application is ready to adapt to potential future mobile network changes that might impact its performance. Therefore, it is recommended to provide the update interface (hard- and software) to protect the investment over the application life time. For more information on firmware updates see also [3].

Since the module cannot be removed from the SMT application, the following notes should be taken into account as a pre-requisite to updating.

3.3.1 SMT Application Using the Serial (UART-) Interface ASC0

If the SMT application uses the UART interface of the module (ASC0), the SMT application's microcontroller should be able to transfer the module's UART signals transparently to a defined microcontroller interface - thus initializing a transparent UART mode. This defined microcontroller interface should link to an externally accessible connector. A special update mode may be introduced to temporarily block the defined interface for update purposes. In this case the microcontroller's defined interface is used only temporarily to download the new firmware.

The RXD0 and TXD0 signals should be transparently transferred through the SMT application's microcontroller with as little delay as possible. In addition, an IGT signal may be required to restore original baud rate settings in case these were changed during a firmware update with gWinSwup (for details on firmware updates see also [3]). It should then be ensured that IGT is based on DTR's rising edge and implemented as open drain/collector or high impedance. The following figure show how to create this signal differentiation- the rising DTR edge generates an IGT low pulse longer than 400ms. The circuit can be implemented on the SMT application's PCB, but it may also be part of the "debug adapter" connection (see Section 3.2.1).

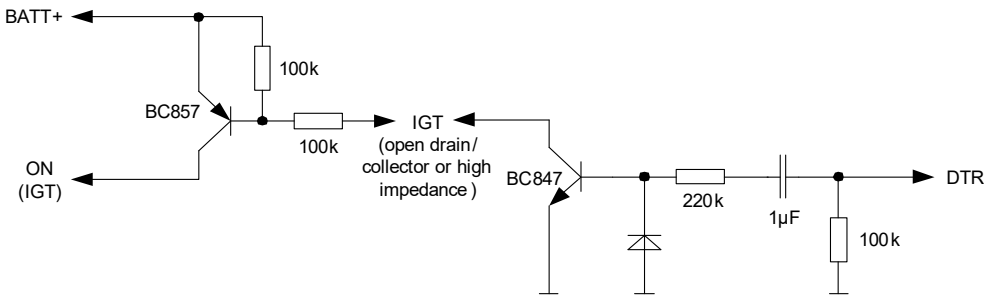

Figure 5: ON based on DTR's rising edge (Cinterion® TX62/TX82)

4 SMT Application Development Equipment

To support the development of SMT applications, Telit Cinterion provides optional equipment such as daisy chain modules or evaluation modules. The following sections introduce this equipment and list ordering details. For more information please contact Telit Cinterion.

4.1 Daisy Chain Modules (BGS2/AGS2)

Daisy chain modules are an optional aid in developing SMT applications. The daisy chain modules provide a "line bus" that connects the module's pads in series and allows for electrical signals to be passed from pad to pad depending on the wiring scheme as for example given in Section 4.1.1.

Thus, the daisy chain modules are especially suited to verify soldering stencils, check electrical connections, evaluate solder joints etc.

Daisy chain modules may be soldered onto the connection carrier shown in Figure 7 just as the real SMT modules would onto the application boards. Mechanical dimensions and footprints of the daisy chain modules correspond to the SMT modules. For details refer to [2].

4.1.1 Wiring Scheme

The following figures show the daisy chain wiring scheme, i.e., the pad interconnections on the soldering sample module as well as on the carrier including IN and OUT pads. The daisy chain module provides two daisy chain circuits: Standard pads and RF pads. The daisy chain connection is build up as double daisy chain. With two different signals it can be tested whether a connection is valid and whether a short circuit is not valid.

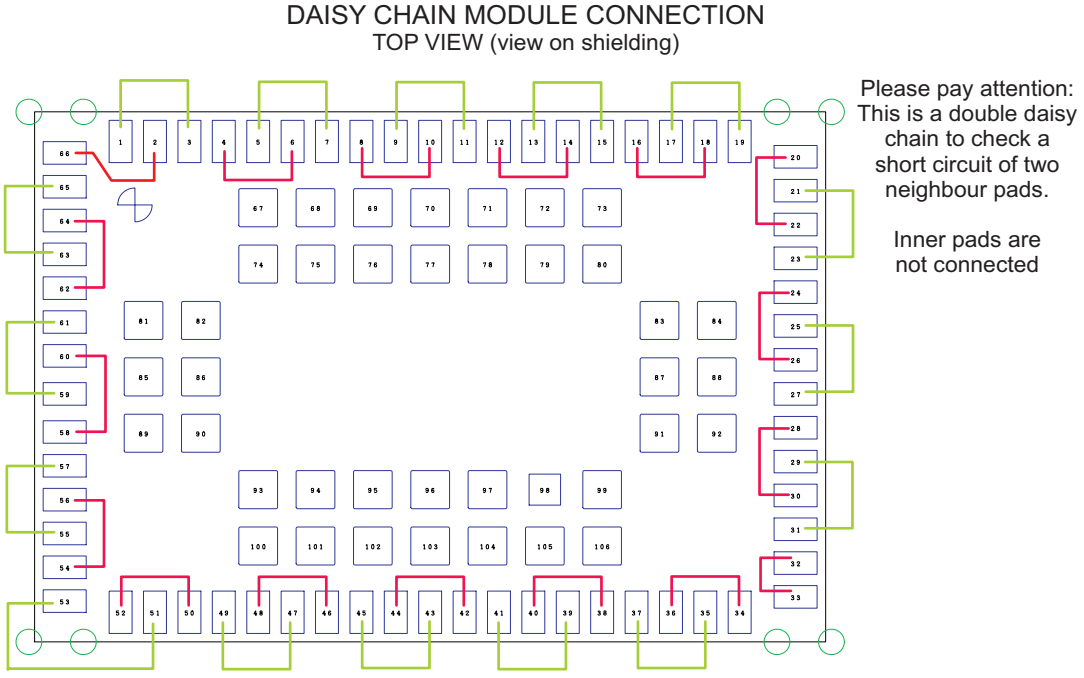

Figure 6: Daisy Chain interconnections of the soldering sample

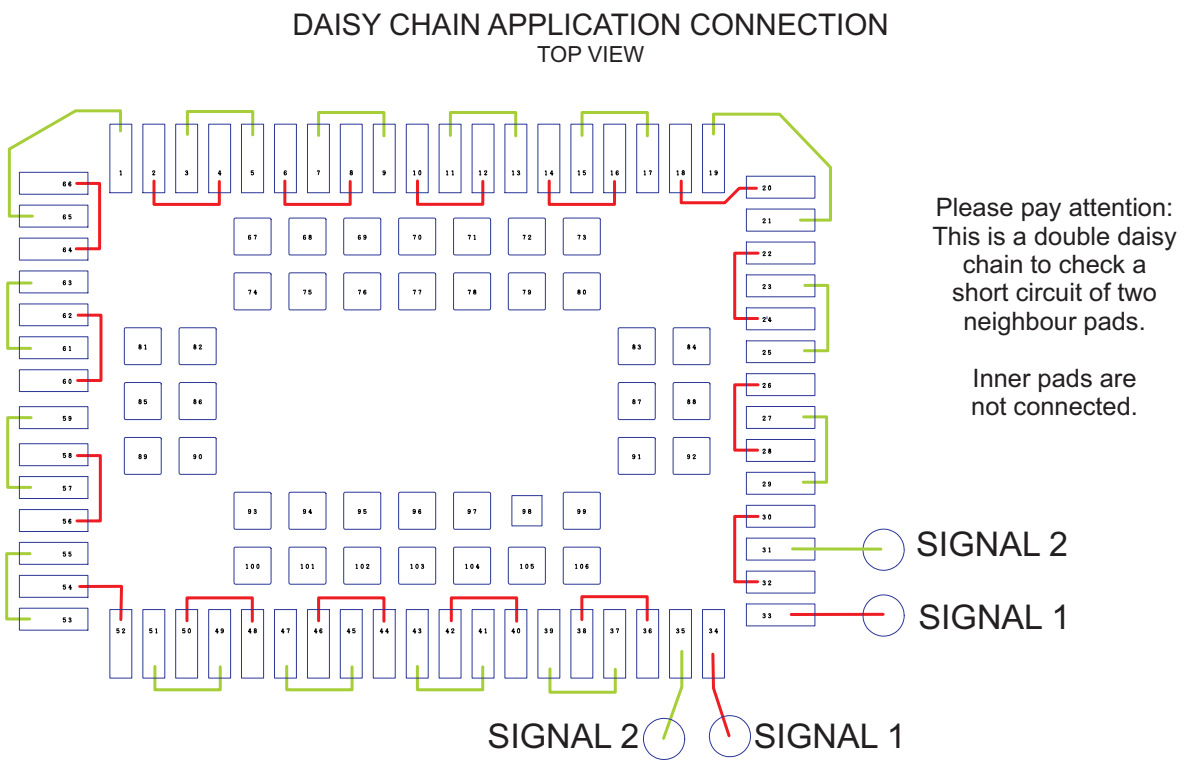

Figure 7: **Daisy Chain interconnections of the carrier**

4.2 Evaluation Modules

4.2.1 TX62/TX82 Evaluation Modules

For testing and debugging purposes it is possible to use an TX62/TX82 evaluation module (see Figure 8 for an TX62/TX82 sample). The evaluation module comprises the actual SMT module soldered onto a PCB with a 80-pin board-to-board connector on its bottom side that can be connected via AH6-DSB75 Adapter to Telit Cinterion DSB75 Evaluation Kit (see Figure 22). The RF antenna can be connected to the AH6-DSB75 Adapter as well.

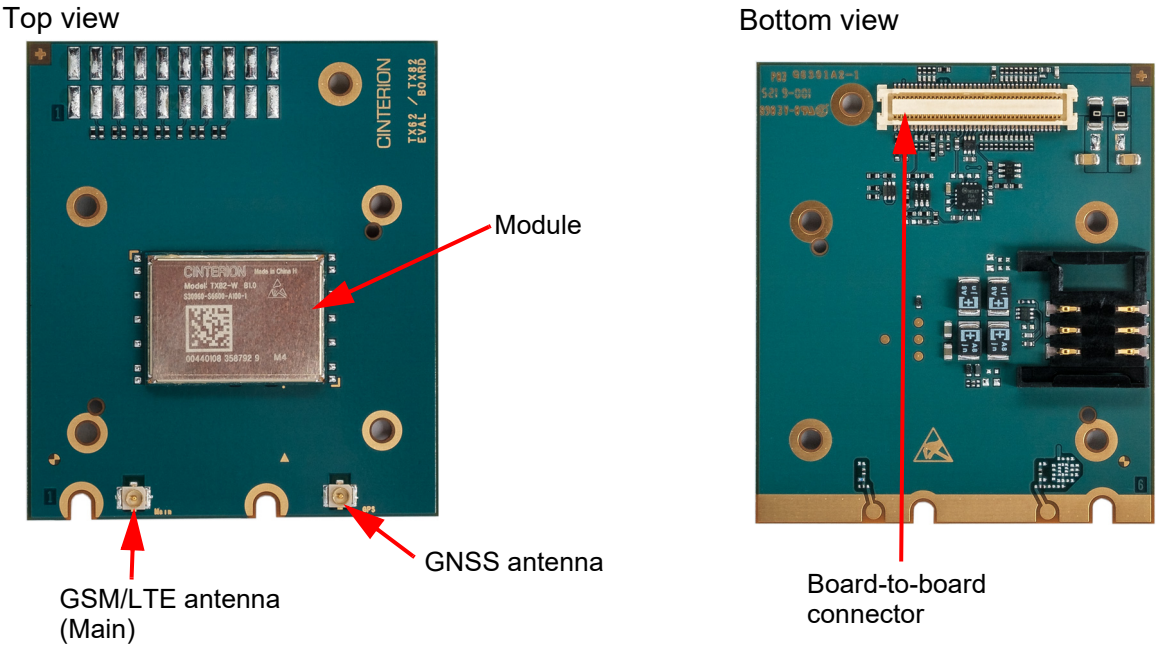

Figure 8: TX62/TX82 evaluation module

4.3 Ordering Information

The following table lists ordering numbers for the above described development support equipment.

Table 3: Ordering information

Equipment	Ordering number
Evaluation module	See [2].
Mounting adapters: 1) AH6-DSB75 Adapter 2) 60/80 Adapter	 L30960-N2301-A100 L30960-N2502-A100
Daisy Chain modules (delivery units of 50 modules)	On request.

5 Module Mounting Issues

Cinterion® TX62/TX82 modules have been designed with an easy integration into SMT processes in mind. Some module mounting issues are discussed in more detail in the sections below.

Please note that the supported modules are specified for one soldering cycle only. Once removed from the application, the module will very likely be destroyed and cannot be soldered onto another application. Please also note that the modules are not sealed and should therefore not be subjected to any post SMT wash or to any environments where condensation could occur.

5.1 Solder Paste

A variety of solder paste types can be used to realize connections to external applications. Soldering using lead free eutectic SnAgCu alloy can be done without any special restrictions, because of its maximum allowed temperature of 245°C.

ENIG finish of the modules soldering pads ensures good wetting properties even after 12 month of storage.

However, there are some restrictions that should be noted before selecting the solder paste: Due to the fact that the top side of the modules is assembled using standard eutectic SnAgCu alloy, no higher melting alloys should be used (even though remelting of top side solder joints also happens with eutectic SnAgCu).

Higher temperatures mean more stress to materials than lower temperatures: Increasing the reflow temperature increases the growth of intermetallics, especially if the temperature lies above the melting point of that alloy. Large intermetallics are commonly considered a reliability risk. They should therefore be kept as small as possible.

Table 4: Solder paste products used for BLR tests

Parameter	Koki S3X58-M406-L3	Senju M31-GRN360-K1Mk
Alloy	SnAg3Cu0,5	SnAg3,5Cu0,75
Powder Type	20-38µm (type 4)	25-45µm (type 3)
Flux content	11,5 wt%	11,5 wt%
Melting point/range	217°C	217-219°C

There are no special restrictions for powder type of solder material used for connections of the SMT module, but it is recommended to use type 3 or 4.

5.2 Stencil Printing

5.2.1 General Stencil Considerations

The higher the stand off formed by the solder paste volume, the better the reliability for land grid array (=LGA) based connections. The solder paste volume in a stencil printing process is formed by aperture size (area) and stencil height:

$Volume_{Solder\ paste} = Area_{Aperture} \times Height_{Stencil}$

It is recommended that customers do their own testing to determine the optimal solder paste volume. This volume can be applied by stencil printing with different stencil heights to fit your existing assembly needs. The volume is kept constant by varying the aperture size accordingly. The most common thicknesses 110µm resp. 120µm and 150µm (stainless steel, laser cut) have been tested with good results with regard to printing process, soldering process and reliability testing. Similar results are expected with stencil thicknesses in between.

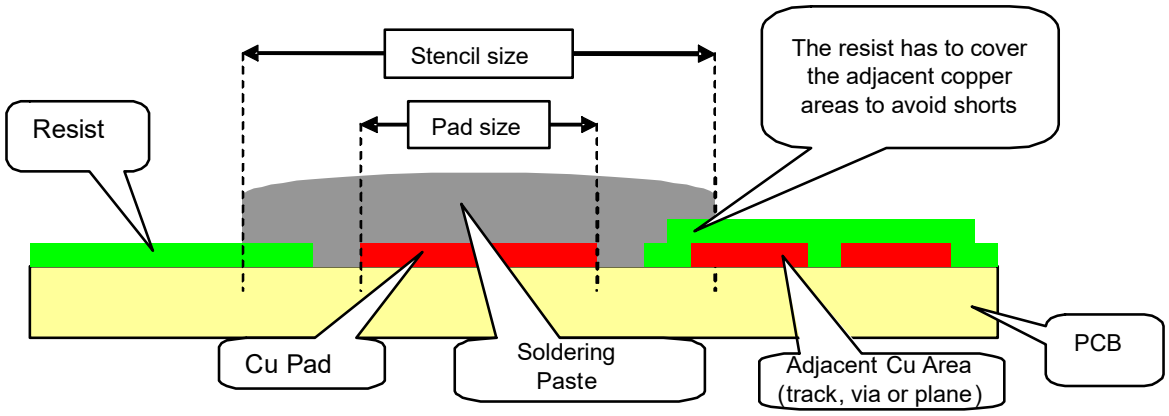

Figure 9: **Overprinting of solder paste**

Different solder paste volumes have been tested too but with much lower volume there is a trend to poor solder joints and a risk for open joints. Much larger solder joints tend to form solder balling in the vicinity of the solder joints.

5.2.2 Used Parameters and Recommendations

For stencil printing, a stainless steel stencil, laser cut (or similar technology) should be used. Parameters must be optimized depending on actual application board design, equipment and solder paste.

For Telit Cinterion reliability testing a DEK printer Infinity and Horizon as well as a Speedline Accela printer were used. The parameters are listed in Table 5 below. The thickness of the used stencil was 110µm and 150µm for TX62/TX82.

Table 5: Parameters for stencil printing used for BLR tests

Parameter	Koki S3X58-M406-L3	Senju M31-GRN360-K1Mk
Squeegee pressure	5kg	4.5kg
Speed	50mm/s	30mm/s
Lift speed	20mm/s	0.5mm/s
Lift height	2mm	2mm
Temperature	24°C	
Humidity	33% r.h.	

For exact pad and aperture dimensions, as well as module geometry and footprint design, please refer to [2].

5.3 Pick and Place

The modules are shipped in tape and reel containers (for packaging information see [2]). These reels fit into standard feeders of pick and place machines for easy integration into assembly environment.

For recognition use pads and fiducial mark.

Placing force should be reduced to minimum (=1N) in order to not squeeze out solder paste. In the Telit Cinterion test a placing force of 3N was used without any complications. Tackiness during testing was still good enough to hold modules in place.

5.3.1 Reflow Profile

Short profiles are recommended for reflow soldering processes in order to prevent top side solder joints from growing large intermetallic compounds. Peak zone temperature should be adjusted high enough to ensure proper wetting and optimized forming of solder joints. On the other hand, a plateau during preheating can help to reduce voiding behavior. Generally speaking, unnecessary long exposure and exposure to more than 245°C should be avoided.

As an example and during Telit Cinterion internal tests, forced convection machines were able to realize a good reflow soldering profile, so there was no need for using vapor phase equipment.

The profile in Figure 12 has been used to assemble daisy chained modules for BLR tests. For analyzing and adapting solder profiles a carrier board was prepared with thermocouples (TC). Figure 10 shows carrier and thermocouple positions in principle, Figure 11 shows the positions for a daisy chain carrier.

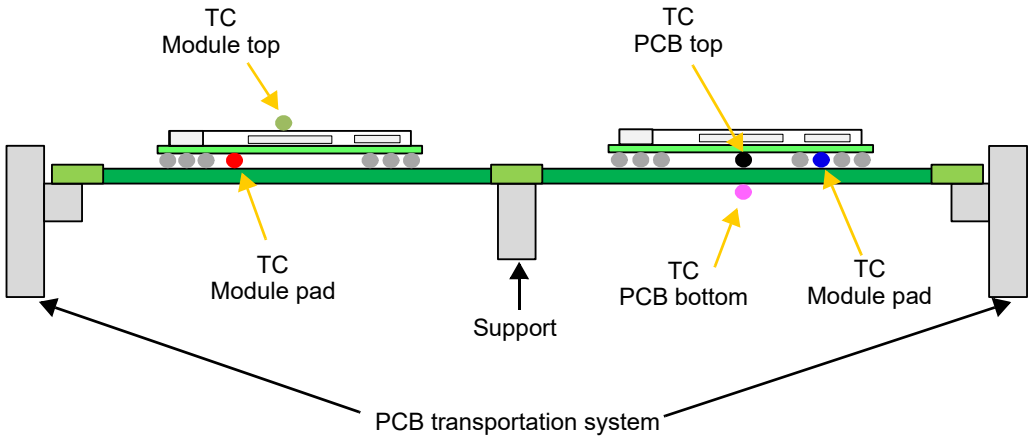

Figure 10: Sensor positions for reflow profile analysis

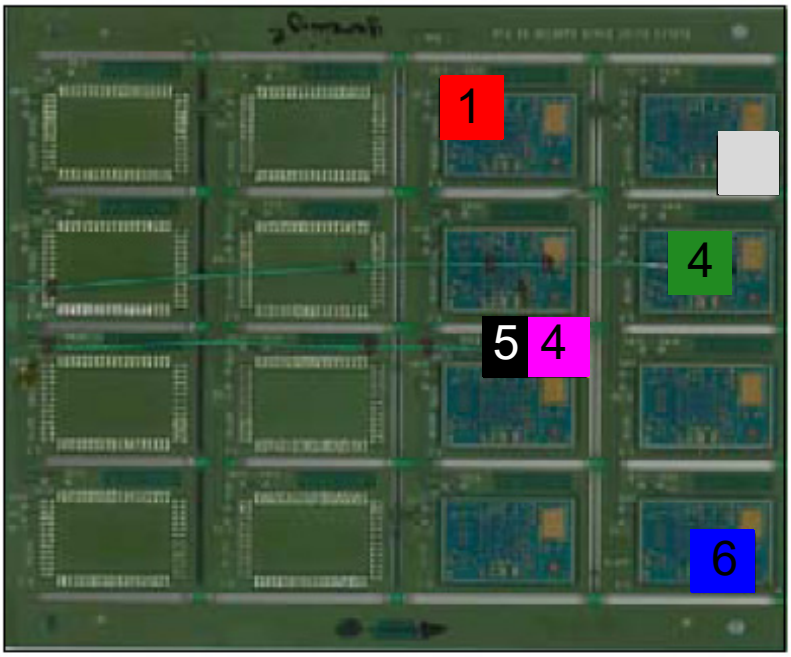

Figure 11: Carrier with sensor positions

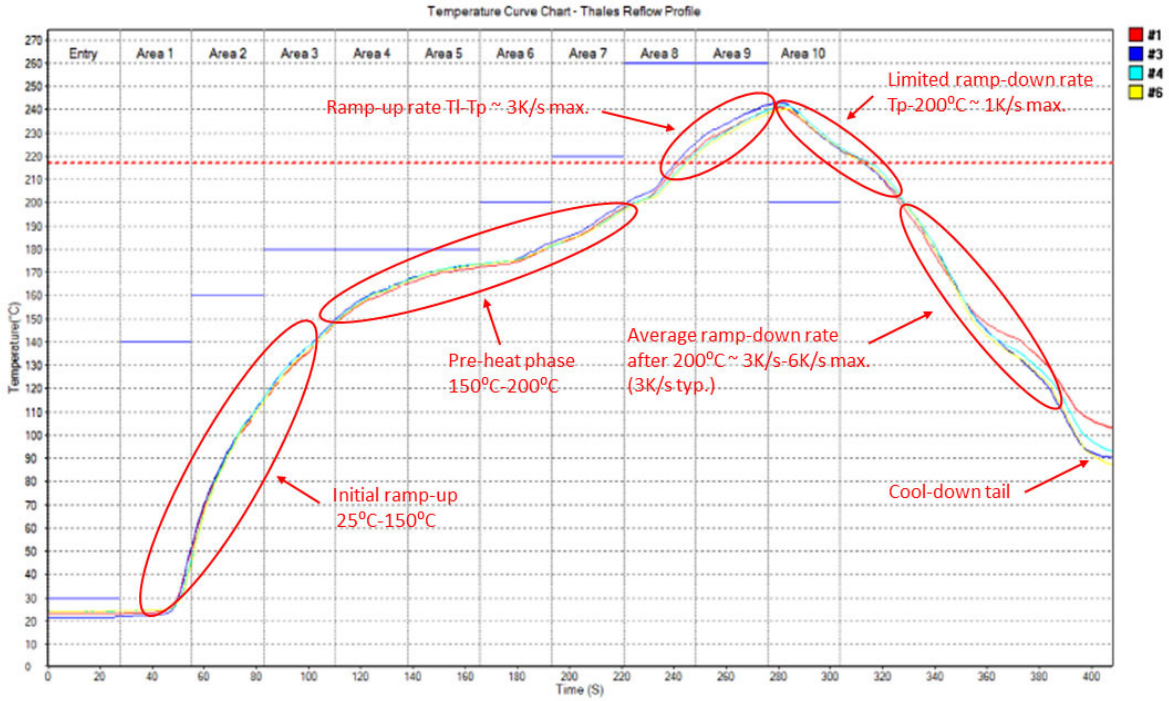

Figure 12: Short reflow profile for SnAgCu alloys

Please note that ramp-down rate from T_{Peak} to 200°C should be controlled in order to reduce thermally induced stress during the solder solidification phase. Therefore, a cool-down step in the oven's temperature program between 200°C and 180°C should be considered - as shown in Figure 12. For product specific recommended reflow ratings please refer to [2].

In order to get a good overall performance the resulting voiding and the formation of inter-metallics as well as other thermal induced degradations must be well balanced. As mentioned above a longer preheating phase can help gasses to escape from solder joints before solidification. To not overstress the assembly, the complete reflow profile should be as short as possible. Here an optimization considering all components on the application must be performed.

The optimization of a reflow profile is a gradual process. It needs to be performed for every paste, equipment and product combination. The presented profiles are only samples and valid for the used pastes, reflow machines and test application boards. Therefore a "ready to use" reflow profile can not be given.

5.4 Soldering Process Evaluation

5.4.1 Visual Inspection

As a rule, automated optical inspection (AOI) of solder joints is not suitable for evaluating LGA modules, because most of the I/O pins are hidden underneath the module. However, with the supported modules all of the interface signal pads are located at the module's edge. This allows for a possible non-automated visual inspection of solder joints.

5.4.2 X-Ray Inspection and Void Content

X-Ray inspection is an appropriate method for evaluating solder joints after reflow. X-Ray images can show wetting problems, missing solder volume or of course bridging.

X-Ray inspection is made somehow more difficult by overlaying module components and by possible bottom side (application) assemblies. However, module connections are characterized by their shape and size, so in most cases they can easily be distinguished from the mentioned overlaying structures.

The following picture shows a typical X-Ray image of a sample module. .

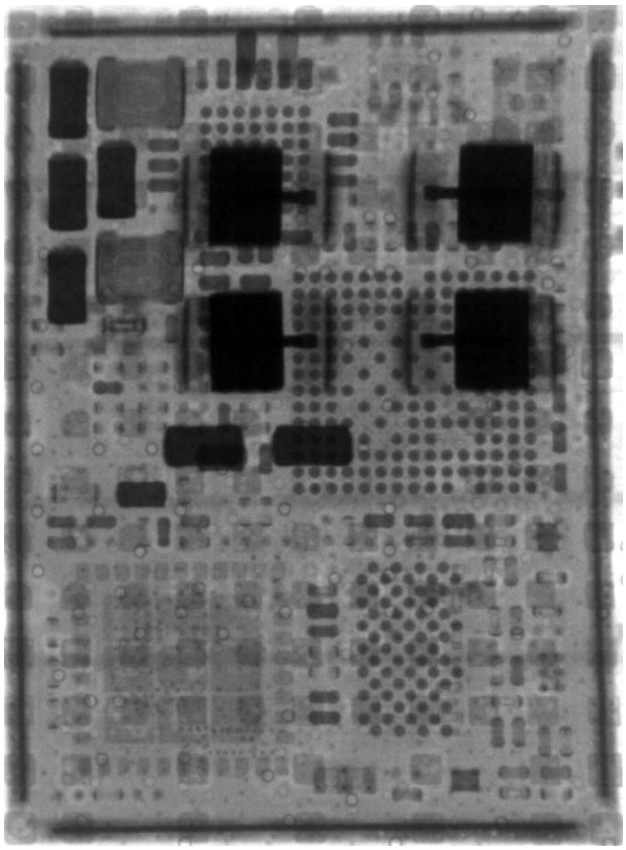

Figure 13: **120µm stencil: Good reflow result in X-Ray Image. Note the normal level of voiding**

It is recommended to use X-Ray to determine level of voiding. Entrapments of gases can often not be completely avoided, if large flat solder joints are used. Currently there are no standards available defining limits for void content. The available IPC610 standard for ball grid arrays (=BGA) must not be applied to LGAs and hence to the supported Telit Cinterion modules.

Only if solder paste spreading is limited, which can occur with lead free solder on Cu-OSP or immersion tin PCB surfaces, a little difference in solder joint shape can be expected but with no effect on quality or yield. This is a characteristic of lead free solders and not a wetting issue.

In Telit Cinterion internal testing no significant difference in overall performance between the discussed stencil thicknesses could be found. Hence it is expected, that thicknesses between the tested values will work too, if the volume is adjusted accordingly.

5.5 Board Level Reliability Investigation

5.5.1 Temperature Cycle Tests

TX62/TX82 modules with implemented daisy chain wiring and soldered with 110µm and 150µm solder paste thickness were tested in accelerated aging tests: Thermal shock (air to air) -40/125°C. Dwell time at extremes was 30 minutes and transition time was 10 seconds. The tests were performed according to DIN EN 60068-2-14Na.

Every 500 cycles all modules were removed from the thermal shock chamber and measured electrically (daisy chain only). An electrical failure is defined as a raise of electrical resistance by 0,5 mOhms above average resistance after soldering.

During the 2000 cycles performed in this test, no module was found to meet the failure criterion. This means, every stencil variant worked well and the connections were very strong and could withstand extensive temperature cycling.

Cross sectioning was not done due to the clear results of the electrical test.

5.5.2 Vibration and Mechanical Shock Tests

Random vibration and mechanical shock tests were completed according to

EC 60068-2-27:2008-02 Basic environmental testing procedures,
Part 2-27: Tests - Test Ea and guidance: Shock

EC 60068-2-64: 2008-04 Environmental testing,
Part 2-64: Tests - Test Fh: Vibration, broadband random and guidance

These additional stress tests were intended to reveal aging in the soldering connections introduced during the temperature stress test described in Section 5.5.1.

No defects were observed in the consequent electrical tests of the soldering connections.

5.5.3 Bending Test

As an example for bending, tests according to IEC60068-2-21 were performed to ensure functionality under bending of the assembly (application + wireless module).

During the test, the functionality of the module itself as well as the functionality of the application test board solder joints (Daisy Chain) was monitored: No interruption of functionality neither of the module function nor the daisy chain was observed. All tested modules passed the bending test.

5.5.4 Shear Test

As an example for shearing, tests according to IEC 60068-2-21 were performed to investigate the functionality under shearing of the LGA module.

Differing from the IEC standard, the shear tool employed for testing allowed applying the force at the whole side of the module, i.e., the shear tool had no sharp tool tip. The force

was applied to the module without damaging the sides.

Forces were applied in ascending order and onto all four sides. Functions of the module and the daisy chain function were observed during the test. All tested modules passed the shear test.

5.6 Desoldering Process

In case of persisting module issues, the module may be desoldered from the application board. Desoldering however should only be the final means of diagnosis after all other possible electrical on-board tests using the implemented test points (see above Section 3.1) were not successful.

The desoldering process is very similar to the employed soldering process, meaning that it is quite specific for any type of external application.

The intention of desoldering is to provide a possibility to employ the standard RMA process. Even if a further usage of the application board cannot be guaranteed (because of the potential impact on neighboring components throughout the desoldering process), a high reuse probability is expected, if the desoldering process is done in a professional manner.

There are a various types of desoldering machines available. The choice of a desoldering machine (e.g., a Martin machine) strongly depends on the layout of the external application board, the size and position of other components close to the module have an impact on the temperature profile and type of heating.

The below figure shows the LGA desoldering process flow:

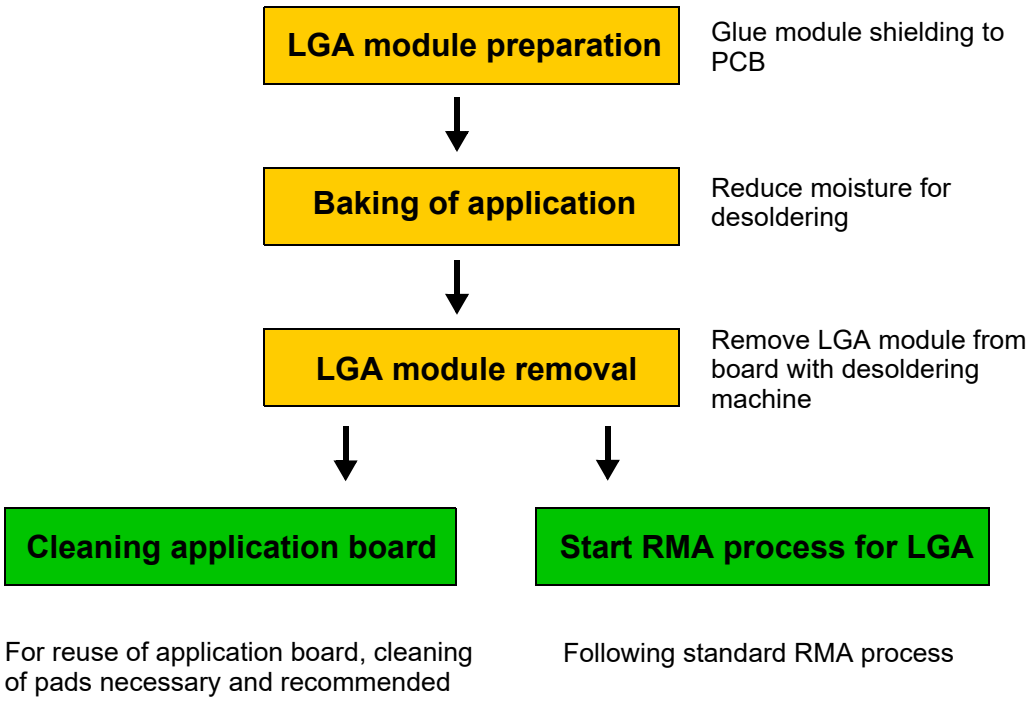

Figure 14: LGA desoldering process flow

5.6.1 Preparation of LGA Module

It is recommended to use a vacuum lift system to pick up the desoldered module from the application board. To secure a fixed connection between module shielding and module PCB, additional glue points have to be provided. A special SMT glue (e.g., PD 955 M from Heraeus) is required to endure the high temperature ranges during desoldering, and care should be taken about the right handling of the selected SMT glue (e.g., temperature and time for hardening as described by the glue manufacturer). Two glue points around the shielding of the LGA module seem to be sufficient - depending on the used vacuum lift system. The module can be desoldered (see Section 5.6.3) after the SMT glue has hardened and the whole application was baked (see Section 5.6.2).

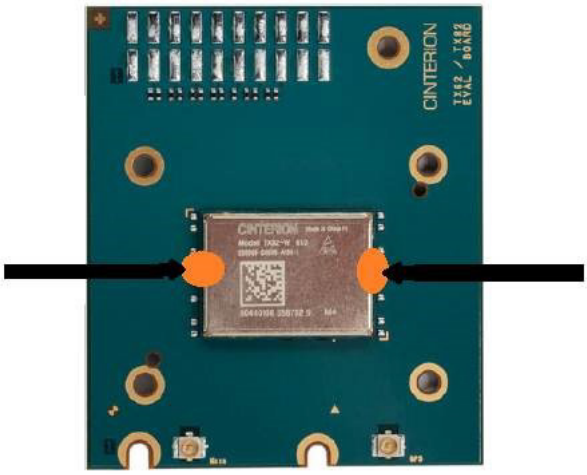

Figure 15: **Position of the two glue points**

5.6.2 Baking of Application Board

For a reliable desoldering process the moisture level has to taken into account. As known from the soldering process, the moisture has to be limited to a certain level to avoid any damages to components. Therefore, the complete application board including the module will have to be baked before the desoldering process begins. It is recommended to bake the complete application at 125°C ± 5°C for 48 hours. For the allowed level of humidity for soldering/desoldering please refer to [2].

5.6.3 Removal of LGA Module

After preparation (glueing, baking) the module can be desoldered from the application board. The desoldering temperature profile has to be selected that fits to the application and module requirements (e.g., used soldering paste, soldered components, PCBs). As recommended for the LGA modules' soldering process, the temperature profile should not exceed a temperature of 245°C (see Chapter 5 or [2]). It has to be ensured that all soldering joints are heated for removal. The temperature difference on the application has to taken into account - otherwise warpage effects would impact the desoldering process. It is recommended to heat the complete board to a minimum of +90°C.

It is recommended to carry out the module removal by means of a vacuum lift system. The used nozzle of the system needs to be adapted to the LGA module's dimensions and weight.

The nozzle has to be positioned around the LGA module. After heating the board and the module soldering joints, the module can be lifted by the vacuum lift system. The components on the application board as well as the module itself will have to be handled very carefully in order to prevent any unintenional movements of components, even under the module shielding. Any jerky movements of application components or the module will have to be avoided.

The LGA module can only be removed if all soldering joints are melted - otherwise damages or even demolition could be the result.

6 Document History

Preceding document: "AN48: SMT Module Integration", Version 01

New document: "AN 48: SMT Module Integration", Version 02

Chapter	What is new?
5.3.1	Figure 12 updated together with description.

New document: "AN 48: SMT Module Integration", Version 01

Chapter	What is new?
--	Initial document setup.