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| Floating Point Multiplier |
| [Type the document subtitle] |
| Floating point multiplier that supports single precision/double precision and custom precision floating point in binary format |

9/23/2012

1. Features

Fully pipelined architecture with adjustable latency

Single precision, double precision and custom non-standard precision

Compliant with IEEE754 binary format with the following exceptions:

* Subnormal numbers are not supported and will be rounded to be zero before calculation is carried out. Subnormal results are rounded to zero.
* Only round-to-neatest even is supported

1. Interface

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| --- | --- | --- | --- |
| Parameter | IO | Required | Description and *Default* value |
| pTechnology |  | Y | Possible values:  ***“ALTERA”*** |
| pFamily |  | Y | Possible values:  ***“CYCLONE V”*** |
| pPrecision |  | Y | Possible Values  0: Custom precision, widths of mantissa and exponent are defined by pWidthMan and pWidthExp  ***1: Single Precision***  2: Double Precision |
| pWidthExp |  | Y | Width of Exponent for custom Precision, do not assign if pPrecision = 1 or 2 |
| pWidthMan |  | Y | Width of Mantissa for custom Precision, do not assign if pPrecision = 1 or 2 |
| pPipeline |  | Y | Latency of the denormalizer multiplier  Default = 5  Minimum Latency = 3 |

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| --- | --- | --- | --- |
| Name | Size | Required | Description |
| iv\_InputA | I[S-1:0] | Y | Input A following IEEE754 binary format of single or double precision  S = pWidthMan+pWidthExp+1 |
| iv\_InputB | I[S-1:0] | Y | Input B following IEEE754 binary format of single or double precision |
| i\_Dv | I | Y | Data valid input |
| o3\_InputID | O[2:0] | N | ID of the input, this is to track input and output values  When i\_Dv is asserted, a non-zero ID is returned in the same cycle at o4\_InputID. When i\_Dv is deasserted, o4\_InputID = 0 |
| o3\_OutputID | O[2:0] | N | ID of the output, non-zero values indicate valid data |
| ov\_Result | O[S-1:0] | Y | Floating point output Result |
| o\_Overflow | O | N | Overflow flag |
| o\_NAN | O | N | Not a number flag |
| o\_Underflow | O | N | Underflow flag |
| o\_PINF | O | N | Positive infinity |
| o\_NINF | O | N | Negative Infinity |
|  |  |  |  |
| i\_Clk | I | Y | Clock input |
| i\_ClkEn | I | Y | Clock enable input, deassert this input to disable the whole engine |
| i\_Arst | I | Y | Async active high reset |

1. Performance

Table 1 Area and Performance for Altera Devices

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Device | Setting | Post-fit LEs/LUT  LAB/ALUT | Register | DSP block | Post Fit Max Frequency (Restricted) in MHz |
| Cyclone III | Single Precision  Latency =5  SpeedGradeC8 | 281/246 | 149 | 7 x 9-bit | 208 (200) |
| Cyclone IV GX | Single Precision  Latency = 5  SpeedGradeC8 | 280/246 | 149 | 7 x 9-bit | 211 (200) |
| Cyclone V GX | Single Precision  Latency = 5  SpeedGradeC8 | 153 | 154 | 1 x 27-bit | 207 |
| Arria II GX | Single Precision  Latency = 3  SpeedGradeC6 | 170 | 85 | 4 x 18-bit | 157 |
|  | Single Precision  Latency = 5  SpeedGradeC8 | 157 | 119 | 4 x 18-bit | 257 (220) |
|  |  |  |  |  |  |
| Cyclone III | Double Precision  Latency =5  SpeedGradeC8 | 851/582 | 612 | 28 x 9-bit | 123 |
| Cyclone IV | Double Precision  Latency = 5  SpeedGradeC8 | 381 | 368 | 28 x 9-bit | 123 |
| Cyclone V | Double Precision  Latency=5  SpeedGrade C8 | 435 | 478 | 4 x 27 bit | 186 |
| Arria V | Double Precision  Latency=5  SpeedGrade C4 | 435 | 506 | 4 x 27 bit | 2751 |
| Note | Quartus II 12.0sp2 Webpack Build 263 8/2/2012   1. Quartus II 12.0sp2 SE Build 263 8/2/2012 | | | | |

1. Revision History

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| Date | Author | Core’s Revision | Description |
| 21/09/2012 | Jeff Lieu | 1.0 | Initial Release  Clock Enable has not been tested |