FPGA System Design (ET5009701)

Fall 2022 **Instructor: M. B. Lin, Ph.D.**

Course Objective: System-on-a-chip (SoC) has become an essential technique to lower product costs and maximize power efficiency, particularly as the mobility and size requirements of electronics continue to grow. It has become increasingly important for electrical engineers to develop a strong understanding of the key stages of hardware description language (HDL) design flow based on cell-based libraries or field-programmable gate array (FPGA) devices. As a consequence, this course focuses on developing, verifying, and synthesizing designs of practical digital systems through the most widely used hardware description Language: Verilog HDL.

Prerequisite: You must have read thoroughly at least one of the following textbooks or one equivalent.

1. Ming-Bo Lin, *Digital Logic Design*, 6th ed., Taipei, Taiwan: Chuan Hwa Book Ltd., 2017. (Chinese edition, ISBN: 9789864635948)
2. M. Morris Mano and Michael D. Ciletti, *Digital Design: With An Introduction to the Verilog HDL*, 5th Ed., Upper Saddle River, NJ: Prentice-Hall, 2013. (Traditional Chinese or English edition) (ISBN: 9780132774208)
3. Jr. Charles H. Roth and Larry L. Kinney, *Fundamentals of Logic Design*, 7th Ed., Cengage Learning, 2013. (Only English edition) (ISBN: 9781133628477)

Textbook: You must at least need to read one of the following books.

1. Ming-Bo Lin, *Digital System Designs and Practices: Using Verilog HDL and FPGAs,* John Wiley & Sons, Inc., 2008. (ISBN-13: 978-0470823231)
2. Ming-Bo Lin, *FPGA Class Notes,* 2021.

References:

1. IEEE 1364-2001 Standard, *IEEE Standard Verilog Hardware Description Language*, 2001.
2. IEEE 1364-2005 Standard, *IEEE Standard for Verilog Hardware Description Language*, 2006.

Course Outline:

1. **An Introduction to Verilog HDL:** Introduce the basics of Verilog HDL and how it can be applied to design, simulate, and realize digital systems, including design flow, introduction to Verilog HDL, modeling and synthesis, module modeling styles, modules, and simulation tutorial.
2. **Structural modeling:** Describe the basic features and applications of structural modeling, including structural modeling and switch-level modeling.
3. **Dataflow modeling:** Describe the dataflow modeling related expression, operator, and other topics.

4. **Behavioral modeling:** Describe the behavioral modeling related statements, assignments, timing control, selection constructs, loop constructs, generate blocks, and other topics.

5. **Tasks, functions, and UDPs:** Introduce tasks and functions used in Verilog HDL. The difference between tasks and functions are summarized as a table. Reentrant task and Recursive functions are also explained. Finally, both combinational and sequential user defined primitives are introduced.

6. **Modeling techniques:** Describe some techniques and Verilog HDL supported constructs commonly used in modeling a system. In this unit, we include procedure continuous assignments, overriding parameters, initializing memory from file, modeling PLA, types of delays, and timing checks.

7. **Combinational logic modules:** Give some basic and commonly used combinational modules. Extensive Verilog HDL examples are given in this lecture.

8. **Sequential logic modules:** Give some basic and commonly used sequential modules. Extensive Verilog HDL examples are given in this lecture.

9. **Subsystems design:** Introduce digital systems design techniques, design hierarchy, system-level design approaches, finite-state machine (fsm), ASM (algorithmic-state machine) chart, datapath and controller design, and RTL realization options.

10. **Synthesis:** Introduce ASCI/VLSI design flow, logic synthesis (logic optimization), and language structural synthesis.

11. **Verification:** Introduce verification methodology, testbench design, simulation, code coverage analysis, and static timing analysis.

Homework: One term project (two parts).

Grading method: Homework: 50 pts; midterm exam: 30 pts; final exam: 30 pts; class participation and extra homework: bonus.

$$\begin{aligned} Raw\_score &= homework + (midterm\ exam + final\ exam) \times 0.30 \\ Bonus &= 78 - Averaage\ of\ raw\_scores \text{ (excluding midexam + final } < 50.) \\ Final\_score &= raw\_score + Bonus \text{ (may be zero)} \end{aligned}$$

Nothing great was ever achieved without enthusiasm. *R. W. Emerson.*

The reward of a thing well done is to have done it. *R. W. Emerson.*

The only limit to our realization of tomorrow will be our doubts of today.

Franklin D. Roosevelt.
