Amorphous silicon thin-film transistors and arrays fabricated by jet printing

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Phase-change wax-based printed masks, in place of conventional photolithography, were used to fabricate hydrogenated amorphous silicon thin-film transistors (TFTs). Wax-mask features with a minimum feature size of ~20 μm were achieved using an acoustic-ink-printing process. Both discrete and matrix addressing structured bottom-gate TFTs with source–drain contacts overlapping the channel were created using a four-mask process. The TFTs had current–voltage characteristics comparable to photolithographically patterned devices, with mobility of 0.6–0.9 $cm^2/V\,s$, threshold voltage of 2–3 V, and on/off ratios exceeding 10^7 for devices with channel lengths below 50 μm.
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The fabrication of large-area thin-film transistor (TFT) arrays is relatively expensive due in large part to the cost and complexity of photolithographically-based processing techniques. These steps require large-area coverage of spin-on photoresist,[1] pattern definition, resist pattern development, and definition of the underlying material by wet or dry chemical etching. In applications such as flat panel displays or imagers, simplifying and reducing these processes will result in reducing the fabrication cost for large-area arrays. One approach to simplification is by using direct-writing methods to define device or interconnect features on a substrate, replacing the more costly and complicated conventional photolithographic process.

Direct-write techniques have been demonstrated for fabricating organic/polymeric transistor and optoelectronic devices.[2–5] Recently, the use of laser printed toner etch masks has also been demonstrated in fabricating hydrogenated amorphous silicon (*a*-Si:H) TFTs having a minimum feature size of several hundred microns.[6–8] Although the process simplifies TFT fabrication, the laser printed feature size does not allow for reasonable resolution in a display or imager array. The use of ink-jetted liquids to directly write etch masks is a practical alternative to printed toner although jet printing also possesses inherent complexities. For example, when liquid drops are put onto a surface, the droplet configuration is largely determined by its wetting properties. Typically, small wetting angles are required to obtain good adhesion to a surface but this condition allows the liquid to spread and form relatively large features. On the other hand, if the liquid does not wet the surface due to its high surface energy, a large contact angle will form resulting in small drop features but having poor adhesion to the printed surface. Neither situation is desirable in semiconductor processing—the former increases the feature size and the latter gives unreliable patterning.

The use of a phase-change media circumvents many of these problems. A material slightly above its liquid/solid phase transition temperature may be ejected from a jet-printing nozzle; the droplet solidifies quickly upon contact onto a cooler surface. The feature size will then depend more on the cooling rate and less on the materials wetting properties since a frozen droplet can not spread. In this situation, the substrate temperature controls the printed feature size for materials having excellent wetting properties.

Although drop-on-demand jet printing of low-temperature solders ($T_m < 300\,^\circ$C) have been reported,[9] direct writing of many metals is unrealistic due to their higher melting temperatures. For example, refractory metals such as Cr are commonly used as gate metals in TFT fabrication but the ejection of liquid Cr from a printhead would be impractical in conventional jet-printing processes. A more functional approach is to deposit the thin-film material by conventional techniques and subsequently use an etch-mask process to define the device structures. This letter describes a method for fabricating *a*-Si:H TFTs using jet-printed phase-change materials, in place of conventional photolithography, to define the mask features. The printed mask process described is capable of 20 μm feature sizes, which can enable the fabrication of arrays with 200 μm pixels.

Jet printing of the phase-change wax droplets, formed using an acoustic wave, was accomplished with a nozzleless printhead.[10] Droplet ejection is accomplished using bursts of focused acoustic energy to form a pressure wave to overcome the restraining force of the liquid surface tension. The resulting expelled droplet from the liquid surface can travel at a velocity of several meters per second with a droplet volume of 2–3 picoliters. By generating droplets in this fashion, an acoustic ink-jet printing (AIP) process capable of ~20 μm minimum feature size was developed to generate the printed etch-mask patterns.

In addition to the small drop volumes afforded by the AIP process, printing of phase-change waxes permits additional feature size and print quality management via the substrate temperature. Figure 1 shows the variation of printed line features as a function of the glass substrate temperature. At 30 °C, the rapid cooling of the phase-change material as it comes in contact with the glass is evident from the optical micrograph image showing jagged edges outlining the individual droplets [Fig. 1(a)]. By raising the substrate tempera-

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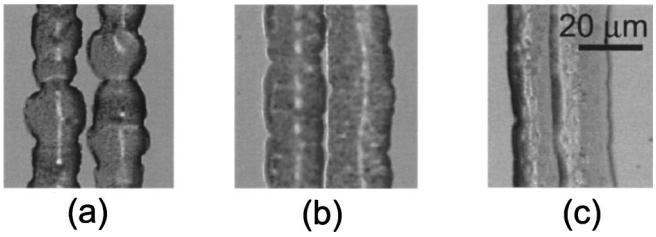

FIG. 1. Variation in print quality of AIP ejected phase-change wax as a function of substrate temperature. (a) $T_s = 30\,^{\circ}\mathrm{C}$, (b) $T_s = 40\,^{\circ}\mathrm{C}$, and (c) $T_s = 50\,^{\circ}\mathrm{C}$.

ture 10 °C [Fig. 1(b)], the wax cools more slowly allowing improved coalescence between subsequent droplets while minimizing the spreading of the line features. At 50 °C [Fig. 1(c)], the droplet spreading is more pronounced and print resolution is reduced due to a lower quench rate that results in significant feature spreading and contact between the two adjacent lines.

Insulated-gate thin-film transistors were fabricated on 4 in. glass substrates using a three-layer wax-mask process. Mask layers were used to define the gate metal, active device island, and source–drain metal contacts. A bottom-gate Cr electrode configuration was employed. First, a 100 nm thick Cr film was deposited onto glass that was then patterned using the Kemamide-based wax ejected from an AIP printhead. Next, a 300 nm thick Si_3N_4 layer followed by a 50 nm *a*-Si layer and a 200 nm Si_3N_4 layer were deposited over the Cr gate creating the $Si_3N_4/a{:}Si/Si_3N_4$ (NSN) device stack. Fixing the substrate position and offsetting the mask image-file, which enabled layer-to-layer registration to within 10 μm, accomplished the mask alignment.

In patterning the active-device island features, the relatively high vapor pressure of the wax material presented a potential incompatibility within vacuum systems used for dry chemical etching of the top dielectric and the *a*-Si layer. To circumvent the problem, a sacrificial mask layer compatible with the dry-etch process and patterned by the printed wax masks was applied. In this step, an Al sacrificial mask layer was first deposited onto the NSN stack and defined by the printed wax. Following the removal of the wax mask with tetrahydrafuran, the active-device island feature was then formed by etching the NSN stack in a CF_4/O_2 plasma using the patterned Al as an etch mask. The Al mask layer was then stripped to finish the island definition step.

Following the island definition, the top nitride layer was defined using a self-aligned process in which spin-on photoresist was applied onto the glass/Cr/gate/NSN-island structures. In this step, the mask aligner is bypassed by using back side blanket ultraviolet exposure through the transparent glass substrate to define the top nitride feature, self-aligned to the Cr gate. The top nitride was then etched away and a 100 nm thick n^+ Si layer was deposited followed by the Al source–drain contact metal deposition to complete the device stack. The source–drain metal was defined by printed mask patterning and the device was completed by removing the exposed n^+ Si layer by plasma etching using the source–drain contacts as etch masks. The process flow is shown in Fig. 2.

By using the process flow described in Fig. 2, TFT devices were fabricated and tested in comparison to transistors

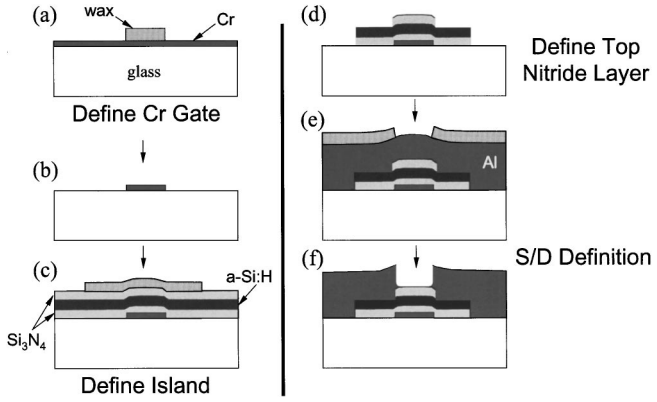

FIG. 2. Process flow for fabricating the bottom-gate TFT structures: (a) pattern Cr film with wax masks, (b) etch Cr film and remove wax to define bottom-gate electrodes, (c) deposit NSN layer and pattern island feature with wax mask, (d) etch island feature and define top nitride layer, (e) deposit Al source/drain metal and pattern with wax mask, and (f) etch Al film and remove mask to define source/drain contacts.

made by conventional semiconductor device processing. These transistors had gate widths and lengths ranging from 40–370 μm. The output characteristics of a TFT device with dimensions $W/L = 370\ \mu\mathrm{m}/140\ \mu\mathrm{m}$ (40 μm overlap gap) fabricated by printed wax masks are shown in Fig. 3(a). The threshold voltage for these devices were measured to be ~2–3 V with the gate voltage varied from 0 V to the maximum drain voltage, $V_D = 15$ V. Figure 3(b) shows the transfer characteristics for devices with a $W/L = 130\ \mu\mathrm{m}/40\ \mu\mathrm{m}$ (10 μm overlap gap) having a measured mobility between 0.6 to 0.9 $\mathrm{cm}^2/\mathrm{V\,s}$ and an on/off ratio of 10^7. Except for the slightly high gate leakage current, the resulting device per-

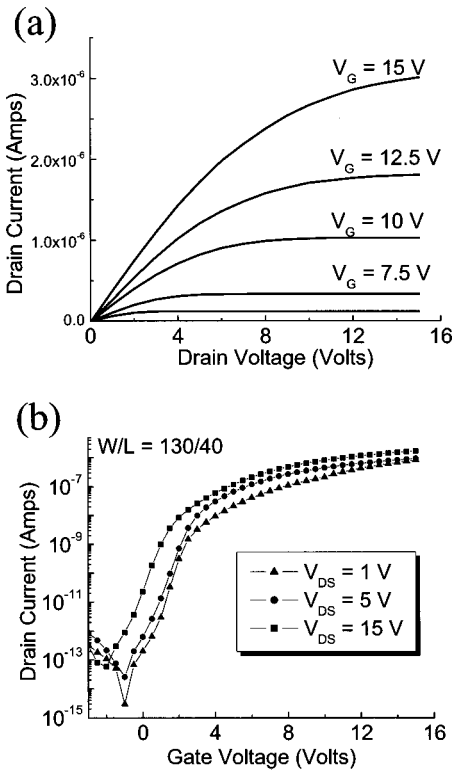

FIG. 3. (a) Output characteristics for a TFT device with dimension $W/L = 370\ \mu\mathrm{m}/140\ \mu\mathrm{m}$. (b) Transfer characteristics for a transistor with a $W/L = 130\ \mu\mathrm{m}/40\ \mu\mathrm{m}$, on/off ratio of 10^7, and mobility ranging from 0.6–0.9 $\mathrm{cm}^2/\mathrm{V\,s}$.

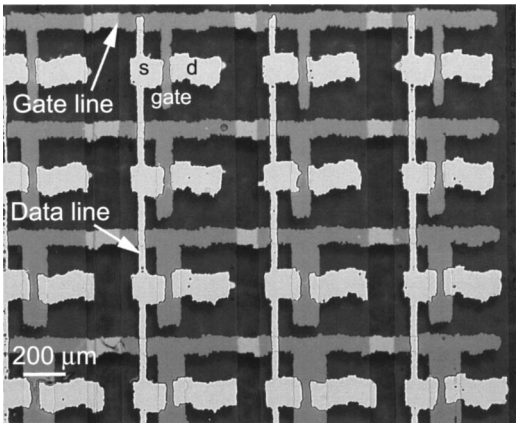

FIG. 4. Optical micrograph of a matrix addressing array structure. The gate line, data line, source/drain (labeled s and d, respectively), and gate features are labeled.

formance was comparable to *a*-Si:H TFT devices fabricated using conventional photolithographic techniques. It is probable that the higher gate leakage is due to poor isolation of the device island structure during the device fabrication. A possible remedy for reducing the leakage is by isolating the island structure better with the top nitride using a via contact to the bottom-gate electrode.

As a demonstration for fabricating arrays, interconnected TFTs were made using the wax-mask patterning technique. The 8×5 arrays were fabricated using the same process described in making the discrete devices with common gate and drain electrode configurations having a 170 μm gate width and gate lengths varying between 60 to 500 μm. Figure 4 shows an optical micrograph of an array of transistors processed using the printed wax masks with a pixel size of $\sim$350 μm. The transfer characteristics for a typical transistor with a $W/L=170$ μm/70 μm (10 μm overlap gap) had mobility of $\sim$0.8 $cm^2/V\,s$, threshold voltage of $\sim$3–4 V, and on/off ratio of 10^7, similar to the performance of the discrete TFT devices. The functioning array demonstrates the feasibility of printed mask patterning as a viable alternative to conventional photolithography processes. The feature size obtained by acoustic ink-jet printing and the compatibility of the wax material to conventional semiconductor processing offer substantial advantages in process simplification and cost reduction in the fabrication of large-area TFT arrays.

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