Appendix C - CHIP-8 Interpreter

CHIP-8 Interpreter Listing

To use the CHIP-8 language you must first load the following interpreter program into memory locations 0000-01FF (2 pages). This interpreter will allow you to run the games in Appendix D or write your own programs using the CHIP-8 instruction set described in section III.

```
0000  91 BB FF 01 B2 B6 F8 CF
0008  A2 F8 81 B1 F8 46 A1 90
0010  B4 F8 1B A4 F8 01 B5 F8
0018  FC A5 D4 96 B7 E2 94 BC
0020  45 AF F6 F6 F6 F6 32 44
0028  F9 50 AC 8F FA 0F F9 F0
0030  A6 05 F6 F6 F6 F6 F9 F0
0038  A7 4C B3 8C FC 0F AC 0C
0040  A3 D3 30 1B 8F FA 0F B3
0048  45 30 40 22 69 12 D4 00
0050  00 01 01 01 01 01 01 01
0058  01 01 01 01 01 00 01 01
0060  00 7C 75 83 8B 95 B4 B7
0068  BC 91 EB A4 D9 70 99 05
0070  06 FA 07 BE 06 FA 3F F6
0078  F6 F6 22 52 07 FA 1F FE
0080  FE FE F1 AC 9B BC 45 FA
0088  0F AD A7 F8 D0 A6 93 AF
0090  87 32 F3 27 4A BD 9E AE
0098  8E 32 A4 9D F6 BD 8F 76
00A0  AF 2E 30 98 9D 56 16 8F
00A8  56 16 30 8E 00 EC F8 D0
00B0  A6 93 A7 8D 32 D9 06 F2
00B8  2D 32 BE F8 01 A7 46 F3
00C0  5C 02 FB 07 32 D2 1C 06
00C8  F2 32 CE F8 01 A7 06 F3
00D0  5C 2C 16 8C FC 08 AC 3B
00D8  B3 F8 FF A6 87 56 12 D4
00E0  9B BF F8 FF AF 93 5F 8F
00E8  32 DF 2F 30 E5 00 42 B5
00F0  42 A5 D4 8D A7 87 32 AC
00F8  2A 27 30 F5 00 00 00 00
```

```
0100  00 00 00 00 00 45 A3 98
0108  56 D4 F8 81 BC F8 95 AC
0110  22 DC 12 56 D4 06 B8 D4
0118  06 A8 D4 64 0A 01 E6 8A
0120  F4 AA 3B 28 9A FC 01 BA
0128  D4 F8 81 BA 06 FA 0F AA
0130  0A AA D4 E6 06 BF 93 BE
0138  F8 1B AE 2A 1A F8 00 5A
0140  0E F5 3B 4B 56 0A FC 01
0148  5A 30 40 4E F6 3B 3C 9F
0150  56 2A 2A D4 00 22 86 52
0158  F8 F0 A7 07 5A 87 F3 17
0160  1A 3A 5B 12 D4 22 86 52
0168  F8 F0 A7 0A 57 87 F3 17
0170  1A 3A 6B 12 D4 15 85 22
0178  73 95 52 25 45 A5 86 FA
0180  0F B5 D4 45 E6 F3 3A 82
0188  15 15 D4 45 E6 F3 3A 88
0190  D4 45 07 30 8C 45 07 30
0198  84 E6 62 26 45 A3 36 88
01A0  D4 3E 88 D4 F8 F0 A7 E7
01A8  45 F4 A5 86 FA 0F 3B B2
01B0  FC 01 B5 D4 45 56 D4 45
01B8  E6 F4 56 D4 45 FA 0F 3A
01C0  C4 07 56 D4 AF 22 F8 D3
01C8  73 8F F9 F0 52 E6 07 D2
01D0  56 F8 FF A6 F8 00 7E 56
01D8  D4 19 89 AE 93 BE 99 EE
01E0  F4 56 76 E6 F4 B9 56 45
01E8  F2 56 D4 45 AA 86 FA 0F
01F0  BA D4 00 00 00 00 00 00
01F8  00 00 00 00 00 E0 00 4B
```

CHIP-8 Memory Map

Location	Use
0000 • • • 01FF	CHIP-8 LANGUAGE INTERPRETER
0200 • • •	User programs using CHIP-8 instruction set (1184 bytes available in 2048-byte system)
0YA0 • • • 0YCF	CHIP-8 stack (48 bytes max. for up to 12 levels of subroutine nesting)
0YD0 • • • 0YEF	Reserved for CHIP-8 INTERPRETER work area
0YF0	V0
0YF1	V1
0YF2	V2
0YF3	V3
0YF4	V4
0YF5	V5
0YF6	V6
0YF7	V7
0YF8	V8
0YF9	V9
0YFA	VA
0YFB	VB
0YFC	VC
0YFD	VD
0YFE	VE
0YFF	VF
0X00 • • • 0XFF	256-byte RAM area for display refresh

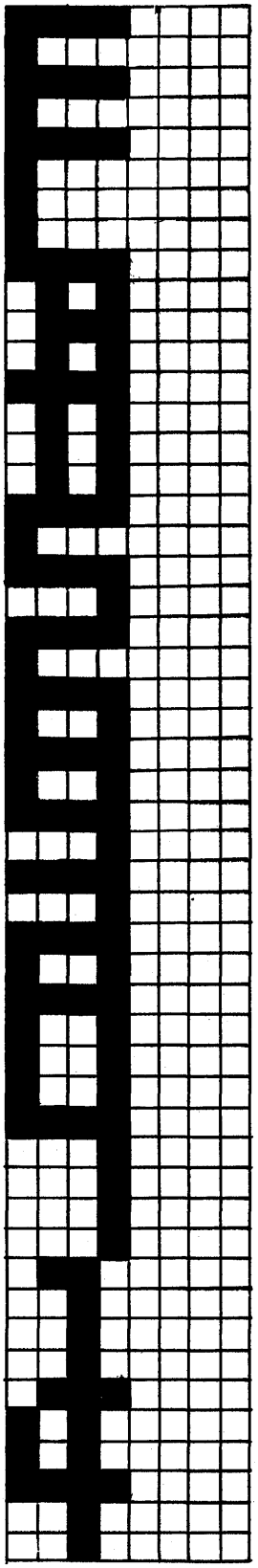
0X = Highest on-card RAM page (07 for 2048-byte system)
0Y = 0X – 1 (06 for 2048-byte system)

CDP1802 Register Use for CHIP-8 Interpreter

R0 = DMA pointer (page 0X for display refresh)
R1 = INTERRUPT routine program counter
R2 = Stack pointer
R3 = INTERPRETER subroutine program counter
R4 = CALL subroutine program counter
R5 = CHIP-8 instruction program counter
R6 = VX pointer (R6.1 must not be changed)
R7 = VY pointer (available for machine-language subroutines)
R8 = Timers (R8.1 = timer, R8.0 = tone duration)
R9 = Random number (+1 in INTERRUPT routine)
RA = I pointer
RB = Display page pointer (RB.1 = 0X)
RC = Available
RD = Available
RE = Available
RF = Available

CHIP-8/Operating System Standard Digit Display Format

HEX DIGIT	ROM ADDRESS	BYTE	BITS 7 6 5 4 3 2 1 0
E-	8110	F0	
	11	80	
F-	8112	F0	
	13	80	
C-	8114	F0	
	15	80	
	16	80	
	17	80	
B-	8118	F0	
	19	50	
	1A	70	
	1B	50	
D-	811C	F0	
	1D	50	
	1E	50	
	1F	50	
5-	8120	F0	
	21	80	
2-	8122	F0	
	23	10	
6-	8124	F0	
	25	80	
8-	8126	F0	
	27	90	
9-	8128	F0	
	29	90	
3-	812A	F0	
	2B	10	
	2C	F0	
	2D	10	
A-	812E	F0	
	2F	90	
0-	8130	F0	
	31	90	
	32	90	
	33	90	
7-	8134	F0	
	35	10	
	36	10	
	37	10	
	38	10	
1-	8139	60	
	3A	20	
	3B	20	
	3C	20	
	3D	70	
4-	813E	A0	
	3F	A0	
	40	F0	
	41	20	
	42	20	



CHIP-8 User Notes

1. Do not use any of the CDP1802 three-cycle machine language instructions in CHIP-8 programs.

2. CDP1802 R5 is used as the CHIP-8 instruction counter. It will be addressing the byte following a 0MMM instruction for machine language subroutines and can be used to pass 2-byte parameters. Refer to the operating system register table in Appendix B to examine this register during CHIP-8 program debugging.

3. Display page 0X is erased to all 0's before beginning CHIP-8 programs at 0200. To inhibit erasing page 0X, change 00E0 at location 01FC to 11FE.

4. To change the display page from 0X, use a machine language subroutine to set RB.1 equal to the new display page.

5. R7, RC, RD, RE, and RF can be used as working registers in machine language subroutines. Changing other registers can cause the CHIP-8 interpreter to malfunction.

6. Do not turn off the CDP1861 video display chip in machine language subroutines. This will interfere with proper operation of the CHIP-8 interpreter.

7. Program bugs can destroy the CHIP-8 interpreter at locations 0000-01FF. If you suspect that this has happened, reload the interpreter.

8. The CHIP-8 interpreter uses subroutines and digit patterns contained in the operating system ROM. If you modify this operating system, the CHIP-8 interpreter should not be used.