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80386 TARGET SPECIFICATION

REVISION 1.4

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1. INTRODUCTION

1.1 PRODUCT DESCRIPTION

The 80386 is a 32-bit, high-performance member of the 8086 family of processors. It is object code compatible with previous processors in the family, including the 8086, 186, and 286. The most significant architectural extension is the definition of 32-bit machine state and instructions in a fashion that is upwards compatible with the 16-bit processors. Paging support is included on-chip to significantly enhance the memory management hardware.

The 80386 system architecture is centered around a new bus. This bus is a demultiplexed, synchronous, 32-bit bus. To support this new bus, a clock chip will be developed which will provide the necessary clocks for the 80386, the 80287 and other 286 bus components. If desired, it is possible to design an external interface that converts the 80386 bus to an 80286-like bus.

The 80386 is a highly complex part, containing over 275,000 devices. In order to make testing such a complex part manageable, special testability facilities have been incorporated. These include an internally driven self-test, and "back-door" access to the on-chip caches.

As with the other 86 Family members, floating point operations are supported by an optional numerics coprocessor. A new coprocessor, the 80387, is defined for use with the 80386. The 80386 supports using either the 80287 or the 80387 as a numeric coprocessor. The protocols used between the 80386 and the 80287 or the 80387 are similar except that the PEACK# signal is not used. Instead, the 80386 does the appropriate checks for PEREQ. In addition data transfers are stretched to 32 bits, and certain refinements were made to the 80386-80387 protocol to improve system performance.

1.2 PURPOSE OF THIS DOCUMENT

This document describes the system architecture and physical environment of the 80386 processor. The software architecture of the 80386 is described in the 386 Architecture Specification. The Architecture Specification is intended to describe the software architecture that is independent of a particular implementation. In the Architecture Specification, several details are noted as implementation defined.

The Target Specification complements the Architecture Specification by defining the "implementation defined" aspects of the architecture, along with a description of the physical implementation and system architecture of the 80386.

1.3 PROCESSOR INITIALIZATION

The processor is initialized whenever the RESET pin is activated for at least 16 CLK2 periods. On the falling edge of RESET the BUSY# pin is sampled to determine whether self-test is to be activated. At some time > 10 clocks after RESET goes inactive and the time the 386 runs its first bus cycle, the ERROR# pin is sampled to set the type of numerics coprocessor present in the system, if any. The coprocessor need not strobe the line, it need only assert the pin to an appropriate state. It is the programmer's responsibility to issue a command to reset the ERROR# pin when an 80387 is used. These topics are discussed in detail in sections 6 and , respectively.

At the end of self-test (or immediately after reset, if self-test was not selected), the on-chip CS descriptor contents and the EIP register values are such that the program starting at linear address OFFFFF0 (hex) begins to execute. Since paging is also disabled, the physical address (i.e. the address seen at the pins) matches the linear address. Details of initial CS:IP and other architecturally visible states are in the 80386 Architecture Specification.

2. PINS

The 80386 uses a 132 pin package with pins grouped by functions: processor execution control (6 pins), bus interface (74 pins), processor extension interface (3 pins), power/ground signals (approximately 41 pins). Initially, a 132-pin ceramic pin grid array (PGA) package is used. A # symbol placed after a pin name means that pin is active low. The pinout for the 386 is given in Figure 1.

2.1 PROCESSOR EXECUTION CONTROL PINS

Six inputs control execution of the 80386. The CLK2 input determines the execution rate and timing of the 80386. Pin timing is specified relative to the rising edge of this signal. For the standard 80386 this signal is 32 MHz. The internal operating frequency of the 80386 is one half the frequency of the CLK2 input. A system using any 80286 compatible parts will require a clock signal which is of the same frequency and phase as the internal 80386 clock. This signal is known as the CLK signal in 80286 systems and, therefore, internal 80386 clock periods can be called CLK clock periods, although the 80386 does not use a CLK pin.

The RESET input forces the 80386 to begin execution at a known state. Several operating modes of the 80386 are also programmed by the falling (inactive going) edge of RESET. If the BUSY# input is sampled active (LOW) an internal self test is performed. At some time > 10 clocks after RESET is driven inactive and the time the 386 performs its first bus cycle, the ERROR# pin is sampled to determine whether the coprocessor present is an 80287 (ERROR# sampled inactive or HIGH) or an 80387 (ERROR# is sampled active or LOW).

The HOLD and HLDA signals force the 80386 to release control of the local bus. Instruction execution will stop if any required instruction or data value can not be read from memory while the local bus of the 80386 is not usable. The 386 will continue execution after a single write even if it doesn't have access to the bus (this bus cycle will be queued within the 386 pending access to the bus).

The INTR and NMI interrupt inputs allow interruption of the current instruction stream. The 80386 will then start execution at another location as a function of which interrupt input was used or the id of the interrupt which is supplied later. One interrupt input is maskable (INTR) while the other is not (NMI).

80386 Processor Execution Controls

Type	Pin Name	Number
Clock	CLK2	1
Initialization	RESET	1
Processor Execution	HOLD, HLDA	2
Interrupts	INTR, NMI	2

2.2 BUS INTERFACE PINS

The bus interface pins control bus cycles performed with memories or peripherals. The bus interface has 32 bidirectional data pins to transfer data in 8, 16, 24, or 32-bit quantities. A 30-bit address bus identifies addresses to a 4-byte location. Separate byte enable pins for each byte identify addresses within a 4-byte location. A full 32-bit address bus can be obtained by generating A1 and A0 from the byte enable pins with four external TTL gates.

Four definition pins provide the definition of bus cycle type. These pins differentiate between writes and reads, memory and I/O, data and control, and locked versus non-locked bus cycles.

Special user control over bus cycles is provided with next address and ready control pins. The NA# pin allows the user to specify that address pipelining can be used. After NA# is sampled active, the 386 is free to drive the addresses for the next bus cycle if it has another bus cycle pending. The traditional READY# pin is provided for bus cycle termination. New addresses may be driven onto the bus for the next bus cycle after READY# is returned regardless of the state of NA#. The 386 will not begin a bus cycle unless it has an explicit internal request pending. This means that even if pipelining is enabled, the part will revert to running a non-pipelined cycle when leaving bus idle. The address driven when the bus is idle is arbitrary.

An address status output informs the external world that a new address is available on the address bus. External hardware must gate this signal with the ready signal in order to determine the beginning of a bus cycle at the earliest possible time. This external gating of ready with address status allows bus cycles with improved ratios of memory speed

to bus cycle time.

A bus sizing pin allows a 16-bit bus to be supported with only 4 external gates.

80386 Bus Interface Pins

Type	Pin Name	Number
Address bus	A31 - A2	30
Data bus	D31 - D0	32
Byte enables	BE3# - BE0#	4
Bus cycle definition	LOCK#, M/I/O#, D/C#, W/R#	4
Bus cycle control	NA#, READY#, ADS#, BS16#	4

2.3 PROCESSOR EXTENSION PINS

The 80386 allows external processors to extend the programmable architecture in a manner transparent to the programmer. These external processors are called processor extensions and are controlled by a set of special pins on the 80386. Special instructions in the 80386, called ESC instructions, are used to control and sample these pins. The 80287 and 80387 provide numeric operations as a processor extension.

The numeric processor extensions use a slave interface to the processor. The 80386 performs all memory accesses required for operands; the NPX is never a bus master. The 80386 performs at least two bus cycles for every word transferred. For operand reads, the first cycle reads from memory, the second cycle writes to the NPX. For operand writes, the first cycle reads the operand from the NPX, the second writes to memory. Operand transfers to the NPX are fully aligned.

Two pins indicate the status of numeric processor extensions while one pin controls data transfers to the processor extensions. Special, reserved I/O addresses, are used for communication between the CPU and processor extension.

The processor extension of the 80386 matches that of the 80286 except that the 80386 does not generate the PEACK#

signal of the 80286. The 80287 requires PEACK# to disable its PEREQ input quickly after the last data transfer to prevent the 80286 from transferring an extra word. Since the 80386 will know the operand length in advance, fast removal of PEREQ to 80287 is not required. The 80287 PEACK# input can be connected to I/O port address 00F8H select, I/O select and A31 active (or can just be tied inactive).

80386 Processor Extension Pins

Type	Pin Name	Number
Processor Extension Status	BUSY#, ERROR#	2
Data Transfer Requests	PEREQ	1

The 80386 must know which processor extension is connected. The 80386 ERROR# input identifies at RESET whether an 80387 or 80287 is present. An 80287 requires 16-bit transfers, with minimum delays between transfers, be used for operands and commands. The 80387 allows 32-bit transfers with fewer restrictions.

The BUSY# input is also used for another function at RESET. This function is to determine whether an internal self test mode is to be entered.

2.4 POWER AND GROUNDS

The 80386 has approximately 41 pins for power and ground. These pins are not internally connected together. All power and ground pins must be connected to the appropriate power and ground signals of the system.

These pins must handle the current surges of approximately 40 pins switching at the same time. External decoupling capacitors must be next to the 80386 to supply this charge through a low inductance path. The 80386 connection to system ground and power must be low inductance.

3. PIN FUNCTION DESCRIPTIONS

This section defines the specific functions of each pin. The description is limited to information required by the hardware designer. Other sections of this document state how the pin should be used in terms of function.

Pin Name	Type	Description
CLK2	I	Operating Clock provides the fundamental timing for the 80386. It is divided by two internally to generate the internal clock used by instruction execution. The internal divide-by-two circuitry is synchronized to a known state by the falling edge of RESET.

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Pin Name	Type	Description
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RESET	I	<p>Reset forces the 80386 into a known state. The 80386 may be reinitialized at any time with a LOW to HIGH transition on this input that remains active for more than 16 CLK2 periods. During RESET, the input pins are ignored and the output pins of the 80386 enter the state shown in table 2. Operation of the 80386 begins after a HIGH to LOW transition on RESET. The HIGH to LOW transition of RESET must be synchronous to CLK2 to set the phase of the internal 80386 clock. At some time > 10 CLK2 cycles and < 400 CLK2 cycles the 80386 will fetch the first instruction from memory (if self test is not selected, see next paragraph.) During this time, the 80386 makes no internal requests to its bus, and therefore will relinquish the bus to an external HOLD request even before performing its first prefetch cycle.</p>
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A few clocks after the HIGH to LOW transition of RESET (corresponding to an internal RESET), one other pin is sampled to determine additional information:

BUSY# LOW indicates that self test is to be performed.

The 80386 can not begin execution of instructions until at least 1 millisecond after VCC and CLK2 have reached their proper DC and AC specifications. The 80386 should be kept in the RESET state during this time to avoid spurious outputs.

D31-D0	I/O	<p>Data Bus inputs information during memory, I/O, and interrupt acknowledge read cycles and outputs information during memory and I/O write cycles. The data bus inputs are active HIGH and require setup and hold times be met relative to CLK2 for correct operation. The data bus outputs are active HIGH and float to three state OFF during bus hold acknowledge.</p>
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Pin Name	Type	Description
A31-A2	O	Address Bus outputs physical memory or port I/O addresses or ICE trace messages. A31-A16 are LOW during I/O transfers except for I/O transfers automatically generated by coprocessor instructions. During coprocessor I/O transfers, A30-A16 are driven low, and A31 is driven high so that this address line can be used by external logic to more simply generate the coprocessor select signal. Thus, the I/O address driven by the 386 for coprocessor commands is 800000F8h, the I/O address driven by the 386 for coprocessor data is 800000FCh for cycles to both the 80287 and the 80387. The address bus is active HIGH and floats to three state OFF during bus hold acknowledge.
W/R#	O	Write/read is one of the bus cycle definition pins. It distinguishes write cycles from read cycles. These definitions are given in table 3. This signal floats to three state OFF during bus hold acknowledge.
D/C#	O	Data/control is one of the bus cycle definition pins. It distinguishes Data cycles, either memory or I/O, from control cycles which are: ICE trace, interrupt acknowledge, halt, and code fetch. These definitions are given in table 3. This signal floats to three state OFF during bus hold acknowledge.
M/I0#	O	Memory/I0 is one of the bus cycle definition pins. It distinguishes memory cycles from input/output cycles. These definitions are given in table 3. This signal floats to three state OFF during bus hold acknowledge.

Pin Name	Type	Description
LOCK#	0	Bus Lock is one of the bus cycle definition pins. It indicates that other system bus masters are not to gain control of the system bus while it is active. LOCK# is activated on the CLK2 edge that begins the first locked bus cycle (i.e., it is not active at the same time as the other bus cycle definition pins) and is deactivated when ready is returned at the end of the last bus cycle which is to be locked. The beginning of a bus cycle is determined when READY is returned in a previous bus cycle and another is pending (ADS# is active) or the clock in which ADS# is driven active if the bus was idle. This means that it more closely follows the write data rules for when it is valid. This solves the locking of 16 bit bus cycles, but may cause the bus to be locked longer than desired. The LOCK# signal may be explicitly activated by the LOCK prefix on certain instructions. The XCHG instruction, descriptor updates, interrupt acknowledge, and page table entry updates automatically assert LOCK#. LOCK# is active LOW and floats to three state OFF during bus hold acknowledge.
ADS#	0	Address Status, along with READY# active for the previous bus cycle, indicates that new address, byte enables, and definition signals (except LOCK#) are available. ADS# is an active LOW output. Once ADS# is driven active, valid address, byte enables, and definition will not change. In addition, ADS# will remain active until its associated bus cycle begins (when READY# is returned for the previous bus cycle when the 386 is running pipelined bus cycles.) This means that ADS# (and ICEADS#) will not glitch. When address pipelining is utilized, maximum throughput is achieved by initiating bus cycles when ADS# and READY# are active in the same clock cycle. This signal floats to three state OFF during bus hold acknowledge.

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Pin Name	Type	Description
BS16#	I	Bus Size 16-bit input forces all bus cycles to use only D15-D0 of the data bus. Bus cycles that transfer more than 16 bits of data will be forced to use a second bus cycle if BS16# is sampled active. BS16# is an active LOW input that requires setup and hold times be met relative to CLK2 for correct operation. It is sampled by the 80386 one CLK2 cycle before READY# is activated. BS16# has an internal pull-up resistor.

BS16# is ignored on either read cycles or write cycles if both BE3# and BE2# are inactive.

On write cycles:

BS16# is ignored if both BE1# and BE0# or both BE2# and BE3# are inactive. If BE1# is active and BE2# is active on any particular cycle and BS16# is active, the cycle will be repeated with the same values on A31-A2, LOCK#, M/I0#, D/C#, W/R#, BE3#, and BE2#, but both BE1# and BE0# will be inactive in the second bus cycle.

On read cycles:

When BS16# is activated on read cycles, the data inputs on D31-D16 will be ignored. If both BE1# and BE0# are inactive, and if BE2# or BE3# is active, the data normally associated with BE2# will be read on D7-D0 and the data normally associated with BE3# will be read on D15-D8. When BE1# or BE0# and BE2# or BE3# are active, the first cycle will be used to read the data in on the D15-D0 for the data associated with BE1# and BE0#. The second cycle will be used to read the data associated with BE2# and BE3# on D15-D0.

If BS16# is activated on a bus cycle which activates NA#, it must be activated before the first time the 386 samples the NA# line in that bus cycle.

Even though the 287 numeric coprocessor has only a 16-bit data interface, BS16# need not

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Pin Name	Type	Description
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- | | | |
|--------|---|---|
| | | be driven for its cycles when it is used in a 386 system. This is because the 386 is aware of its limitations, and will therefore only drive 16-bit data cycles when talking to it. |
| NA# | I | Next Address indicates that the system is ready to accept new values of A31-A2, M/I0#, D/C#, W/R#, and BE3#-BE0#. This signal is an active LOW input that must satisfy setup and hold requirements relative to CLK2 for correct operation of the 80386. NA# is ignored on bus cycles which are initiated by ICEADS# and in CLK cycles in which ADS# or READY# is activated. If NA# is activated on any bus cycle that activates BS16#, BS16# must be activated before the first time NA# would be sampled active. |
| READY# | I | Bus Ready indicates that the current bus cycle is to be terminated. Bus cycles can be extended indefinitely until terminated by READY#. READY# is an active LOW input that must satisfy setup and hold requirements relative to CLK2 for correct operation of the 80386. READY# is ignored during the first clock of all bus cycles and during bus hold acknowledge. |

Pin Name	Type	Description
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BE3#-BE0#	0	Byte Enables indicate which data bytes of the data bus take part in the current bus cycle when BS16# is inactive. The byte enables are active LOW and float to three state OFF during bus hold acknowledge. The allowed active combinations of the byte enable signals are: 3-2-1-0, 3-2-1, 2-1-0, 3-2, 2-1, 1-0, 3, 2, 1, and 0. The association of byte enable with data bus bits, when BS16# is HIGH, is as follows:
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BE3# applies to D31 - D24

BE2# applies to D23 - D16

BE1# applies to D15 - D8

BE0# applies to D7 - D0

When BE1# and BE0# are both inactive during write bus cycles, if BE2# is active then D7-D0 is a copy of D23-D16 and if BE3# is active then D15-D8 is a copy of D31-D24.

During interrupt acknowledge cycles, BE3#, BE2# and BE1# are driven inactive while BE0# is driven active.

Address bits A1 and A0 are encoded on the byte enable outputs. The lowest active byte enable (e.g. BE0# is lower than BE1#) encodes the A1 and A0 value. See table 4. Address bits A1 and A0 can be decoded from the byte enables with four external gates.

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Pin Name	Type	Description
HOLD	I	Bus Hold Request input allows another bus master to request control of the local bus. When control is granted, the 80386 floats A31-A2, BE3#-BE0#, D31-D0, LOCK#, M/I0#, D/C#, W/R#, and ADS# to three state OFF and then activates HLDA, thus entering the bus hold acknowledge state. The local bus will remain granted to the requesting master until HOLD becomes inactive. When HOLD becomes inactive, the 80386 will first deactivate HLDA, then drive the local bus, thus terminating the hold acknowledge condition. The HOLD input must be synchronous to CLK2. HOLD is active HIGH. None of the outputs of the 386 that are floated during HOLD have internal pull-up to insure they remain inactive during HOLD. HOLD is not recognized when RESET is active (although there are a number of clocks between RESET going inactive and the first 386 prefetch during which HOLD will be recognized).
HLDA	O	Bus Hold Acknowledge output indicates, when active, that the 80386 has surrendered control of its local bus to another bus master which has requested control by activating the HOLD input signal. At the same time HLDA is activated, the 80386 floats A31-A2, BE3#-BE0#, D31-D0, LOCK#, M/I0#, D/C#, W/R#, and ADS# to three state OFF (ADS# will have already been driven inactive through normal bus operation). These pins remain OFF throughout the time that HLDA remains active. When the hold condition is to be terminated due to deactivation of the HOLD input, the 80386 first deactivates HLDA as these pins continue to remain OFF. Later, the 80386 will resume control of the local bus by driving these pins. HLDA is active HIGH.

Pin Name	Type	Description
INTR	I	<p>Interrupt Request input signals that the 80386 should suspend execution of the current program and execute an interrupt acknowledge function. This interrupt request can be masked by an enable bit in the flag word. When the 80386 responds to the INTR input, it performs two interrupt acknowledge bus cycles to read an 8-bit vector that identifies the source of the interrupt.</p> <p>To assure program interruption, INTR must be held active until the interrupt acknowledge operation is performed. INTR is sampled at the beginning of every instruction, and if enabled, must be active at least eight CLK2 clock periods before the beginning of the instruction to interrupt the 80386 before executing the next instruction. The INTR input may be asynchronous to CLK2. Setup and hold times relative to CLK2 must be met to guarantee recognition at a particular clock edge. INTR is active HIGH, and 8259A compatible.</p>
NMI	I	<p>Non-Maskable Interrupt Request input interrupts the 80386 at the beginning of the next instruction. The interrupt vector is internally supplied; no interrupt acknowledge cycles are performed. After servicing NMI, it is masked until the next IRET instruction is executed.</p> <p>NMI is edge sensitive after internal synchronization. For proper recognition, the input must have been previously LOW for at least eight CLK2 clock periods and remain HIGH for at least eight CLK2 clock periods. The NMI input may be asynchronous to CLK2. Setup and hold times relative to CLK2 must be met to guarantee recognition at a particular clock edge. NMI is active HIGH.</p>

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Pin Name	Type	Description
BUSY#	I	BUSY# signals a busy condition from a processor extension. The active LOW BUSY# input can be asynchronous to CLK2. BUSY# has an internal pull-up resistor. Setup and hold times relative to CLK2 must be met to guarantee recognition at a particular clock edge. If BUSY# is LOW at RESET HIGH to LOW, then an internal self test will occur.
ERROR#	I	ERROR signals an error condition from a processor extension. The active LOW ERROR# input can be asynchronous to CLK2. ERROR# has an internal pull-up resistor. Setup and hold times relative to CLK2 must be met to guarantee recognition at a particular clock edge. It is also used at RESET to indicate the type of processor extension present. If ERROR# is active (LOW) 10 cycles after RESET goes inactive and remains active until at least the beginning of the first 386 bus cycle, an 80387 is present, otherwise an 80287 (or no coprocessor) is present.
PEREQ	I	Processor Extension Request indicates that the processor has data to be transferred by the 80386. The active HIGH PEREQ input can be asynchronous to CLK2. Setup and hold times relative to CLK2 must be met to guarantee recognition at a particular clock edge. This input is provided with a weak internal pulldown device to allow it to remain not connected in a 386 system that doesn't include a processor extension.
VCC	I	System power provides the +5V nominal DC supply input. The VCC pins are not internally tied together within the 80386.
VSS	I	System ground provides the 0V connection from which all inputs and outputs are measured. The VSS pins are not internally tied together within the 80386.

Pin Value	Pin Names
HIGH	LOCK#, D/C#, W/R#, ADS#, A31-A2
LOW	M/IO#, HLDA, BE3#-BE0#
Three state OFF	D31-D0

Table 1. Output Pin State During Reset

Pin Value	Pin Names
HIGH	HLDA
Three state OFF	LOCK#, M/IO#, D/C#, W/R#, ADS#, A31-A2, BE3#-BE0#, D31-D0

Table 2. Output Pin State During HOLD

M/IO#	D/C#	W/R#	Bus Cycle Initiated
0 (LOW)	0	0	Interrupt Acknowledge
0	0	1	Reserved
0	1	0	I/O read
0	1	1	I/O write
1 (HIGH)	0	0	Code read
1	0	1	Halt
1	1	0	Memory read
1	1	1	Memory write

Table 3. ADS# Initiated Bus Cycle Definitions

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BE3#	BE2#	BE1#	BE0#	A1 Value	A0 Value
X	X	X	0	0	0
X	X	0	1	0	1
X	0	1	1	1	0
0	1	1	1	1	1

Table 4. A1 and A0 Decoding from BE3#-BE0#

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	A	B	C	D	E	F	G	H	J	K	L	M	N	P
14	+	+	+	+	+	+	+	+	+	+	+	+	+	+
13	+	+	+	+	+	+	+	+	+	+	+	+	+	+
12	+	+	+	+	+	+	+	+	+	+	+	+	+	+
11	+	+	+									+	+	+
10	+	+	+									+	+	+
9	+	+	+		i	80386						+	+	+
8	+	+	+									+	+	+
7	+	+	+									+	+	+
6	+	+	+									+	+	+
5	+	+	+									+	+	+
4	+	+	+									+	+	+
3	+	+	+	+	+	+	+	+	+	+	+	+	+	+
2	+	+	+	+	+	+	+	+	+	+	+	+	+	+
1	+	+	+	+	+	+	+	+	+	+	+	+	+	+

TOP VIEW

Figure 1. 80386 PINOUT

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pin	label	pin	label	pin	label
A1	VCC	B1	VSS	C1	A8
A2	VSS	B2	A5	C2	A7
A3	A3	B3	A4	C3	A6
A4	N.C.	B4	N.C.	C4	A2
A5	VCC	B5	VSS	C5	VCC
A6	VSS	B6	N.C.	C6	ICE1
A7	VCC	B7	INTR	C7	N.C.
A8	ERROR#	B8	NMI	C8	PEREQ
A9	VSS	B9	BUSY#	C9	RESET
A10	VCC	B10	W/R#	C10	LOCK#
A11	D/C#	B11	VSS	C11	VSS
A12	M/I/O#	B12	N.C.	C12	VCC
A13	BE3#	B13	BE2#	C13	BE1#
A14	VCC	B14	VSS	C14	BS16#
D1	A11	E1	A14	F1	A15
D2	A10	E2	A13	F2	VSS
D3	A9	E3	A12	F3	VSS
D12	VCC	E12	BEO#	F12	CLK2
D13	NA#	E13	N.C.	F13	N.C.
D14	HOLD	E14	ADS	F14	VSS
G1	A16	H1	A17	J1	A20
G2	VCC	H2	A18	J2	VSS
G3	VCC	H3	A19	J3	VSS
G12	VCC	H12	D0	J12	VSS
G13	READY	H13	D1	J13	VSS
G14	VCC	H14	D2	J14	D3
K1	A21	L1	A23		
K2	A22	L2	A24		
K3	A25	L3	A28		
K12	D7	L12	VCC		
K13	D5	L13	D8		
K14	D4	L14	D6		
M1	A26	N1	A27	P1	A30
M2	A29	N2	A31	P2	VCC
M3	VCC	N3	VSS	P3	D30
M4	VSS	N4	VCC	P4	D29
M5	D31	N5	D27	P5	D26
M6	D28	N6	D25	P6	VSS
M7	VCC	N7	VCC	P7	D24
M8	VSS	N8	D23	P8	VCC
M9	D20	N9	D21	P9	D22
M10	VSS	N10	D17	P10	D19
M11	D15	N11	D16	P11	D18
M12	D10	N12	D12	P12	D14
M13	VCC	N13	D11	P13	D13
M14	HLDA	N14	D9	P14	VSS

4. MEMORY INTERFACE

The 80386 bus interface is designed for optimum performance in three basic types of systems: local cache, local DRAM, and remote DRAM. The next address pin allows the user to dynamically control address pipelining for bus cycle optimization. The bus size pin allows dynamic switching between 16 and 32-bit memories.

4.1 PHYSICAL MEMORY AND I/O INTERFACE

A maximum of 4 gigabytes (2^{32}) of memory and 65536 bytes of I/O locations can be addressed by the 80386 in protected mode. Real address mode can address one megabyte of physical memory and 65536 bytes of I/O locations.

To the programmer, memory locations and I/O ports are accessible as 8-bit bytes, 16-bit Words, and 32-bit Dwords. A Word is any two consecutively addressed bytes. A Dword is any four consecutively addressed bytes. The 80386 automatically converts the programmer's view into the hardware's organization.

In hardware, memory space and I/O space for the 80386 is organized as a sequence of 32-bit Dwords (2^{30} 32-bit memory locations and 2^{14} 32-bit I/O ports maximum). Each 32-bit memory and I/O Dword has four individually addressable bytes at consecutive memory addresses. With four bytes in each Dword, each 32-bit memory location starts at a physical address that is a multiple of 4. The A31 address bus output corresponds to the 32nd bit (2^{31} position) of the physical address and the A2 address bus output corresponds to the 3rd bit (2^2 position) in the binary physical address.

Each byte in memory or I/O space is individually addressable by taking the physical address and dividing it by 4 and using the remainder to activate the appropriate byte enable output. Each byte of physical memory is always transferred, except if BS16# is active, on the same 8-bits of the data bus. Table 5 shows the association of memory bytes with data bus location when BS16# is inactive.

Byte Address	DWord Address	Data Bus Bits Used	Byte Enable Activated
0	0	7-0	0
1	0	15-8	1
2	0	23-16	2
3	0	31-24	3
4	4	7-0	0
5	4	15-8	1
6	4	23-16	2
7	4	31-24	3
201	200	15-8	1

Table 5. Data Byte Location When BS16# Is Inactive

Data transfers can use more than one byte in a physical memory or I/O location. The legal combinations of bytes transferred within a single bus cycle are: 3-2-1-0, 3-2-1, 2-1-0, 3-2, 2-1, 1-0, 3, 2, 1, and 0. Data byte 3 is bits 31-24 and data byte 0 is bits 7-0.

The 80386 data bus can transfer any 32-bit data item, that is at a physical address which is a multiple of 4, in one bus cycle. Any Word can be transferred in a single bus cycle if it is at a physical address whose remainder mod 4 is less than 3. Any byte can be transferred in a single bus cycle.

Some Dword or Word data references require two bus cycles. Such transfers are called misaligned data transfers. The 80386 will automatically perform the two bus transfers and assemble or disassemble the data as required. Even though misaligned transfers are invisible to programs they are slower than aligned transfers and should be avoided. Misaligned transfer processing with BS16# inactive is given in table 6.

Data Type	Operand Address	First Physical Address	First Data Bus Bits, BE	Second Physical Address	Second Data Bus Bits, BE
Dword	N*4+1	N*4+4	7-0, 0	N*4	31-8, 3-1
Dword	N*4+2	N*4+4	15-0, 1-0	N*4	31-16, 3-2
Dword	N*4+3	N*4+4	23-0, 2-0	N*4	31-24, 3
Word	N*4+3	N*4+4	7-0, 0	N*4	31-24, 3

Table 6. Misaligned Data Transfers with BS16# Inactive

4.2 16-BIT BUSSES.

The 80386 can connect to 16-bit wide memories and I/O ports and automatically convert data transfers larger than 16-bits or misaligned 16-bit transfers into two transfers. The selection of memory or I/O bus width is made by the BS16# input on each bus cycle.

16-bit memories or I/O devices are connected to the lower 16 data bus bits D15 - D0. External logic needs to generate the two byte enables (BHE# and A0) for a 16-bit bus and A1 to provide 16-bit word addressing. The truth table for this generation is given in table 7 (entries with dots will never be generated by the 80386).

BE3#..BE0#	A1	A0	BHE#
1111	.	.	.
1110	0	0	1
1101	0	1	0
1100	0	0	0
1011	1	0	1
1010	.	.	.
1001	0	1	0
1000	0	0	0
0111	1	1	0
0110	.	.	.
0101	.	.	.
0100	.	.	.
0011	1	0	0
0010	.	.	.
0001	0	1	0
0000	0	0	0

Table 7. BHE#, A1, A0 Generation

16-bit memories or I/O ports are addressed much the same way as 32-bit memories except that each word is 16-bits wide and starts at a physical address that is a multiple of 2.

The 80386 monitors the BS16# pin in the middle of each CLK cycle of a bus cycle except for the first CLK cycle. If the READY# pin is activated at the end of a particular CLK cycle, then the value of the BS16# pin which was sampled in the middle of that CLK cycle is used by the 80386 to determine the bus size of the current bus cycle. See figure 7 which illustrates the sampling of BS16#.

Address pipelining is not allowed on 16-bit bus cycles. Therefore if BS16# is detected in a bus cycle, it will internally lock out NA#. In order for this to work properly, BS16# must be driven active before the 386 first attempts to sample NA#, which is in the middle of the CLK cycle after valid addresses are driven onto the external address bus for non-pipelined cycles (after 3 CLK2 cycles), or the middle of the first CLK cycle after ready is returned for the previous bus cycle with pipelined bus cycles.

The only cases in which BS16# can change the operation of a bus cycle are when BE2# or BE3# are active, otherwise BS16# is ignored by the 80386. BS16# does two things during a read cycle: determine where to get the read data on the data bus and determine whether another bus cycle is required. For

write cycles, BS16# can cause a subsequent write cycle but does not affect the current cycle.

Two cases of bus read cycles are affected by BS16#: reading something in each half of the 32-bit data bus and reading something in only the upper half of the 32-bit data bus. When BS16# is active, the 80386 will only use the data found on D15-D0. If a read cycle has BE1# active, BE2# active, and BS16# active the 80386 to use the data read on D15-D0, ignore data read on D31-D16, and repeat the bus cycle with the same address, byte enables, and definition except BE1# and BE0# will be inactive.

If a read cycle has both BE1# and BE0# HIGH (inactive), BS16# LOW(active) will cause the 80386 to read the data on the lower 16 bits of the data bus and ignore data on the upper 16-bits of the data bus. Data which would have been read on D31-D16 will be read on D15-D0.

BS16# can cause a write cycle to be repeated. If a write bus cycle has either BE1# or BE0# active and either BE3# or BE2# active, BS16# active will cause the 80386 to repeat the write with the same address, byte enables, and definition except that BE1# and BE0# will be inactive and the write data that had been on bits D31-D16 will be copied to bits D15-D0. If either BE2# or BE3# are activated and neither BE0# or BE1# are activated, the write data on the top half of the data bus is duplicated on both 16-bit halves of the 32-bit data bus; thus in this case, the write bus cycle will not need to be repeated.

The relationship between the byte enables driven in the first cycle and those driven in the second cycle when BS16# is asserted (and if a second cycle is even required) is given in table 8.

1st Cycle BE3#..BE0#	2nd Cycle BE3#..BE0#
1111	...
1110	none
1101	none
1100	none
1011	none
1010	...
1001	1011
1000	1011
0111	none
0110	...
0101	...
0100	...
0011	none
0010	...
0001	0011
0000	0011

Table 8. BS16# second cycle byte enables

4.3 BUS OPERATION

The 80386 uses a double frequency clock input (CLK2) to generate the internal processor clock. Internal cycles require two CLK2 cycles and are called CLK cycles. All input and output signals are measured relative to CLK2.

Seven types of bus operations are supported: memory read, memory write, I/O read, I/O write, code read, interrupt acknowledge, and halt. Data can be transferred at a maximum rate of one 32-bit Dword every two clock periods (e.g. 32 megabytes/second at 16 Mhz).

4.3.1 INTERRUPT ACKNOWLEDGE

In response to an interrupt request on the INTR input line, the 386 will run two interrupt acknowledge bus cycles. These bus cycles are similar to normal bus cycles in that the control lines of the 386 are used to signal the bus cycle, and that READY# must be returned active at the end of the cycle to allow it to terminate. The address driven during the first interrupt acknowledge cycle is 4; the address driven during the second interrupt acknowledge cycle is 0. During both interrupt acknowledge cycles, BE1#-BE3# are all driven

inactive while BE0# is driven active. During both interrupt acknowledge cycles D0-D31 float. LOCK# is asserted from the beginning of the first interrupt acknowledge cycle to the end of the second interrupt acknowledge cycle. At least 160ns of (locked) bus idle time will be inserted by the 386 between these two cycles for all selections of the 386 up to 24MHz to insure compatibility with the 8259A interrupt controller. During the second interrupt acknowledge cycle the 386 will read the external interrupt vector from bits 0-7 of the data bus.

4.3.2 HALT

The 386 signals an internal halt or an internal shutdown by initiating a halt bus cycle. Like other bus cycles, this MUST be terminated by a ready, i.e., READY# must be sampled active to complete the "bus cycle." If READY# is not returned, the 386 will wait forever. Any data returned on the data bus is ignored.

The halt state is entered when the HALT instruction is executed; shutdown is entered when a protection fault occurs when attempting to handle a double fault. They are externally differentiated by the address driven onto the address bus when the halt status is signaled. The address driven for halt is 2, while the address driven for shutdown is 0. Both of these cycles are 8-bit cycles, and since the 386 has byte select pins instead of low-order address pins, halt is indicated by BE2# being active while shutdown is indicated by BE0# being active.

The 386 will leave halt when an external INTR is received (and interrupts were enabled), NMI is received, ICEMD# is received, or the part is reset. The 386 will leave shutdown only when the part is reset, NMI is received, or if the ICEMD# signal is received.

4.3.3 BUS HOLD

During hold acknowledge, the 80386 will float all address, byte enable, data, definition, and address strobe output pins enabling another bus master to use the local bus. The 80386 HOLD input is used to place the 80386 into the HOLD state. The 80386 HLDA signal indicates that the CPU has entered the hold acknowledge condition.

The HOLD signal has priority over most bus cycles, however it is not honored between the two interrupt acknowledge cycles,

repeated cycles due to BS16#, or locked cycles. Note that HOLD will be acknowledged between the two cycles that are required to access a non-aligned variable, whereas on the 286 and the 8086 HOLD would not be acknowledged. This could lead to some very subtle software incompatibilities.

4.3.4 BUS CYCLES

When ADS# goes active, it means that the 80386 is ready to perform another bus cycle if the previous cycle is complete or is completing. Once ADS# is driven active, the 386 is committed to performing the bus cycle indicated by its address and control lines. Neither ADS# nor the address or control lines will glitch. If external hardware can handle multiple outstanding requests, it is free to begin this bus cycle. The outstanding bus requests must be returned to the 386 in order, and under no conditions will the 386 attempt to begin yet another bus cycle until the first one completes.

After RESET the 80386 bus enters an idle state during which the address strobe output (ADS#) is inactive. A bus cycle begins by the address, byte enables, and definition signals becoming valid and an address strobe going active, all in the first CLK cycle of the bus cycle. In the second CLK cycle, the address, byte enables, and definition signals remain valid and the 80386 begins monitoring the ready pins to determine if the bus cycle should terminate and monitoring the "next address" pin, NA#, to determine if the address, byte enables, and definition signals for the next bus cycle should be output.

If the bus cycle is terminated by the ready pin, then the next bus cycle may begin in the next CLK cycle, if the 80386 is ready to perform another bus cycle.

If the bus cycle is not terminated by the ready pin in this second CLK cycle of the bus cycle, then a wait state will occur in the third CLK cycle. In this case the value of the NA# pin during the second CLK cycle determines whether, in the third CLK cycle, the address, byte enable, and definition signals will continue to retain valid values for this bus cycle (NA# inactive) or output the values for the next bus cycle (NA# active) provided that the 80386 is ready with the next bus cycle. The outputting of new address, byte enables, and definition before the previous bus cycle is complete is known as "address pipelining" and is accompanied by activation of ADS#.

In each subsequent CLK cycle the ready pin is monitored to determine when the bus cycle should be terminated. There is no limit to the number of wait states which may be inserted due to withholding the proper activation of the ready pin. If the NA# pin is activated on any wait state and if the 80386 is ready with another bus cycle, then the 80386 enters an address pipelining condition in which new address, byte enables, and definition are output. Once the address pipelining condition has been entered, the 80386 will retain the new values of address, byte enables, and definition regardless of the subsequent state of the NA# pin.

Figures 2 through 8 illustrate the timing of different bus cycles. Figure 9 gives the 386 bus state machine.

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	<-- READ -->		<- WRITE ->		<- WRITE ->		<-- READ -->		<-- READ -->	
CLK	1	2	1	2	1	2	1	2	1	2
A31-A2, BE3#-BE0#, M/I0#,D/C#	X	.	X	.	X	.	X	.	X	X
W/R#
LOCK#	\	/	\	/	\	/	\	/	\	/
ADS#	\	/	\	/	\	/	\	/	\	/
NA#	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
READY#	XXXXX	XXX	XXX	XXX	XXX	XXX	XXX	XXX	XXX	XXX
DATA IN
DATA OUT	-----	-<	>-	-----	-----	-----	-<	>-	-----	-----

Figure 2. Fastest Possible Non-address Pipelined Cycle

	<-- READ -->		<- WRITE ->		<- WRITE ->		<-- READ -->		<-- READ -->	
CLK	1	2	1	2	1	2	1	2	1	2
A31-A2, BE3#-BE0#, M/I0#,D/C# W/R#	.	.	X	X	.	X	.	X	.	X
LOCK#	\	/	.	.	/	.	.	/	.	.
ADS#	/	.	\	/	\	/	\	/	\	/
NA#	X	X	XXXXX	X	X	XXXXX	X	X	XXXXX	X
READY#	XXXXX	XXX	XXXX	XXX	XXXX	XXX	XXXX	XXX	XXXX	XXX
DATA IN
DATA OUT	-----	--<	-->	-----	-----	-----	--<	-->	-----	--<

Figure 3. Fastest Possible Address Pipelineing Cycles

	<---- READ ----->			<---- WRITE ----->			<---- READ ----->			<----		
CLK	1	2	3	1	2	3	1	2	3	1	2	3
A31-A2, BE3#-BE0#, M/I0#,D/C#	X			X			X			X		
W/R#
LOCK#	\				/
ADS#	\	/	.	\	/	.	\	.		\	/	.
NA#	XXXXX	X	.	XXXXX	XXXXX	X	.	X	XXXXX	XXXXX	X	.
READY#	XXXXX	XXX		XX	XXXX	XXX	XX	XXXX	XXX	XX	XXXX	X
DATA IN	.	.		<	>		.	.		<	>	
DATA OUT	.	.		<X		

Figure 4. Non-add. Pipelineing Cycle with Wait State

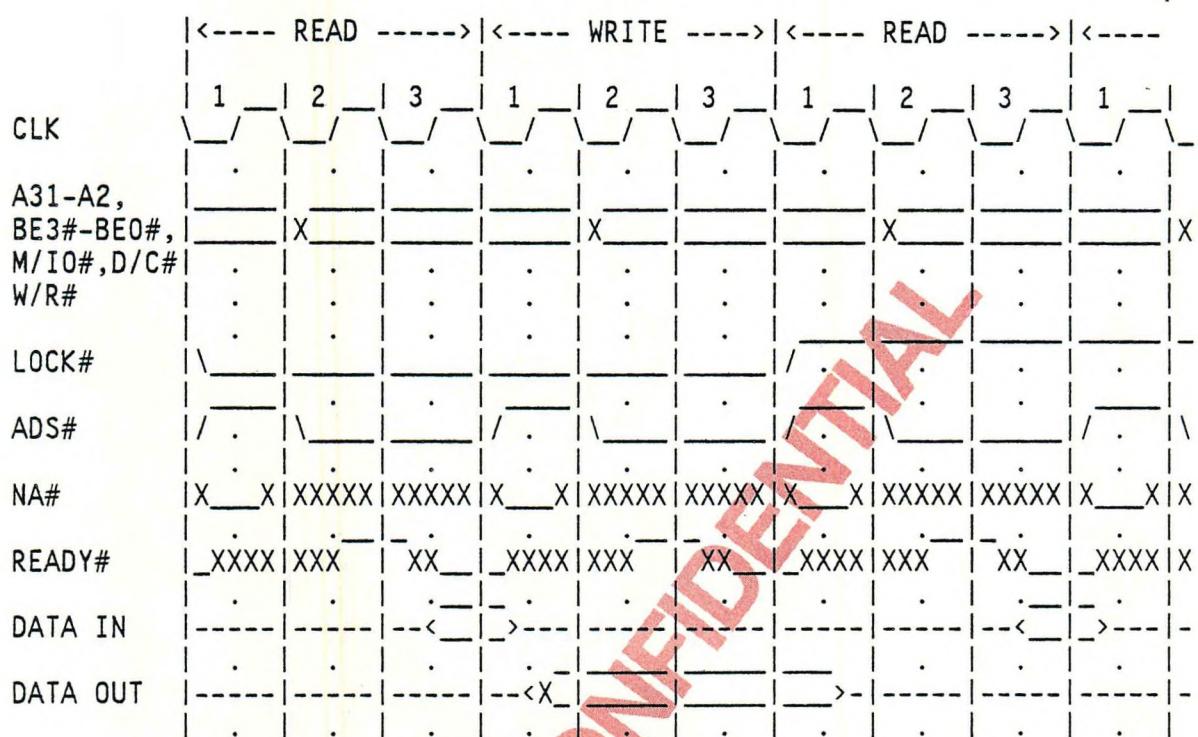


Figure 5. Address Pipelineing Cycle with Wait State

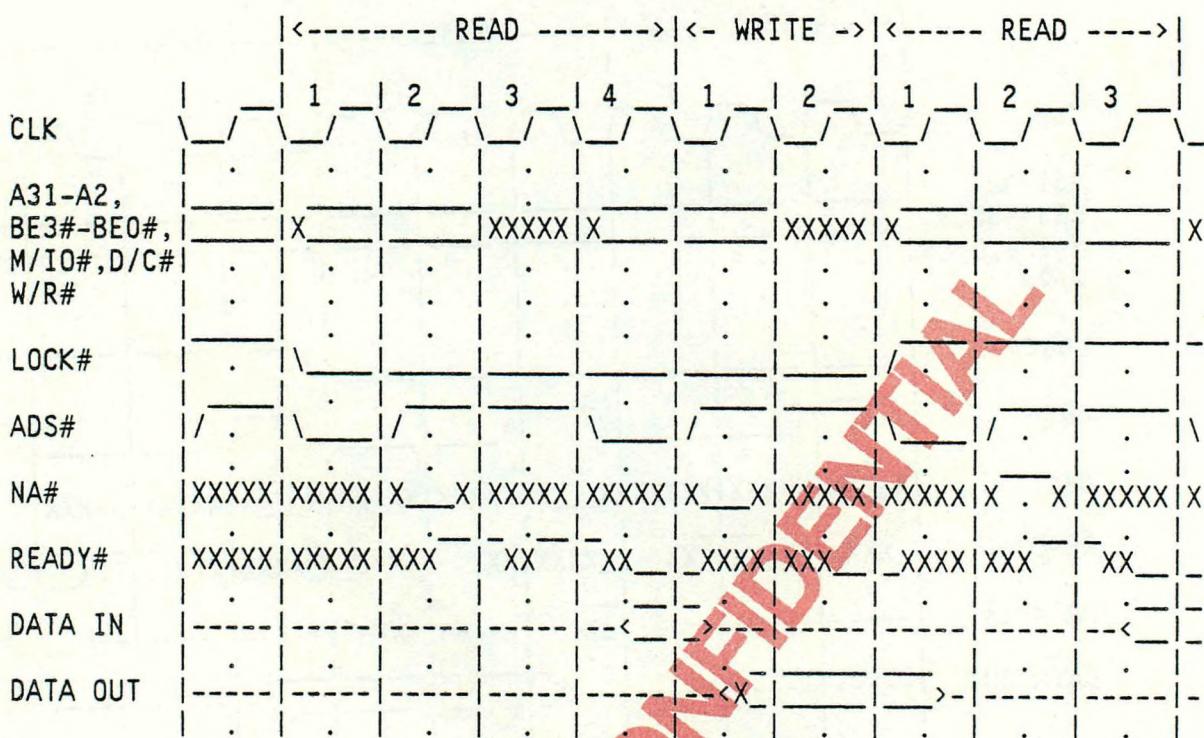


Figure 6. Bus Cycles of Mixed Types

	32-BIT				16-BIT				
	<----READ (part 1)---->				< (part 2)>		READ ---->		
CLK	1	2	3	4	1	2	1	2	3
A31-A2, BE3#-BE0#, M/I0#,D/C#	.	X			X		X		X
W/R#
LOCK#	.	\				/	.	.	.
ADS#	.	\	/	.	.	\	/	.	\
NA#	XXXXX	XXXXX	X . X	X . X	XXXXX	XXXXX	XXXXX	X . X	X . X X
BS16#	XXXXX	XXXXX	XXXXX	XXXXX	X _ X	XXXXX	XXXXX	XXXXX	XXXXX X
READY#	XXXXX	XXXXX	XXX	XX	XX	XXXX	XXX	XXX	XX
DATA IN	-----	-----	-----	-----	-----	-----	-----	-----	-----

Figure 7. 16 and 32-Bit Bus Cycles

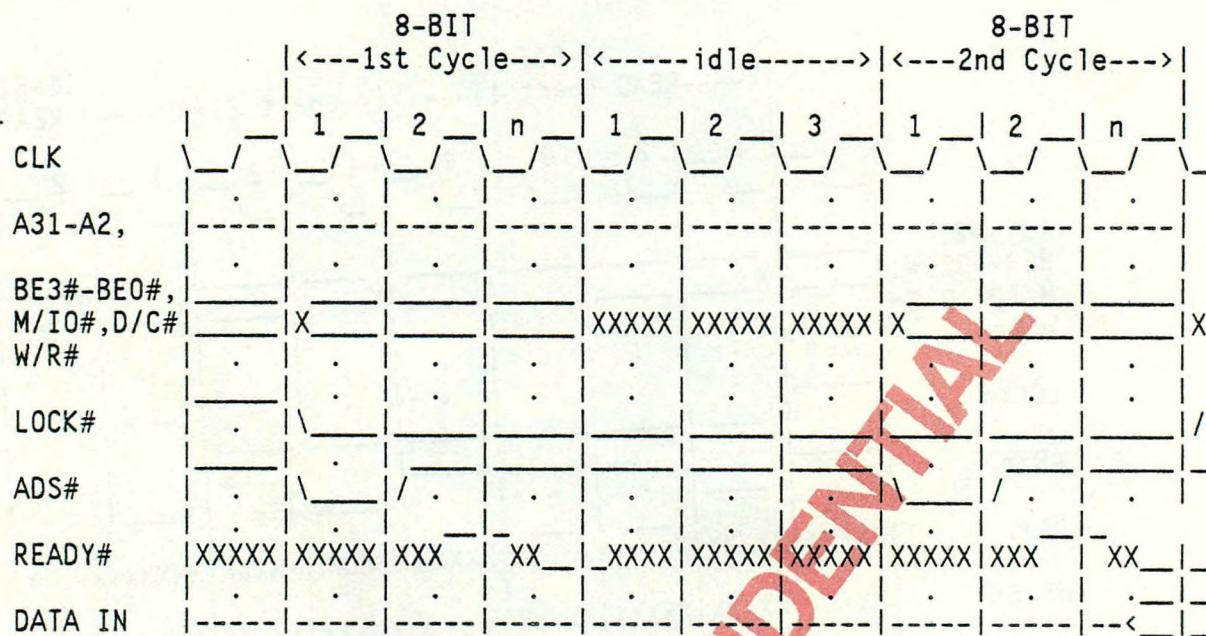
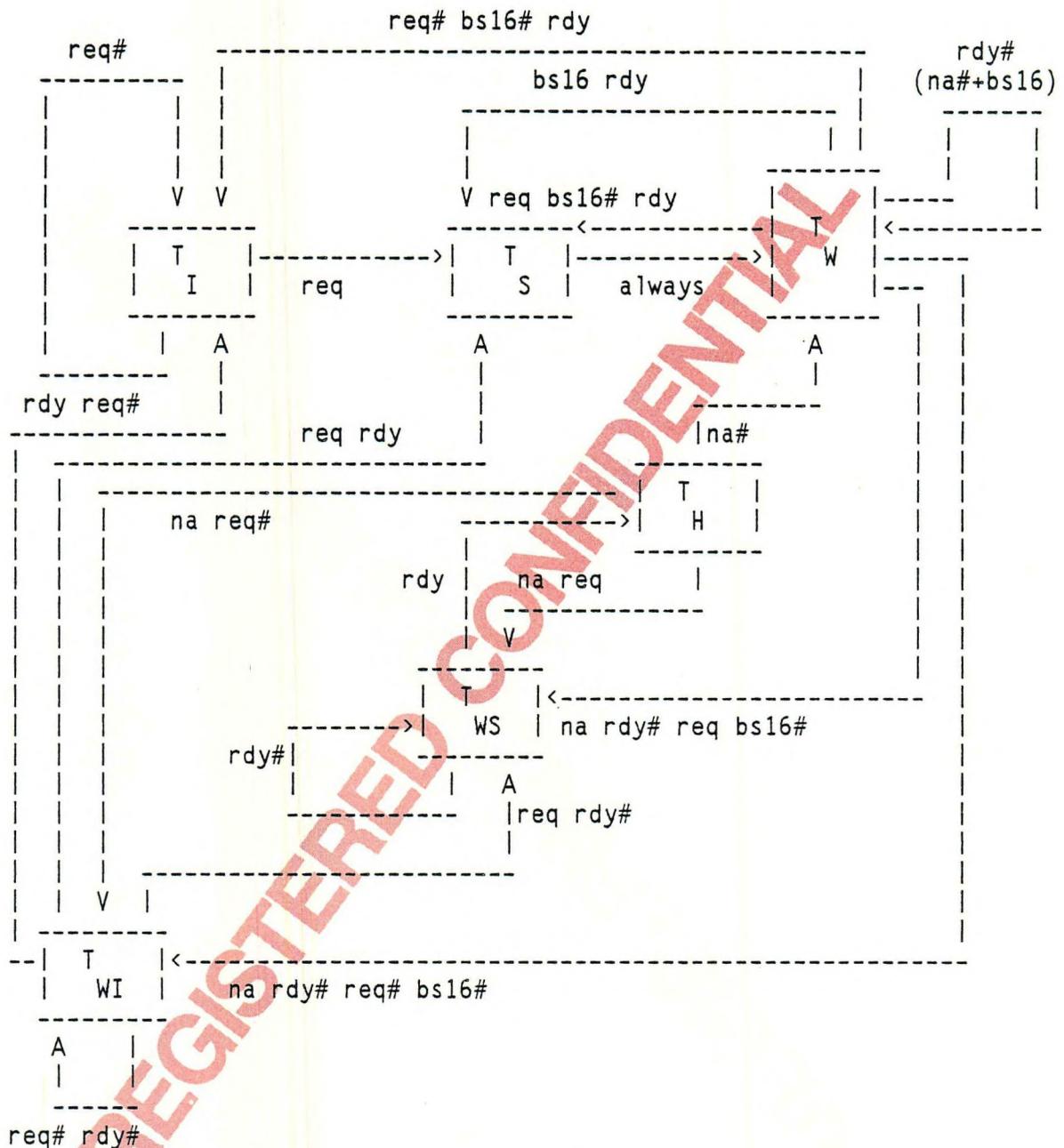


Figure 8. interrupt acknowledge Bus Cycles



NOTE: for all signals, s indicates the signal is asserted, while s# indicates that the signal is not asserted, e.g., bs16 means that external bs16 is asserted (the external signal is low) while bs16# means the external signal is not asserted (the external signal is high).

Figure 9. Bus State Diagram

signal	description
req	an internal request from the 386
rdy	ready
na	next address
bs16	bs16 signal
state	description
TI	idle bus
TS	first clock of a non-pipelined bus cycle
TW	subsequent clocks of a non-pipelined bus cycle
TWI	wait states with no internal request pending but with NA asserted (the 386 will NOT drive new addresses or ADS)
TWS	wait states after NA asserted and an internal request has been received (the 386 will drive new addresses and ADS)
TH	the first clock of a pipelined bus cycle

5. AC/DC SPECIFICATIONS

This section describes the AC and DC specifications for the 386 pins.

Data sheet DC specifications are given in table 9. All input and output levels are TTL compatible, except for the MOS level CLK2 input clock.

AC specifications are given in table 10. This table uses the waveforms shown in figures 10 through 14. All input and output timings are specified relative to the 2.0 volt level of the rising edge of CLK2 and refer to the time at which the signal reaches the TTL logic levels of LOW (0.8V) or HIGH (2.0V). See figure 10.

All AC testing should be done with input voltages of .4V and 2.4V. DC testing whould be done to the VIL and VIH specs of .8V and 2.0V respectively.

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ABSOLUTE MAXIMUM RATINGS:

Ambient Temperature Under Bias 0 C to 70 C
 Storage Temperature -65 C to +150 C
 Voltage on Any Pin with Respect to Ground . . -0.5 to VCC+0.5V
 Power Dissipation 3.6 Watt

DC CHARACTERISTICS (TC = 0 deg C to 70 deg C, VCC = 5V+-10%)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIL	INPUT LO VOLTAGE	-0.3	+0.8	V	
VIH	INPUT HI VOLTAGE	2.0	VCC+0.3	V	
VCL	CLK2 INPUT LO VOLTAGE	-0.3	+0.8	V	
VCH	CLK2 INPUT HI VOLTAGE	VCC-0.8	VCC+0.3	V	
VOL	OUTPUT LO VOLTAGE		0.45	V	See note 1
VOH	OUTPUT HI VOLTAGE	2.4		V	See note 2
ICC	POWER SUPPLY CURRENT		400	mA	TA=25 deg C
ILI	INPUT LEAKAGE CUR.		+15	uA	0V<=VIN<=VCC
ILO	OUTPUT LEAKAGE CUR.		+15	uA	0.45V<=VO<=VCC
CIN	INPUT CAPACITANCE		10	pF	fc=1MHz
CO	I/O OR OUTPUT CAP.		12	pF	fc=1MHz
CCLK	CLOCK CAPACITANCE		20	pF	fc=1MHz

NOTE 1: This parameter is measured at:

Address, data 4.0mA
 Byte enables, definition,
 control 5mA
 0.5mA on BE3#-BE0#

NOTE 2: This parameter is measured at:

Address, data 1mA
 Byte enables, definition,
 control 0.9mA

Table 9. DC Specifications

AC CHARACTERISTICS (TC = 0 deg C to 70 deg C, VCC = 5V+-10%)

PIN	SYMBOL	PARAMETER	MIN	MAX	TEST CONDITIONS
CLK2	1	period	31.25	125	at 2.0V
CLK2	2a	low time	9		at 2.0V
CLK2	2b	low time	7*		at 0.8V
CLK2	3a	high time	9		at 2.0V
CLK2	3b	high time	5*		at VCC-0.8V
CLK2	4	fall time		8*	VCC-0.8 to 0.8V
CLK2	5	rise time		8*	0.8 to VCC-0.8V
A31-A2	6	out delay	1	40	CL=120pF
A31-A2	7	hold time	1		CL=120pF
A31-A2	7A	float time	1	40	
BE3-0#,LOCK#	8a	out delay	1	40	CL= 75pF
ADS#,M/IO#	8b	out delay	1	35	CL= 75pF
D/C#,W/R#	9	hold time	1		CL= 75pF
HLDA	12	out delay	4	35	CL=75pF
HLDA	13	hold time	4		CL=75pF
D31-D0	18	out delay	1	48	CL=120pF
D31-D0	19	hold time	1		CL=120pF
D31-D0	20	setup time	10		
D31-D0	21	hold time	3		
D31-D0	21A	float time	1	30	
NA#	22	setup time	10		
BS16#	22	setup time	12		
NA#, BS16#	23	hold time	20		
READY#	24	setup time	20		
READY#	25	hold time	3		
HOLD	28	setup time	25		
HOLD	29	hold time	4		
RESET	30	setup time	12		
RESET	31	hold time	3		

* not tested

Table 10. AC Specifications - MIN/MAX IN NS

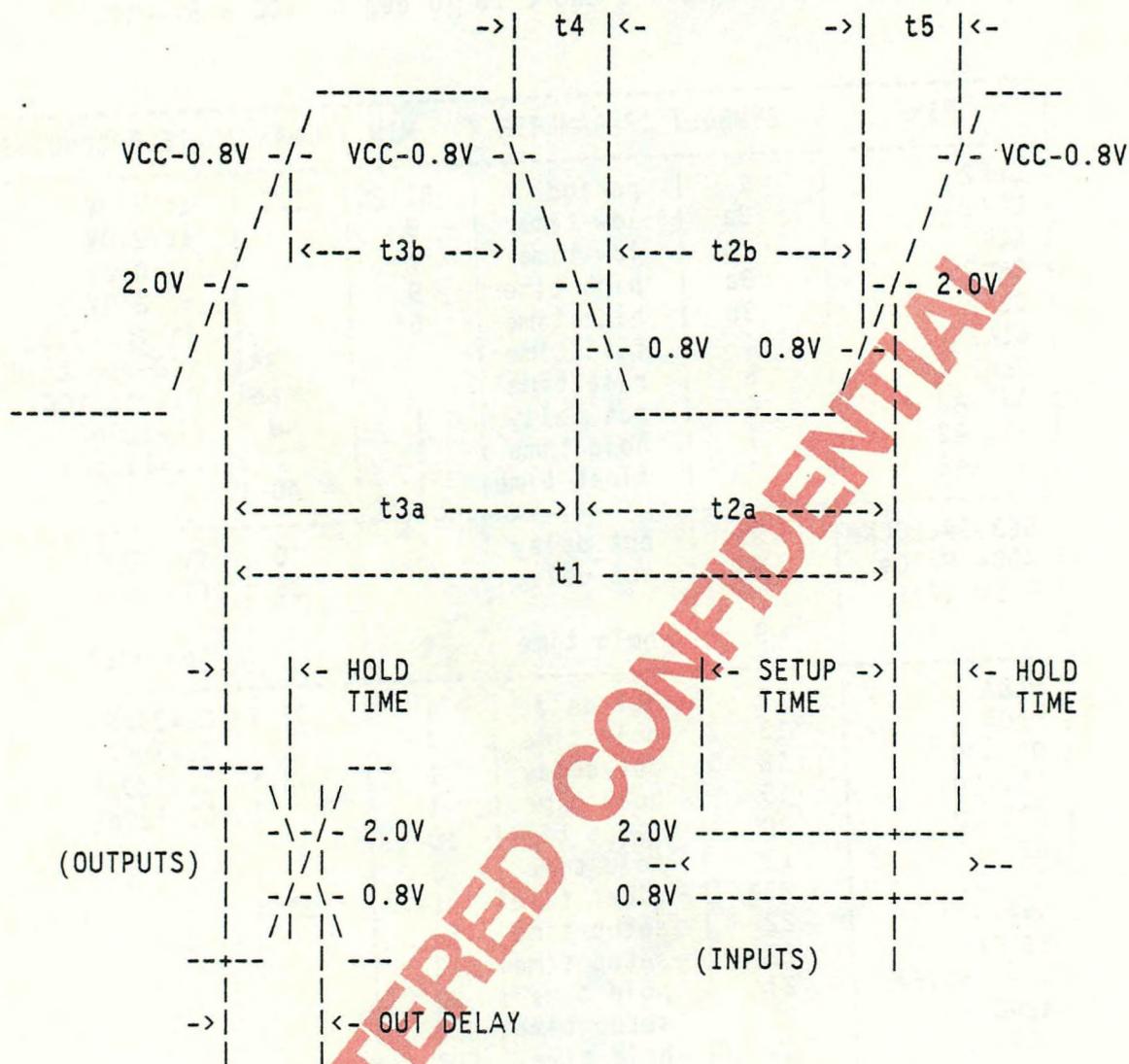


Figure 10. CLK2 Waveform

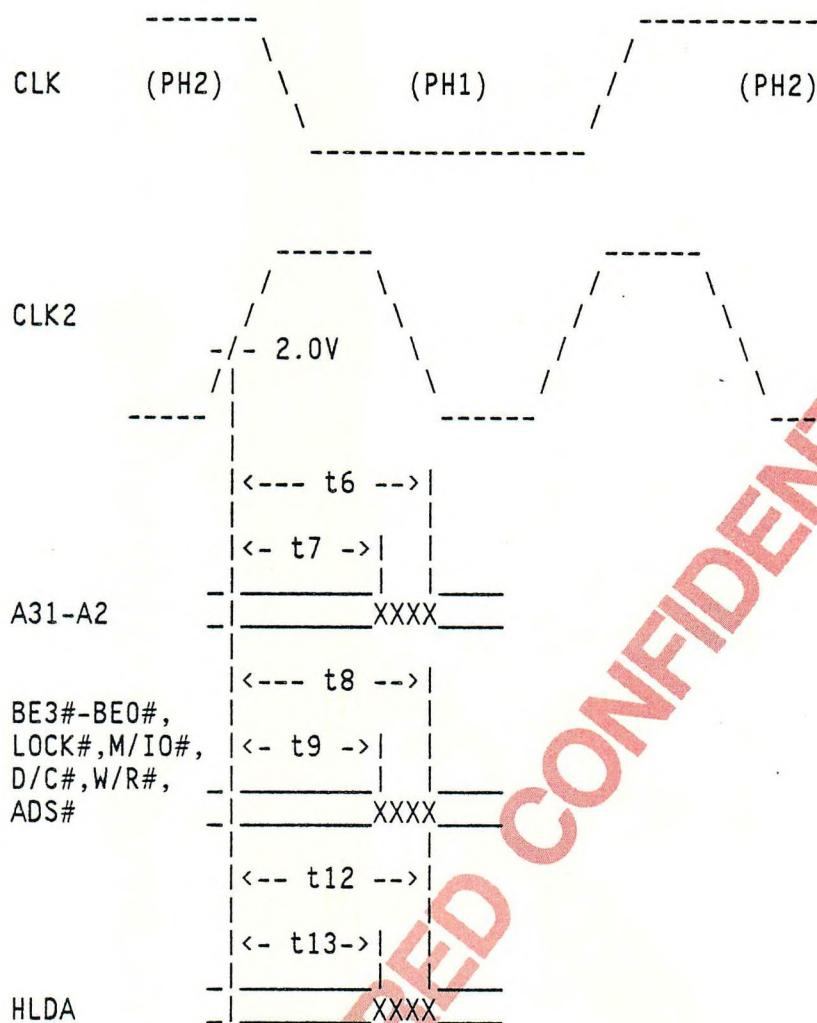


Figure 11. AC TIMING WAVEFORMS -- OUTPUT SIGNALS

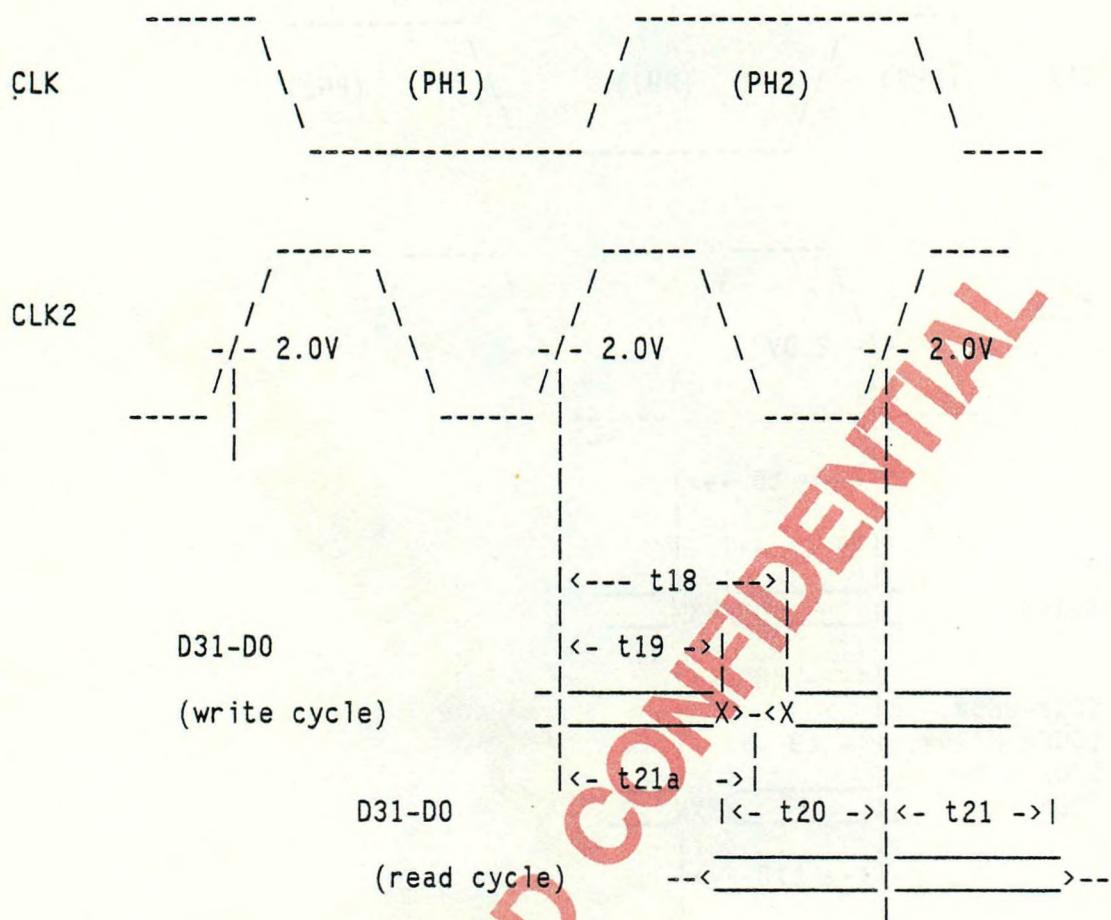


Figure 12. AC TIMING WAVEFORMS -- I/O SIGNALS

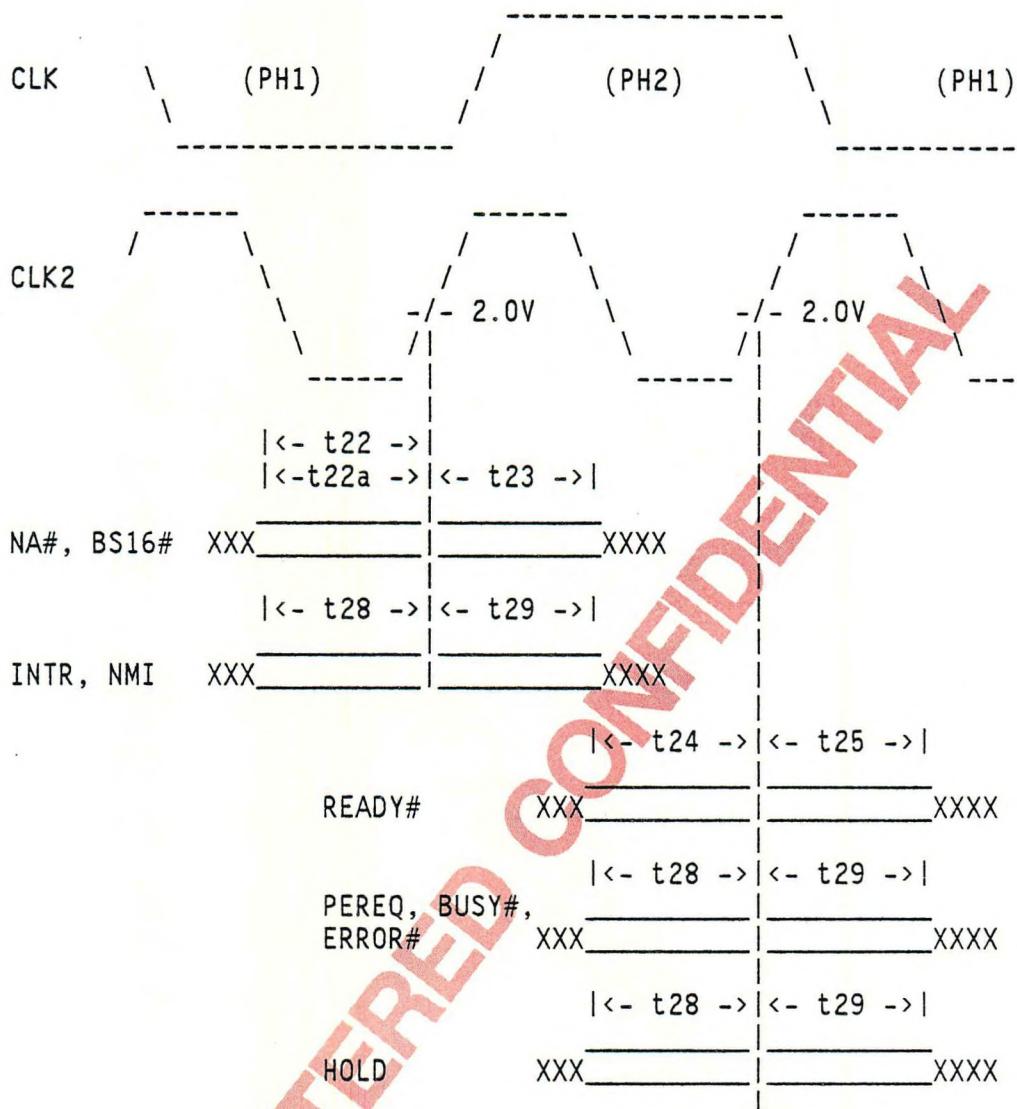
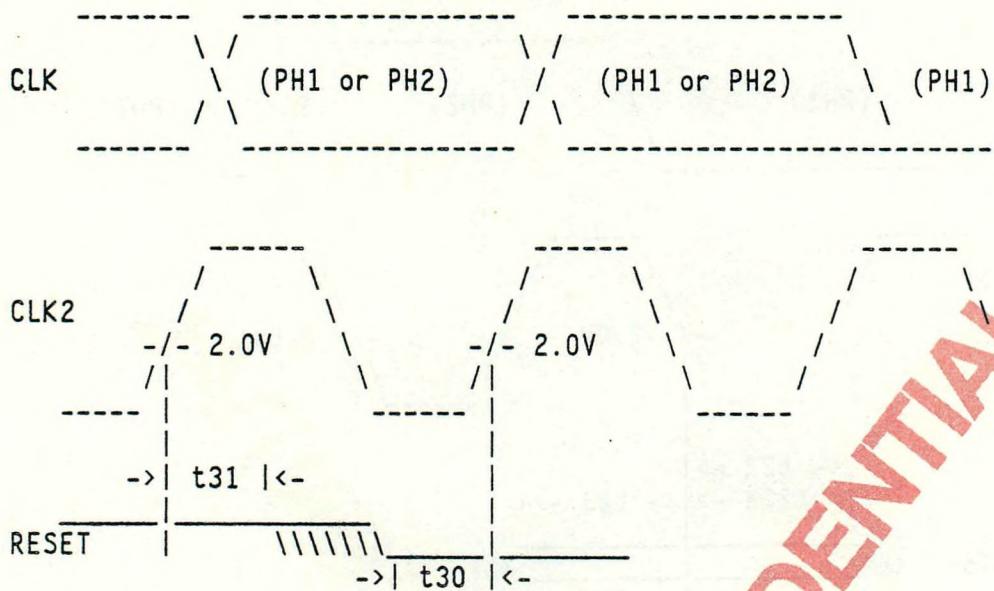


Figure 13. AC TIMING WAVEFORMS -- INPUT SIGNALS



NOTE: The second internal processor phase following
RESET high to low transition is PH1.

Figure 14. AC TIMING WAVEFORMS -- RESET SIGNAL

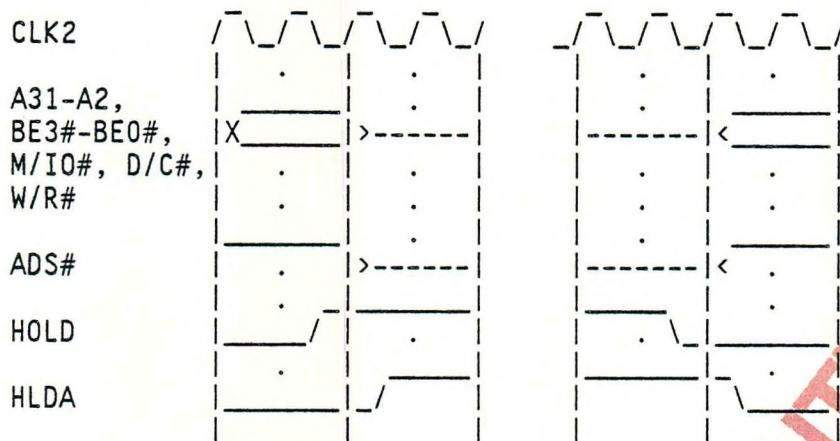


Figure 15. HOLD TIMING FOR AN IDLE BUS

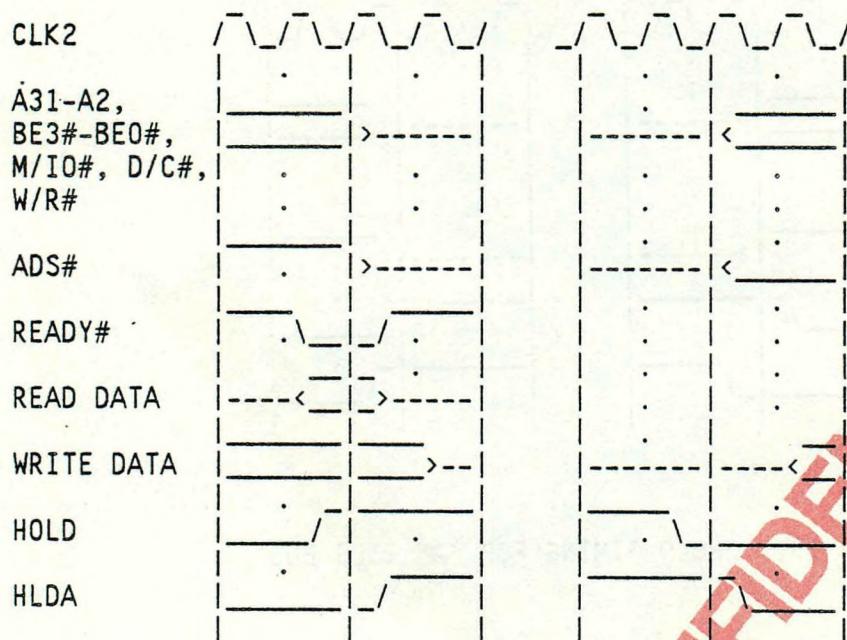


Figure 16. HOLD/HLDA TIMING WITH BUS CYCLES

6. TESTABILITY

This section describes the features which are included in the 80386 for the purpose of enhancing 80386 testability.

6.1 OVERVIEW OF TESTABILITY

The 80386 combines several forms of classical testability: Signature Analysis, Divide and conquer and Ad Hoc techniques. These have been combined in such a way to provide a minimal overhead on the designers and chip size while providing 100% test coverage on the regular blocks (regular blocks comprise one half of all devices in the 80386). No attempt is made to provide random logic self test features. Random logic testing will be done by standard testing methods (eg. diagnostic programs).

The following list summarizes the 80386 testability features:

1. PLA - self test of three large PLAs.
2. CROM - self test of the control ROM.
3. CROM - contents dump
4. TLB - Hooks for assembly language test of TLB
5. Tristate - isolate the 80386 from external world.

6.2 EXTERNAL VIEW

This section describes how the 80386 testability features appear at the pins. The pin definitions, the test register definition and the in circuit test definition are provided here.

6.2.1 SELF TEST

Self test is entered with BUSY# LOW at RESET HIGH to LOW. This will cause the 80386 to enter internal self test mode. During self test all outputs are in their reset state (see table 1) and all inputs are don't cares. The self test is $2^{**}19+E$ clocks in duration where E is about 30 clocks. At the completion of self test the chip performs a normal reset sequence and begins normal operation while preserving the results of the self test. The results of the self test are then available in the EAX and EDX registers to be read by

macro-instructions.

6.2.2 TRISTATE

All outputs are tristated and all inputs are ignored with the assertion of HOLD (with the exception of HLDA and HOLD of course). CLK2 needs to continue however.

6.2.3 SELF TEST REGISTERS

The following diagram shows the definition of test registers.

	31	0
TR0	Reserved	
TR1	Reserved	
TR2	Reserved	
TR3	Reserved	
TR4	Reserved	
TR5	Reserved	
TR6	TLB command reg	
TR7	TLB data reg	

The signatures from the self-test are available in the EAX and EDX registers at reset, with the signature mapping as follows:

	----- 16 -----	----- 16 -----	
	31	0	
EAX	Ent PLA	Ctr PLA	
EDX	Test PLA	CROM	

EAX and EDX hold the signatures which are broken into 2 16 bit sections each. EAX reflects the results of the entry point and control PLA self tests. EDX reflects the results of the Test PLA and CROM (control ROM) self tests. When the register is read a successful self test results in the

register to read out 0.

TR6, TR7 provide read and write access to the TLB. The detailed operation of these registers is given below.

Access to the test registers is provided by the MOV Reg,TREG and MOV TREG,Reg instructions (refer to the 386 EAS).

6.3 DETAILED DESCRIPTION

This section describes in detail the actual test modes which were summarized above.

6.3.1 TRISTATE OUTPUTS

This is useful for isolating the 80386, except for HOLD and HLDA, from the remainder of the system for insystem board checks etc. The part will isolate itself from the system following the assertion of HOLD (normal HOLD/HLDA timings are obeyed) and will remain isolated until HOLD is deasserted. As noted in the definition of the HOLD pin in chapter 3, if HOLD is asserted after RESET, but before the first bus cycle, the 386 will enter the HLDA state before running the first bus cycle.

6.3.2 SELF TEST MODE

When self test mode is entered the 80386 begins an exhaustive internal self test of three large PLAs and the CROM. As described above this test takes $2^{**}19+E$ cycles to complete and is followed by a normal reset.

6.3.3 PLA TESTING

During test mode the three major PLAs of the 80386 are exhaustively tested. The normal inputs to the PLA are disabled and the inputs come from a maximal length LFSR (Linear Feedback Shift Register) operating as a $2^{**}n-1$ counter. As inputs, this counter provides a pseudorandom sequence of all possible counts to the PLA and, thus activates every possible PLA term.

While all possible inputs are being forced, the outputs of the PLA are being accumulated into a parallel load LFSR. The single bit result of the modulus division is accumulated in a Serial load LFSR which is later normalized to 0 (if correct)

and transferred to EAX and EDX.

This technique provides 100% coverage of all single bit faults (which statistically implies an extremely high overall fault coverage).

After completion of the self test, the RESET microcode will normalize the accumulated signature by XORing it with a constant stored in the 80386 to always produce the same result (these constants will vary with stepping to always yield the same result). In this way the reading of the correct signature always results in 0, regardless of stepping.

6.3.4 CROM TESTING

During self test the CROM contents are also analyzed by a LFSR register. The CROM is sequenced through all possible words. All CROM outputs are fed into a parallel load LFSR to accumulate a signature result. The result of this polynomial division is serially accumulated into the LFSR and available in the lower word of EDX after RESET.

As in the PLA test described above the correct results are exclusive ored with the appropriate constant to always yield a result of 0.

6.3.5 RAM CAM ACCESS

The TLB of 32 entries is a RAM/CAM area of the 80386 which requires special testability features. The technique employed requires the test pattern to be driven from the tester or an assembly language program rather than being built into the 80386. By using this technique extensive pattern sensitivity tests can be developed and executed well after the design is complete to reveal weaknesses in the design or test program.

The P unit has two test registers associated with it. One is a test command register, the other is the test data register. The PUNIT command register is TR6, and TR7 is the PUNIT data register.

Commands and addresses are written into the command register. The low order bit of the value written into this register indicates the command to be performed, while the upper bits usually give an address (TAG) to use in performing the operation.

The data register holds data read from or to be written to the RAM areas of the cache. On cache writes the data register is loaded with the new RAM value before the command register is loaded with the address (CAM value) and command bits. On cache lookups, after the command register is loaded with the command and TAG value, the data register will receive the data read out from the cache if a hit occurs, or will indicate a miss if a miss occurs.

These testability hooks attempt to use as much of the normal operating circuitry as possible. Since the machine needs to be operating normally (eg. executing the test instructions!!) the mechanisms are not identical. When testing the TLB paging must be disabled.

6.3.5.1 PUNIT TLB ACCESS

Several different operations are provided to access the TLB. The two allowed operations are:

1. Write New TLB Entry
2. Perform TLB Lookup

The command code for these operations is contained in bit 0 when writing to the test command register.

6.3.5.1.1 WRITE NEW TLB ENTRY

When the PUNIT command register is written with a value that has the low order bit 0, a new entry is written into the TLB using data from the upper bits of the command register along with the contents of the data register.

The data register gives the value to write into the RAM portion of the TLB, and also specifies the replacement pointer location and/or value to use for the write. The upper bits of the command register give the Linear address and attributes to write into the CAM portion of the TLB.

The entry to (over)write with the new information is determined by a replacement pointer. The replacement pointer used can be either the Replacement Pointer in the PUNIT, or can be taken from bits 2 and 3 of the data register. Bit 4 of the PUNIT data register is used to select between these cases, as follows:

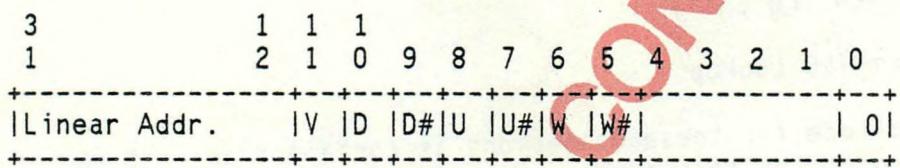
Bit 4 Replacement Pointer
 0 Use PUNIT replacement pointer
 1 Use PUNIT Data Reg<3..2>

Behavior of the replacement is consistent but not controllable and predictable. It increments with every bus cycle that is a TLB hit (even when paging is disabled).

It is important that the same Linear address tag not be written to more one location in the CAM. If this is done the hit information for a Cache lookup will be undefined.

6.3.5.1.2 FORMAT OF COMMAND REGISTER

The tags stored in the TLB are 24 bits wide. They contain the high-order 20 bits of the linear address, the valid bit, and 2 bits each (attribute and attribute#) of the D, W (R/W), and S (U/S) bits from the page table entry. The fields are aligned in the 32-bit test register (for the write command) as follows:



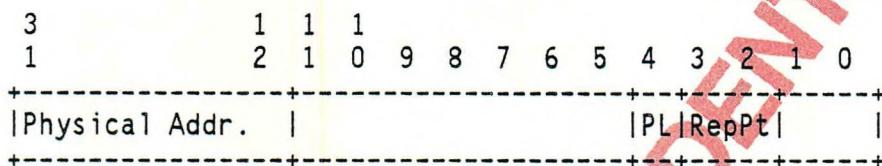
The high-order 20 bits are the high-order 20 bits of the linear address. Bit 11 is the Valid bit, to permit writing invalid entries. The V-bit functions as another bit of address for testability. For paging or ICE mapping the V-bit must be set as the lookups in these modes look for a 1 in the V-bit. The V bit prevents uninitialized tags from matching, so that lookups with V=0 are unpredictable if any of the CAM tags are uninitialized. All V bits are cleared by a write to CR3. The remaining six bits are used to provide the D, R/W, and U/S bits from the page table entry. Both the attribute bit and its complement are provided as tag bits, to permit forcing a don't care on reads. The meaning of a pair of these attribute bits is given in the following table:

A	A#	Read	Write
0	0	Miss all	Undefined
0	1	Match 0	Write 0
1	0	Match 1	Write 1
1	1	Match any	Undefined

6.3.5.1.3 FORMAT OF DATA REGISTER

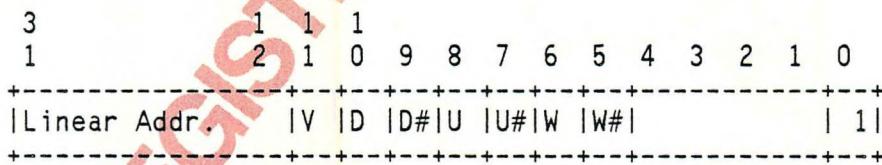
The location and/or value for the Replacement Pointer, along with the RAM data for the new TLB entry are obtained from the PUNIT data test register. A preceding instruction must have loaded the data test register with the intended data for the RAM data before the PUNIT command register is loaded with the Write command (lower bit 0).

The RAM portion of the TLB contains only the upper 20 bits of the physical address which is the output of the page translation process. The format for the PUNIT data register is:



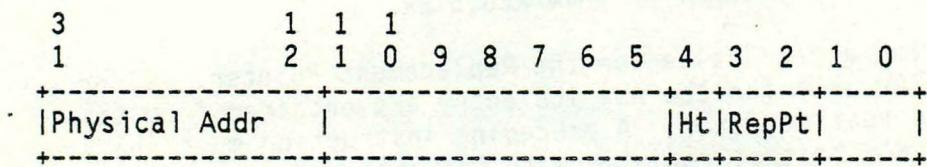
6.3.5.1.4 PERFORM CACHE LOOKUP

This command "reads" the TLB by using the normal lookup mechanism to try to find a match for the TAG presented in the command register. This operation also allows determination of Hit/Miss information. Loading the Read command into the PUNIT command register will initiate a lookup of the TLB, and will store hit and Replacement Pointer back into the command register, and if a hit occurs, store the contents of the RAM part of the TLB into the PUNIT data register. If there is no hit, the data register is undefined. The format of the PUNIT command register for a lookup command is:



After a read command the data register is loaded with a bit indicating whether the access resulted in a hit or not, and if there was a hit, the new value of the Replacement Pointer and the contents of the TLB RAM. After the lookup command, the data register has the following format:

DO NOT REPRODUCE



The Ht bit is the Hit/Miss indication. If the result of the lookup is a miss, Ht=0, and the values in bits 31..12 and 3..2 are undefined. If the result of the lookup is a hit, Ht=1, bits 31..12 will contain the Physical address read from the TLB RAM, and bits 3..2 contain the Replacement Pointer value that would correspond to the entry that was a hit.