

SM16704PB

Feature

- ◆ Built-in power clamp, support input power-supply voltage 5~24V
- ◆ OUTR/ G/ B constant current value defaults to 17mA
- ◆ OUTR/ G/ B power-on state: off
- ◆ OUTR/ G/ B port withstand voltage 26V
- ◆ OUTR/ G/ B output grayscale: 256 level
- ◆ Display data synchronization refresh in the same frame
- ◆ Single-line return-to-zero code SID data protocol
- ◆ Data serial cascade transmission, strong anti-interference ability
- ◆ Signal transfer rate: 800kbps
- ◆ Package: SOP8

Description

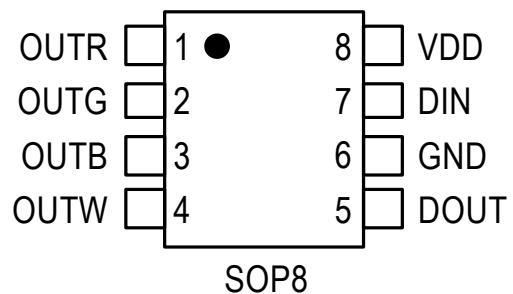
The SM16704PB is a single-line transmission 4-channel output LED driver, which adopts single-line return-to-zero code SID data protocol.

The SM16704PB default output current of the OUT R/G/B/W port is 17mA. The peripheral components of the chip are few, simple and reliable.

Application

- ◆ Indoor LED decorative lighting
- ◆ Architecture exterior/circumstance lighting
- ◆ Point source, perforation
- ◆ Soft light strip, line light

Pin Diagram



Internal Function Diagram

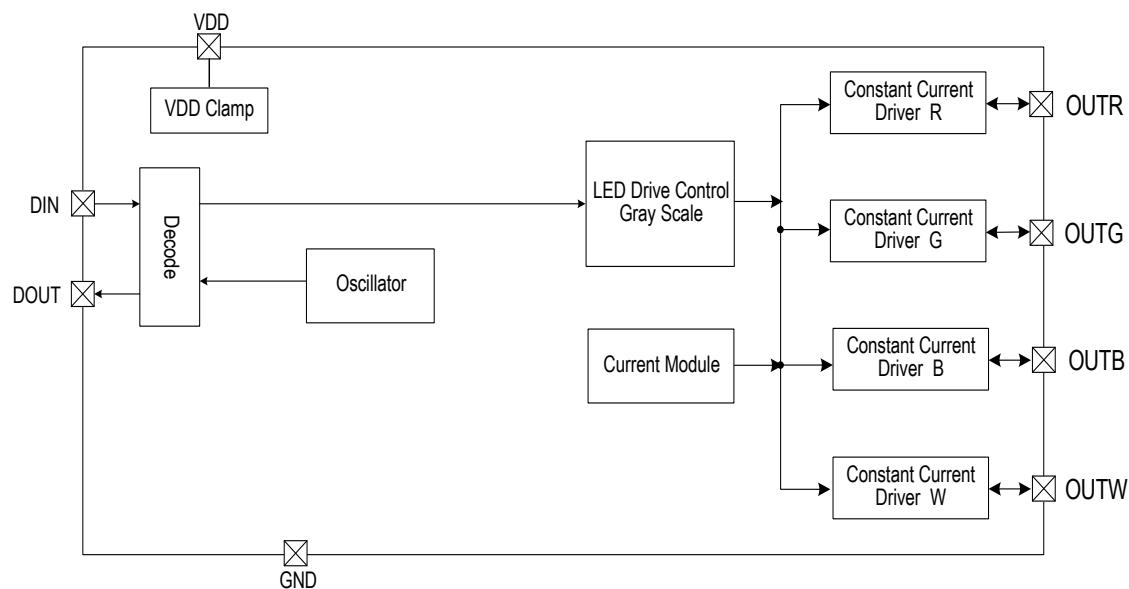


Fig. SM16704PB internal function diagram

Pin Definition

| Pin No. | Pin Name | Description |
|---------|----------|-----------------------------|
| 1 | OUTR | Constant current drive port |
| 2 | OUTG | Constant current drive port |
| 3 | OUTB | Constant current drive port |
| 4 | OUTW | Constant current drive port |
| 5 | DOUT | Cascaded signal output |
| 6 | GND | Ground |
| 7 | DIN | Signal input port |
| 8 | VDD | Power port |

Order Information

| Type | Package | Packing | | Reel Size |
|-----------|---------|----------------|---------------|-----------|
| | | Tube | Tape | |
| SM16704PB | SOP8 | 100000 pcs/box | 4000 pcs/tape | 13 inches |

Absolute Maximum Parameter (Note 1)

Unless otherwise stated, $T_A=25^\circ\text{C}$.

| Symbol | Description | Range | Unit |
|-----------------|--|--------------|------|
| V_{DD} | IC power voltage | -0.4~+5.5 | V |
| V_I | Logic input voltage | -0.4~VDD+0.4 | V |
| BV_{OUT} | R/G/B withstand voltage | 30 | V |
| I_{OUT} | R/G/B Output current | 18 | mA |
| $R_{\theta JA}$ | PN junction to ambient thermal resistance (Note 2) | 130 | °C/W |
| P_D | Power consumption (Note 3) | 0.5 | W |
| T_J | Operating junction temperature range | -40~150 | °C |
| T_{STG} | Storage temperature range | -55~150 | °C |
| V_{ESD} | HBM ESD | 2 | kV |

Note 1: The maximum output power is limited to chip junction temperature, the maximum limit means that the chip can be damaged beyond the scope of the work. The maximum limit value is the work in the limit parameter range, the device function is normal, but it is not completely guaranteed to meet the individual performance indexes.

Note 2: $R_{\theta JA}$ measures the flow of water according to the JEDEC JESD51 thermal measurement standard on the single-layer thermal conductivity test board under $T_A=25^\circ\text{C}$.

Note 3: The maximum power consumption is decreased when temperature rising, this depends on T_{JMAX} , $R_{\theta JA}$ and T_A . Maximum allowable power consumption is $P_D = (T_{JMAX}-T_A)/R_{\theta JA}$ or the lower value of the value given in the limit range.

Electrical Operating Parameter (Note 4, 5)

Unless otherwise stated, $V_{DD} = 5.0\text{V}$, $T_A=25^\circ\text{C}$.

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|------------|---|--|------------------|------|------------------|------|
| V_{DD} | Internal clamp voltage | External power $VCC=12\text{V}$, current limiting resistor $RD = 1\text{k}\Omega$ between VCC and VDD | 4.8 | 5.2 | 5.5 | V |
| | Power voltage | $VCC \leq 5\text{V}$ | 3.0 | - | 5.0 | V |
| IDD | Quiescent current | $VDD = 4.5\text{V}$, I_{OUT} "OFF" | - | 1.2 | - | mA |
| VIH | Input signal threshold voltage | DIN input high level | $0.7 \times VDD$ | - | - | V |
| VIL | | DIN input low level | - | - | $0.3 \times VDD$ | V |
| IOH | DOUT output current | DOUT output is high, serially connect 10Ω resistor to GND | - | -40 | - | mA |
| IOL | DOUT sink current | DOUT output is low, shorted to VDD | - | 40 | - | mA |
| VDS_S | OUT R/G/B/W constant current knee point voltage | $I_{OUT} = 17\text{mA}$ | - | 0.8 | - | V |
| %VS.VDS | OUT R/G/B/W output current variation | $I_{OUT} = 17\text{mA}$, $VDS = 1.0\sim 3.0\text{V}$ | - | 0.5 | - | % |
| %VS.VDD | | $I_{OUT} = 17\text{mA}$, $VDD = 4.5\sim 5.5\text{V}$ | - | 0.5 | - | % |
| %VS.TA | | $I_{OUT} = 17\text{mA}$, $T_A = -40\sim +85^\circ\text{C}$ | - | 5.0 | - | % |
| I_{leak} | OUT R/G/B/W leakage current | $VDS = 26\text{V}$, I_{OUT} "OFF" | - | - | 1 | uA |

Note 4: The electrical operating parameters define the DC parameters of the device within the working range and under test conditions that ensure a specific performance indicator. The specification does not guarantee the accuracy of the parameters that are not given the upper and lower limit values, but the typical values reflect the performance of the device.

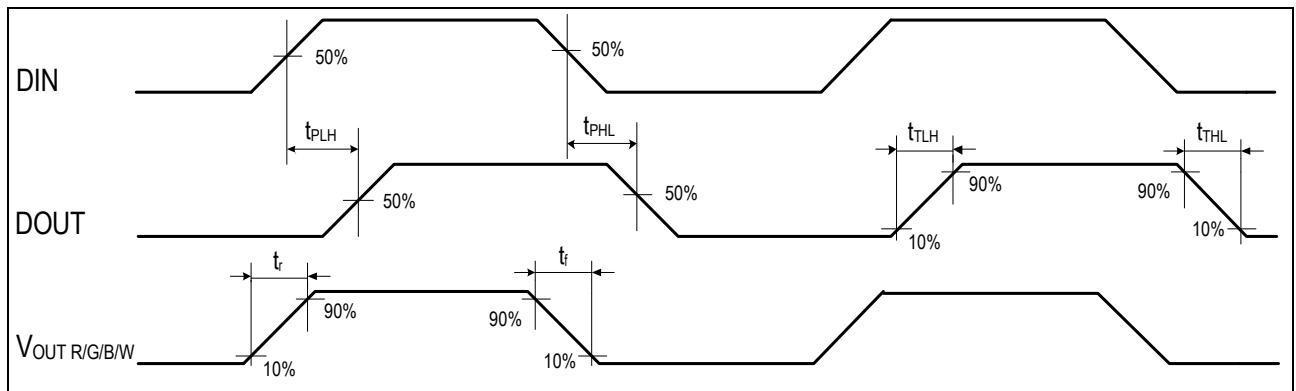
Note 5: The minimum and maximum parameter range of the datasheet is guaranteed by the test, and the typical value is guaranteed by design, test or statistical analysis.

Switching Characteristic

Unless otherwise stated, $T_A=25^\circ\text{C}$.

| Symbol | Description | Measurement Condition | Min. | Typ. | Max. | Unit |
|------------------|---------------------------------------|--|------|------|------|------|
| f_{PWM} | OUT R/G/B output PWM frequency | $I_{\text{OUT}}=17\text{mA}$, OUT port serially connects 200Ω resistor to VDD | - | 1.2 | - | KHz |
| t_{PLH} | Signal transmission delay (Note 6) | DOUT port load capacitance to ground is 30pF , DIN to DOUT signal transmission delay | - | 85 | - | ns |
| t_{PHL} | | | - | 70 | - | ns |
| t_{TLH} | DOUT Conversion time (Note 7) | DOUT port load capacitance to ground is 30pF | - | 18 | - | ns |
| t_{THL} | | | - | 20 | - | ns |
| t_r | OUT R/G/B Conversion time (Note 8) | $I_{\text{OUT R/G/B/W}}=17\text{mA}$, OUT R/G/B port serially connects 200Ω resistor to VDD, load capacitance to ground is 15pF | - | 55 | - | ns |
| t_f | | | - | 75 | - | ns |

Note 6, note 7 and note 8: as shown below



Data Communication Protocol (Note 9, 10)

1、Code Description

The protocol of the SM16704PB adopts single polarity RZ code, LOW level must be contained in each code element. Each code element in the protocol initiates with HIGH level, and the width of the HIGH level time determines 0 code or 1 code.

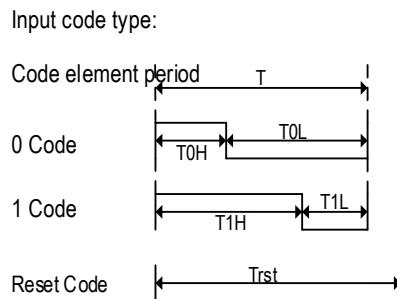


Fig. SM16704PB RZ code data communication protocol diagram

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------|---------------------|------|------|------|------|
| T | Code element period | 1200 | - | - | ns |
| $T0H$ | 0, HIGH level | 200 | 300 | 400 | ns |
| $T0L$ | 0, LOW level | 800 | 900 | - | ns |
| $T1H$ | 1, HIGH level | 800 | 900 | 1000 | ns |
| $T1L$ | 1, LOW level | 200 | 300 | - | ns |
| $Trst$ | Reset, LOW level | 200 | - | - | us |

Note 9: when writing the program, the minimum code period is 1.2us;

Note 10: The high level time of 0 and 1 code should be in accordance with the specified scope of the above table, and the low level time of 0 yards and 1 yard is less than 20us;

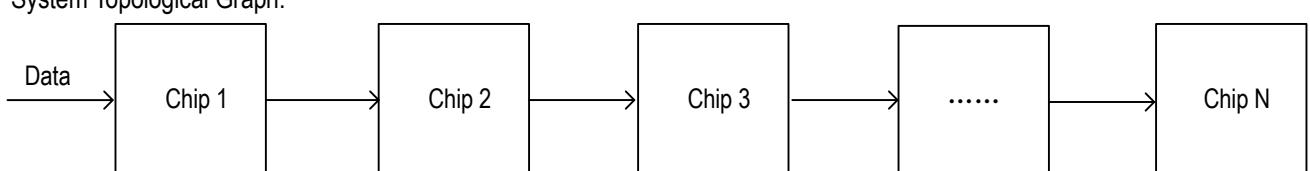
2、Protocol Data Format:

$Trst +$ First chip 32bits data +Second chip 32bits data +.....+ The N chip 32bits data + $Trst$

- 32bits gray scale data structure: High levels first, sent by the order of RGB

| | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | G7 | G6 | G5 | G4 | G3 | G2 | G1 | G0 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Bit31.....bit0 | | | | | | | | | | | | | | | | | | | | | | | |

● System Topological Graph:



- Input Data Stream of every chip (3 chips as an example):

| | | | | | | | |
|--------|------|------------------------|------------------------|------------------------|------|--|--|
| Chip 1 | Trst | 1st Set of 32bits Data | 2nd Set of 32bits Data | 3rd Set of 32bits Data | Trst | | |
| Chip 2 | Trst | | 2nd Set of 32bits Data | 3rd Set of 32bits Data | Trst | | |
| Chip 3 | Trst | | | 3rd Set of 32bits Data | Trst | | |

Constant Current characteristics

After reaching the constant current knee point, the SM16704PB output current is not affected by the OUT port voltage V_{DS} .

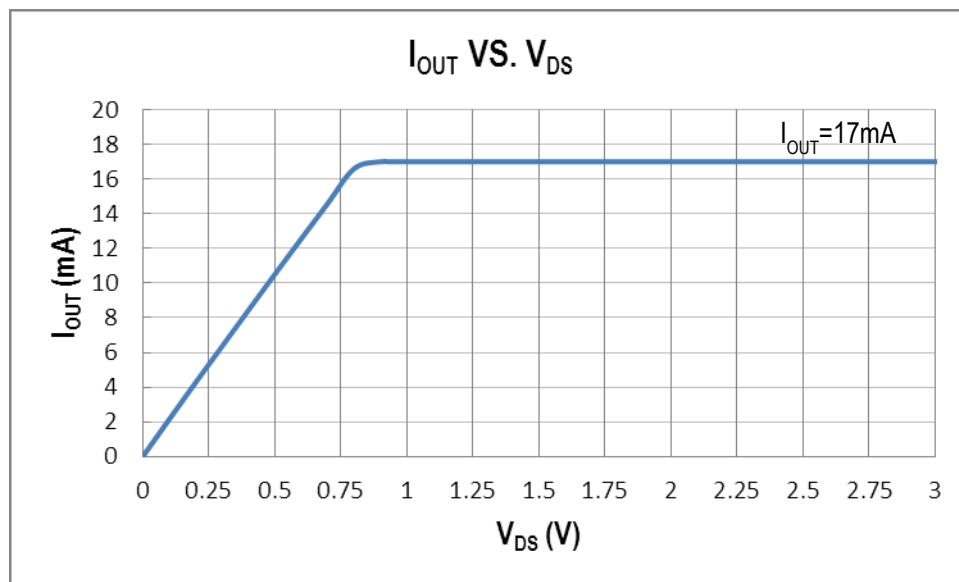


Fig. SM16704PB I_{OUT} vs. OUT Port Voltage V_{DS} Curve

Typical Application

Typical application circuit diagram of SM16704PB RGB scheme

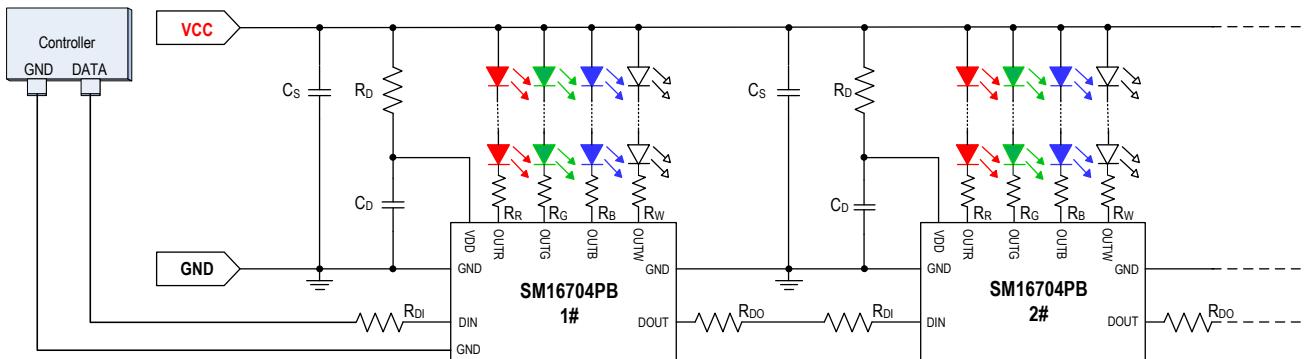


Fig. SM16704PB typical application diagram

SM16704PB typical application circuit parameters include external input voltage VCC, system power supply filter capacitor C_S , chip current limiting resistor R_D , VDD voltage regulator capacitor C_D and OUTR/G/B LED voltage divider resistor R_R , R_G , R_B , DAI signal input port cascades resistor R_{DI} and DAO signal output port cascades resistor R_{DO} .

(1) VCC is the external input voltage, and R_D is the current limiting resistor, which is used to limit the operating current of the internal voltage regulator module when the chip voltage regulator function is turned on. Chip operating voltage, $V_{DD} = VCC - I_{DD} \times R_D$, where I_{DD} is the chip quiescent current, R_D resistance must ensure $VDD > 3V$. The larger the R_D resistance is, the lower the system power consumption is, but the system anti-interference ability is weak; the smaller the R_D resistance is, the larger the system power consumption is, the higher the operating temperature is. The design needs to properly select the resistor R_D according to the system application environment. The design reference values of different input power supply voltages VCC and current limiting resistor R_D are as follows:

| VCC(V) | 5 | 6 | 9 | 12 | 15 | 18 | 24 |
|---------------|----|-----|-----|----|------|----|----|
| $R_D(\Omega)$ | 33 | 100 | 470 | 1K | 1.5K | 2K | 3K |

(2) C_S is the capacitance of the system power to ground, used to reduce power fluctuations, can choose $0.1\mu F \sim 10\mu F$ capacitor according to the actual load of the system, when the load is large, it is recommended to choose electrolytic capacitor;

(3) The C_D is a chip filter capacitor, which is used to stabilize the VDD voltage of the chip to ensure the normal operation of the chip. The C_D is recommended to be a $100nF$ capacitor;

(4) R_D is a DAI signal input port protection resistor to prevent damage to the signal port caused by hot plugging, reverse polarity of the power supply and reverse connection of the signal line.

(5) R_{DO} is a DAO signal output port protection resistor to prevent damage to the signal port caused by hot plugging, reverse polarity of the power supply and reverse connection of the signal line.

(6) R_R , R_G , and R_B are voltage divider resistors of the OUTR/G/B port, which are used to reduce the OUTR/G/B port voltage and reduce the power consumption of the chip. The calculation formula is

$$R_R / R_G / R_B / R_W (\Omega) = \frac{VCC - V_{DS} - N \times V_{LED}}{I_{OUT}}$$

Where VCC is the external input voltage, V_{LED} is the voltage drop of the LED lamp, I_{OUT} is the port output current, and V_{DS} is the

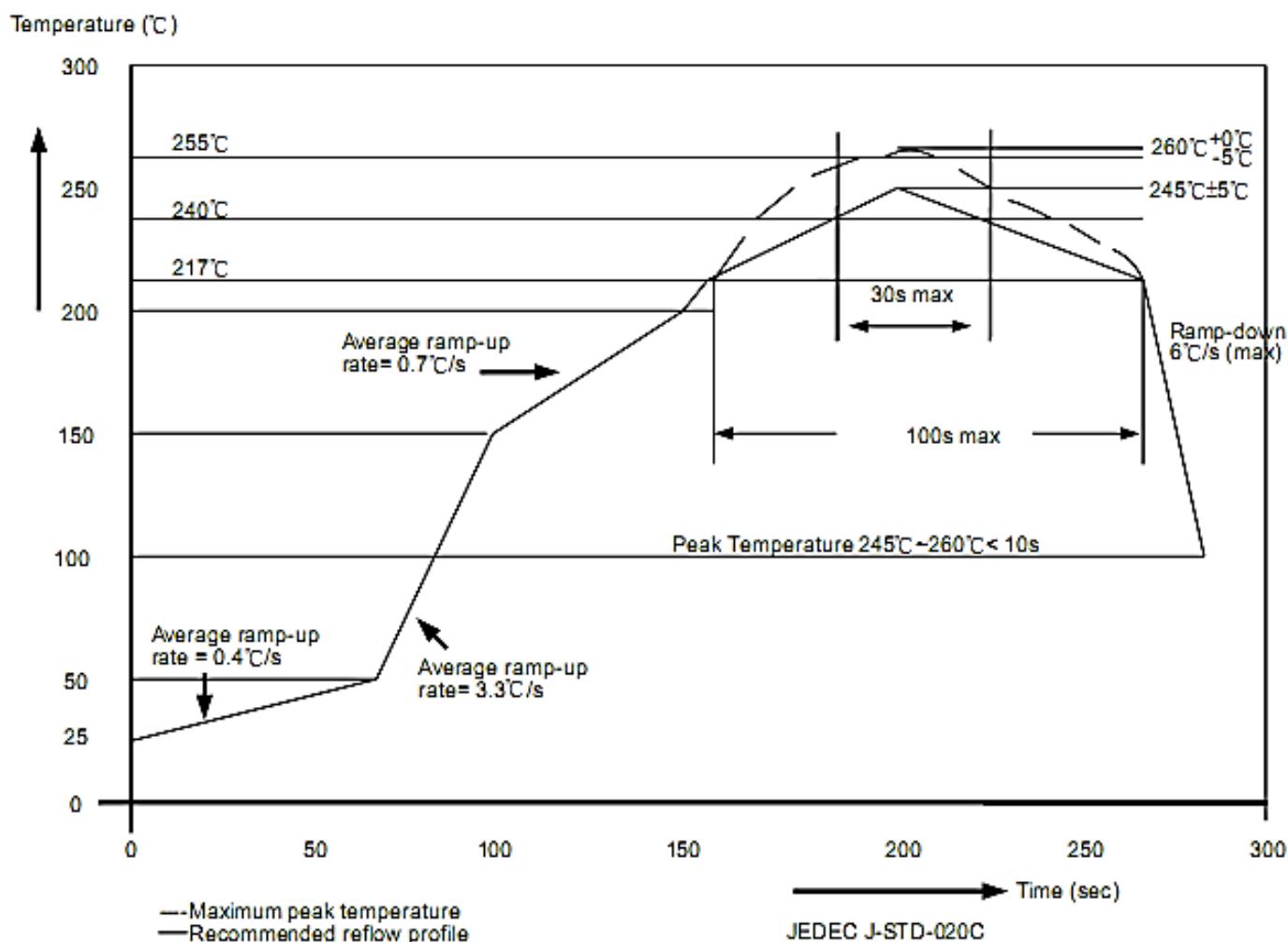
OUTR/G/B port voltage. In practical applications, the value of V_{DS} should be higher than the constant current inflection point voltage, and the chip will generate less power loss. The actual application is subject to the standard. The reference value of the voltage drop V_{LED} of different colors is as follows: the red lamp voltage drop is about 2.0~2.2V, and the green, blue and white lamp voltage drop is about 3.0~3.2V. Please refer to the actual lamp bead specification.

In a typical application, depending on the input voltage and the number of different beads, it is recommended that the values of the parameters be as follows:

| VCC(V) | OUT port serial connection | $R_D(\Omega)$ | $C_D(nF)$ | $R_{DI}(\Omega)$ | $R_{DO}(\Omega)$ | $R_R(\Omega)$ | $R_G(\Omega)$ | $R_B(\Omega)$ | $R_W(\Omega)$ |
|--------|----------------------------|---------------|-----------|------------------|------------------|---------------|---------------|---------------|---------------|
| 5 | 1 | 33 | 100 | - | - | - | - | - | - |
| 12 | 3 | 1K | 100 | 51 | 150 | 150 | - | - | - |
| 24 | 6 | 3K | 100 | 100 | 300 | 510 | 150 | 150 | 150 |

Encapsulation Soldering Process

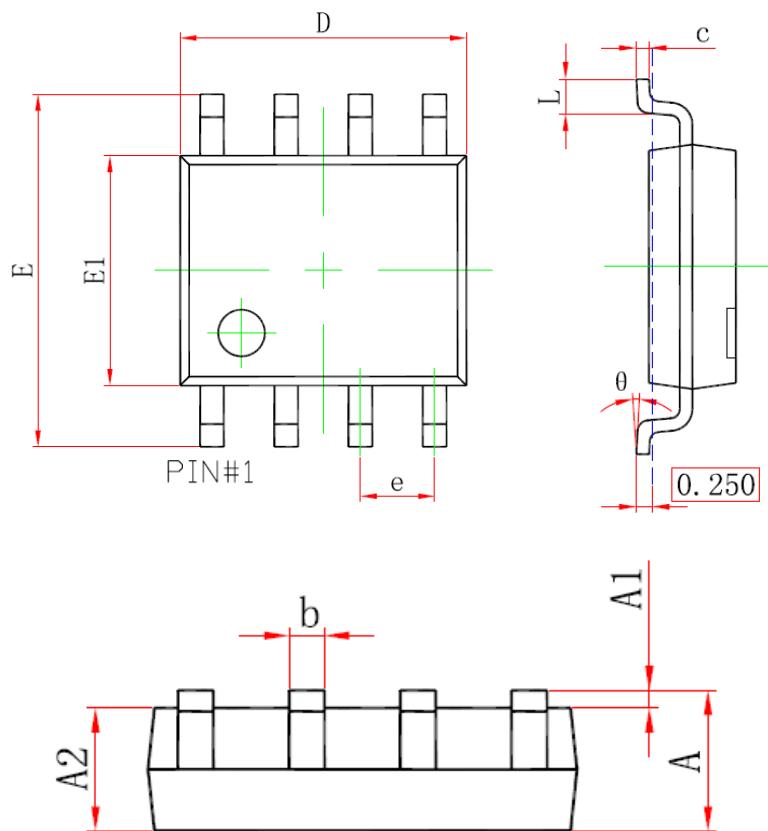
Semiconductors of Sunmoon follow the European RoHs standard, solder temperature in encapsulation soldering process follows J-STD-020 standard.



| Encapsulation Thickness | Volume mm ³ < 350 | Volume mm ³ : 350~2000 | Volume mm ³ ≥ 2000 |
|-------------------------|------------------------------|-----------------------------------|-------------------------------|
| <1.6mm | 260+0°C | 260+0°C | 260+0°C |
| 1.6mm~2.5mm | 260+0°C | 250+0°C | 245+0°C |
| ≥2.5mm | 250+0°C | 245+0°C | 245+0°C |

Package

SOP8



| Symbol | Min(mm) | Max(mm) |
|--------|-----------|---------|
| A | 1.25 | 1.95 |
| A1 | - | 0.25 |
| A2 | 1.25 | 1.75 |
| b | 0.25 | 0.7 |
| c | 0.1 | 0.35 |
| D | 4.6 | 5.3 |
| e | 1.27(BSC) | |
| E | 5.7 | 6.4 |
| E1 | 3.7 | 4.2 |
| L | 0.2 | 1.5 |
| θ | 0° | 10° |

Declaration

Sunmoon owns the right of, alteration, correction, modification, improvement and termination about our products, files and services. To the rights above, recommend customers to contact our business representative for the latest product information before purchasing. All technical applications need to be designed in strict accordance with the latest product specifications.

Sunmoon electronic products cannot be used in medical or military areas without our legal authorization. If users get injured or life threat even to dead, we are not responsible for any damage.

All verbal content, pictures and trademark are intellectual property of Sunmoon. Any individuals and organizations cannot use, correct, redo, public, remake, spread, publish or vend it to damage the legitimate rights and interests of Sunmoon, For the relevant infringement, we will immediately start a full legal process, held accountable.