



HC32L110 series
32 -bit ARM® Cortex®-M0+ microcontroller
data sheet

Product Features

- ÿ 32MHz Cortex-M0+ 32-bit CPU platform
 - 1 low-power 16-bit timer/counter
- ÿ HC32L110 series has a flexible power management system,
 - Low power performance
 - 0.5µA @ 3V deep sleep mode: all clocks off, power-on reset valid, IO status maintained, IO interrupt valid,
 - All registers, RAM and CPU data save status
 - power consumption when
 - 1.0µA @3V deep sleep mode + RTC operation – 6µA@32.768kHz low speed operation mode: CPU and external
 - Set the module to run, run the program from the flash
 - 20µA/MHz@3V@16MHz Sleep mode: CPU stop
 - stop working, peripheral modules are running, main clock is running
 - 120µA/MHz@3V@16MHz Working mode: CPU and peripheral modules to run programs from Flash
 - 4µs ultra-low power wake-up time, making mode switching more flexible
 - Lively and efficiently, the system response is more agile
 - The above characteristics are typical values at room temperature, the specific electrical characteristics, Power consumption characteristics refer to the Electrical Characteristics chapter
 - ÿ 16K/32K bytes Flash memory with erase and write protection
 - ÿ 2K/4K bytes RAM memory with parity, enhanced
 - system stability
 - ÿ General purpose I/O pins (16IO/20pin, 12IO/16pin)
 - ÿ Clock, crystal oscillator
 - External high-speed crystal oscillator 4 ~ 32MHz
 - External low-speed crystal oscillator 32.768KHz
 - Internal high-speed clock 4/8/16/22.12/24MHz
 - Internal low speed clock 32.8/38.4KHz
 - Hardware supports internal and external clock calibration and monitoring
 - ÿ Timer/Counter
 - 3 general purpose 16-bit timers/counters
 - 3 high-performance 16-bit timers/counters with PWM support
 - Complementary, dead-time protection function
 - ÿ 1 programmable 16-bit timer/counter with capture support
 - ÿ Compare, PWM output
 - ÿ 1 20-bit programmable counting watchdog circuit, built-in dedicated Ultra-low power RC-OSC provides WDT counting
 - ÿ Communication interface
 - UART0-UART1 standard communication interface
 - LPUART supports ultra-low-power communication using low-speed clocks
 - ÿ Buzzer frequency generator, supports complementary output
 - ÿ Hardware perpetual calendar RTC module
 - ÿ Hardware CRC-16 Module
 - ÿ Unique 10-byte ID number
 - ÿ 12-bit 1Msps sampling high-speed high-precision SARADC, internal Placed on amp, can measure external weak signal
 - ÿ 2 voltages with integrated 6-bit DAC and programmable reference input
 - ÿ Comparator VC
 - ÿ Integrated low voltage detector LVD, configurable 16-level comparator
 - ÿ Embedded debugging solution, providing full-featured real-time debugging
 - ÿ level to monitor port voltage as well as supply voltage
 - ÿ Working temperature: -40 ~ 85ÿ
 - ÿ Working voltage: 1.8 ~ 5.5V
 - ÿ Package: QFN20, TSSOP20, TSSOP16, CSP16
 - ÿ Supported models

HC32L110C6UA	HC32L110C6PA
HC32L110C4UA	HC32L110C4PA
HC32L110B6PA	HC32L110B4PA
HC32L110B6YA	



statement

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content

Product Features.....	1
Statement	2
Table of Contents	3
1. Introduction	4
Lineup	14
Configuration...	17
function description	19
5. Block Diagram	23
6. Memory map.....	24
Electrical Characteristics	26
7.1 Test Conditions	26
Minimum and maximum values	26
7.1.2. Typical values	26
Absolute Maximum Ratings.....	27
Operating Conditions	29
7.3.1. Generic work condition.....	29
Operating conditions at power-up and power-down.....	29
7.3.3. Embedded Reset and LVD Module Features	30
7.3.4. Built-in reference voltage	32
7.3.5. Operating current characteristics	32
7.3.6. Wake-up time from low power mode	34
External Clock Source Characteristics	35
7.3.8. Internal Clock Source Characteristics	40
7.3.9 . Memory Features	41
EFT characteristics	41
ESD Characteristics	42
7.3.12. Port Features	42
7.3.13. RESETB pin characteristics	45
7.3.14. ADC Characteristics	45
VC characteristics.....	48
TIM timer features.....	49
Communication interface	51
Typical application circuit diagram	55
Package Information	56
Package Dimensions	56
Diagram	60
Instructions	64
Package Thermal Resistivity	65
10. Ordering Information	66
11. Version History & Contact	67



1. Introduction

The HC32L110 series is an ultra-low power, Low Pin Count, wide voltage designed to extend battery life in portable measurement systems

working range of the MCU. Integrated 12-bit 1Msps high-precision SARADC and integrated comparator, multi-channel UART, SPI, I²C, etc.

Rich communication peripherals, featuring high integration, high anti-interference, high reliability and ultra-low power consumption. The core of this product adopts Cortex-M0+

The kernel, with mature Keil & IAR debugging and development software, supports C language, assembly language, and assembly instructions.

Typical application of ultra-low power **MCU**

- ÿ Sensor applications, IoT applications;
- ÿ Intelligent transportation, smart city, smart home;
- ÿ Smart sensor applications such as fire alarm probes, smart door locks, and wireless monitoring;
- ÿ Various portable devices that are battery-powered and power-hungry.



32-bit CORTEX M0+ kernel

The ARM® Cortex®-M0+ processor is derived from Cortex-M0 and includes a 32-bit RISC processor with a computing power of 0.95

Dhrystone MIPS/MHz. Several new designs have also been added to improve debug and trace capabilities, reduce the number of cycles per instruction (IPC)

It also incorporates energy-saving and consumption-reducing technologies. Full Cortex-M0+ processor support integrated

Keil & IAR debugger.

The Cortex-M0+ includes a hardware debug circuit that supports a 2-pin SWD debug interface.

ARM Cortex-M0+ Features:

Instruction	Thumb / Thumb-2
Set Pipeline	2-stage pipeline
Performance	2.46 CoreMark/MHz
Efficiency	0.95 DMIPS/MHz in Dhrystone
Performance	32 fast interrupts
Efficiency Interrupt Priority	Configurable 4-level Interrupt Priority
Enhanced instruction	Single-cycle 32-bit multiplier
debugging	Serial-wire debug port, supports 4 hard break points and 2 watch points

16K/32K Byte Flash

Built-in fully integrated Flash controller, no external high voltage input is required, and the high voltage is generated by the fully built-in circuit for programming. Support ISP, IAP, ICP function can.

2K/4K Byte RAM

According to the different ultra-low power consumption modes selected by the customer, the RAM data will be retained. Comes with hardware parity bit, in case the data is accidentally broken If it is bad, when the data is read, the hardware circuit will be interrupted immediately to ensure the reliability of the system.

clock system

A high-precision internal clock RCH with a configurable frequency of 4~24MHz. From low power mode to active mode at 16MHz configuration

The wake-up time is 4µs, and the frequency deviation within the full voltage and full temperature range is small, and an expensive high-frequency crystal can not be connected.

An external crystal oscillator XTH with a frequency of 4~32MHz.

An external crystal oscillator XTL with a frequency of 32.768KHz mainly provides the RTC real-time clock.

An internal clock RCL with a frequency of 32.8/38.4KHz.



Operating mode

- 1) Operation mode (Active Mode): CPU is running, peripheral function modules are running.
- 2) Sleep Mode: CPU stops running and peripheral function modules run.
- 3) Deep sleep mode: CPU stops running, high-speed clock stops running, and low-power function modules run.

real time clock RTC

RTC (Real Time Counter) is a register that supports BCD data. It uses a 32.768Hz crystal oscillator as its clock, which can achieve

Perpetual calendar function, the interruption period can be configured as year/month/day/hour/minute/second. 24/12 hour time mode with automatic hardware correction for leap years. have

Accuracy compensation function, the highest accuracy is 0.96ppm. Accuracy compensation can be performed using an internal temperature sensor or an external temperature sensor, which can

Adjust year/month/day/hour/minute/second with software +1/-1, the minimum adjustable precision is 1 second.

The RTC calendar recorder used to indicate time and date does not clear the retained value when the MCU is reset by external factors and is required

The best choice for measuring equipment meter with permanent high precision real time clock.

Port Controller GPIO

Up to 16 GPIO ports can be provided, some of which are multiplexed with analog ports. Each port is controlled by independent control register bits

control. It supports edge-triggered interrupts and level-triggered interrupts, which can wake up the MCU to the working mode from various ultra-low power consumption modes. support

Push-Pull CMOS push-pull output, Open-Drain open-drain output. Built-in pull-up resistor, pull-down resistor, with Schmitt trigger input

filter function. The output drive capability is configurable, with a maximum current drive capability of 12mA. 16 general-purpose IOs can support external asynchronous

break.

Interrupt Controller NVIC

The Cortex-M0+ processor has a built-in Nested Vectored Interrupt Controller (NVIC) that supports up to 32 interrupt request (IRQ) inputs; there are four priority levels.

Each interrupt priority level can handle complex logic, enabling real-time control and interrupt handling.

32 interrupt entry vector addresses are:

interrupt vector number	interrupt source
[0]	GPIO_P0
[1]	GPIO_P1
[2]	GPIO_P2
[3]	GPIO_P3
[4]	-
[5]	-
[6]	UART0
[7]	UART1
[8]	LPUART
[9]	-
[10]	SPI
[11]	-
[12]	I2C_
[13]	-
[14]	Timer0
[15]	Timer1
[16]	Timer2
[17]	LPTimer
[18]	Timer4
[19]	Timer5
[20]	Timer6
[21]	PCA
[22]	WDT
[twenty three]	RTC
[twenty four]	ADC
[25]	-
[26]	VC0
[27]	VC1
[28]	LVD
[29]	-
[30]	RAM FLASH fault
[31]	Clock trim



reset controller RESET

This product has 7 reset signal sources, each reset signal can make the CPU run again, most registers will be reset again,

The program counter PC is reset to point to 00000000.

	reset source
[0]	Power-on power-down reset POR BOR
[1]	External Reset Pin reset
[2]	WDT reset
[3]	PCA reset
[4]	Cortex-M0+ LOCKUP hardware reset
[5]	Cortex-M0+ SYSRESETREQ software reset
[6]	LVD reset

timer TIM

		Bit width prescaler	Counting direction	PWM capture	complementary output	
Basic timer Timer0		16/32 32/64/256	count up no no no			
	Timer1	16/32 32/64/256	count up no no no			
	Timer2	16/32 32/64/256	count up no no no			
Low Power Timer LPTimer	16 Programmable	without	count up no no no			
Count Array PCA Advanced Timer Timer	4 16	2/4/8/16/32	count up 5 count up/	5	without	
		16 64/256/1024	count down/ count up and down	2	2	1
	Timer5	16 64/256/1024	count up/ count down/ count up and down	2	2	1
	Timer6	16 64/256/1024	count up/ count down/ count up and down	2	2	1

The basic timer includes three timers Timer0/1/2. Timer0/1/2 function exactly the same. Timer0/1/2 are synchronous timers/counters that can be

It can be used as a 16-bit timer/counter with automatic reload function, or as a 32-bit timer/counter without reload function. Timer0/1/2

External pulses can be counted or system timing can be implemented.

The low-power timer is an asynchronous 16-bit timer/counter, which can still pass the internal low-speed RC or external low-speed after the system clock is turned off.

Crystal oscillator timing/counting. Wake up the system in low power mode by interrupt.



PCA (Programmable Counter Array) supports up to five 16-bit capture/compare modules. The timer/meter

The counter can be used as a general-purpose clock count/event counter with capture/compare functions. Each module of PCA can be programmed independently

program to provide input capture, output compare or pulse width modulation. In addition module 4 has an additional watchdog timer mode.

The advanced timer is a Timer4/5/6 that contains three timers. Timer4/5/6 high-performance counter with the same function, can be used for count generation

Different forms of clock waveforms, one timer can generate a complementary pair of PWM or two independent PWM outputs, which can be captured

External input for pulse width or period measurement.

The basic functions and features of the advanced timer are shown in the table:

Waveform mode	sawtooth wave, triangular wave
basic skills	ÿ Up, down counting direction
	Software synchronization ÿ Hardware
	synchronization ÿ Buffer function
	Quadrature code count ÿ General
	PWM output Interrupt Short Circuit
	Monitor Interrupt
interrupt type	

Watchdog WDT

WDT (Watch Dog Timer) is a configurable 20-bit timer that provides reset in case of MCU abnormality; built-in 10K

The low-speed clock input is used as the counter clock. In debug mode, you can choose to pause or continue running; the WDT can only be restarted by writing a specific sequence.

Universal Synchronous Asynchronous Transceiver **UART0~UART1, LPUART**

2-way Universal Asynchronous Receiver/Transmitter

General UART basic functions:

ÿ Half-duplex and full-duplex transmission

ÿ 8/9-Bit transmission data length

ÿ Hardware parity

ÿ Support 1 Bit stop bit



ÿ Four different transmission modes

ÿ Multi-machine communication

ÿ Hardware address recognition

1-way Asynchronous Receiver (Low Power Universal Asynchronous Receiver/Transmitter) that can work in low power mode

LPUART basic functions:

ÿ Transmission clock SCLK (SCLK can choose XTL, RCL and PCLK)

ÿ Send and receive data in system low power mode

ÿ Half-duplex and full-duplex transmission

ÿ 8/9-Bit transmission data length

ÿ Hardware parity

ÿ Support 1 Bit stop bit

ÿ Four different transmission modes

ÿ Multi-machine communication

ÿ Hardware address recognition

Serial Peripheral Interface **SPI**

1-way synchronous serial interface (Serial Peripheral Interface), support master-slave mode.

SPI basic features:

ÿ Can be configured as master or slave through programming

ÿ Four-wire transmission mode, full duplex communication

ÿ 7 kinds of baud rate can be configured in host mode

ÿ The maximum frequency division factor of host mode is PCLK/2, and the maximum communication rate is 16M bps

ÿ The maximum frequency division factor of slave mode is PCLK/8, and the maximum communication rate is 4M bps

ÿ Configurable serial clock polarity and phase

ÿ Support interrupt

ÿ 8-bit data transmission, the high-order bits are transmitted first and then the low-order bits



I2C bus _

1 channel I2C, using serial synchronous clock, can realize data transmission between devices at different rates.

I2C basic features:

- ÿ Support host send/receive and slave send/receive four working modes
- ÿ Support standard (100Kbps) / fast (400Kbps) / high speed (1Mbps) three working rates
- ÿ Support 7-bit addressing function
- ÿ Support noise filtering function
- ÿ Support broadcast address
- ÿ Support interrupt status query function

Buzzer _

3 basic timers and 1 low-power timer function multiplexed output provides programmable drive frequency for the Buzzer. The buzzer port provides

For 12mA sink current, complementary output, no need for additional transistors.

Clock calibration circuit module CLKTRIM

Built-in clock calibration circuit, which can calibrate the internal RC clock through an external precise crystal oscillator clock, or use the internal RC clock to verify

Whether the external crystal clock is working properly.

Basic features of clock calibration:

- ÿ Calibration mode
- ÿ Monitoring mode
- ÿ 32-bit reference clock counter can be loaded with initial value
- ÿ 32-bit clock counter to be calibrated with configurable overflow value
- ÿ 6 reference clock sources
- ÿ 4 clock sources to be calibrated
- ÿ Support interrupt mode

Device Electronic Signature

Each chip has a unique 10-byte device identification number before leaving the factory, including wafer lot information and chip coordinate information. ID address

0x0010_0E74-0x0010_0E7F



Cyclic Redundancy Check CRC

Complies with the polynomial $F(x) = X^{16} + X^{12} + X^5 + 1$ given in ISO/IEC13239

$X^{16} + X^{12} + X^5 + 1$.

The analog-to-digital converter ADC

is a 12-bit successive approximation analog-to-digital converter with monotonic and no missing codes. The sampling rate reaches 1Msps when operating under the 24MHz ADC clock. refer to

The voltage can be selected from on-chip precision voltage (1.5V or 2.5V) or from external input or power supply voltage. 12 input channels, including 9 external

Pin input, 1 channel internal temperature sensor voltage, 1 channel 1/3 power supply voltage, 1 channel built-in BGR 1.2V voltage. Built-in configurable input

into a signal amplifier to detect weak signals.

SAR ADC basic characteristics:

ÿ 12-bit conversion precision;

ÿ 1Msps conversion speed;

ÿ 12 input channels, including 8 external pin inputs, 1 internal temperature sensor voltage, 1 VCC/3 voltage, 1 built-in

BGR 1.2V voltage;

ÿ 4 kinds of reference sources: VCC voltage, ExRef pin, built-in 1.5V reference voltage, built-in 2.5V reference voltage;

ÿ ADC voltage input range: 0~Vref;

ÿ 3 conversion modes: single conversion, sequential scan continuous conversion, continuous conversion accumulation;

ÿ Input channel voltage threshold monitoring;

ÿ The conversion rate of ADC can be configured by software;

ÿ Built-in signal amplifier, which can convert high-impedance signals;

ÿ Supports on-chip peripherals to automatically trigger ADC conversion, effectively reducing chip power consumption and improving real-time conversion.

Analog voltage comparator VC

Chip pin voltage monitoring/comparison circuit. 8 configurable positive/negative external input channels; 5 internal input channels, including 1 internal temperature

sensor voltage, 1 channel built-in BGR 2.5V reference voltage, 1 channel built-in BGR 1.2V voltage, 1 channel 64-step resistor divider. VC

Output for basic timer, low power timer, advanced timer and programmable count array PCA capture, gating, external count clock

use. Asynchronous interrupts can be generated based on rising/falling edges to wake up the MCU from low power modes. Configurable software anti-shake function.

Low Voltage Detector LVD

Detect chip power supply voltage or chip pin voltage. 16 levels of voltage monitoring values (1.8 ~ 3.3V). Can be generated from rising/falling edges



Asynchronous interrupt or reset. With hardware hysteresis circuit and configurable software anti-shake function.

LVD basic characteristics:

- ÿ 4 monitoring sources, VCC, PC13, PB08, PB07;

- ÿ 16-step threshold voltage, 1.8~3.3V optional;

- ÿ 8 trigger conditions, high level, rising edge, falling edge combination;

- ÿ 2 trigger results, reset and interrupt;

- ÿ 8th-order filter configuration to prevent false triggering;

- ÿ With hysteresis function, strong anti-interference.

Embedded debugging system

Embedded debugging solution, providing full-featured real-time debugger, with standard mature Keil/IAR and other debugging development software. Support 4

hard breakpoints and multiple soft breakpoints.

programming mode

One programming mode is supported: offline programming.

Two programming protocols are supported: ISP protocol, SWD protocol.

ISP protocol programming interface: P35, P36 or P27, P31.

SWD protocol programming interface: P27, P31.

When the chip receives the **ISP** programming command within the time window of several milliseconds after the reset is completed , the chip works in the ISP programming mode, and can use the programming

program the FLASH with the controller.

When the chip does not receive the **ISP** programming command within the time window of several milliseconds after the reset is completed , the chip works in user mode, and the chip executes

Program code in FLASH.

Notice:

- It is recommended to reserve P35 and P36 as the **ISP** programming interface; if you need to use P27 and P31 as the **ISP** programming interface, please refer to **PCN**:

[PCN20200304-1_HC32L110HC32F003HC32F005](#) improves the burning speed.

High security

Encrypted embedded debugging solution that provides a full-featured real-time debugger.



2. Product Lineup

product name

HC32 L 1106 UA

Huada Semiconductor

CPU bit width

32: 32bit

product type

L: Ultra low power consumption

CPU type

1: Cortex-M0+

Performance ID 1:

Basic

Function configuration ID 0:

Configuration 1

Number of pins

C: 20Pin

B: 16Pin

FLASH capacity

6: 32KB

4: 16KB

Package type

P: SOP

U: QFN

Y: CSP

Ambient temperature range

A: -40-85°C, industrial grade



Function

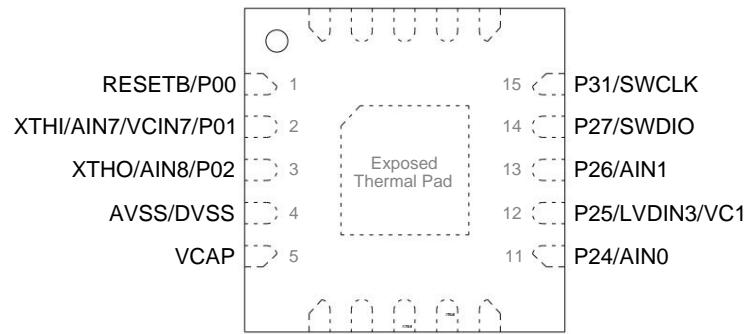
product name		HC32L110C6UA / HC32L110C6PA HC32L110C4UA / HC32L110C4PA	HC32L110B4PA / HC32L110B6PA HC32L110B6YA
Number of pins		20	16
Number of GPIO pins		16	12
CPU	kernel	Cortex M0+	
	frequency	32MHz	
Supply voltage range		1.8~5.5V	
Single/Dual Power		single power supply	
temperature range		-40 ~ 85°C	
Debug function		SWD debug interface	
unique identifier		support	
Communication Interface		UART0/1	LPUART
		SPI I2C	
timer		General purpose timer TIM0/1/2	Low Power Timer LPTIM
		Advanced Timer TIM4/5/6	
12-bit A/D converter		9ch	6ch
Analog Voltage Comparator		VC0/1	
Real Time Clock		1	
port interrupt		16	12
Low voltage detection reset/interrupt		1	
clock	Internal high-speed oscillator	RCH 4/8/16/22.12/24MHz	
	Internal low speed oscillator	RCL 32.8/38.4KHz	
	External high-speed crystal oscillator	4~32MHz	
	External low-speed crystal oscillator	32.768kHz	
buzzer		Max 4ch	
FLASH security protection		support	



product name	HC32L110C6UA / HC32L110C6PA HC32L110C4UA / HC32L110C4PA	HC32L110B4PA / HC32L110B6PA HC32L110B6YA
RAM parity	support	

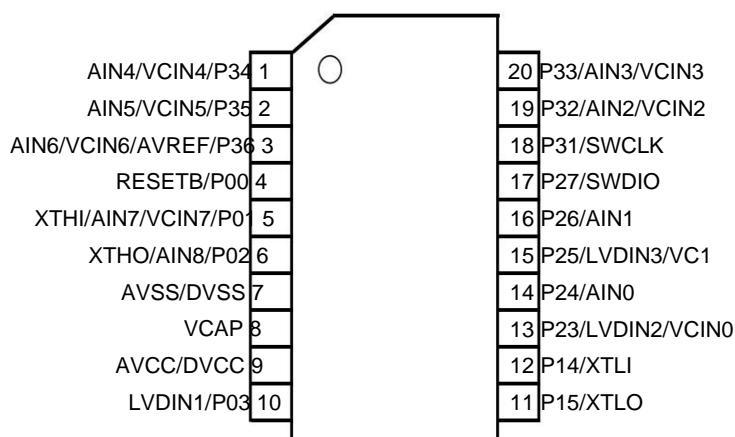
3. Pin Configuration

HC32L110C6UA / HC32L110C4UA

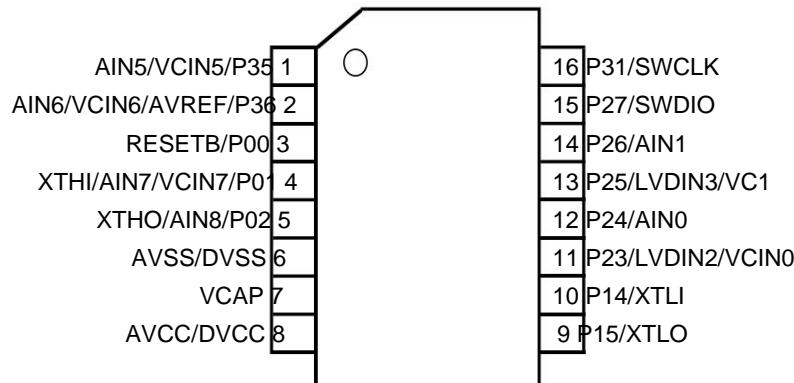


Note: Exposed Thermal Pad needs to be connected to DVSS.

HC32L110C6PA / HC32L110C4PA



HC32L110B4PA / HC32L110B6PA



Note: In the application, it is necessary to set the package as input and enable the pull-up to the IO pin that is not led out of the **TSSOP20**.

HC32L110B6YA

CSP16 TOP VIEW



Note:

- In the application, it is necessary to set the package as input and enable pull-up to the IO pin that is not drawn out of the **TSSOP20**.

- **A1** is Pin 1.

4. Pin function description

Pin No.	Pin No.	Pin No.	Pin No.	Pin Name Pin Type		Description
QFN20 TSSOP20 TSSOP16 CSP16						
1	4	3	B2	RESETB P00	RESETB	Reset input port, active low, chip reset
					GPIO	P00 digital input
2	5	4	B3	P01	GPIO	P01 General purpose digital input/output pin
					UART0_RXD	UART0 RXD
					I2C_SDA _	I2C data
					UART1_TXD	UART1 TXD
					TIM0_TOG	Timer0 toggle output
					TIM5_CHB	Timer5 capture input/compare output B
					SPI_SCK	SPI clock
					TIM2_EXT	Timer2 external clock
					AIN7/VC7	analog input
					XTHI	External XTH crystal clock input
3	6	5	A4	P02	GPIO	P02 General purpose digital input/output pin
					UART0_TXD	UART0 TXD
					I2C_SCL _	I2C clock
					UART1_RXD	UART1 RXD
					TIM0_TOGN	Timer0 toggles the inverted output
					TIM6_CHA	Timer6 capture input/compare output A
					SPI_CS	SPI CS
					TIM2_GATE	Timer2 gate
					AIN8	analog input
					XTHO	External XTH crystal clock output
4	7	6	B4	AVSS/DV SS	GND	chip ground
5	8	7	C3	Vcap	Power	LDO core supply output (internal circuit only use, connect a 4.7uF capacitor)
6	9	8	C4	AVCC/DV CC	Power	Chip power 1.8v~5.5v
7	10	Note	Note	P03	GPIO	P03 General purpose digital input/output pin
					PCA_CH3	PCA capture input/compare output 3
					SPI_CS	SPI CS
					TIM6_CHB	Timer6 capture input/compare output B
					LPTIM_EXT	LPTimer external clock input
					RTC_1HZ	RTC 1Hz output
					PCA_ECI	PCA external clock input
					VC0_OUT	VC0 output
					LVDIN1	analog input
8	11	9	D2	P15	GPIO	P15 General purpose digital input/output pin
					I2C_SDA _	I2C data
					TIM2_TOG	Timer2 toggle output
					TIM4_CHB	Timer4 capture input/compare output B
					LPTIM_GATE	LPTimer Gating
					SPI_SCK	SPI clock



Pin No.	Pin No.	Pin No.	Pin No.	Pin Name Pin Type		Description
QFN20 TSSOP20 TSSOP16 CSP16					UART0_RXD	UART0 RXD
			LVD_OUT		LVD output	
			XTLO		External XTL crystal clock output	
			GPIO		P14 General purpose digital input/output pin	
9	12	10	D1	P14	I2C_SCL_	I2C clock
					TIM2_TOGN	Timer2 toggles the inverted output
					ECI	PCA external clock input
					ADC_RDY	ADC ready
					SPI_CS	SPI CS
					UART0_TXD	UART0 TXD
					XTLI	External XTL crystal clock input
					GPIO	P23 General purpose digital input/output pin
					TIM6_CHA	Timer6 capture input/compare output A
10	13	11	C2	P23	TIM4_CHB	Timer4 capture input/compare output B
					TIM4_CHA	Timer4 capture input/compare output A
					PCA_CH0	PCA capture input/compare output 0
					SPI_MISO	SPI module master input slave output data signal
					UART1_TXD	UART1 TXD
					IR_OUT	38K carrier output
					LVDIN2/VC0 analog input	
					GPIO	P24 General purpose digital input/output pin
					TIM4_CHB	Timer4 capture input/compare output B
11	14	12	C1	P24	TIM5_CHB	Timer5 capture input/compare output B
					HCLK_OUT	HCLK output
					PCA_CH1	PCA capture input/compare output 1
					SPI_MOSI	SPI module master output slave input data signal
					UART1_RXD	UART1 RXD
					VC1_OUT	VC1 output
					AIN0	analog input
					GPIO	P25 General purpose digital input/output pin
					SPI_SCK	SPI clock
12	15	13	B1	P25	PCA_CH0	PCA capture input/compare output 0
					TIM5_CHA	Timer5 capture input/compare output A
					LVD_OUT	LVD output
					LPUART_RXD	LPUART RXD
					I2C_SDA_	I2C data
					TIM1_GATE	Timer1 gate
					LVDIN3/VC1 analog input	
					GPIO	P26 General purpose digital input/output pin
					SPI_MOSI	SPI module master output slave input data signal
13	16	14	A1	P26	TIM4_CHA	Timer4 capture input/compare output A
					TIM5_CHB	Timer5 capture input/compare output B
					PCA_CH2	PCA capture input/compare output 2
					LPUART_TXD	LPUART TXD
					I2C_SCL_	I2C clock



Pin No.	Pin No.	Pin No.	Pin No.	Pin Name Pin Type		Description
QFN20 TSSOP20 TSSOP16 CSP16					TIM1_EXT	Timer1 clock input
					AIN1	analog input
14	17	15	D3	P27	GPIO	P27 General purpose digital input/output pin
					SPI_MISO	SPI module master input slave output data signal
					TIM5_CHA	Timer5 capture input/compare output A
					TIM6_CHA	Timer6 capture input/compare output A
					PCA_CH3	PCA capture input/compare output 3
					UART0_RXD	UART0 RXD
					RCH_OUT	24M oscillator output
					XTH_OUT	32M oscillator output
					SWDIO	SWDIO
15	18	16	D4	P31	GPIO	P31 General purpose digital input/output pin
					TIM3_TOG	Timer3 toggle output
					PCA_ECI	PCA external clock
					PCLK_OUT	PCLK output
					VC0OUT	VC0 output
					UART0_TXD	UART0 TXD
					RCL_OUT	RCL oscillator output
					HCLK_OUT	HCLK output
					SWCLK	SWCLK
16	19	Note	Note	P32	GPIO	P32 General purpose digital input/output pin
					TIM3_TGN	LPTimer flips the reverse output
					PCA_CH2	PCA capture input/compare output 2
					TIM6_CHB	Timer6 capture input/compare output B
					VC1OUT	VC1 output
					UART1_TXD	UART1 TXD
					PCA_CH4	PCA capture input/compare output4
					RTC_1HX	RTC1HZ output
					AIN2/VC2	analog input
17	20	Note	Note	P33	GPIO	P33 General purpose digital input/output pin
					LPUART_RXD	LPUART RXD
					PCA_CH1	PCA capture input/compare output 1
					TIM5_CHB	Timer5 capture input/compare output B
					PCA_ECI	PCA external clock
					UART1_RXD	UART1 RXD
					XTL_OUT	32K oscillator output
					TIM1_TOGN	Timer1 toggles reverse output
					AIN3/VC3	analog input
18	1	Note	Note	P34	GPIO	P34 General purpose digital input/output pin
					PCA_CH0	PCA capture input/compare output 0
					LPUART_TXD	LPUART TXD
					TIM5_CHA	Timer5 capture input/compare output A
					TIM0_EXT	Timer0 clock input
					TIM4_CHA	Timer4 capture input/compare output A
					RTC_1HZ	RTC1HZ output



Pin No.	Pin No.	Pin No.	Pin No.	Pin Name Pin Type		Description
QFN20 TSSOP20 TSSOP16 CSP16					TIM1_TOG	Timer1 toggle output
				AIN4/VC4	analog input	
19	2	1	A2	P35	GPIO	P35 General purpose digital input/output pin
					UART1_TXD	UART1 TXD
					TIM6_CHB	Timer6 capture input/compare output B
					UART0_RXD	UART0 RXD
					TIM0_GATE	Timer0 gate
					TIM4_CHB	Timer4 capture input/compare output B
					SPI_MISO	SPI module master input slave output data signal
					I2C_SDA_	I2C data
					AIN5/VC5	analog input
20	3	2	A3	P36	GPIO	P36 General purpose digital input/output pin
					UART1_RXD	UART1 RXD
					TIM6_CHA	Timer6 capture input/compare output A
					UART0_RXD	UART0 RXD
					PCA_CH4	PCA capture input/compare output4
					TIM5_CHA	Timer5 capture input/compare output A
					SPI莫斯	SPI module master output slave input data signal
					I2C_SCL_	I2C clock
					AIN6/VC6/ AVREF	analog input

Note: It is necessary to set this package as input and enable pull-up to the IO pins that are not drawn out of TSSOP20.

5. Block Diagram

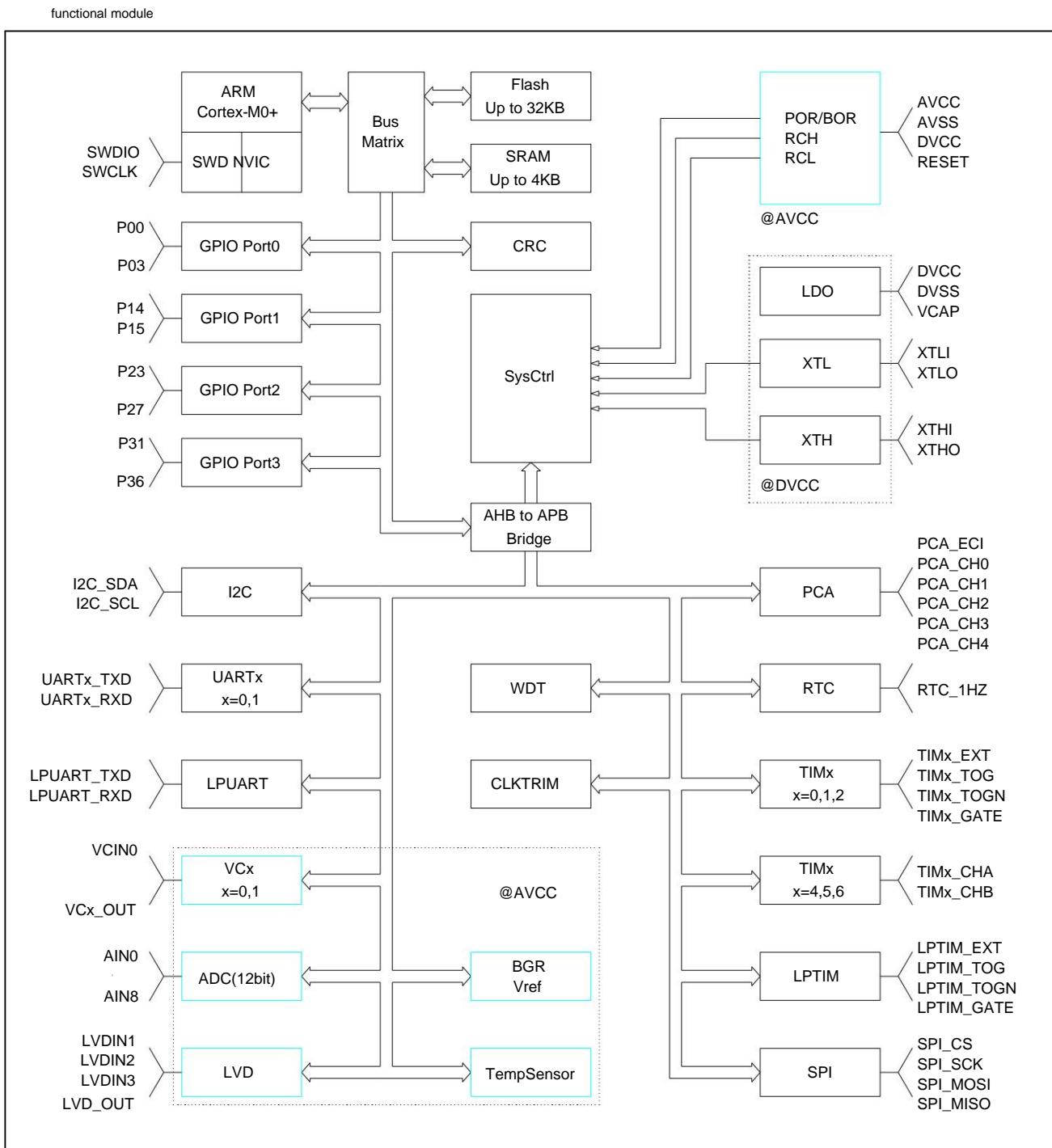
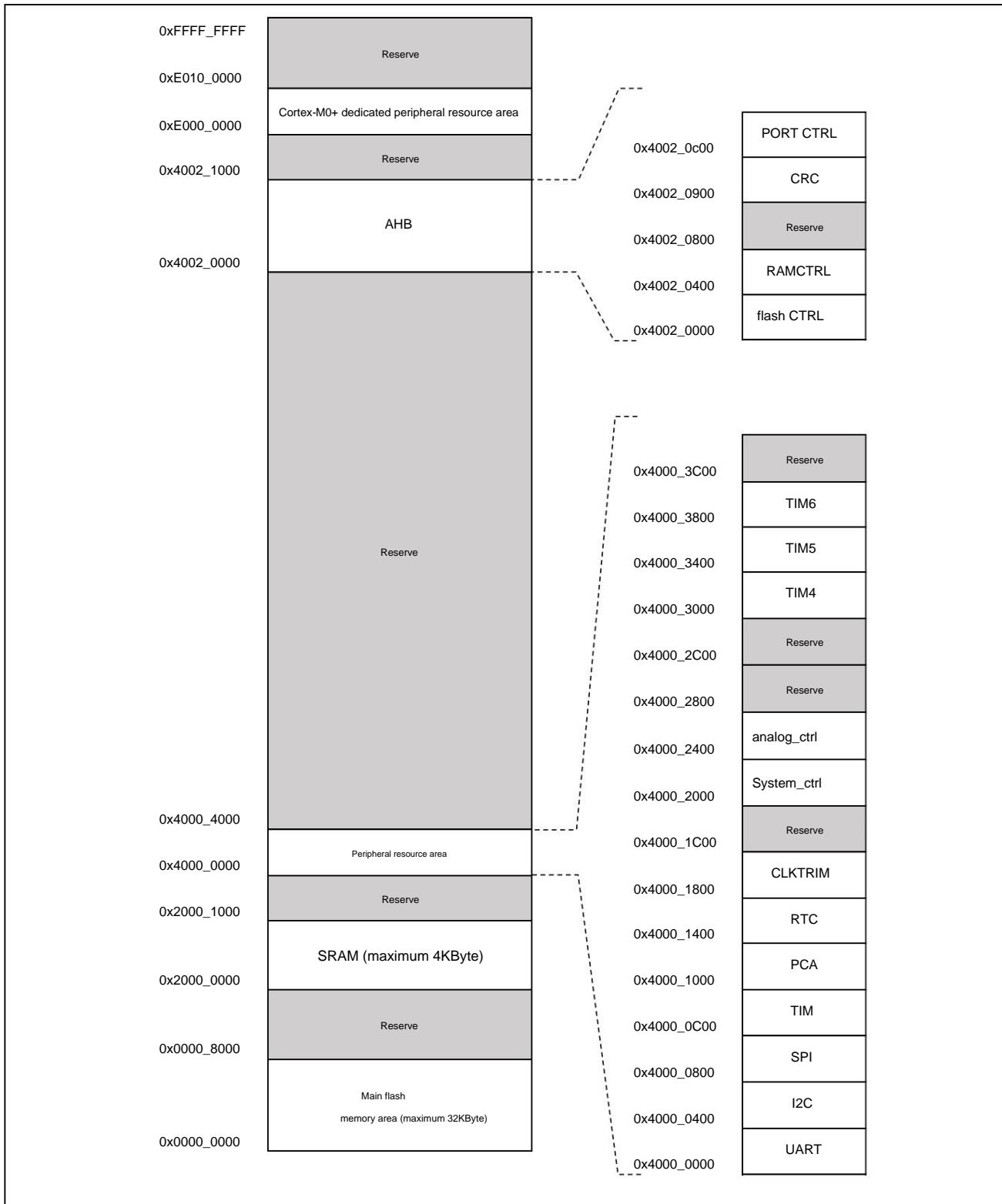


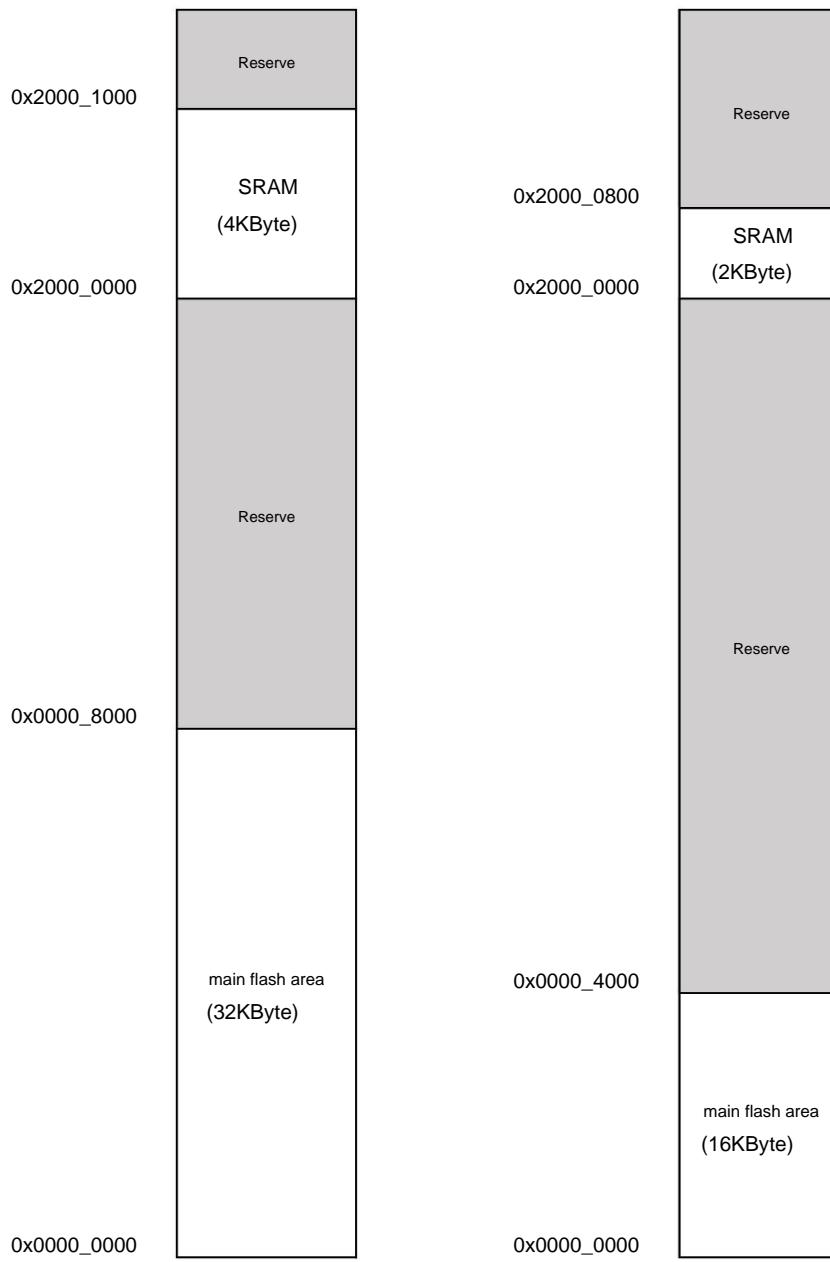
Figure 5-1 Function Module

6. Storage area map



HC32L110C6UA
HC32L110C6PA
HC32L110B6PA
HC32L110B6YA

HC32L110C4UA
HC32L110C4PA
HC32L110B4PA





7. Electrical Characteristics

7.1 Test Conditions

All voltages are referenced to VSS unless otherwise specified.

7.1.1. Minimum and maximum values

Unless otherwise specified, 100% of the products are tested on the production line at ambient temperature TA=25°C and TA=T_{Amax}

(T_{Amax} matches selected temperature range), all min and max values will be at worst ambient temperature, supply voltage and clock frequency conditions

guaranteed below.

Data stated in the notes below each table as derived from comprehensive evaluations, design simulations and/or process characterization, will not be available on the production line

Test; on the basis of comprehensive evaluation, the minimum and maximum values are after passing the sample test, take the average value plus or minus three times the standard

distribution (mean $\pm 3\sigma$) was obtained.

7.1.2. Typical values

Unless otherwise specified, typical data is based on TA=25°C and VCC=3.3V (1.8V \leq VCC \leq 5.5V voltage range). These data are only used

As a design guide and not tested.

Typical ADC accuracy values are obtained by sampling a standard batch, tested over all temperature ranges, 95% product error

Less than or equal to the given value (mean $\pm 2\sigma$).



7.2 Absolute Maximum Ratings

Loads applied to the device in excess of those given in the Absolute Maximum Ratings list may cause permanent damage to the device. here

Merely giving the maximum load that can be tolerated, it does not imply correct functional operation of the device under these conditions. The device operates at the maximum bar for long periods of time

This will affect the reliability of the device.

symbol	describe	minimum	maximum value	unit
VCC – VSS	External main supply voltage (including AVCC and DVCC)(1)	-0.3	5.5	V
VIN	Input voltage on other pins (2) Voltage	VSS-0.3	VCC + 0.3	V
VCCx	difference between different supply pins		50	mV
VSSx – VSS Voltage difference between different ground pins			50	mV
VESD(HBM)	ESD Electrostatic Discharge Voltage (Human Body)	Refer to the absolute maximum electrical parameter V		

(Model) Table 7-1 Voltage Characteristics

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to an external power supply within the allowable range.

2. IINJ (PIN) must not exceed its limit, that is, ensure that VIN does not exceed its maximum value. If there is no guarantee that VIN does not exceed its maximum

value, and also ensure that IINJ(PIN) is limited externally not to exceed its maximum value. When VIN>VCC, there is a forward injection current; when VIN<VSS

, there is a reverse injection current.

symbol	describe	max(1) unit	
IVCC	Total current through DVCC/AVCC power lines (supply current)	300	mA
IVSS	(1) Total current through VSS ground (sink current) (1) Output sink	300	mA
IIO	current on any I/O and control pins	25	mA
	Output current on any I/O and control pins	-25	mA
IINJ(PIN)(2) (3)	Injection current at RESETB pin	+/-5	mA
	Injection current at XTHI pin of XTH and XTLI pin of XTL	+/-5	mA
	Injection current on other	+/-5	mA
ÿIINJ(PIN) (2)	pins(4) Total injection current on all I/O and control pins(4)	+/-25	mA

Table 7-2 Current characteristics

mA

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to the external power supply within the allowable range.

2. IINJ (PIN) must not exceed its limit, that is, ensure that VIN does not exceed its maximum value. If there is no guarantee that VIN does not exceed its maximum

value, and also ensure that IINJ(PIN) is limited externally not to exceed its maximum value. When VIN>VCC, there is a forward injection current; when VIN<VSS

, there is a reverse injection current.

3. Back-injected current can interfere with the analog performance of the device.

4. When several I/O ports have injection current at the same time, the maximum value of ÿI INJ(PIN) is the instant absolute value of forward injection current and reverse injection current.

sum of values. The results are based on the characterization of the maximum value of ÿIINJ(PIN) on the device's four I/O ports.



symbol	describe	Numerical value	unit
TSTG	Storage Temperature Range	-60 ~ +150	°C
TJ	Maximum Junction Temperature	105	°C

Table 7-3 Temperature characteristics



7.3 Working conditions

7.3.1. General operating conditions

symbol		condition	Min	Max	Unit
fHCLK	Parameters Internal AHB Clock		0	32	MHz
fPCLK	Frequency Internal APB Clock Frequency		0	32	MHz
DVCC	digital part operating voltage		1.8	5.5	V
AVCC(1)	analog part working voltage	Must be the same as DVCC(2)	1.8	5.5	V
PD	Power dissipation TA=85 $^{\circ}$	TSSOP20		283	mW
TA	ambient temperature	maximum power consumption	-40	85	$^{\circ}$ C
		Low power consumption(3)	-40	105	$^{\circ}$ C
TJ	Junction temperature range		-40	105	$^{\circ}$ C

Table 7-4 General working conditions

1. When using the ADC, see ADC electrical parameters.
2. It is recommended to use the same power supply to power DVCC and AVCC, the maximum voltage between DVCC and AVCC during power-up and normal operation. A difference of more than 300mV is allowed.
3. In the state of lower power dissipation, TA can be extended to this range as long as TJ does not exceed TJmax.

7.3.2. Operating conditions at power-up and power-down

symbol	parameter	condition	Min	Max	Unit
tVcc	VCC rise rate		0	\ddot{s}	\ddot{s}/V
tVcc	VCC fall rate		10	\ddot{s}	\ddot{s}/V

Table 7-5 Power-up and power-down operating conditions

7.3.3. Embedded reset and LVD module features

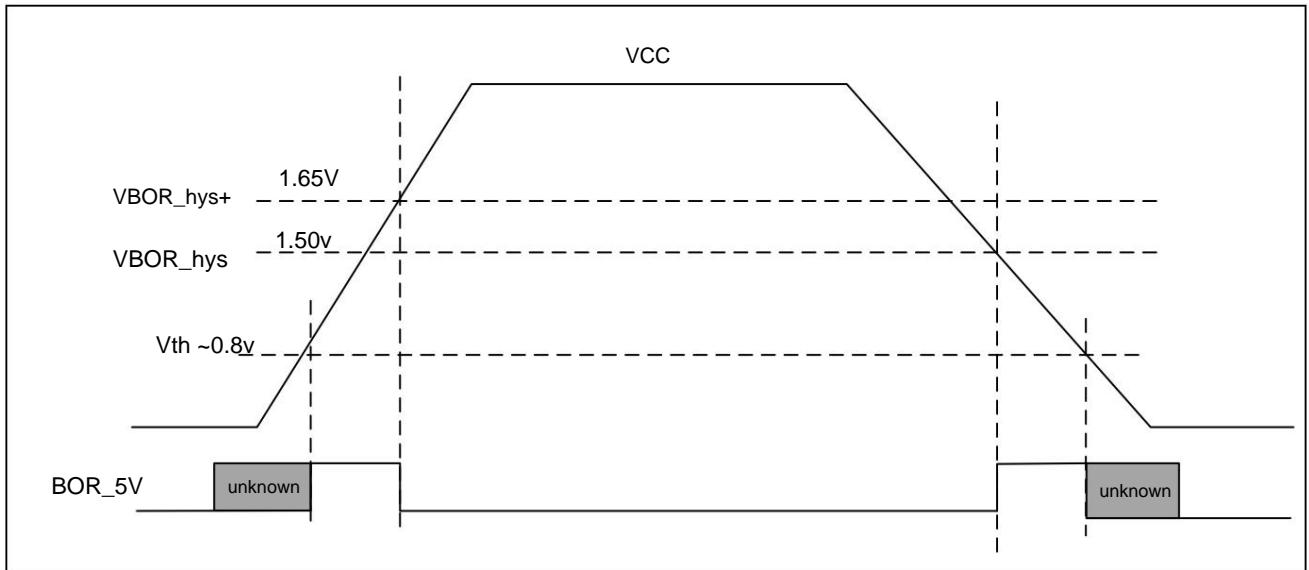


Figure 7-1 POR/Brown Out schematic diagram

1. Guaranteed by design, not tested in production.

symbol	parameter	condition	Min	Typ	Max	Units		
Vpor	POR release voltage (power-on process) BOR detection voltage (power down process)		1.45	1.50	1.65	V		

Table 7-6 POR/Brown Out



symbol	parameter	condition	Min	Typ	Max	Units		
Vex	External input voltage range		0			VCC	V	
Vlevel	detection threshold	LVD_CR.VTDS=0000 LVD_CR.VTDS=0001 LVD_CR.VTDS=0010 LVD_CR.VTDS=0011 LVD_CR.VTDS=0100 LVD_CR.VTDS=0101 LVD_CR.VTDS=0110 LVD_CR.VTDS=0111 LVD_CR.VTDS=1000 LVD_CR.VTDS=1001 LVD_CR.VTDS=1010 LVD_CR.VTDS=1011 LVD_CR.VTDS=1100 LVD_CR.VTDS=1101 LVD_CR.VTDS=1110 LVD_CR.VTDS=1111		1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3			V	
icomp	Power consumption			0.12			µA	
Tresponse	response time			80			µs	
Tsetup	setup time			400			µs	
Vhyste	Hysteresis voltage			40			mV	
Tfilter	filter time	LVD_debounce = 000 LVD_debounce = 001 LVD_debounce = 010 LVD_debounce = 011 LVD_debounce = 100 LVD_debounce = 101 LVD_debounce = 110 LVD_debounce = 111		7 14 28 112 450 1800 7200 28800			µs	

Table 7-6 LVD module features



7.3.4. Built-in reference voltage

symbol	parameter	condition	Min	Typ	Max	Units		
VREF25	Internal 2.5V Reference Voltage	Room temperature 25°C 3.3V	2.475	2.5	2.525V			
VREF25	Internal 2.5V Reference Voltage	-40~85°C 2.8~5.5V	2.463	2.5	2.525	V[1]		
VREF15	Internal 1.5V Reference Voltage	Room temperature 25°C 3.3V	1.485	1.5	1.515V			
VREF15	Internal 1.5V Reference Voltage	-40~85°C 1.8~5.5V	1.477	1.5	1.519	V[1]		
Tcoeff	Internal 2.5V 1.5V temperature coefficient	-40~85°C			120	ppm/°C		

1. The data is based on the assessment results and is not tested in production.

7.3.5. Operating current characteristics

Current consumption is a composite indicator of various parameters and factors including operating voltage, ambient temperature, I/O pin loading,

The software configuration of the product, the operating frequency, the toggle rate of the I/O pins, the location of the program in the memory, and the executed code, etc.

The microcontroller is in the following conditions:

ŷ All I/O pins are in input mode and connected to a static level - VCC or VSS (no load).

ŷ All peripherals are turned off unless otherwise specified.

ŷ The access time of FLASH memory is adjusted to the frequency of fHCLK (0 wait cycles when 0~24MHz, 1 when 24~48MHz

wait period).

ŷ When the peripheral is turned on: fPCLK = fHCLK.

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
IDD (Run in RAM)	All peripherals clock OFF, Run While(1) in RAM.	VCAP=1.55V VCC=3.3V	RCH clock source	4M	220		ŷA
				8M	400		
				16M	740		
				24M	1080		
				32M	1400		
IDD (Run CoreMark)	All peripherals clock OFF, Run	VCAP =1.55V VCC=3.3V	RCH clock source	4M	670		ŷA
	CoreMark in			8M	1300		
	Flash.			16M	2380		
				24M	3410		
				32M	3530		
				(Flash Wait=1)			
IDD (Run mode)	All peripherals clock ON,	VCAP =1.55V VCC=1.8-5.5V	RCH clock source	4M	700	880	ŷA
				8M	1350	1600	
				16M	2500	3000	



Symbol	Parameter	Conditions			Typ	Max(1)	Unit
IDD (Sleep mode)	Run while(1) in Flash			24M	3600	4300	mA
	All peripheral clock OFF, Run while(1) in Flash	VCAP =1.55V VCC=1.8-5.5V	RCH clock source	4M	550	750	
				8M	1050	1300	
				16M	1900	2400	
				24M	2700	3300	
				32M	2850	3000	
				(Flash Wait=1)			
IDD (LP Run)	All peripheral clock ON	VCAP =1.55V VCC=1.8-5.5V	RCH clock source	4M	260	280	mA
				8M	500	520	
				16M	950	970	
				24M	1400	1420	
	All peripheral clock OFF	VCAP =1.55V VCC=1.8-5.5V	RCH clock source	4M	110	125	
				8M	190	210	
				16M	330	360	
				24M	470	500	
				32M	580	610	
IDD (LP Sleep)	All peripherals clock ON, Run while(1) in Flash	VCAP =1.55V VCC=1.8-5.5V	XTL 32.768kHz (Driver = 1)	TA = -40 to 25°C	7	9	mA
				TA = 50 °C	7.3	9.2	
				TA = 85 °C	8.9	11.3	
	All peripherals clock OFF, Run while(1) in Flash	VCAP =1.55V VCC=1.8-5.5V	XTL 32.768kHz (Driver = 1)	TA = -40 to 25°C	6	8	
				TA = 50 °C	6.1	8.2	
				TA = 85 °C	7.7	10.1	
IDD (DeepSleep)	All peripherals clock OFF except RTC,	VCAP =1.55V VCC=1.8-5.5V		TA = -40 to 25°C	1.5	1.65	mA
				TA = 50 °C	1.85	2.2	
				TA = 85 °C	3.5	4.2	

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
	WDT, LPTimer						
All peripherals clock OFF except WDT	VCAP =1.55V VCC=1.8-5.5V		TA = ȳ40 to 25°C TA = 50 °C TA = 85 °C	1.2	1.3		
				1.5	1.8		
				3.1	3.7		
All peripherals clock OFF except LPTimer	VCAP =1.55V VCC=1.8-5.5V		TA = ȳ40 to 25°C TA = 50 °C TA = 85 °C	0.9	1		
				1.1	1.3		
				2.6	3		
All peripherals clock OFF except RTC	VCAP =1.55V VCC=1.8-5.5V		TA = ȳ40 to 25°C TA = 50 °C TA = 85 °C	1.0	1.1		
				1.2	1.5		
				2.6	3.4		
All peripherals clock OFF	VCAP =1.55V VCC=1.8-5.5V		TA = ȳ40 to 25°C TA = 50 °C TA = 85 °C	0.42	0.6		
				0.75	0.95		
				2.2	2.7		

1. Unless otherwise specified, the value of this Typ is measured at 25 °C & VCC = 3.3V.

2. Unless otherwise specified, the value of Max is the maximum value in the range of VCC = 1.8-5.5 & Temperature = N40 – 85 °C.

3. Data is based on assessment results and is not tested in production.

Table 7-9 Operating current characteristics

7.3.6. Wake-up time from low power mode

Wake-up time is measured during the wake-up phase of the RCH oscillator. The clock source used on wakeup depends on the current operating mode:

ȳ Sleep mode: the clock source is the RCH oscillator

ȳ Deep sleep mode: the clock source is the RCH oscillator when entering deep sleep

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Twu	Sleep mode wake-up time			1.8		ȳs
	Deep sleep wake-up time	FMCLK = 4MHz		9.0		ȳs
		FMCLK = 8MHz		6.0		ȳs
		FMCLK = 16MHz		5.0		ȳs
		FMCLK = 24MHz		4.0		ȳs

1. The wake-up time is measured from the wake-up event until the first instruction is read by the user program.



7.3.7. External clock source characteristics

External input high-speed clock

symbol	parameter	condition	Min	Typ	Max	Units		
Fxth_ext	User external clock frequency(1)		0	8	32	MHz		
VXTHH	input pin high level voltage		0.7VCC		VCC	V		
VXTHL	input pin low level voltage		VSS		0.3VCC	V		
Tr(XTH)	time to rise (1)				20	ns		
Tf(XTH)	time to fall (1)				20	ns		
Tw(XTH)	Input high or low time (1) Input		16			ns		
Cin(XTH)	capacitive reactance (1)			5		pF		
Duty	duty cycle		40		60	%		
IL	Input leakage current				±1	µA		

1. Guaranteed by design, not tested in production.

External input low-speed clock

symbol	parameter	condition	Min	Typ	Max	Units		
Fxtl_ext	User external clock frequency(1)		0	32.768	1000	kHz		
VXTLH	input pin high level voltage		0.7VCC		VCC	V		
VXTLL	input pin low level voltage		VSS		0.3VCC	V		
Tr(XTL)	time to rise (1)				50	ns		
Tf(XTL)	time to fall (1)				50	ns		
Tw(XTL)	Input high or low time (1) Input		450			ns		
Cin(XTL)	capacitive reactance (1)			5		pF		
Duty	duty cycle		30		70	%		
IL	Input leakage current				±1	µA		

1. Guaranteed by design, not tested in production.



High-speed external clock XTH

A high-speed external clock (XTH) can be generated using a 4~32MHz crystal/ceramic resonator oscillator, given in this section

Information is based on comprehensive characterization results using the typical external components listed in the table below. In applications, the resonator and

The load capacitor must be placed as close to the oscillator pins as possible to reduce output distortion and settling time at start-up, about crystal resonators

For detailed parameters (frequency, package, accuracy, etc.), please consult the corresponding manufacturer.

External XTH crystal(1) (2)

symbol	parameter	condition	Min	Typ	Max	Units		
FCLK	Oscillation frequency		4		32	MHz		
Crystal ESR range supported by ESRCLK		32M		30	60	Ohm		
		4M		400	1500	Ohm		
CLX(3)	load capacitance	Configure as required by the crystal manufacturer.						
Duty	duty cycle		40	50	60	%		
Idd(4)	current	32M Xtal, CL=12pF, ESR=30ohm		600			µA	
gm	transconductance	vibrate	700				µA/V	
Tstart (5) start time		32MHz @XTH_CR.Driver=1111		400			µs	
		4MHz @XTH_CR.Driver=0011		2			ms	

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.

2. Based on comprehensive evaluation, not tested in production.

3. CLX refers to the load capacitance of the two pins of XTAL, and the user must select the capacitance value of the capacitor according to the crystal manufacturer's requirements.

If the crystal manufacturer gives The value of the load capacitor , the value of the matching capacitor should be the load capacitance given by the crystal manufacturer

twice the value.

If the crystal manufacturer gives Capacitance value of matching capacitor you can directly use the capacitance value of the matching capacitor given by the crystal manufacturer.

Example: The crystal manufacturer gives the crystal's load capacitance When it is 8pF, the value of the matching capacitor should be 16pF. Consider PCB vs MCU

For the distributed capacitance between pins, it is recommended to choose a matching capacitor with a capacitance value of 15pF or 12pF.

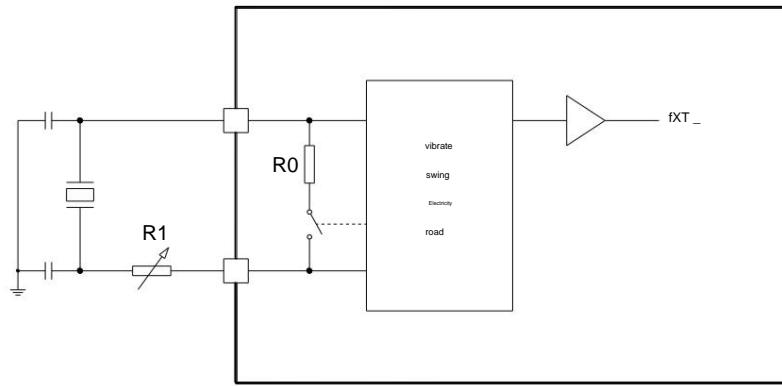
The crystal manufacturer gives the crystal's matching capacitor When it is 12pF, the value of the matching capacitor should be 12pF. Consider PCB vs MCU

For the distributed capacitance between pins, it is recommended to choose a matching capacitor with a capacitance value of 10pF or 8pF.

4. The current changes with the frequency, test condition: XTH_CR.Driver=1110

5. Tstart is the start-up time, which is the time from when XTH is enabled by software until a stable 32MHz/4MHz oscillation is obtained.

This value is measured on a standard crystal resonator and may vary widely depending on the crystal manufacturer and model.



Notice:

– The matching capacitance of the crystal must be configured according to the crystal manufacturer's technical manual.

If the crystal manufacturer gives The value of the load capacitor , the value of the matching capacitor should be the load capacitance given by the crystal manufacturer twice the value.

If the crystal manufacturer gives Capacitance value of matching capacitor you can directly use the capacitance value of the matching capacitor given by the crystal manufacturer.

– The feedback resistor R0 has been integrated into the chip.

– Please refer to the relevant application notes for the tuning method of the resistance value of the damping resistor R1.



Low-speed external clock XTL

The low-speed external clock (XTL) can be generated using a 32.768kHz crystal/ceramic resonator oscillator, given in this section

Information is based on a comprehensive characterization of typical external components. In the application, the resonator and load capacitance must be as small as possible

can be placed close to the oscillator pins to reduce output distortion and settling time at start-up. Detailed parameters about the crystal resonator (frequency, package

installation, accuracy, etc.), please consult the corresponding manufacturer.

External XTL crystal oscillator(1)

Symbolic parameters	condition	Min	Typ	Max	Units		
FCLK oscillation frequency			32.768				kHz
Crystal ESR range supported by ESRCLK			65	85			k Ω
CLx(2) load capacitance	Configure as required by the crystal manufacturer.						
DCACLK duty cycle		30	50	70	%		
Idd(3) current	ESR= 65k Ω CL=12pF		850	1000		nA	
gm	vibrate	2.5				μ A/V	
Tstart start time	ESR=65k Ω CL=12pF 40% - 60% duty cycle has been reached		500			ms	

1. Based on comprehensive evaluation, not tested in production.

2. CLX refers to the load capacitance of the two pins of XTAL, and the user must select the capacitance value of the capacitor according to the crystal manufacturer's requirements.

If the crystal manufacturer gives The value of the load capacitor , the value of the matching capacitor should be the load capacitance given by the crystal manufacturer twice the value.

If the crystal manufacturer gives Capacitance value of matching capacitor you can directly use the capacitance value of the matching capacitor given by the crystal manufacturer.

Example: The crystal manufacturer gives the crystal's load capacitance When it is 8pF, the value of the matching capacitor should be 16pF. Consider PCB vs MCU

For the distributed capacitance between pins, it is recommended to choose a matching capacitor with a capacitance value of 15pF or 12pF.

The crystal manufacturer gives the crystal's matching capacitor When it is 12pF, the value of the matching capacitor should be 12pF. Consider PCB vs MCU

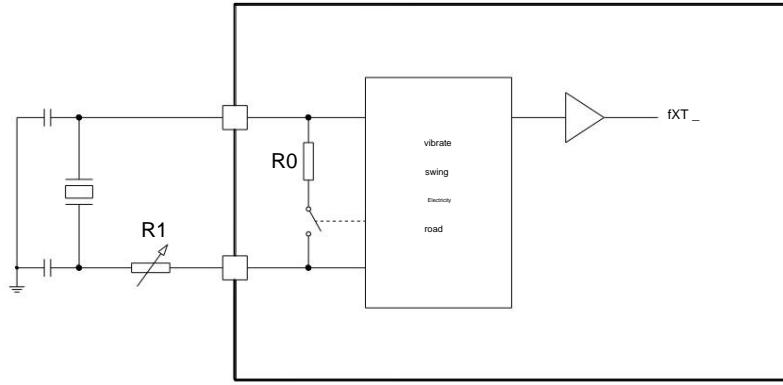
For the distributed capacitance between pins, it is recommended to choose a matching capacitor with a capacitance value of 10pF or 8pF.

3. Typical value is power consumption when XTL_CR.Driver=1001. Choose a high-quality oscillator with a small ESR value (such as MSIV

TIN32.768kHz), the current consumption can be optimized by reducing the XTL_CR.Driver setting.

4. Tstart is the start-up time, which is measured from the software enabling XTL until the stable 32768 oscillation is obtained. this number

Values are measured on a standard crystal resonator and may vary widely depending on crystal manufacturer and model.



Notice:

- The matching capacitance of the crystal must be configured according to the crystal manufacturer's technical manual.

If the crystal manufacturer gives	The value of the load capacitor , the value of the matching capacitor should be the load capacitance given by the crystal manufacturer twice the value.
-----------------------------------	---

If the crystal manufacturer gives	Capacitance value of matching capacitor you can directly use the capacitance value of the matching capacitor given by the crystal manufacturer.
-----------------------------------	---

- The feedback resistor R0 has been integrated into the chip.

- Please refer to the relevant application notes for the tuning method of the resistance value of the damping resistor R1.



7.3.8. Internal clock source characteristics

Internal RCH oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dev	RCH oscillator accuracy	User trimming step for given VCC and TA conditions		0.25		%
		VCC = 1.8 ~ 5.5V TAMB = -40 ~ 85°C	-3.5		+3.5	%
		VCC = 1.8 ~ 5.5V TAMB = -20 ~ 50°C	-2.0		+2.0	%
FCLK	oscillation frequency		4.0 8.0 16.0 22.12 24.0	4.0 8.0 16.0 22.12 24.0	24.0	MHz
ICLK	Power consumption	FMCLK = 4MHz		80		µA
		FMCLK = 8MHz		100		µA
		FMCLK = 16MHz		120		µA
		FMCLK = 24MHz		140		µA
DCCLK	Duty Cycle(1)		45	50	55	%

1. Based on comprehensive evaluation, not tested in production.

Internal RCL oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dev	RCL Oscillator Accuracy	User trimming step for given VCC and TA conditions		0.5		%
		VCC = 1.8 ~ 5.5V TAMB = -40 ~ 85°C	-5		+5	%
		VCC = 1.8 ~ 5.5V TAMB = -20 ~ 50°C	-3		+3	%
FCLK	oscillation frequency			38.4 32.768		kHz
TCLK	start-up time			150		µs
DCCLK	Duty Cycle(1)		25	50	75	%
ICLK	Power consumption			0.25		µA

1. Based on comprehensive evaluation, not tested in production.



7.3.9. Memory characteristics

symbol	parameter	condition	Min	Typ	Max	Units		
ECFLASH erasing	times	Regulator voltage=1.5V, TAMB = 25°C	20				kcycles	
RETFETCH data retention period		TAMB = 85°C, after 20 kcycles	20				Years	
Tw_prog	programming time		6			7.5	µs	
Tp_erase	Page Erase Time		4			5	ms	
Tm_erase chip erase time			30			40	ms	

7.3.10. EFT Characteristics

A chip reset can restore the system to normal operation.

symbol	Level/Type
EFT to IO (IEC61000-4-4)	Class: 4(B)
EFT to Power (IEC61000-4-4)	Class: 4(B)

software advice

The software process must include controls to deal with program runaways, such as:

- ÿ Corrupted program counter

- ÿ Unexpected reset

- ÿ Critical data is corrupted (control registers, etc.)

During the EFT test, the interference that exceeds the application requirements can be directly applied to the chip power supply or IO, and when an unexpected action is detected

where the software part is hardened to prevent unrecoverable errors from occurring.



7.3.11. ESD Characteristics

Using specific measurement methods, the chip is strength tested to determine its performance in terms of electrical sensitivity.

symbol	parameter	condition	minimum	Typical value	maximum value	unit
VESDHBM	ESD @ Human Body Mode			4		KV
VESDCDM	ESD @ Charge Device Mode			1		KV
VESDMM	ESD @ machine Mode			200		V
Ilatchup	Latch up current			200		mA

7.3.12. Port Characteristics

Output Characteristics - Ports

Symbol	Parameter	Conditions	Min	Max	Unit
VOH	High level output voltage Source Current	Sourcing 4 Ma, VCC = 3.3 V (see Note 1)	VCC-0.25		V
		Sourcing 6 Ma, VCC = 3.3 V (see Note 2)	VCC-0.6		V
VOL	Low level output voltage Sink Current	Sinking 4 Ma, VCC = 3.3 V (see Note 1)		VSS+0.25	V
		Sinking 6 Ma, VCC = 3.3 V (see Note 2)		VSS+0.6	V
VOHD	High level output voltage Double source Current	Sourcing 8 Ma, VCC = 3.3 V (see Note 1)	VCC-0.25		V
		Sourcing 12 Ma, VCC = 3.3V (see Note 2)	VCC-0.6		V
VOLD	Low level output voltage Double Sink Current	Sinking 8 Ma, VCC = 3.3 V (see Note 1)		VSS+0.25	V
		Sinking 12 Ma, VCC = 3.3 V (see Note 2)		VSS+0.6	V

Table 7-10 Port output characteristics

NOTES:

1. The maximum total current, IOH(max) and IOL(max), for all outputs combined, should not exceed 40 Ma to satisfy the maximum specified voltage drop.
2. The maximum total current, IOH(max) and IOL(max), for all outputs combined, should not exceed 100 Ma to satisfy the maximum specified voltage drop.

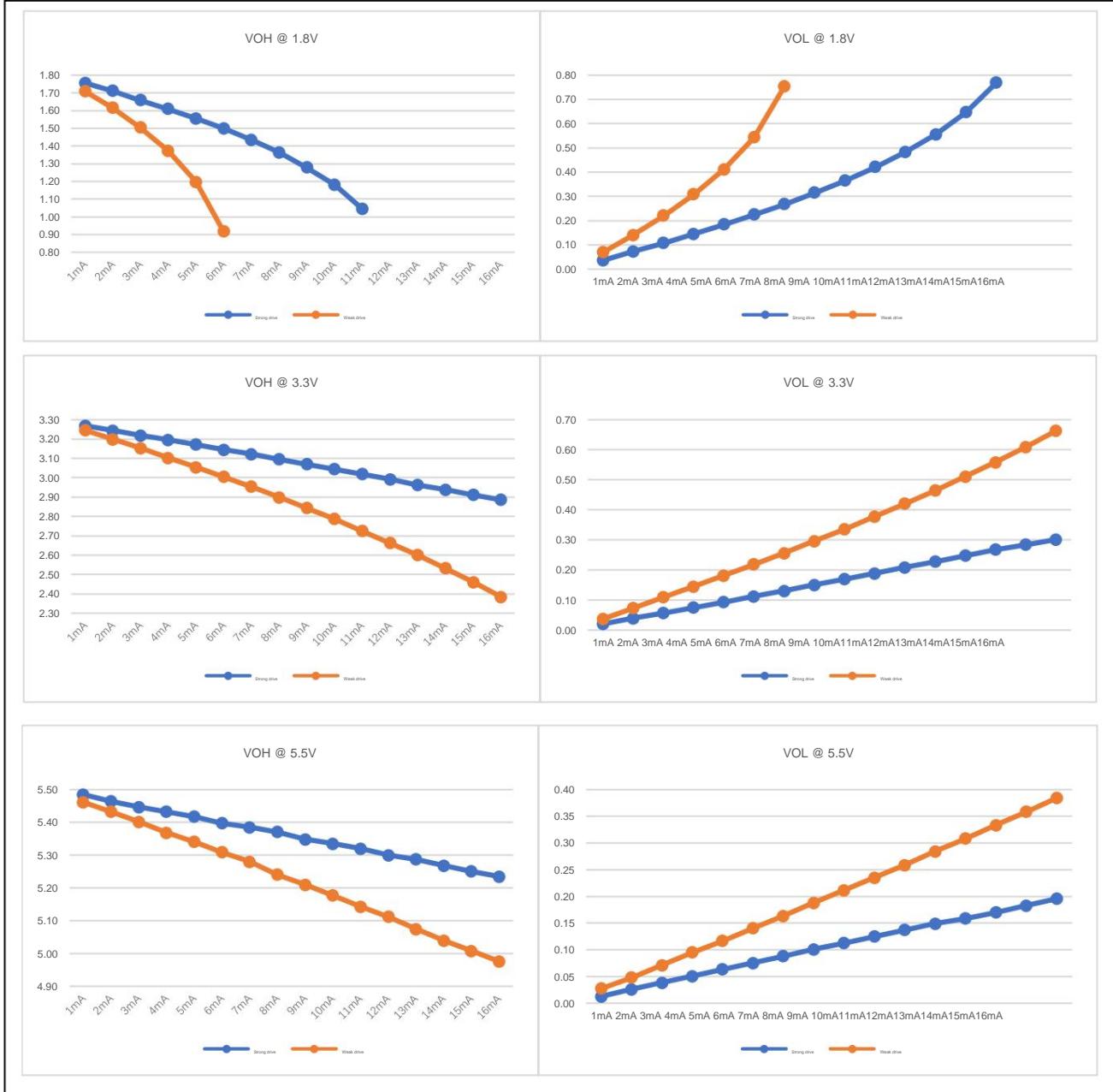


Figure 7-2 Measured curve of output port VOH/VOL

Input Characteristics - Ports P0, P1, P2, P3

Symbolic parameters	parameters	condition	minimum	Typical value	maximum value	unit
VIH	Positive-going input threshold voltage	VCC=1.8V	0.7VCC			V
		VCC=3.3V	0.7VCC			V
		VCC=5.5V	0.7VCC			V
VIL	Negative-going input threshold voltage	VCC=1.8V			0.3VCC	V
		VCC=3.3V			0.3VCC	V
		VCC=5.5V			0.3VCC	V



Symbolic parameters		condition	minimum	Typical value	maximum value	unit
Vphys(1)	Input voltage hysteresis (VIH – VIL)	VCC=1.8V		0.3		V
		VCC=3.3V		0.4		V
		VCC=5.5V		0.6		V
Rpullhigh	Pullup resistor	Pullup enabled VCC=3.3V		80		k Ω
Rpulllow	Pulldown resistor	Pulldown enabled VCC=3.3V		40		k Ω
Cinput	Input capacitance			5		pF

1. Based on comprehensive evaluation, not tested in production.

Port External Input Sampling Requirements - Timer Gate/Timer Clock

Symbol	Parameter	Conditions	VCC	Min	Max	Unit
t(int)	External interrupt timing	External trigger signal for the interrupt flag (see Note 1)	1.8V	30		ns
			3.3V	30		ns
			5.5V	30		ns
t(cap)	Timer capture timing	Timer4/5/6 capture pulse width Fsystem = 4MHz	1.8V	0.5		μ s
			3.3V	0.5		μ s
			5.5V	0.5		μ s
t(clk)	Timer clock frequency applied to pin	Timer0/1/2/4/5/6 external clock input Fsystem = 4MHz	1.8V		PCLK/2	MHz
			3.3V		PCLK/2	MHz
			5.5V		PCLK/2	MHz
t(pca)	PCA clock frequency applied to pin	PCA external clock input Fsystem = 4MHz	1.8V		PCLK/8	MHz
			3.3V		PCLK/8	MHz
			5.5V		PCLK/8	MHz

NOTE:

- The external signal sets the interrupt flag every time the minimum t(int) parameters are met. It may be set even with trigger signals shorter than t(int).

Port leakage characteristics - P0, P1, P2, P3

Symbol	Parameter	Conditions	VCC	Max	Unit
I _{lk} (Px,y)	Leakage current	V(Px,y) (see Note 1,2)	1.8V/3.6V	± 50	nA

NOTES:

- The leakage current is measured with VSS or VCC applied to the corresponding pin(s), unless otherwise noted.
- The port pin must be selected as input.

7.3.13. RESETB Pin Characteristics

The RESETB pin input driver uses CMOS technology, and it is connected with a pull-up resistor that cannot be disconnected.

symbol	parameter	condition	Min	Typ	Max	Units		
VIL(RESETB)	(1) Input low level voltage		-0.3			0.3V	VCC	
V _{IH} (RESETB)	Input high level voltage		0.7V	VCC		VCC+0.3	V	V
V _{hys} (RESETB)	Schmitt Trigger Voltage Hysteresis			200			mV	
R _{PU}	Weak pull-up equivalent resistance	V _{IN} = V _{SS}		80			k Ω	
V _F (RESETB) ⁽¹⁾	input filter pulse				100		ns	
V _{NF} (RESETB) ⁽¹⁾	Input unfiltered pulse		300				ns	

)
1. Guaranteed by design, not tested in production.

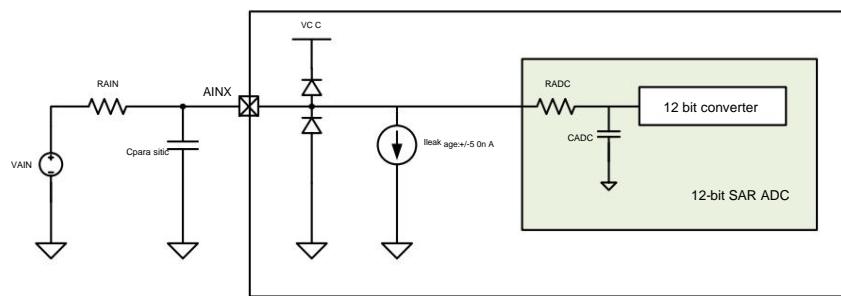
7.3.14. ADC Characteristics

symbol	parameter	condition	Min	Typ	Max	Units		
V _{ADCIN}	Input voltage range	Single ended	0			V _{ADCREFIN}	V	
V _{ADCREFIN}	Input range of external reference voltage	Single ended	0			V _{CC}	V	
DEV _{VCC/3}	V _{CC} /3 accuracy			3			%	
I _{ADC1}	Active current including reference generator and buffer	200Ksps		2			mA	
I _{ADC2}	Active current without reference generator and buffer	1Msps		0.5			mA	
C _{ADCIN}	ADC input capacitance			16	19.2	pF		
R _{ADC(1)}	ADC sampling switch impedance			1.5			k Ω	
R _{AIN(1)}	ADC external input resistor(2)				100		k Ω	
F _{ADCCLK}	ADC clock Frequency				24M	Hz		
T _{ADCSTART}	Startup time of reference generator and ADC core			30			μ s	
T _{ADCCONV}	Conversion time		20			28	cycles	
E _{NOB}	Effective Bits	1Msps@V _{CC} >=2.7V 500Ksps@V _{CC} >=2.4V 200Ksps@V _{CC} >=1.8V REF=EXREF		10.3			Bit	

symbol	parameter	condition	Min	Typ	Max	Units		
		1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=VCC			10.3			Bit
		200Ksps@VCC>=1.8V REF=internal 1.5V			9.4			Bit
		200Ksps@VCC>=2.8V REF=internal 2.5V			9.4			Bit
SNR	Signal to Noise Ratio	1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=EXREF			68.2			dB
		1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=VCC			68.2			dB
		200Ksps@VCC>=1.8V REF=internal 1.5V			60			dB
		200Ksps@VCC>=2.8V REF=internal 2.5V			60			dB
DNL(1)	Differential non-linearity	200KSps; VREF=EXREF/VCC	-1			1		LSB
INL(1)	Integral non-linearity	200KSps; VREF=EXREF/VCC	-3			3		LSB
Eo	offset error				0			LSB
Eg	Gain error				0			LSB

1. Guaranteed by design, not tested in production.

2. The typical application of ADC is shown in the figure below:



For the requirement of 0.5LSB sampling error accuracy, the calculation formula of external input impedance is as follows:

$$RAIN = \frac{M}{\ln(2) \cdot (N+1)} \cdot RADC$$



Among them is the ADC clock frequency, and the relationship between the register ADC_CR0<3:2> and PCLK can be set, as shown in the following table:

The following table shows the relationship between ADC clock frequency and PCLK divider ratio:

ADC_CR0<3:2>	N
00	1
01	2
10	4
11	8

M is the number of sampling cycles, set by register ADC_CR0<13:12>.

The following table shows the relationship between sampling time and ADC clock frequency:

ADC_CR0<13:12>	M
00	4
01	6
10	8
11	12

The following table shows the relationship between ADC clock frequency and external resistance (M=12, under the condition of sampling error 0.5LSB):

(k \ddot{y})	(kHz)
10	5600
30	2100
50	1300
80	820
100	660
120	550
150	450

For the above typical applications, it should be noted that:

- Minimize parasitic capacitance of ADC input port ;
- In addition to considering the value, if the internal resistance of the signal source is large, it also needs to be considered.

7.3.15. VC Features

symbol	parameter	condition	Min	Typ	Max	Units		
Vin	Input voltage range		0			5.5	V	
Vincom	Input common mode range		0			VCC-0.2V		
Voffset	Input offset	Room temperature 25°C 3.3V	-10			+10	mV	
icomp	Comparator's current	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11		0.3 1.2 10 20			µA	
Tresponse	Comparator's response time when one input cross another	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11		20 5 1 0.2			µs	
Tsetup	Comparator's setup time when ENABLE. Input signals unchanged.	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11		20 5 1 0.2			µs	
Twarmup	From main bandgap enable to 1.2V BGR reference, Temp sensor voltage, ADC internal 1.5V, 2.5V reference stable			20			µs	
Tfilter	Digital filter time	VC_debounce = 000 VC_debounce = 001 VC_debounce = 010 VC_debounce = 011 VC_debounce = 100 VC_debounce = 101 VC_debounce = 110 VC_debounce = 111		7 14 28 112 450 1800 7200 28800			µs	



7.3.16. TIM Timer Features

See the table below for details on the characteristics of the I/O alternate function pins (output compare, input capture, external clock, PWM output).

symbol	parameter	condition	minimum	maximum value	unit
tres	timer resolution time		1		tTIMCLK
		fTIMCLK=32MHz	31.3		ns
fext	External clock frequency		0	fTIMCLK/2	MHz
		fTIMCLK=32MHz	0	16	MHz
ResTim	Timer resolution			16	bit
Tcounter	When internal clock is selected, when 16-bit counter clock cycle		1	65536	tTIMCLK
		fTIMCLK=32MHz	0.0313	2051	ÿs
TMAX_COUNT	maximum possible count			67108864	tTIMCLK
		fTIMCLK=32MHz		2.1	s

1. Guaranteed by design, not tested in production.

Table 7-7 Advanced Timer (ADVTIM) Features

symbol	parameter	condition	minimum	maximum value	unit
tres	timer resolution time		1		tTIMCLK
		fTIMCLK=32MHz	31.3		ns
fext	External clock frequency		0	fTIMCLK/2	MHz
		fTIMCLK=32MHz	0	16	MHz
ResTim	Timer resolution	reload count		16	bit
		free count		32	bit
Tcounter	When internal clock is selected, when 16-bit counter clock cycle		1	65536	tTIMCLK
		fTIMCLK=32MHz	0.0313	2051	ÿs
TMAX_COUNT	maximum possible count (overload mode)			16777216	tTIMCLK
		fTIMCLK=32MHz		524.3	ms

1. Guaranteed by design, not tested in production.

Table 7-8 Basic timer characteristics



symbol	parameter	condition	minimum	maximum value	unit
tres	timer resolution time		1		tTIMCLK
		fTIMCLK=32MHz	31.3		ns
fext	External clock frequency		0	fTIMCLK/2	MHz
		fTIMCLK=32MHz	0	16	MHz
ResTim	Timer resolution			16	bit
Tcounter	When internal clock is selected, when 16-bit counter clock cycle		1	65536	tTIMCLK
		fTIMCLK=32MHz	0.0313	2051	µs
TMAX_COUNT	maximum possible count			2097152	tTIMCLK
		fTIMCLK=32MHz		65.54	ms

1. Guaranteed by design, not tested in production.

Table 7-9 PCA characteristics

symbol	parameter	condition	minimum	maximum value	unit
tres	timer resolution time		1		tTIMCLK
		fTIMCLK=32MHz	31.3		ns
fext	External clock frequency		0	fTIMCLK/2	MHz
		fTIMCLK=32MHz	0	16	MHz
ResTim	Timer resolution			16	bit
Tcounter	When internal clock is selected, when 16-bit counter clock cycle		1	65536	tTIMCLK
		fTIMCLK=32MHz	0.0313	2051	µs
TMAX_COUNT	maximum possible count			65536	tTIMCLK
		fTIMCLK=32MHz		2.05	ms

1. Guaranteed by design, not tested in production.

Table 7-10 Low-power timer features

symbol	parameter	condition	minimum	maximum value	unit
tres	WDT overflow time	fWDTCLK=10kHz	1.6	52000	ms

1. Guaranteed by design, not tested in production.

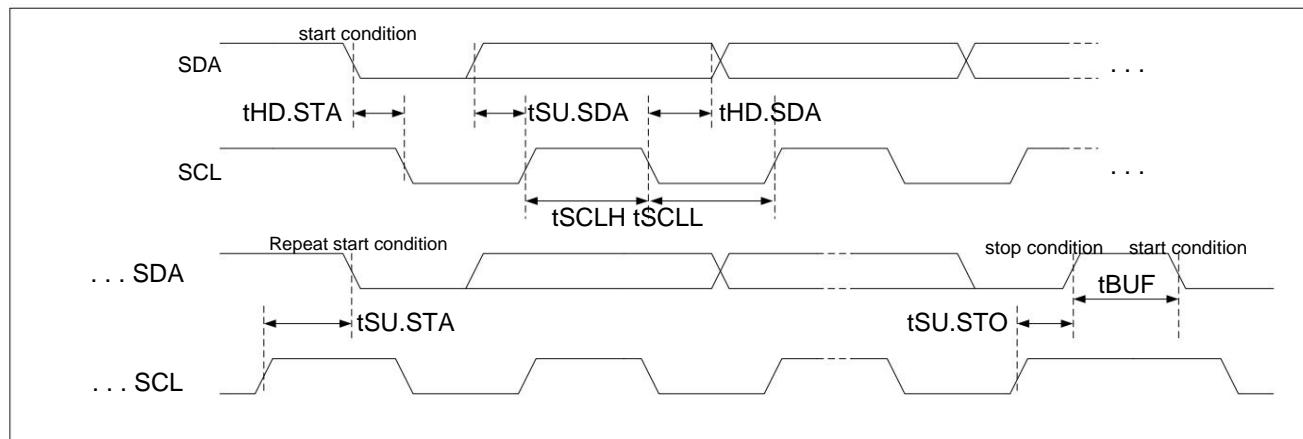
Table 7-11 WDT characteristics

7.3.17. Communication interface

I²C FeaturesThe characteristics of the I²C interface are as follows:

symbol	parameter	Standard Mode (100K)		Fast Mode (400K)		High Speed Mode (1M)		unit
		min	max	min	max	min	max	
tSCLL	SCL clock low time	4.7		1.25		0.5		µs
tSCLH	SCL clock high time	4.0		0.6		0.26		µs
tSU.SDA	SDA setup time	250		100		50		ns
tHD.SDA	SDA hold time	0		0		0		µs
tHD.STA	Start condition hold time	2.5		0.625		0.25		µs
tSU.STA	Repeated Start Condition Setup Time	2.5		0.6		0.25		µs
tSU.STO	Stop condition setup time	0.25		0.25		0.25		µs
tBUF	Bus Idle (Stop Condition to Start Condition)	4.7		1.3		0.5		µs

1. Guaranteed by design, not tested in production.

Table 7-12 I²C interface characteristicsFigure 7-2 I²C interface timing

**SPI features**

symbol	parameter	condition	minimum	Maximum	unit
tc(SCK)	period of serial clock	host mode	62.5	-	ns
		slave mode fPCLK = 16MHz	250	-	ns
tw(SCKH)	serial clock high time	host mode	$0.5 \times tc(SCK)$	-	ns
		slave mode	$0.5 \times tc(SCK)$	-	ns
tw(SCKL)	serial clock low time	host mode	$0.5 \times tc(SCK)$	-	ns
		slave mode	$0.5 \times tc(SCK)$	-	ns
tsu(SSN)	Setup time for slave selection	slave mode	$0.5 \times tc(SCK)$	-	ns
th(SSN)	Slave selected hold time	slave mode	$0.5 \times tc(SCK)$	-	ns
tv(MO)	Effective time of host data output	fPCLK = 32MHz	-	3	ns
th(MO)	Hold time of host data output	fPCLK = 32MHz	2	-	ns
tv(SO)	Effective time of slave data output	fPCLK = 16MHz	-	50	ns
th(SO)	Hold time of slave data output	fPCLK = 16MHz	30	-	ns
tsu(MI)	Setup time for host data input		10	-	ns
th(MI)	Hold time for host data input		2	-	ns
tsu(SI)	Settling time for slave data input		10	-	ns
th(SI)	Hold time for slave data input		2	-	ns

1. Guaranteed by design, not tested in production.

Table 7-13 SPI interface characteristics

The waveform and timing parameters of the SPI interface signals are as follows:

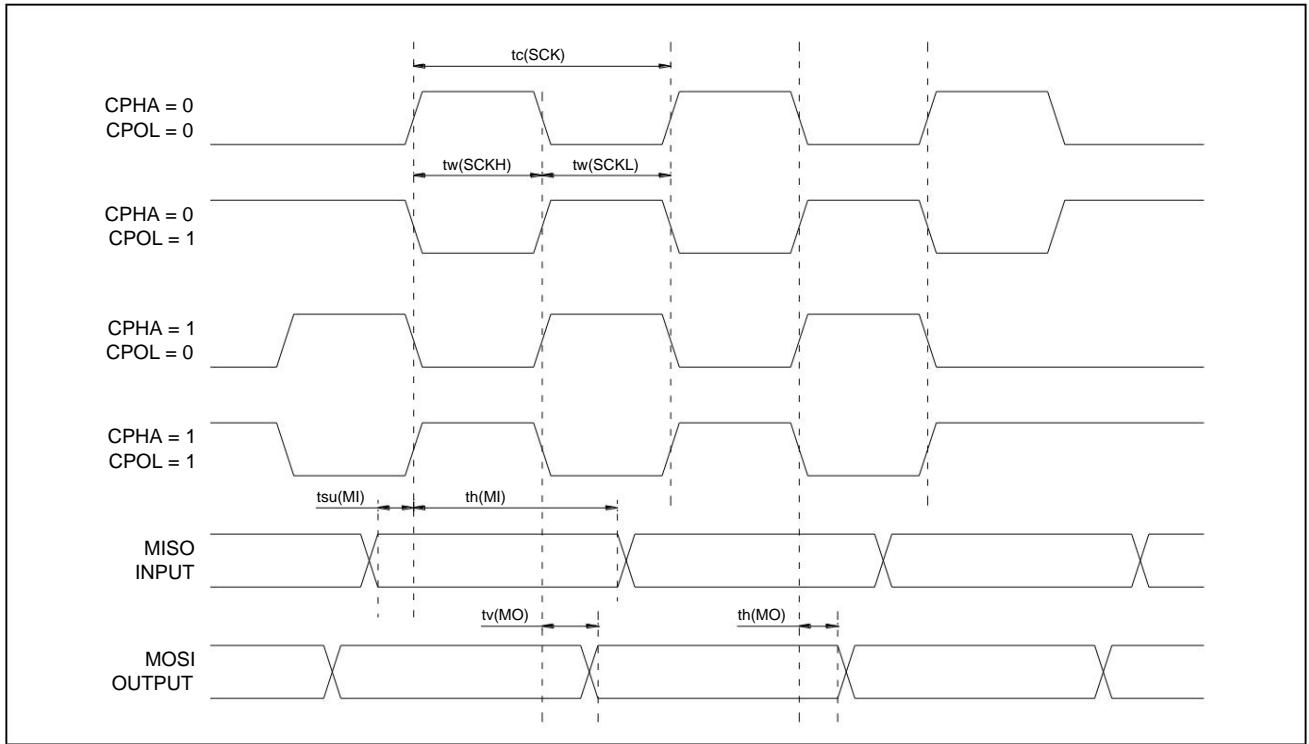


Figure 7-3 SPI Timing Diagram (Master Mode)

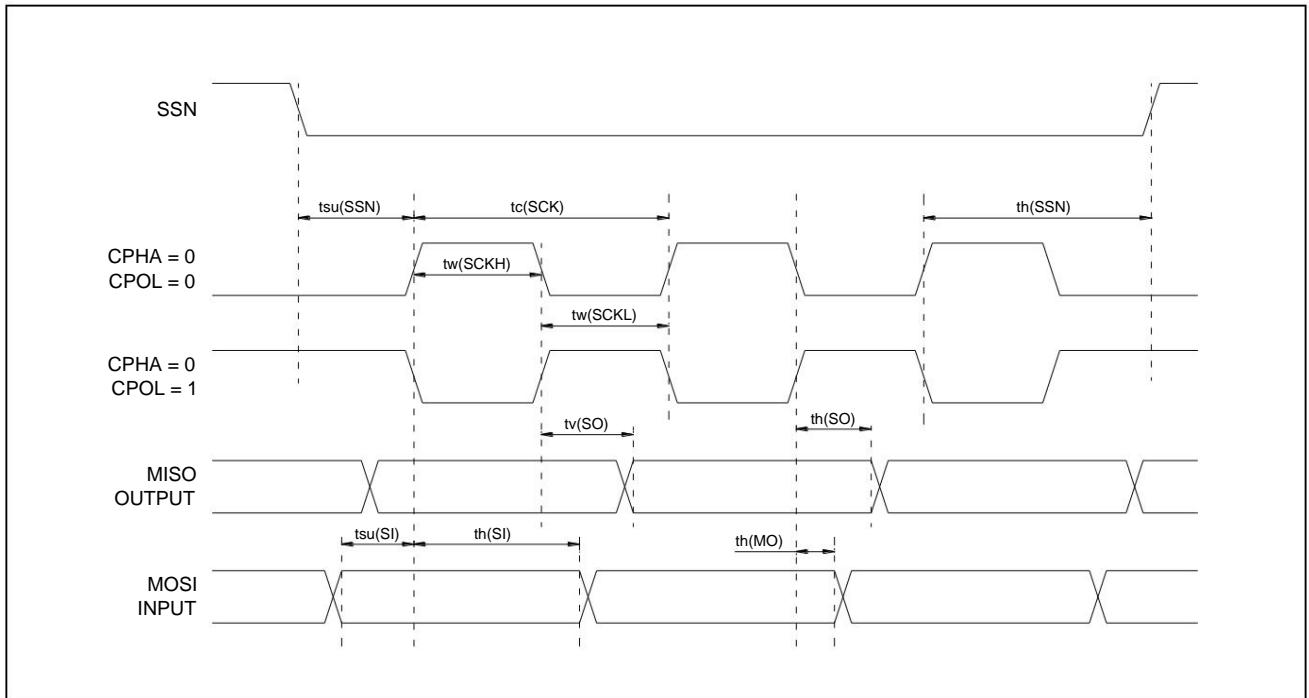


Figure 7-4 SPI timing diagram (slave mode cpha=0)

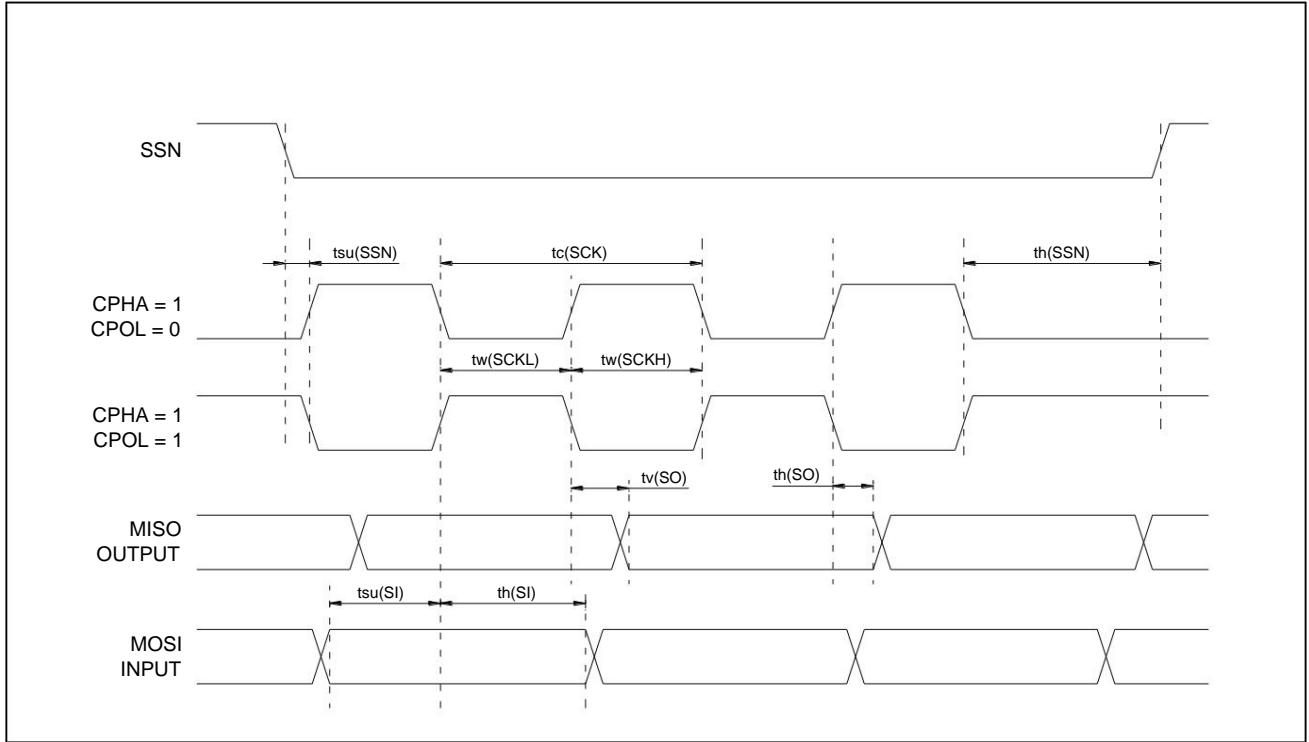
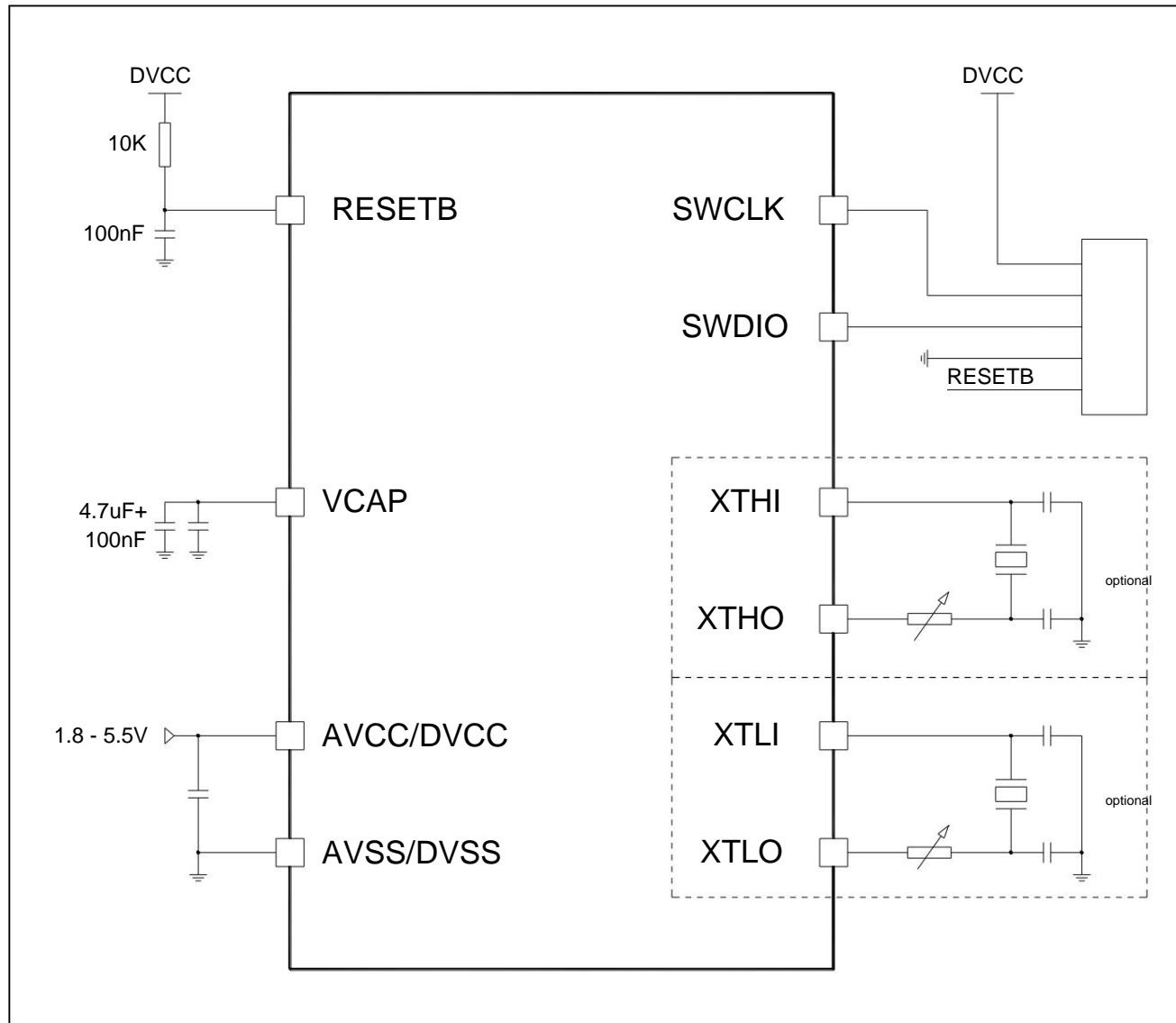


Figure 7-5 SPI timing diagram (slave mode cpha=1)

8. Typical application circuit diagram



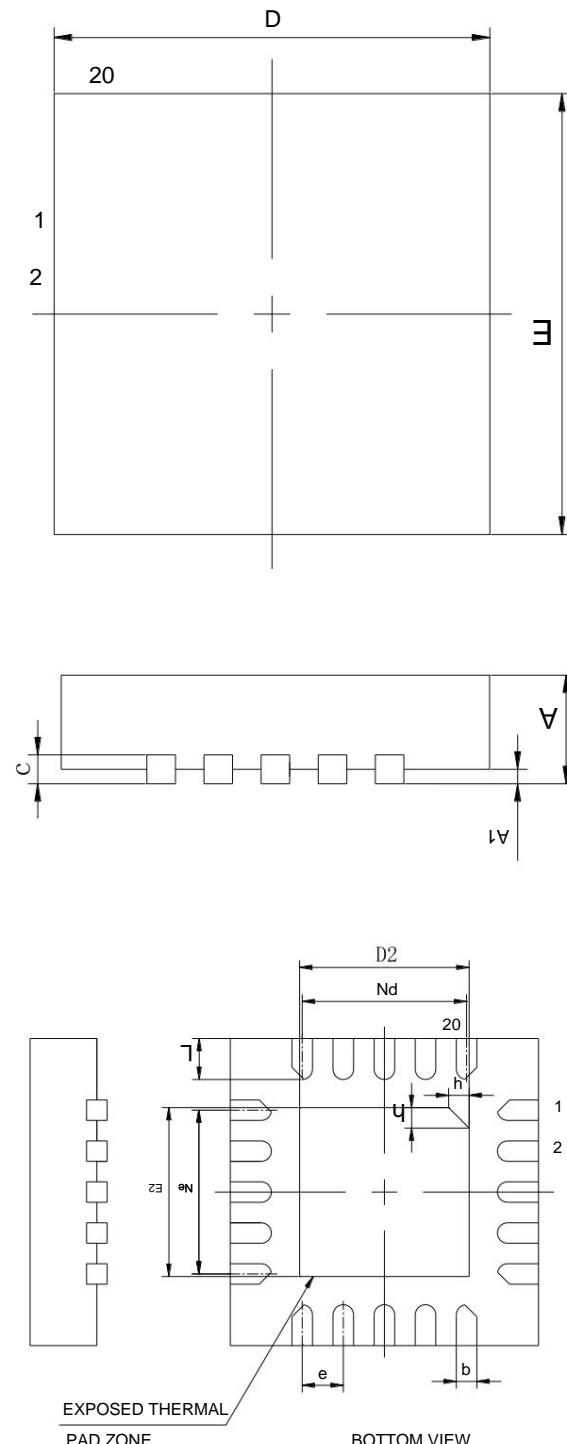
Notice:

- Each group of power supplies requires a decoupling capacitor, and the decoupling capacitor should be as close as possible to the corresponding power supply pins.

9. Package Information

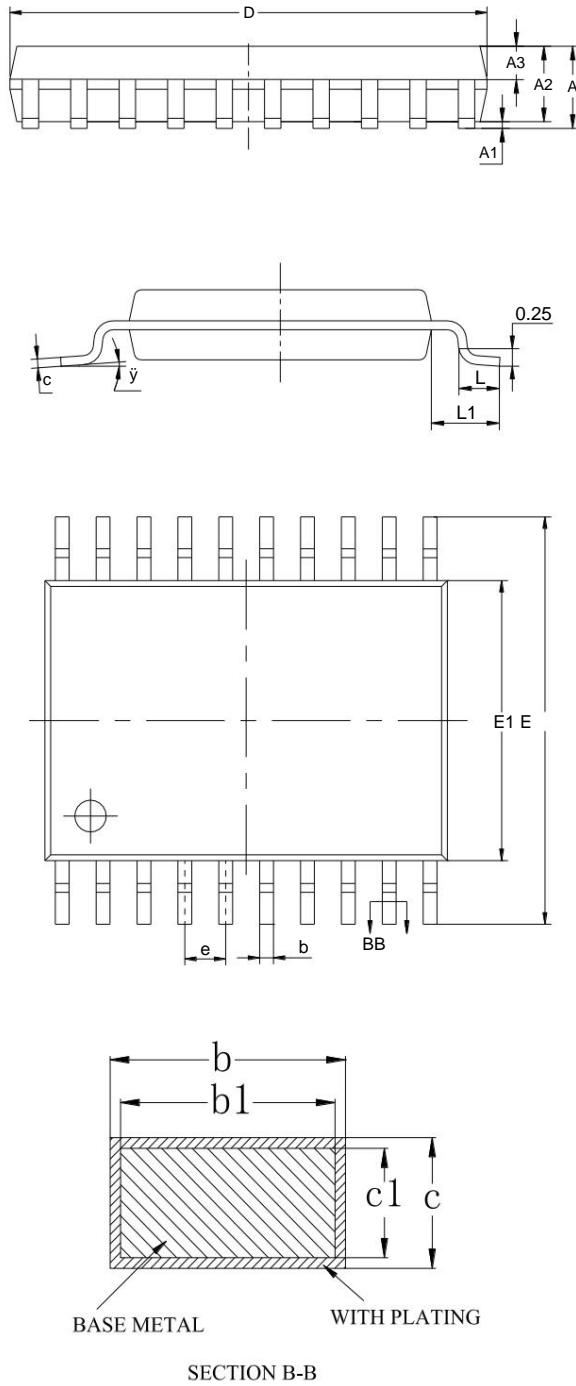
9.1 Package Dimensions

QFN20 package



Symbol	QFN20 (3x3) millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	--	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30
L/F carrier size (Mil)	75x75		

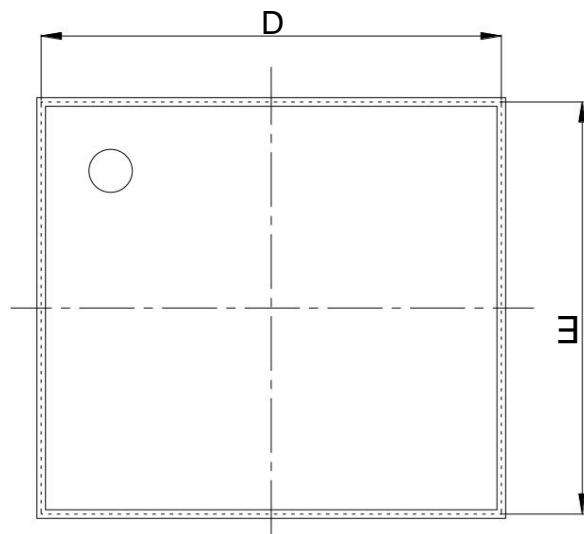
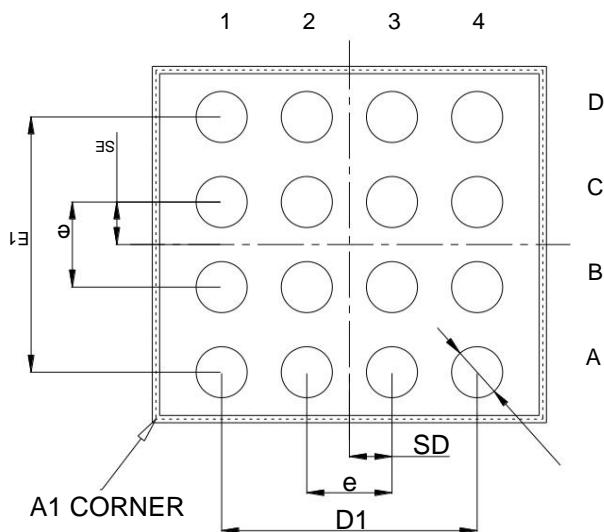
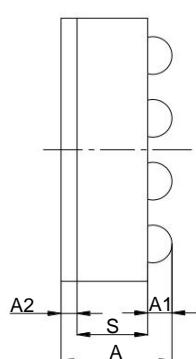
TSSOP20 package



Symbol	TSSOP20 mm		
	Min	Nom	Max
A	--	--	1.20
A1	0.05	--	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	--	0.28
b1	0.19	0.22	0.25
c	0.13	--	0.18
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
ÿ	0	--	8°

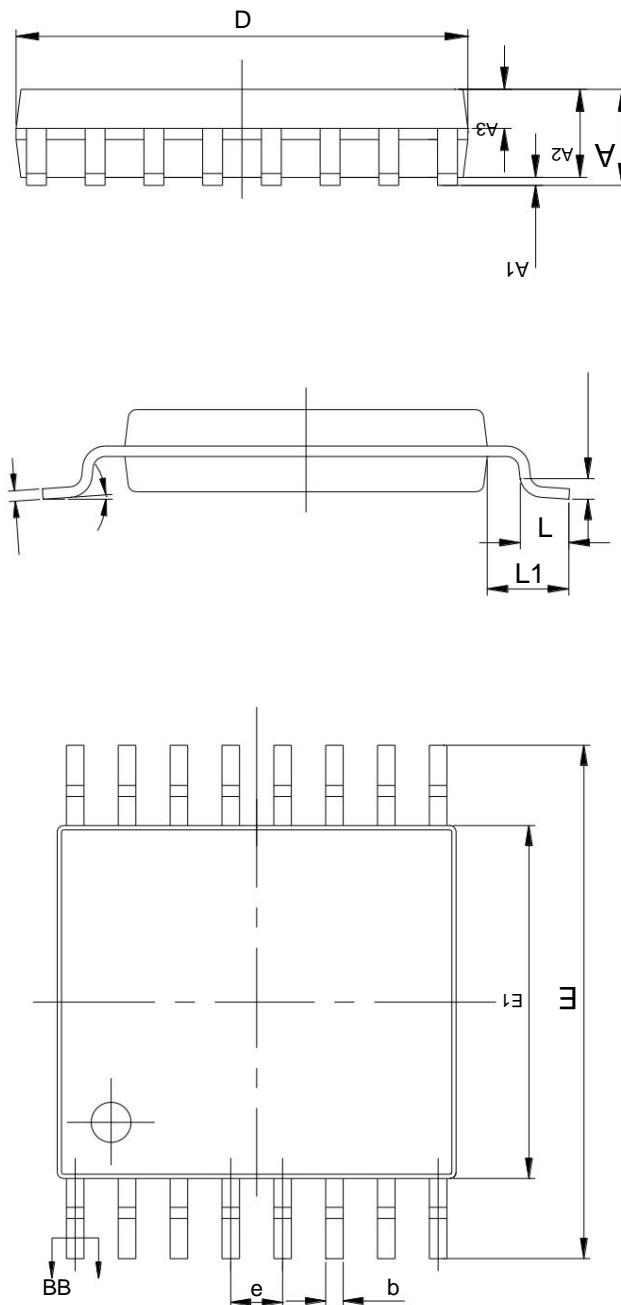
NOTE:

- Dimensions "D" and "E1" do not include mold flash.

CSP16 package**TOP VIEW****BOTTOM VIEW****SIDE VIEW**

Symbol	CSP16 mm		
	Min	Nom	Max
A	0.496	0.533	0.57
A1	0.148	0.168	0.188
A2	0.037	0.04	0.043
b	0.18	0.21	0.24
S	0.3115	0.325	0.3385
D	1.565	1.59	1.615
E	1.411	1.436	1.461
e	0.35BSC		
D1	1.05BSC		
E1	1.05BSC		
SD	0.175		
SE	0.175		
n	16		

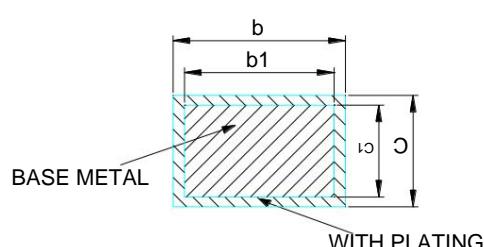
TSSOP16 package



Symbol	TSSOP16 mm		
	Min	Nom	Max
A	--	--	1.20
A1	0.05	--	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	--	0.28
b1	0.19	0.22	0.25
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
ÿ	0	--	8°

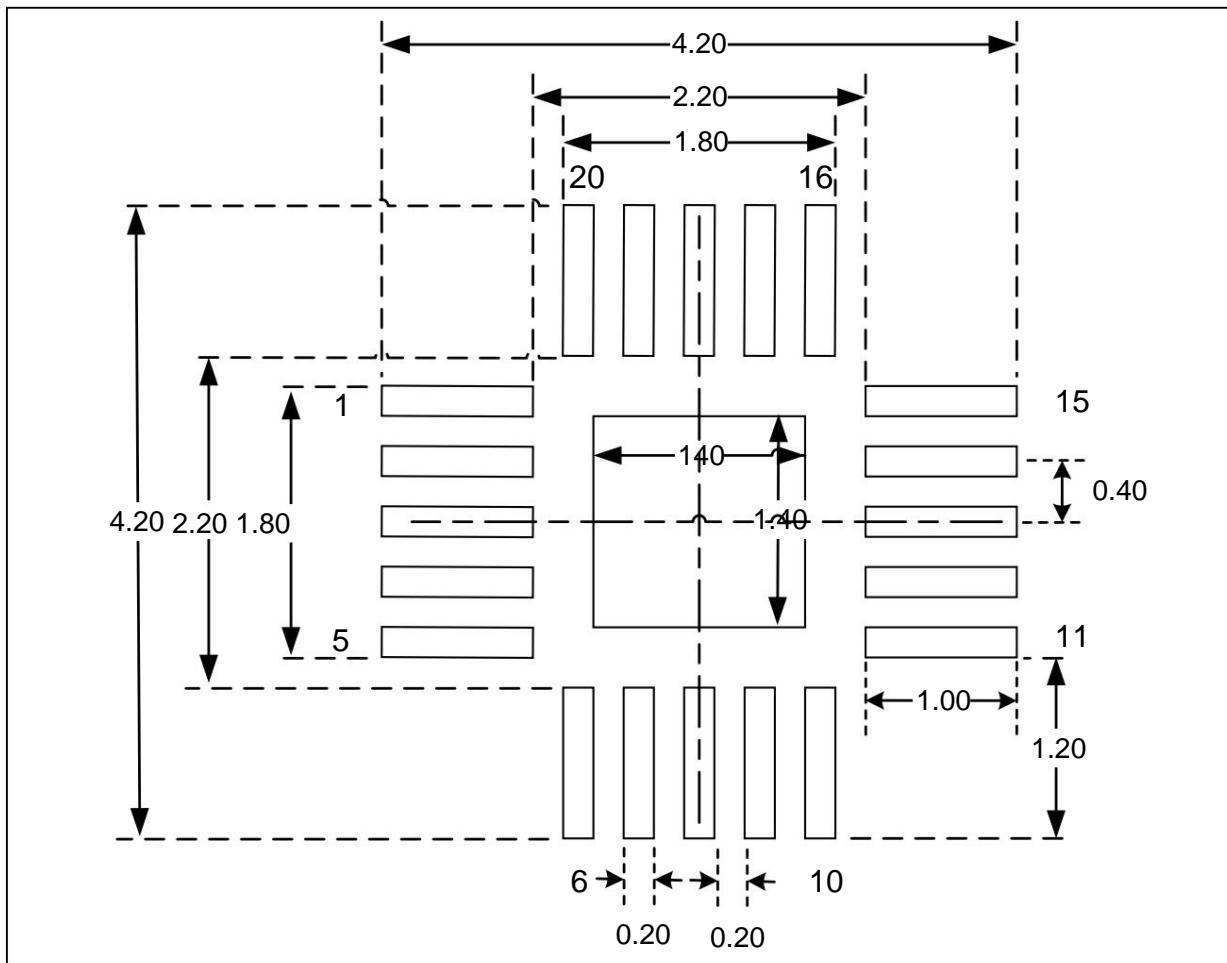
NOTE:

- Dimensions "D" and "E1" do not include mold flash.



9.2 Schematic diagram of pad

QFN20 package (3mm x 3mm)

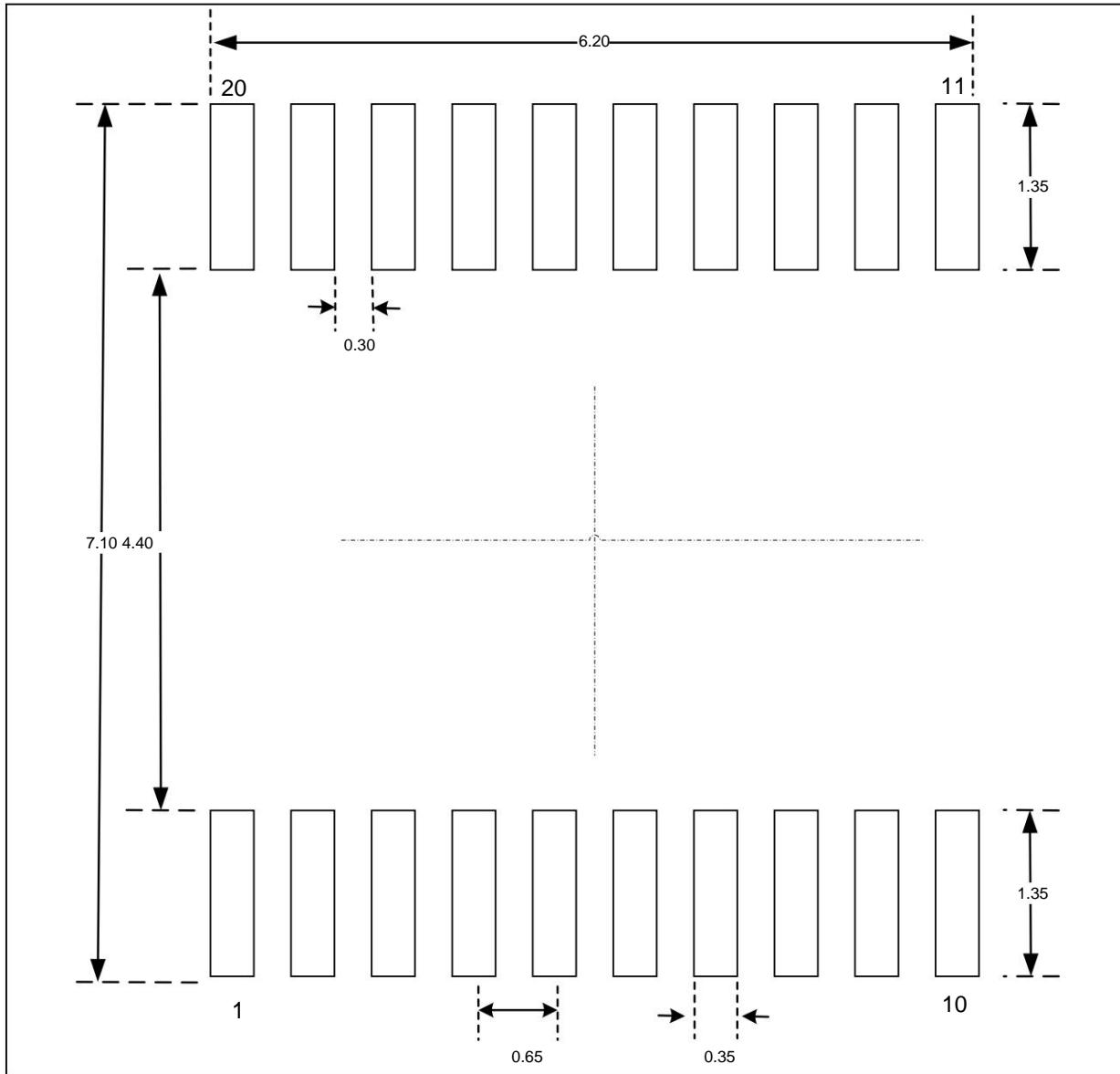


NOTE:

- Dimensions are expressed in millimeters.

- Dimensions are for reference only.

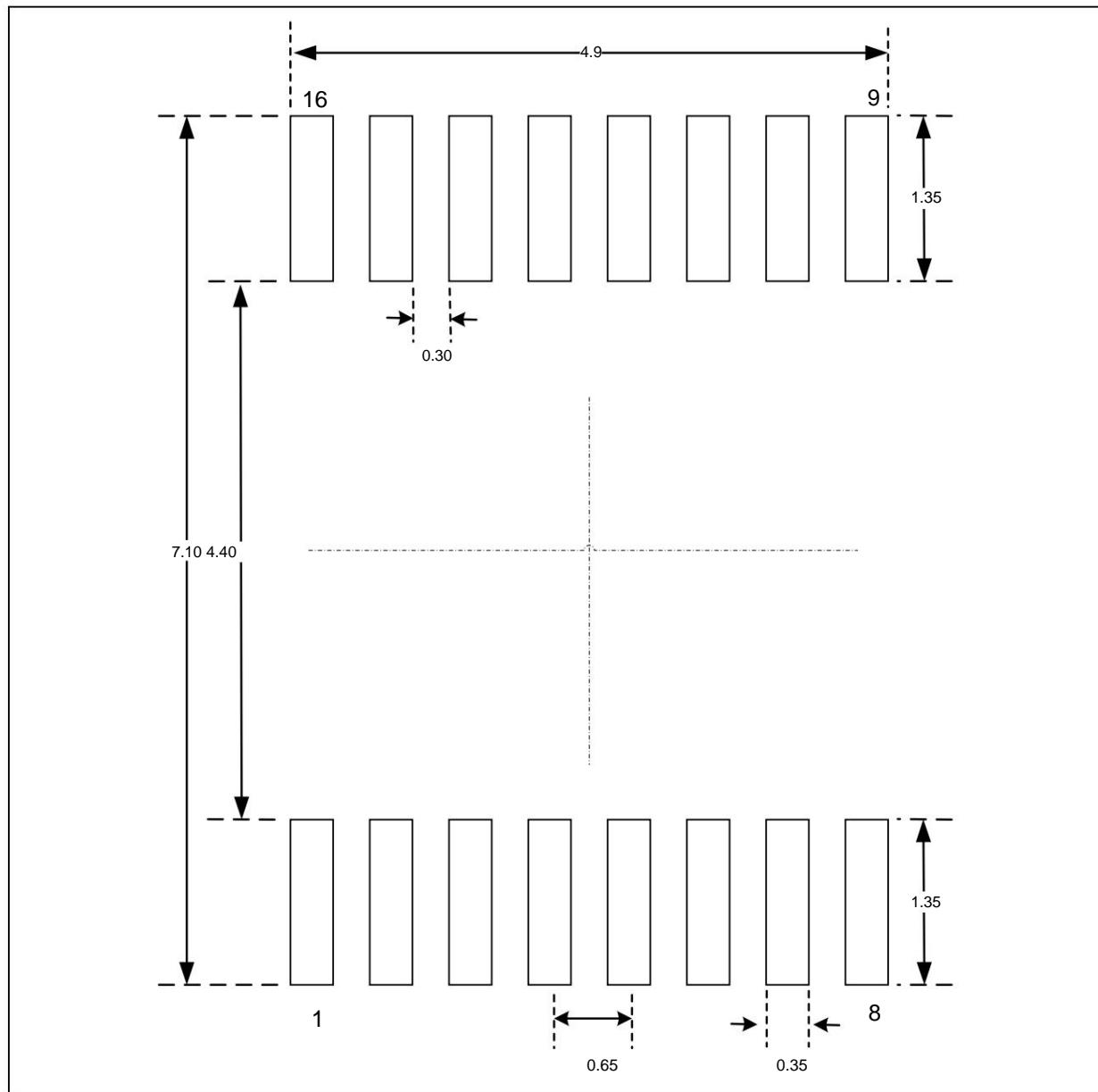
TSSOP20 package

**NOTE:**

- Dimensions are expressed in millimeters.

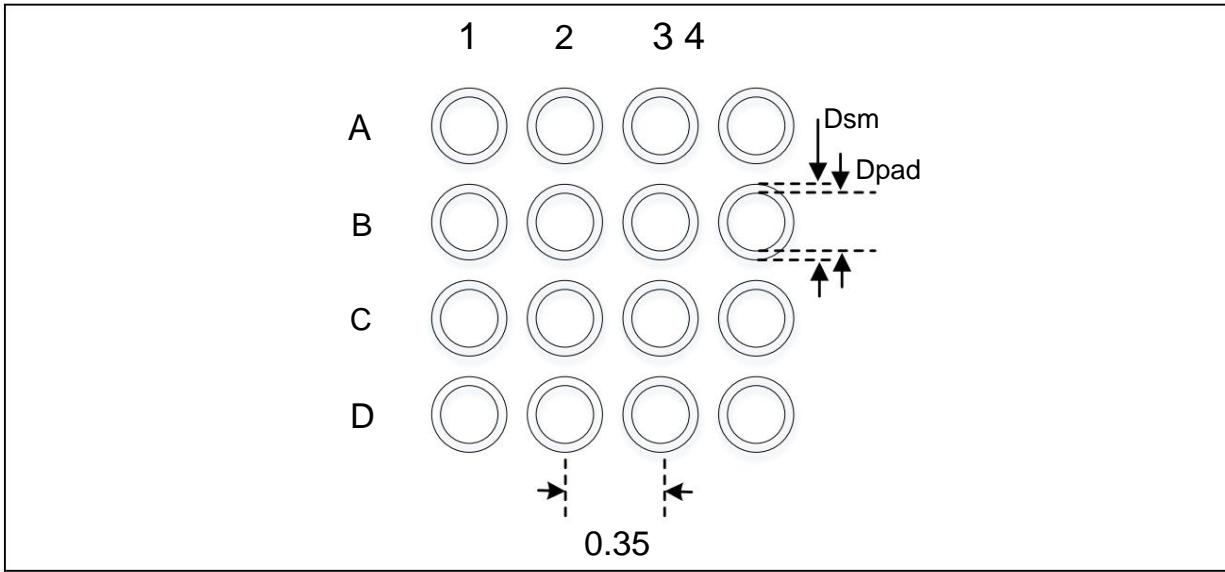
- Dimensions are for reference only.

TSSOP16 package

**NOTE:**

- Dimensions are expressed in millimeters.

- Dimensions are for reference only.

CSP16 package**NOTE:**

- Dimensions are expressed in millimeters.

- Dimensions are for reference only.

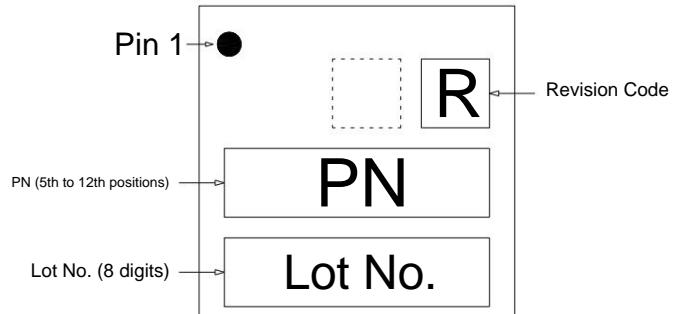
CSP16 recommended PCB design rules(0.35mm pitch)

Dimension	Recommended values
Pitch	0.35mm
Dpad	0.210mm
Dsm	0.275mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.235mm
Stencil thickness	0.100mm

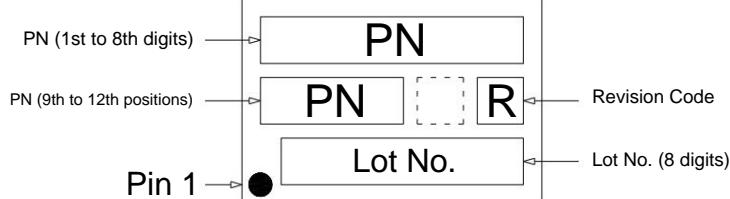
9.3 Silkscreen Instructions

The pin 1 position and information description of the silk screen on the front side of each package are given below.

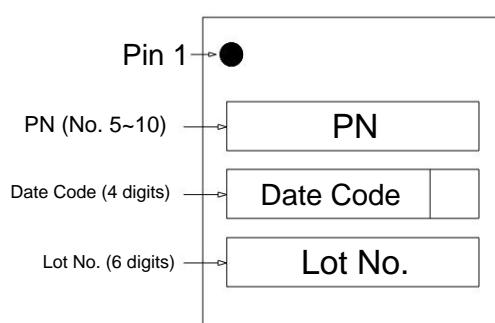
QFN20 package (3mm x 3mm)



TSSOP20 package / TSSOP16 package



CSP16 package



Notice:

- The blank boxes in the figure above represent optional flags related to production, which are not described in this section.



9.4 Package Thermal Resistance Coefficient

When the packaged chip works under the specified working environment temperature, the junction temperature T_j (°) of the chip surface can be calculated according to the following formula:

$$T_j = T_{amb} + (PD \times \dot{\gamma}_{JA})$$

$\dot{\gamma}$ T_{amb} refers to the working environment temperature when the packaged chip is working, the unit is °;

$\dot{\gamma} \dot{\gamma}_{JA}$ refers to the thermal resistance coefficient of the package to the working environment, the unit is °C/W;

$\dot{\gamma} PD$ is equal to the sum of the chip's internal power consumption and I/O power consumption, and the unit is W. The internal power consumption of the chip is the $IDD \times VDD$ of the product, the I/O power

Power consumption refers to the power consumption generated by the I/O pins when the chip is working. Usually, the value of this part is very small and can be ignored.

The junction temperature T_j of the chip surface when the chip works under the specified working environment temperature cannot exceed the maximum allowable junction temperature TJ of the chip.

Package Type and Size	Thermal Resistance Junction-ambient Value ($\dot{\gamma}_{JA}$)	Unit
QFN20 3mm x 3mm / 0.4mm pitch	70 +/- 10%	°C/W
TSSOP16	105 +/- 10%	°C/W
TSSOP20	91 +/- 10%	°C/W

Table 9-1 Thermal resistance coefficient table of each package



10. Ordering Information

Part Number	HC32L110C6UA SFN20TR	HC32L110C6PA TSSOP20	HC32L110B6PA TSSOP16	HC32L110B6YA CSP16TR	HC32L110C4UA SFN20TR	HC32L110C4PA TSSOP20	HC32L110B4PA TSSOP16	HC32L110B4PA TSSOP16TR
Flash	32KB	32KB	32KB	32KB	16KB	16KB	16KB	16KB
RAM	4KB	4KB	4KB	4KB	2KB	2KB	2KB	2KB
GPIO	16+1	16+1	12+1	12+1	16+1	16+1	12+1	12+1
Vdd	1.8~5.5V							
Timer	6	6	6	6	6	6	6	6
LPTimer	1	1	1	1	1	1	1	1
RTC	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
UART	2	2	2	2	2	2	2	2
LPUART	1	1	1	1	1	1	1	1
I2C	1	1	1	1	1	1	1	1
SPI	1	1	1	1	1	1	1	1
ADC(12bit)	9ch	9ch	6ch	6ch	9ch	9ch	6ch	6ch
Vcomp	2	2	2	2	2	2	2	2
LVD	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
LVR	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ	ÿ
Package	QFN20(3*3)	TSSOP20	TSSOP16	CSP16	QFN20(3*3)	TSSOP20	TSSOP16	TSSOP16
pin pitch	0.4mm	0.65mm	0.65mm	0.35mm	0.4mm	0.65mm	0.65mm	0.65mm
chip thickness	0.75mm	1.2mm	1.2mm	0.535mm	0.75mm	1.2mm	1.2mm	1.2mm
Shipping form	reel	Tube	Tube	reel	reel	Tube	Tube	reel

Before ordering, please contact the sales window for the latest mass production information.

11. Version record & contact information

Version revision date	Summary of revisions
Rev1.0 2018/1/23	The first edition of the HC32L110 series data sheet is released.
Rev1.1 2018/4/4	version update.
Rev1.2 2018/4/17	Revised Flash parameters.
Rev1.3 2018/5/3	Updated VC electrical parameters.
Rev1.4 2018/9/25	Adjusted the layout, updated Chapter 7 Electrical Characteristics, and added Chapter 9 Ordering Information.
Rev1.5 2018/11/15	Added "Silkscreen Instructions" in Chapter 8, and corrected QFN20 / Tssop20 / Tssop16 package dimensions.
Rev1.6 2018/11/27	Revised name: UART2yLPUART, added "Note" in Chapters 3 and 4.
Rev1.7 2019/2/22	Revised the following data: yADC characteristics yESD characteristics yECFLASH minimum value in memory characteristics yQFN20/TSSOP16 Package silkscreen instructions yAdd NOTE to package size yUpdate ordering information yAdd AVCC/AVSS to pin configuration.
Rev1.8 2019/6/21	Corrected the following data: y The UID address is corrected to 0x0010_0E74-0x0010_0E7F y The programming mode is corrected y The QFN index is updated Foot layout drawing style yAdd the shipping form to the ordering information.
Rev1.9 2019/12/6	Revised the following data: y Typical application circuit diagram y ADC characteristic unit y XTH and XTL in external clock source characteristics Precautions.
Rev2.0 2020/1/17	Revised the following data: y Added CSP16 package y Description of silk screen.
Rev2.1 2020/3/6	Add a note to "Programming Mode" in the introduction.
Rev2.2 2020/4/30	Corrected the following data: yAdd VCC/3 accuracy in ADC characteristics yCorrect clerical error in 7.3.7 yRCL oscillator accuracy in 7.3.8.
Rev2.3 2020/7/31	Amend the following data: yAdd Sections 7.3.16, 7.3.17, 9.2, 9.4; y7.3.10 Level; y7.3.1 Internal AHB/APB Clock Frequency; y7.3.12 Input Characteristics—The values of VIH and VIL in ports P0, P1, P2, P3, RESET.
Rev2.4 2020/9/30	Revised the following data: yClock system description in Introduction; yRCH oscillator accuracy in 7.3.8; yVIL and VIH in 7.3.13; yAdded SPI feature.
Rev2.5 2021/5/31	Amend the following data: y Modify the statement; y tHD.STA and tSU.STO parameters in I2C characteristics; y Serial peripheral interface SPI in the introduction; yData retention period in the memory feature; yAdd the gm parameter in the external clock source feature.



If you have any comments or suggestions in the process of purchasing and using, please feel free to contact us.

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