HDSC 华大半导体 HUADA SEMICONDUCTOR

32 -bit microcontroller

HC32L110 / HC32F003 / HC32F005 Series Hardware Development Guide

Applicable object

series	Product number
HC32L110	HC32L110C6UA HC32L110C6PA HC32L110C4UA HC32L110C4PA HC32L110B6PA HC32L110B4PA
HC32F003	HC32F003C4UA HC32F003C4PA
HC32F005	HC32F005C6UA HC32F005C6PA HC32F005D6UA

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1 Summary

This application note mainly introduces the peripheral hardware design based on HC32L110 / HC32F003 / HC32F005 series chips, including

Including power supply, GPIO, crystal oscillator, UART, SWD, I2C, device package, minimum system reference hardware design, etc.

Notice:

- This application note is an application supplement for the HC32L110 / HC32F003 / HC32F005 series and is not intended to replace the user manual.

  Please refer to the user manual for specific functions and register operations.

2 Power

Each power supply (DVCC/AVCC) requires a decoupling capacitor of 4.7uF + bypass capacitor of 0.1uF. During PCB layout, the capacitor

As close as possible to the corresponding power supply pins.

The VCAP pin of the chip: LDO core power supply output Pin (for internal circuit use only, need to connect 4.7uF + 10nF

coupling capacitor); no external load can be connected.

All power (DVCC/AVCC) and ground (DVSS/AVSS) pins must always be connected to a power supply within the operating voltage range of the MCU

on the electrical system.

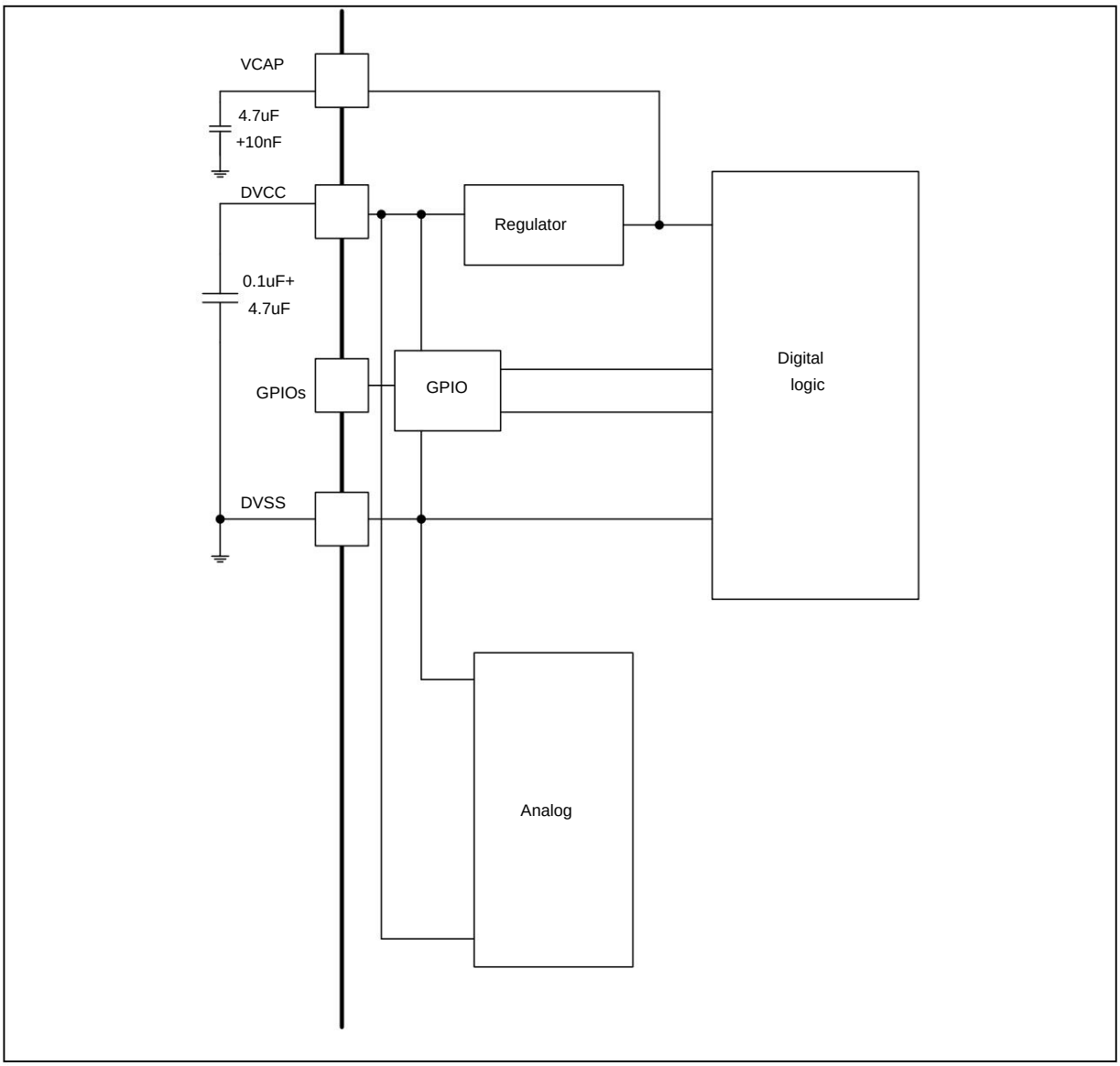

Figure 1 Decoupling capacitor

MCU working voltage range: 1.8VÿDVCC/AVCCÿ5.5V.

3 Reset circuit

When designing, please connect a capacitor between the RESETB pin and ground (DVSS) to form an RC delay circuit with the pull-up resistor;

If RESETB is not used in use, RESETB must be pulled up to DVCC through a resistor (recommended 4.7K).

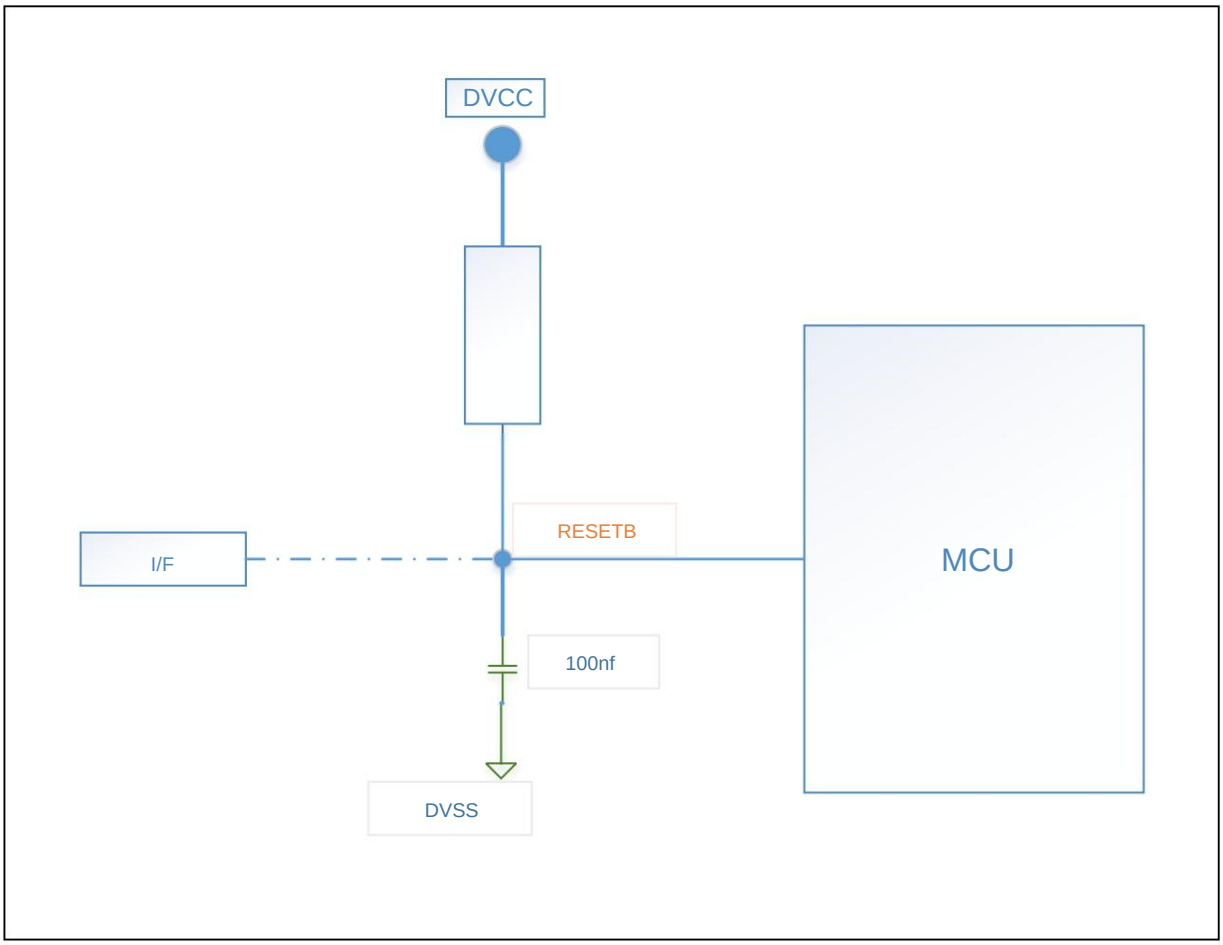

Figure 2 NRST circuit

4 GPIO

Up to 16 GPIO ports can be provided, some of which are multiplexed with analog ports. Each port is registered by an independent control bit to control. Supports edge-triggered interrupts and level-triggered interrupts, which can wake up the MCU from various ultra-low power modes Operating mode. Support Push-Pull CMOS push-pull output, Open-Drain open-drain output. Built-in pull-up resistor, pull-down power resistor, with Schmitt trigger input filtering. The output drive capability is configurable, and the maximum current drive capability is 12mA. force. 16 general-purpose IOs can support external asynchronous interrupts.

Notice:

- When the NRST function is not used, the RESETB port can also be configured as GPIO input port P00.

5 Crystal oscillator circuit design

5.1 Circuit Design

A high-speed external clock (XTH) can be generated using a 4~32MHz crystal/ceramic resonator oscillator. two quotes

Both pins have load capacitors. In applications, the resonator and load capacitors must be placed as close as possible to the oscillator pins to minimize output.

out distortion and settling time at startup. For detailed parameters of crystal resonators (frequency, package, accuracy, etc.), please consult

the corresponding manufacturer.

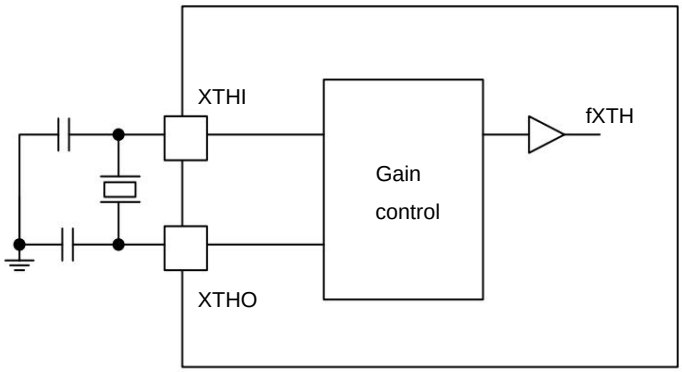

Figure 3 Schematic diagram of external high-speed crystal oscillator

The low-speed external clock (XTL) can be generated using a 32.768KHz crystal/ceramic resonator oscillator. two quotes

The pins have load capacitors. In the application, the resonator and load capacitors must be placed as close as possible to the oscillator pins to minimize the output

out distortion and settling time at startup. For detailed parameters of crystal resonators (frequency, package, accuracy, etc.), please consult the

the appropriate manufacturer.

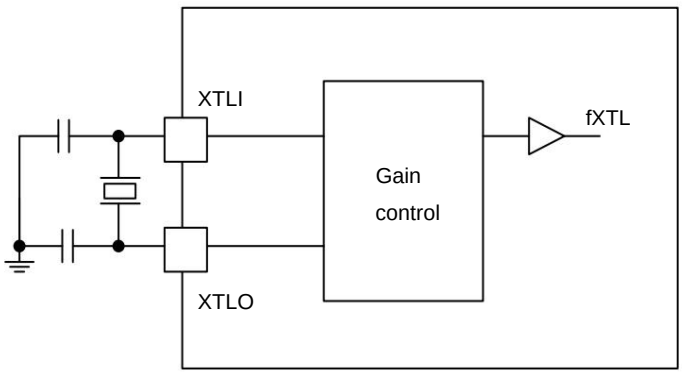

Figure 4 Schematic diagram of external low-speed crystal oscillator

Notice:

- When reading the datasheet provided by the crystal oscillator manufacturer, the parameter load capacitance CL (Load capacitance) refers to the electrical

The total effective capacitance across the two ends of the crystal in the circuit is not the external matching capacitance of the crystal oscillator; in addition, when calculating the crystal oscillator circuit

When matching the capacitance value of the crystal oscillator circuit PCB, the parasitic capacitance from the layout trace to the ground of the crystal oscillator circuit PCB needs to be taken into account.

5.2 Circuit layout

ÿ The external crystal unit and load capacitor should be as close as possible to the chip side.

ÿ The external crystal oscillator signal line should be as short as possible. The trace width should not be too thin, and the thinnest should not be lower than the width of the chip pin.

ÿ There should be a complete ground cover on the adjacent layer of the crystal oscillator local circuit.

ÿ The ground wire should be used as a guard ring around the external crystal oscillator, and the ground ring wire should be fully grounded (more than the ground).

hole) to reduce the mutual interference between the external crystal oscillator signal and other signals. (Refer to Figure 5)

ÿ The crystal oscillator circuit should pay attention to the clean local signal and avoid external interference. Try not to place near the crystal oscillator circuit or adjacent layers

Routing, especially high-speed lines, power lines, clock lines, etc. are not allowed.

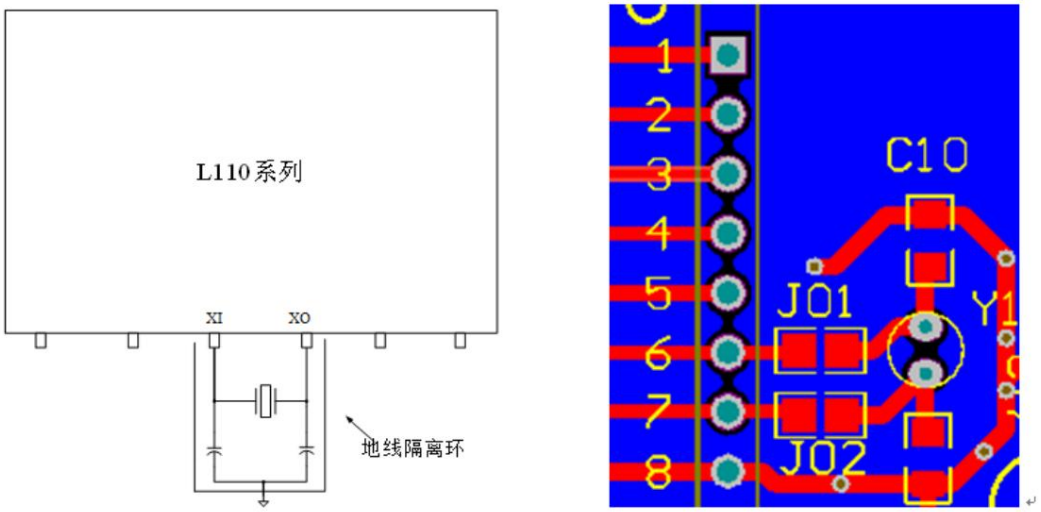

Figure 5 Ground wire isolation ring of crystal oscillator circuit

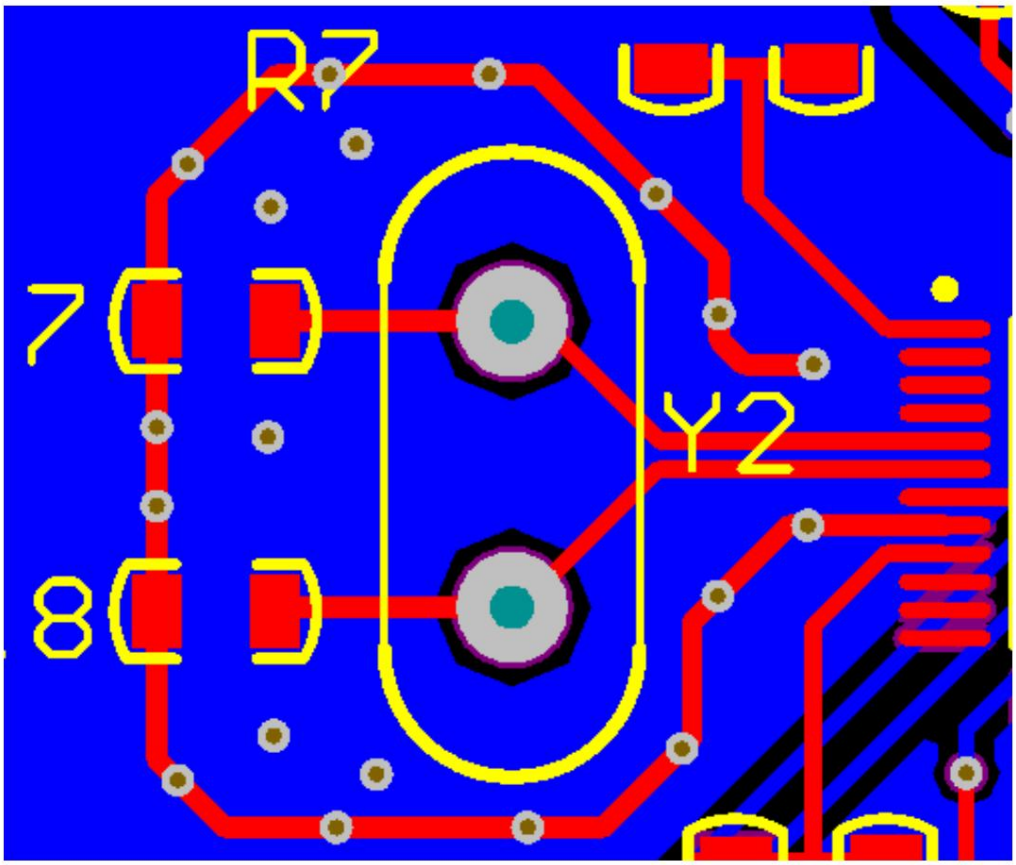

Figure 6 Schematic diagram of the overall layout, filtering, and ground isolation design of the crystal oscillator circuit

6 Common interface design

6.1 UART interface design

For UART interface design, it is recommended that the TX/RX signal line be connected to a 4.7Kÿ pull-up resistor to the power supply.

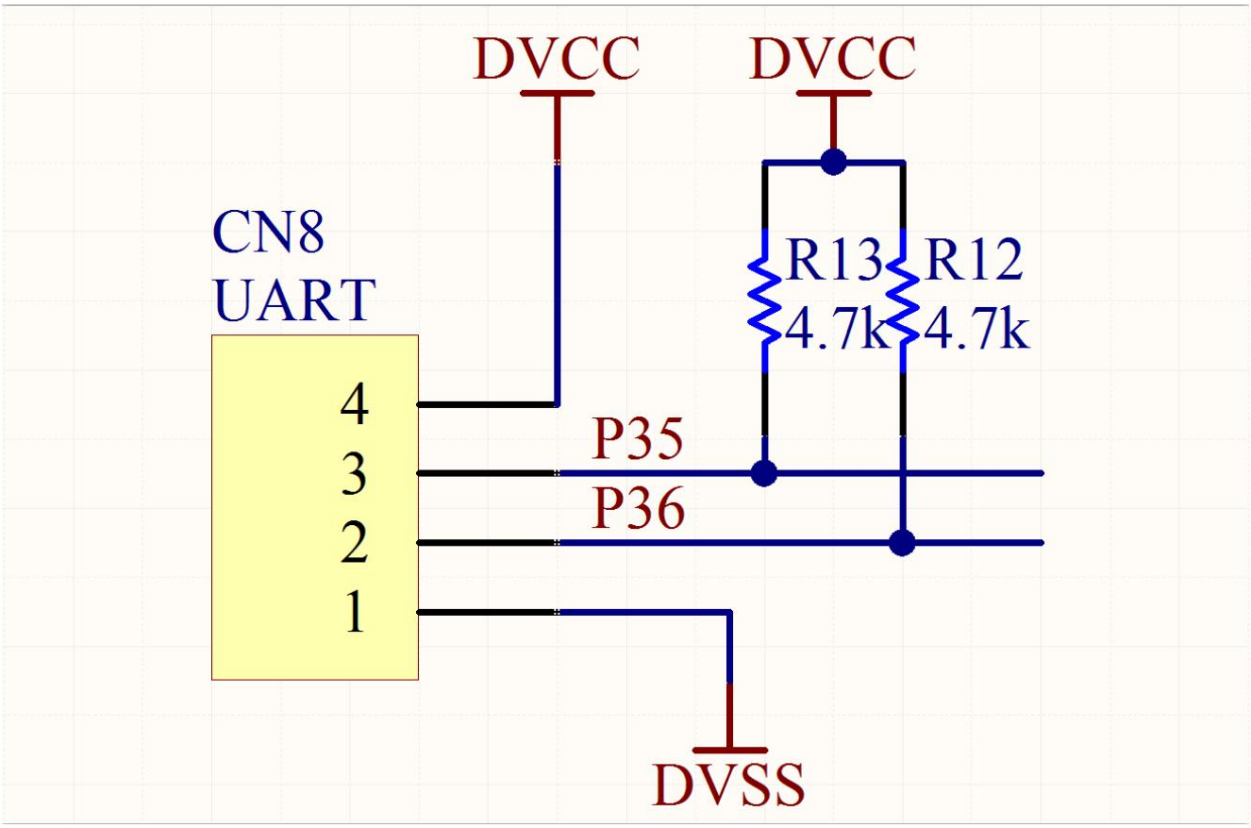

Figure 7 Schematic diagram of UART interface design

6.2 SWD interface design

For SWD interface design, it is recommended that the SWCLK/SWDIO signal line be connected to a 4.7Kÿ pull-up resistor to the power supply.

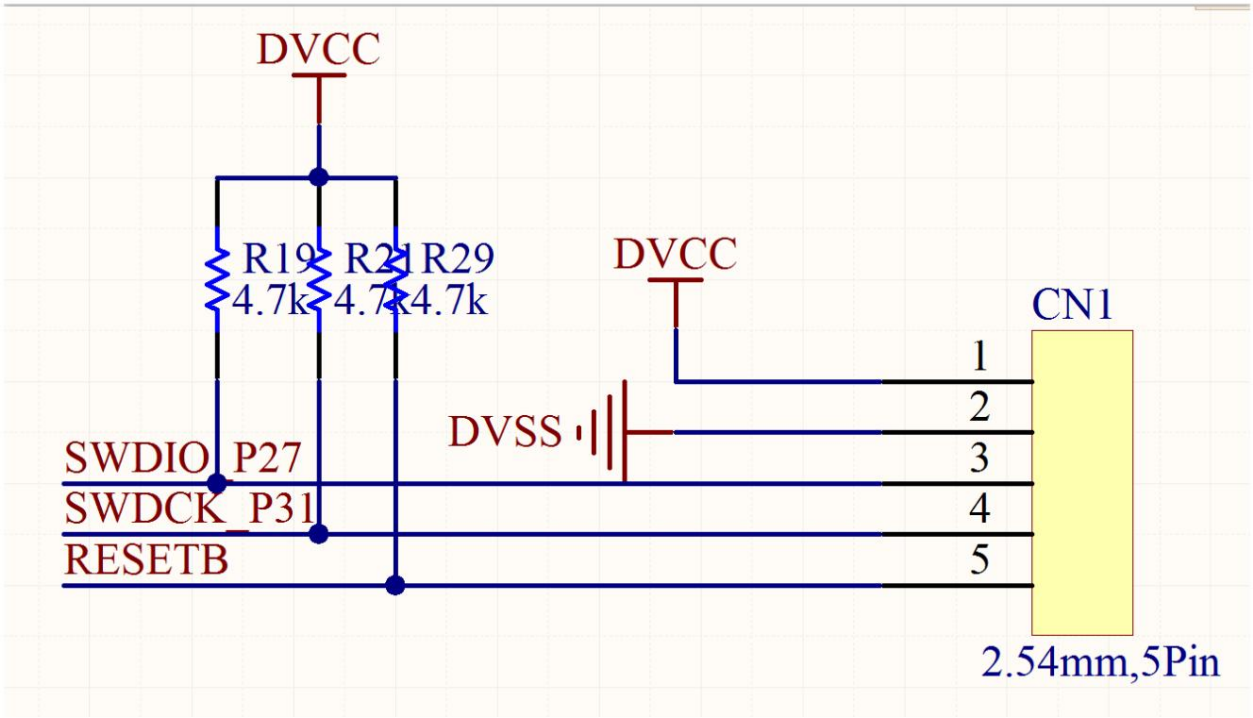

Figure 8 Schematic diagram of SWD interface design

6.3 I2C Interface Design

For I2C interface design, it is recommended that the I2C_SCL/I2C_SDA signal line be connected to a 1Kÿ pull-up resistor to the power supply.

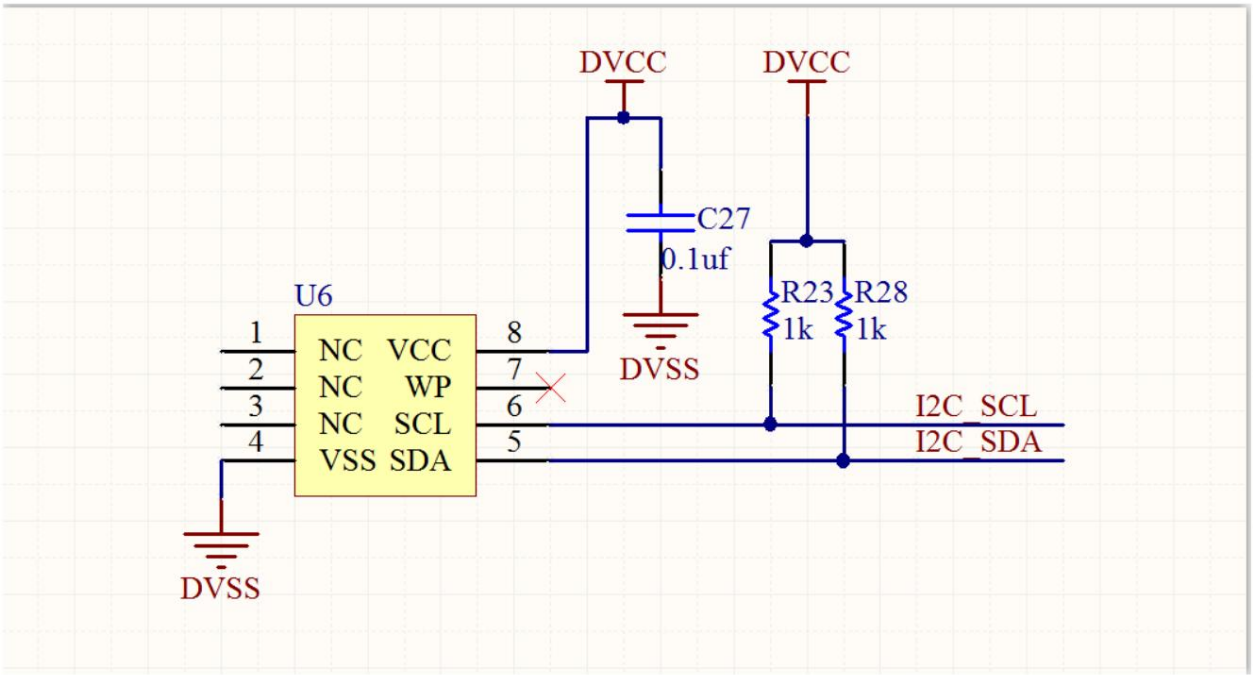

Figure 9 Schematic diagram of I2C interface design

7 Chip Package PCB Layout

Please refer to the "Packaging Information" chapter of the chip data sheet released by our company. Please design the chip strictly according to the data sheet specification Encapsulate Layout. In addition, we provide all PCB package libraries for this series of chips, please refer to

http://www.hdsc.com.cn/mcu.htm.

8 Application circuit (minimum system, for reference only)

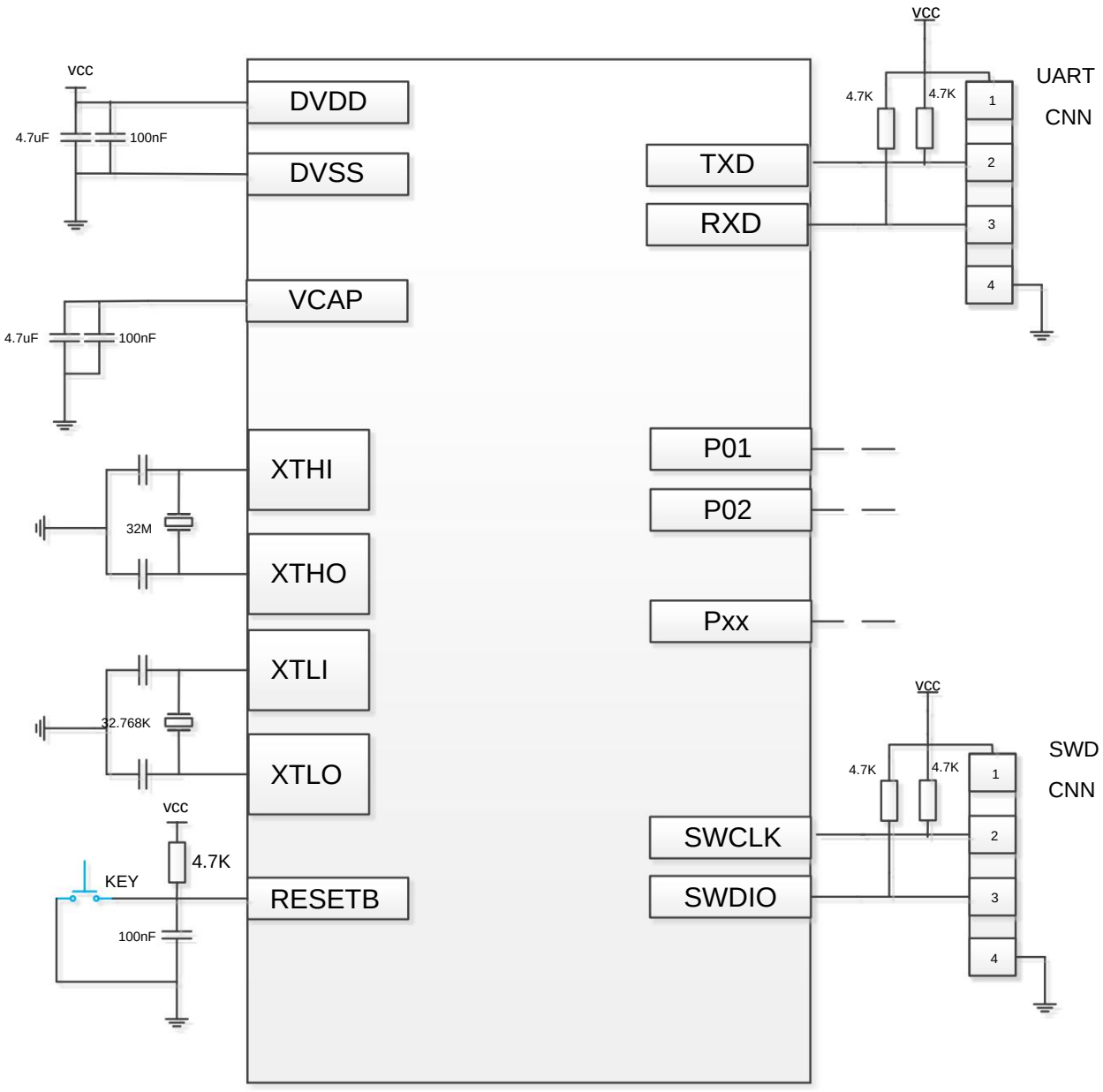

Figure 10 Reference diagram of chip minimum system design

9 Pin configuration comparison between Huada HC32F003/HC32F005 and X003 series of friends

9.1 TSSOP20 Pin Configuration Differences

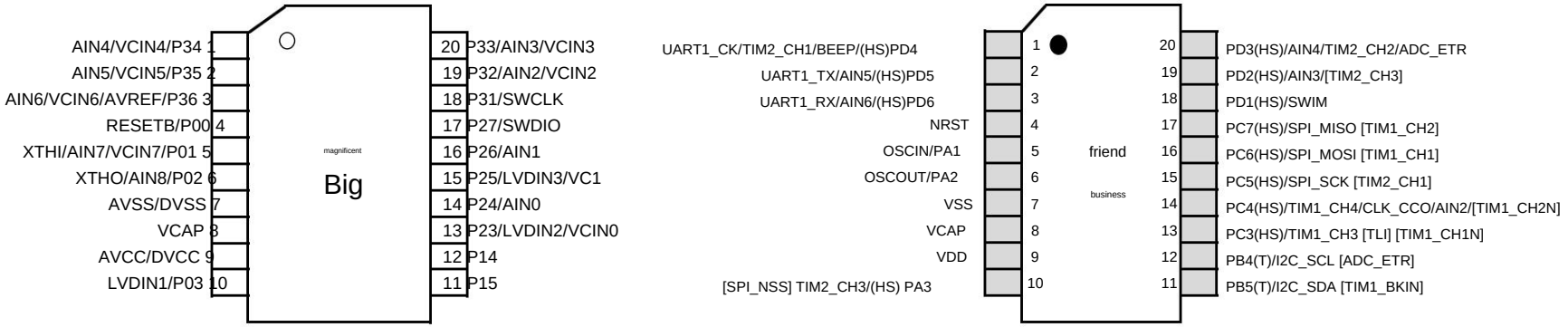

Figure 11 HC32F003/HC32F005 and X003 pin configuration comparison

Table 1 List of differences in pin configuration between Huada chip and TSSOP20 chip from friends

DH	**HC32L110C6PA/ HC32L110C4PA /HC32F005C6PA/ HC32F005C4PA**	**x003**
Pin17	P27/SWDIO	PC7
Pin18	P31/SWCLK	PD1/SWIM

illustrate:

- BGI's chip Pin17/Pin18 constitutes the SWD programming port, and the friend's chip Pin18 is the single-line program programming port SWIM.

10 Additional information

Technical support information: www.hdsc.com.cn

11 Version Information & Contact Information

date	Version revision record	
2019/6/14	The first version of Rev1.0 is released.	

If you have any comments or suggestions in the process of purchasing and using, please feel free to contact us.

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