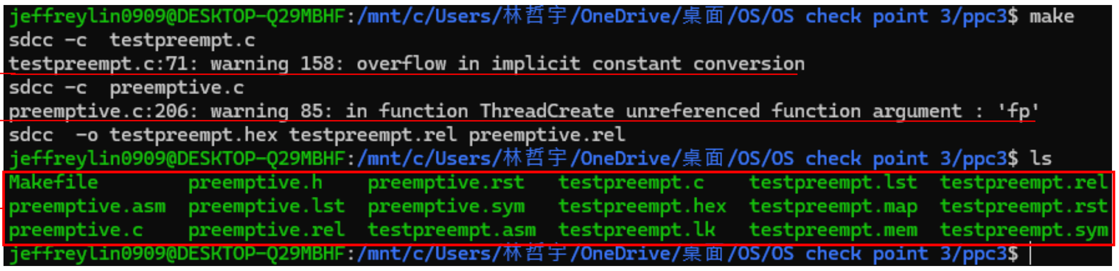
Programming Project Checkpoint 3

111062311 林哲宇

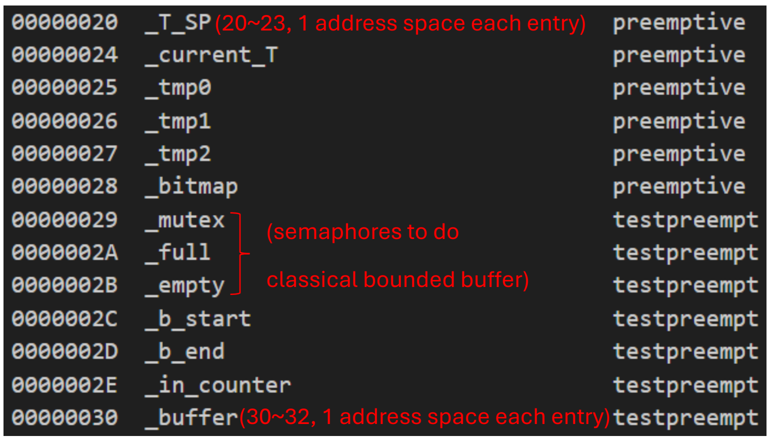
1. Screenshot for compilation:



```
jeffreylin0909@DESKTOP-Q29MBHF:/mnt/c/Users/林哲宇/OneDrive/桌面/OS/OS check point 3/ppc3$ make
sdcc -c  testpreempt.c
testpreempt.c:71: warning 158: overflow in implicit constant conversion
sdcc -c  preemptive.c
preemptive.c:206: warning 85: in function ThreadCreate unreferenced function argument : 'fp'
sdcc  -o testpreempt.hex testpreempt.rel preemptive.rel
jeffreylin0909@DESKTOP-Q29MBHF:/mnt/c/Users/林哲宇/OneDrive/桌面/OS/OS check point 3/ppc3$ ls
Makefile         preemptive.h     preemptive.rst   testpreempt.c    testpreempt.lst  testpreempt.rel
preemptive.asm   preemptive.lst   preemptive.sym   testpreempt.hex  testpreempt.map  testpreempt.rst
preemptive.c     preemptive.rel   testpreempt.asm  testpreempt.lk   testpreempt.mem  testpreempt.sym
jeffreylin0909@DESKTOP-Q29MBHF:/mnt/c/Users/林哲宇/OneDrive/桌面/OS/OS check point 3/ppc3$
```

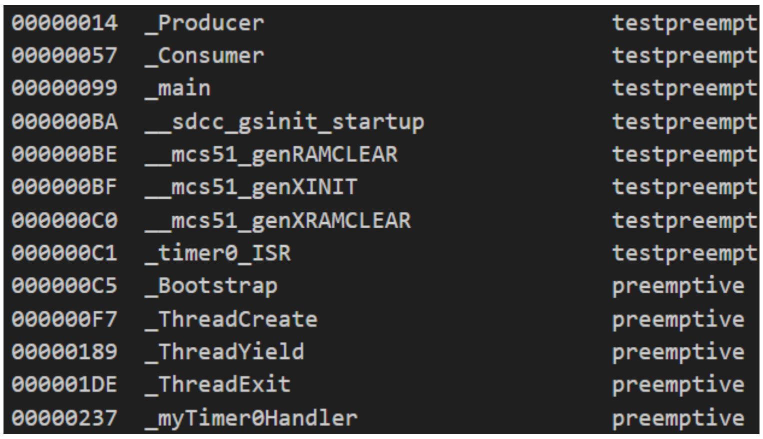
- The warning message is because of setting TH1 to negative number (-6 for UART baud rate), and it's totally safe.
- The warning message is because of using DPH/DPL instead of identifier of parameter, and it's totally safe.
- Files generated after compilation (including .hex and .map).

Note: for better understanding for following explanation, here's the variable address map of my code:



```
00000020  _T_SP (20~23, 1 address space each entry)  preemptive
00000024  _current_T                                 preemptive
00000025  _tmp0                                      preemptive
00000026  _tmp1                                      preemptive
00000027  _tmp2                                      preemptive
00000028  _bitmap                                    preemptive
00000029  _mutex  (semaphores to do                  testpreempt
0000002A  _full                                      testpreempt
0000002B  _empty   classical bounded buffer)         testpreempt
0000002C  _b_start                                   testpreempt
0000002D  _b_end                                     testpreempt
0000002E  _in_counter                                testpreempt
00000030  _buffer(30~32, 1 address space each entry) testpreempt
```

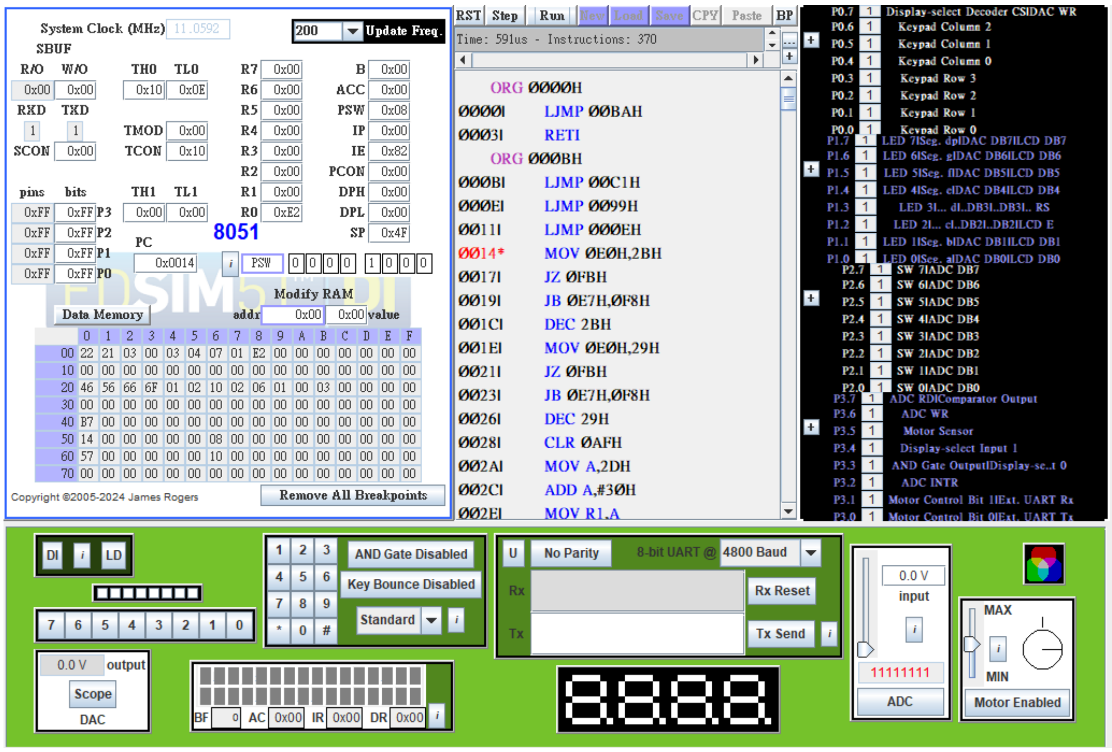
And here's the function address map:



```
00000014  _Producer                 testpreempt
00000057  _Consumer                 testpreempt
00000099  _main                     testpreempt
000000BA  __sdcc_gsinit_startup     testpreempt
000000BE  __mcs51_genRAMCLEAR       testpreempt
000000BF  __mcs51_genXINIT          testpreempt
000000C0  __mcs51_genXRAMCLEAR      testpreempt
000000C1  _timer0_ISR               testpreempt
000000C5  _Bootstrap                preemptive
000000F7  _ThreadCreate             preemptive
00000189  _ThreadYield              preemptive
000001DE  _ThreadExit               preemptive
00000237  _myTimer0Handler          preemptive
```

2. Screenshots and explanation:

- Producer:

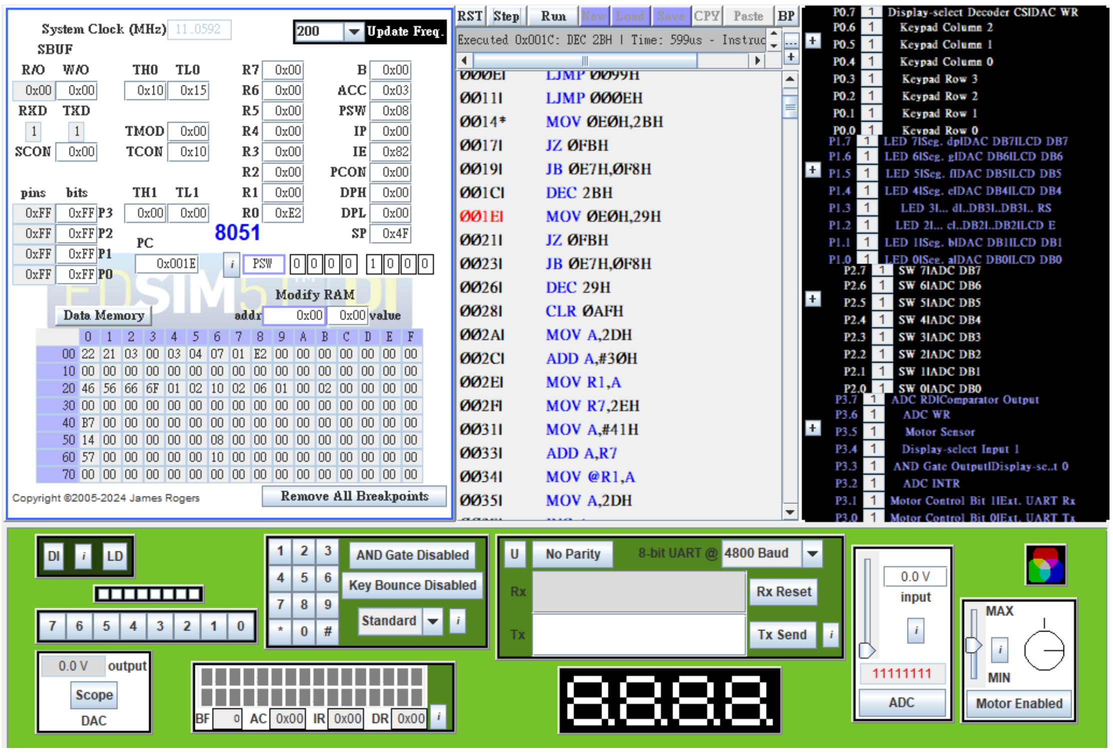


```
System Clock (MHz) 11.0592        200  Update Freq.
SBUF
R/O   W/O     TH0   TL0     R7 0x00     B    0x00
0x00  0x00    0x10  0x0E    R6 0x00     ACC  0x00
RXD   TXD                   R5 0x00     PSW  0x08
1     1       TMOD  0x00    R4 0x00     IP   0x00
SCON  0x00    TCON  0x10    R3 0x00     IE   0x82
                            R2 0x00     PCON 0x00
pins  bits    TH1   TL1     R1 0x00     DPH  0x00
0xFF  0xFF P3 0x00  0x00    R0 0xE2     DPL  0x00
0xFF  0xFF P2              8051         SP   0x4F
0xFF  0xFF P1  PC
0xFF  0xFF P0  0x0014      PSW 0 0 0 0  1 0 0 0
```

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	22	21	03	00	03	04	07	01	E2	00	00	00	00	00	00	00
10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	46	56	66	6F	01	02	10	02	06	01	00	03	00	00	00	00
30	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
40	B7	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
50	14	00	00	00	00	00	08	00	00	00	00	00	00	00	00	00
60	57	00	00	00	00	00	10	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

```
Time: 591us - Instructions: 370

        ORG 0000H
0000|       LJMP 00BAH
0003|       RETI
        ORG 000BH
000B|       LJMP 00C1H
000E|       LJMP 0099H
0011|       LJMP 000EH
0014*       MOV 0E0H,2BH
0017|       JZ 0FBH
0019|       JB 0E7H,0F8H
001C|       DEC 2BH
001E|       MOV 0E0H,29H
0021|       JZ 0FBH
0023|       JB 0E7H,0F8H
0026|       DEC 29H
0028|       CLR 0AFH
002A|       MOV A,2DH
002C|       ADD A,#30H
002E|       MOV R1,A
```

▲ Just enter Producer (mutex=1, full=0, empty=3).

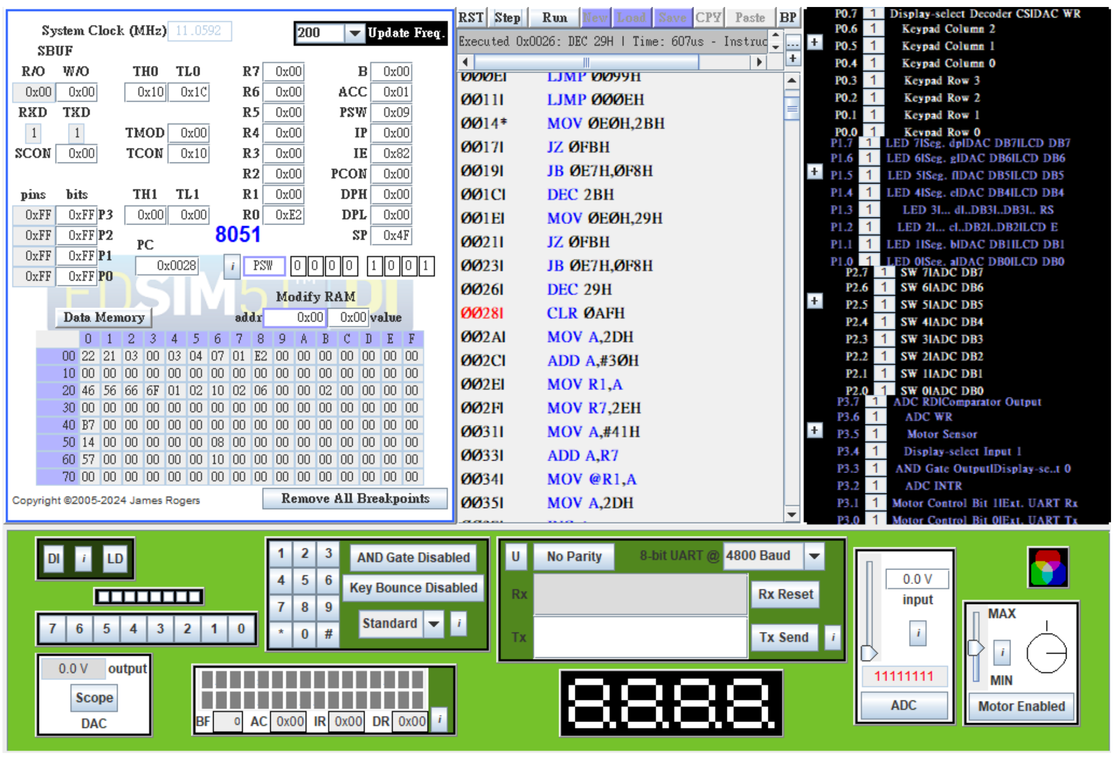


```
System Clock (MHz) 11.0592        200  Update Freq.
SBUF
R/O   W/O     TH0   TL0     R7 0x00     B    0x00
0x00  0x00    0x10  0x15    R6 0x00     ACC  0x03
RXD   TXD                   R5 0x00     PSW  0x08
1     1       TMOD  0x00    R4 0x00     IP   0x00
SCON  0x00    TCON  0x10    R3 0x00     IE   0x82
                            R2 0x00     PCON 0x00
pins  bits    TH1   TL1     R1 0x00     DPH  0x00
0xFF  0xFF P3 0x00  0x00    R0 0xE2     DPL  0x00
0xFF  0xFF P2              8051         SP   0x4F
0xFF  0xFF P1  PC
0xFF  0xFF P0  0x001E      PSW 0 0 0 0  1 0 0 0
```

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	22	21	03	00	03	04	07	01	E2	00	00	00	00	00	00	00
10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	46	56	66	6F	01	02	10	02	06	01	00	02	00	00	00	00
30	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
40	B7	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
50	14	00	00	00	00	00	08	00	00	00	00	00	00	00	00	00
60	57	00	00	00	00	00	10	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

```
Executed 0x001C: DEC 2BH | Time: 599us - Instruc

0011|       LJMP 000EH
0014*       MOV 0E0H,2BH
0017|       JZ 0FBH
0019|       JB 0E7H,0F8H
001C|       DEC 2BH
001E|       MOV 0E0H,29H
0021|       JZ 0FBH
0023|       JB 0E7H,0F8H
0026|       DEC 29H
0028|       CLR 0AFH
002A|       MOV A,2DH
002C|       ADD A,#30H
002E|       MOV R1,A
002F|       MOV R7,2EH
0031|       MOV A,#41H
0033|       ADD A,R7
0034|       MOV @R1,A
0035|       MOV A,2DH
```

▲ After **`SemaphoreWait(empty)`** (mutex=1, full=0, empty=2).

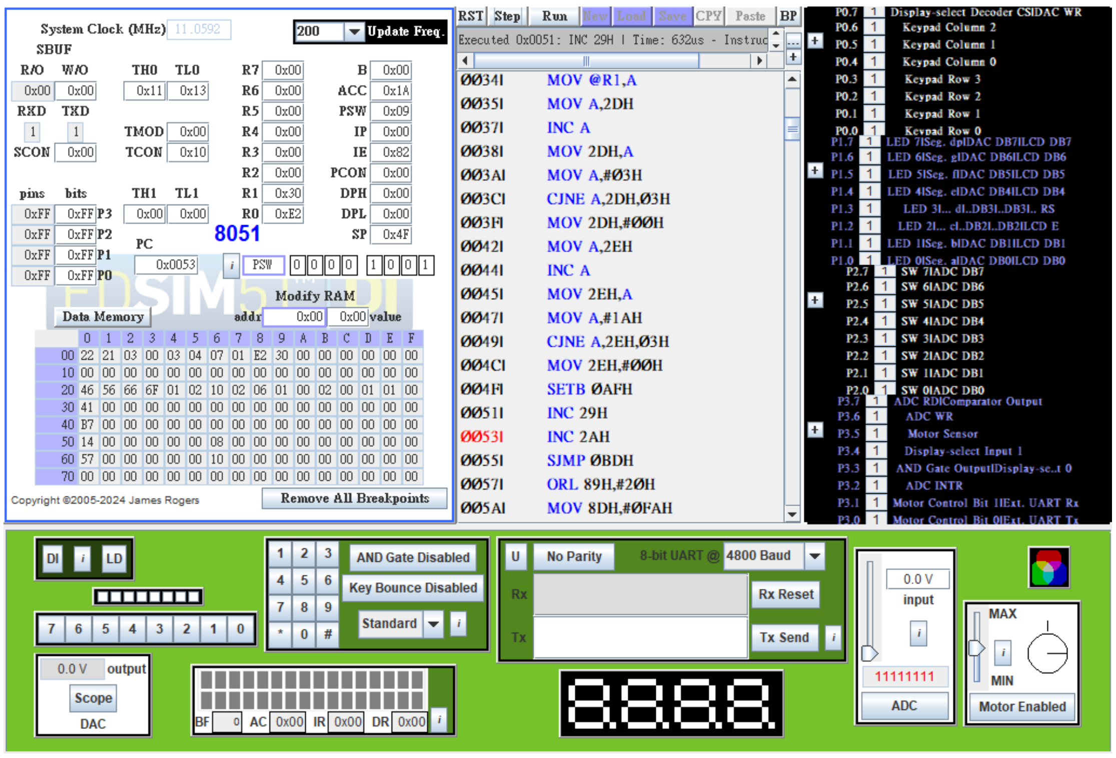


```
System Clock (MHz) 11.0592        200  Update Freq.
SBUF
R/O   W/O     TH0   TL0     R7 0x00    B    0x00
0x00  0x00    0x10  0x1C    R6 0x00    ACC  0x01
RXD   TXD                   R5 0x00    PSW  0x09
1     1       TMOD  0x00    R4 0x00    IP   0x00
SCON  0x00    TCON  0x10    R3 0x00    IE   0x82
                            R2 0x00    PCON 0x00
pins  bits    TH1   TL1     R1 0x00    DPH  0x00
0xFF  0xFF P3 0x00  0x00    R0 0xE2    DPL  0x00
0xFF  0xFF P2          8051            SP   0x4F
0xFF  0xFF P1  PC
0xFF  0xFF P0  0x0028      PSW  0 0 0 0  1 0 0 1
Modify RAM  addr 0x00  0x00 value
```

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	22	21	03	00	03	04	07	01	E2	00	00	00	00	00	00	00
10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	46	56	66	6F	01	02	10	02	06	00	00	02	00	00	00	00
30	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
40	B7	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
50	14	00	00	00	00	00	08	00	00	00	00	00	00	00	00	00
60	57	00	00	00	00	00	10	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

```
Executed 0x0026: DEC 29H | Time: 607us - Instruc
000E|    LJMP 0099H
0011|    LJMP 000EH
0014*    MOV 0E0H,2BH
0017|    JZ 0FBH
0019|    JB 0E7H,0F8H
001C|    DEC 2BH
001E|    MOV 0E0H,29H
0021|    JZ 0FBH
0023|    JB 0E7H,0F8H
0026|    DEC 29H
0028|    CLR 0AFH
002A|    MOV A,2DH
002C|    ADD A,#30H
002E|    MOV R1,A
002F|    MOV R7,2EH
0031|    MOV A,#41H
0033|    ADD A,R7
0034|    MOV @R1,A
0035|    MOV A,2DH
```

▲ After **`SemaphoreWait(mutex)`** (mutex=0, full=0, empty=2).

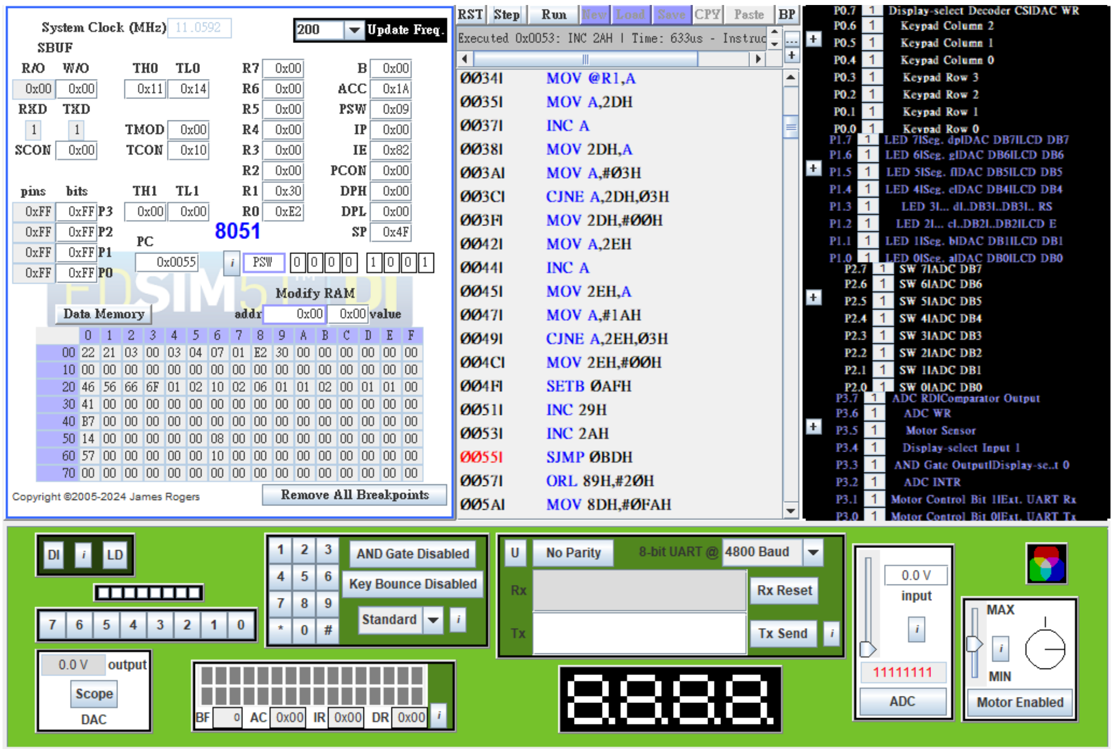


```
System Clock (MHz) 11.0592        200  Update Freq.
SBUF
R/O   W/O     TH0   TL0     R7 0x00    B    0x00
0x00  0x00    0x11  0x13    R6 0x00    ACC  0x1A
RXD   TXD                   R5 0x00    PSW  0x09
1     1       TMOD  0x00    R4 0x00    IP   0x00
SCON  0x00    TCON  0x10    R3 0x00    IE   0x82
                            R2 0x00    PCON 0x00
pins  bits    TH1   TL1     R1 0x30    DPH  0x00
0xFF  0xFF P3 0x00  0x00    R0 0xE2    DPL  0x00
0xFF  0xFF P2          8051            SP   0x4F
0xFF  0xFF P1  PC
0xFF  0xFF P0  0x0053      PSW  0 0 0 0  1 0 0 1
Modify RAM  addr 0x00  0x00 value
```

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	22	21	03	00	03	04	07	01	E2	30	00	00	00	00	00	00
10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	46	56	66	6F	01	02	10	02	06	01	00	02	00	01	01	00
30	41	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
40	B7	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
50	14	00	00	00	00	00	08	00	00	00	00	00	00	00	00	00
60	57	00	00	00	00	00	10	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

```
Executed 0x0051: INC 29H | Time: 632us - Instruc
0034|    MOV @R1,A
0035|    MOV A,2DH
0037|    INC A
0038|    MOV 2DH,A
003A|    MOV A,#03H
003C|    CJNE A,2DH,03H
003F|    MOV 2DH,#00H
0042|    MOV A,2EH
0044|    INC A
0045|    MOV 2EH,A
0047|    MOV A,#1AH
0049|    CJNE A,2EH,03H
004C|    MOV 2EH,#00H
004F|    SETB 0AFH
0051|    INC 29H
0053|    INC 2AH
0055|    SJMP 0BDH
0057|    ORL 89H,#20H
005A|    MOV 8DH,#0FAH
```

▲ After **`SemaphoreSignal(mutex);`** (mutex=1, full=0, empty=2).



```
System Clock (MHz) 11.0592        200  Update Freq.
SBUF
R/O   W/O     TH0   TL0     R7 0x00     B    0x00
0x00  0x00    0x11  0x14    R6 0x00     ACC  0x1A
RXD   TXD                   R5 0x00     PSW  0x09
1     1       TMOD  0x00    R4 0x00     IP   0x00
SCON  0x00    TCON  0x10    R3 0x00     IE   0x82
                            R2 0x00     PCON 0x00
pins  bits    TH1   TL1     R1 0x30     DPH  0x00
0xFF  0xFF P3 0x00  0x00    R0 0xE2     DPL  0x00
0xFF  0xFF P2                           SP   0x4F
0xFF  0xFF P1  PC 0x0055    PSW 0 0 0 0 1 0 0 1
0xFF  0xFF P0
```

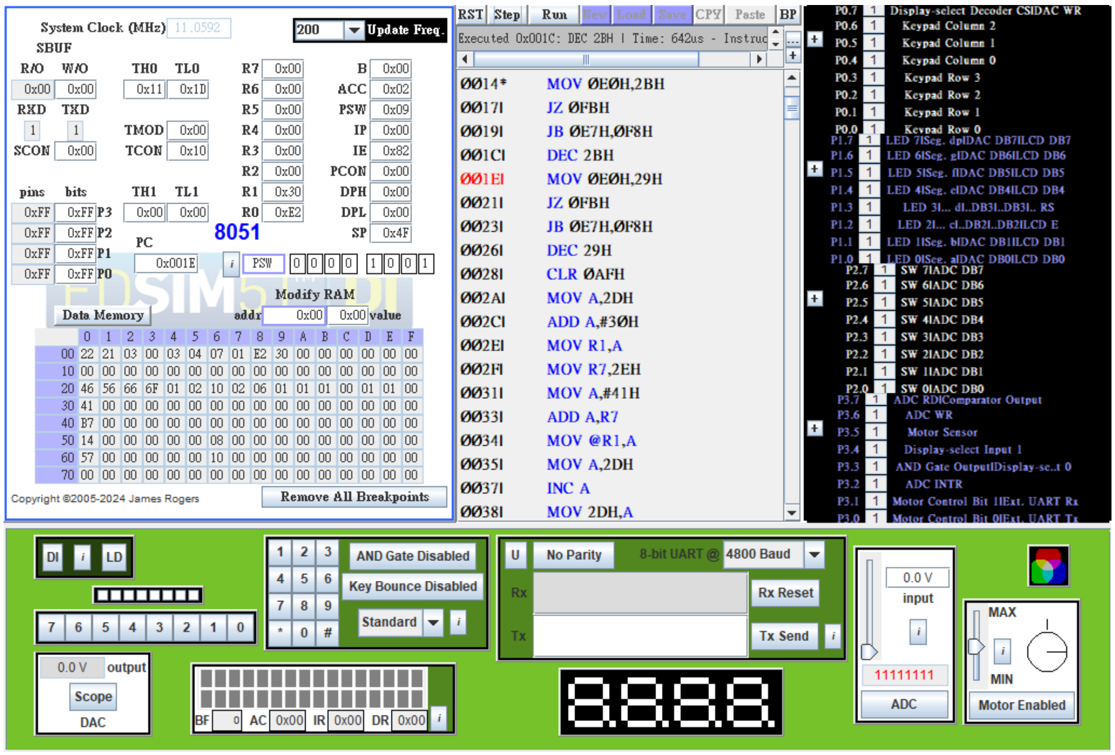
```
Executed 0x0053: INC 2AH | Time: 633us - Instruc
0034|   MOV @R1,A
0035|   MOV A,2DH
0037|   INC A
0038|   MOV 2DH,A
003A|   MOV A,#03H
003C|   CJNE A,2DH,03H
003F|   MOV 2DH,#00H
0042|   MOV A,2EH
0044|   INC A
0045|   MOV 2EH,A
0047|   MOV A,#1AH
0049|   CJNE A,2EH,03H
004C|   MOV 2EH,#00H
004F|   SETB 0AFH
0051|   INC 29H
0053|   INC 2AH
0055|   SJMP 0BDH
0057|   ORL 89H,#20H
005A|   MOV 8DH,#0FAH
```

Data Memory

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	22	21	03	00	03	04	07	01	E2	30	00	00	00	00	00	00
10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	46	56	66	6F	01	02	10	02	06	01	01	02	00	01	01	00
30	41	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
40	B7	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
50	14	00	00	00	00	00	08	00	00	00	00	00	00	00	00	00
60	57	00	00	00	00	00	10	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Copyright ©2005-2024 James Rogers

▲ After **`SemaphoreSignal(full);`** (mutex=1, full=1, empty=2).



```
System Clock (MHz) 11.0592        200  Update Freq.
SBUF
R/O   W/O     TH0   TL0     R7 0x00     B    0x00
0x00  0x00    0x11  0x1D    R6 0x00     ACC  0x02
RXD   TXD                   R5 0x00     PSW  0x09
1     1       TMOD  0x00    R4 0x00     IP   0x00
SCON  0x00    TCON  0x10    R3 0x00     IE   0x82
                            R2 0x00     PCON 0x00
pins  bits    TH1   TL1     R1 0x30     DPH  0x00
0xFF  0xFF P3 0x00  0x00    R0 0xE2     DPL  0x00
0xFF  0xFF P2                           SP   0x4F
0xFF  0xFF P1  PC 0x001E    PSW 0 0 0 0 1 0 0 1
0xFF  0xFF P0
```

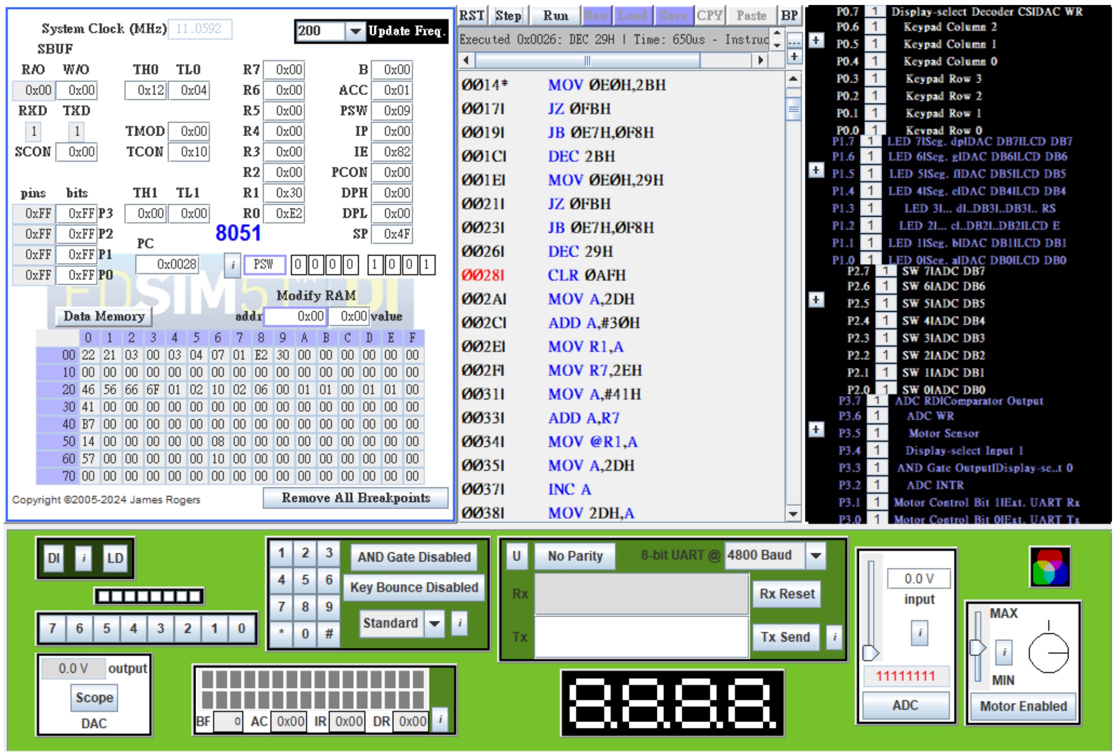
```
Executed 0x001C: DEC 2BH | Time: 642us - Instruc
0014*   MOV 0E0H,2BH
0017|   JZ 0FBH
0019|   JB 0E7H,0F8H
001C|   DEC 2BH
001E|   MOV 0E0H,29H
0021|   JZ 0FBH
0023|   JB 0E7H,0F8H
0026|   DEC 29H
0028|   CLR 0AFH
002A|   MOV A,2DH
002C|   ADD A,#30H
002E|   MOV R1,A
002F|   MOV R7,2EH
0031|   MOV A,#41H
0033|   ADD A,R7
0034|   MOV @R1,A
0035|   MOV A,2DH
0037|   INC A
0038|   MOV 2DH,A
```

Data Memory

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	22	21	03	00	03	04	07	01	E2	30	00	00	00	00	00	00
10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	46	56	66	6F	01	02	10	02	06	01	01	01	00	01	01	00
30	41	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
40	B7	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
50	14	00	00	00	00	00	08	00	00	00	00	00	00	00	00	00
60	57	00	00	00	00	00	10	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Copyright ©2005-2024 James Rogers

▲ After **`SemaphoreWait(empty)`** (mutex=1, full=1, empty=1).



```
System Clock (MHz) 11.0592        200  Update Freq.
SBUF
R/O   W/O      TH0   TL0      R7 0x00      B    0x00
0x00  0x00     0x12  0x04     R6 0x00      ACC  0x01
RXD   TXD                     R5 0x00      PSW  0x09
1     1        TMOD  0x00     R4 0x00      IP   0x00
SCON  0x00     TCON  0x10     R3 0x00      IE   0x82
                              R2 0x00      PCON 0x00
pins  bits     TH1   TL1      R1 0x30      DPH  0x00
0xFF  0xFF P3  0x00  0x00     R0 0xE2      DPL  0x00
0xFF  0xFF P2                 8051         SP   0x4F
0xFF  0xFF P1  PC
0xFF  0xFF P0  0x0028         PSW 0 0 0 0  1 0 0 1
```

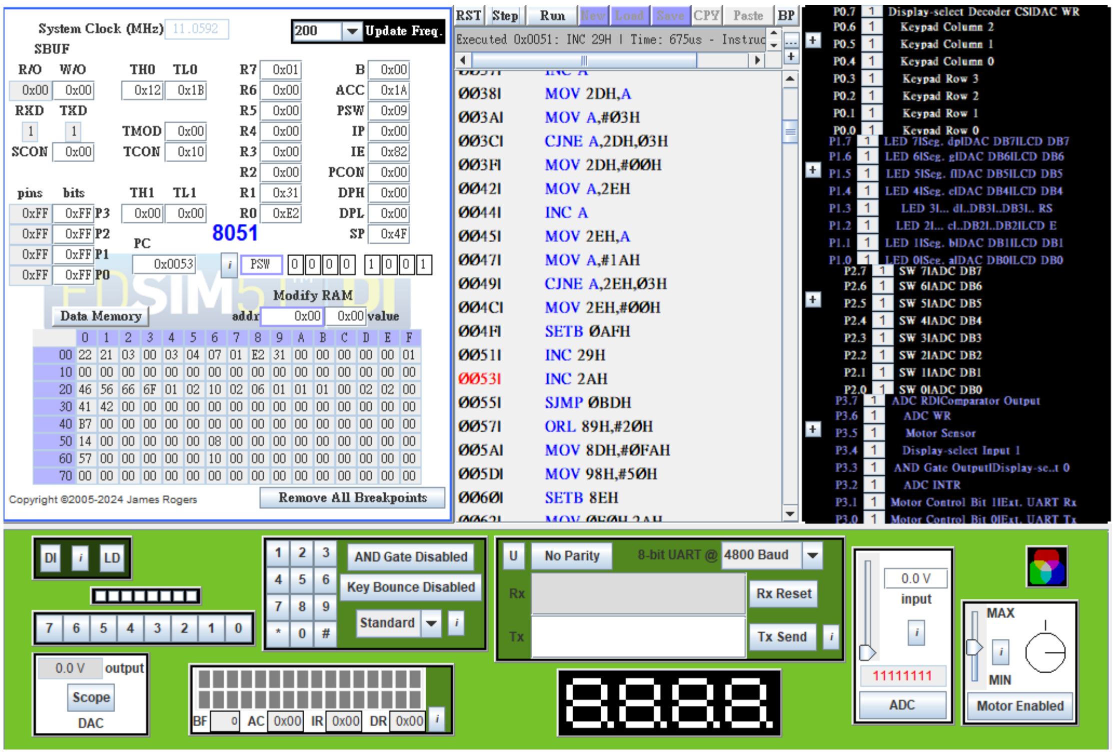
Data Memory — Modify RAM addr 0x00 value 0x00

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	22	21	03	00	03	04	07	01	E2	30	00	00	00	00	00	00
10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	46	56	66	6F	01	02	10	02	06	00	01	01	00	01	01	00
30	41	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
40	B7	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
50	14	00	00	00	00	00	08	00	00	00	00	00	00	00	00	00
60	57	00	00	00	00	00	10	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Copyright ©2005-2024 James Rogers

```
Executed 0x0026: DEC 29H | Time: 650us - Instruc
0014*   MOV 0E0H,2BH
0017|   JZ 0FBH
0019|   JB 0E7H,0F8H
001C|   DEC 2BH
001E|   MOV 0E0H,29H
0021|   JZ 0FBH
0023|   JB 0E7H,0F8H
0026|   DEC 29H
0028|   CLR 0AFH
002A|   MOV A,2DH
002C|   ADD A,#30H
002E|   MOV R1,A
002F|   MOV R7,2EH
0031|   MOV A,#41H
0033|   ADD A,R7
0034|   MOV @R1,A
0035|   MOV A,2DH
0037|   INC A
0038|   MOV 2DH,A
```

▲ After **`SemaphoreWait(mutex)`** (mutex=0, full=1, empty=1).



```
System Clock (MHz) 11.0592        200  Update Freq.
SBUF
R/O   W/O      TH0   TL0      R7 0x01      B    0x00
0x00  0x00     0x12  0x1B     R6 0x00      ACC  0x1A
RXD   TXD                     R5 0x00      PSW  0x09
1     1        TMOD  0x00     R4 0x00      IP   0x00
SCON  0x00     TCON  0x10     R3 0x00      IE   0x82
                              R2 0x00      PCON 0x00
pins  bits     TH1   TL1      R1 0x31      DPH  0x00
0xFF  0xFF P3  0x00  0x00     R0 0xE2      DPL  0x00
0xFF  0xFF P2                 8051         SP   0x4F
0xFF  0xFF P1  PC
0xFF  0xFF P0  0x0053         PSW 0 0 0 0  1 0 0 1
```

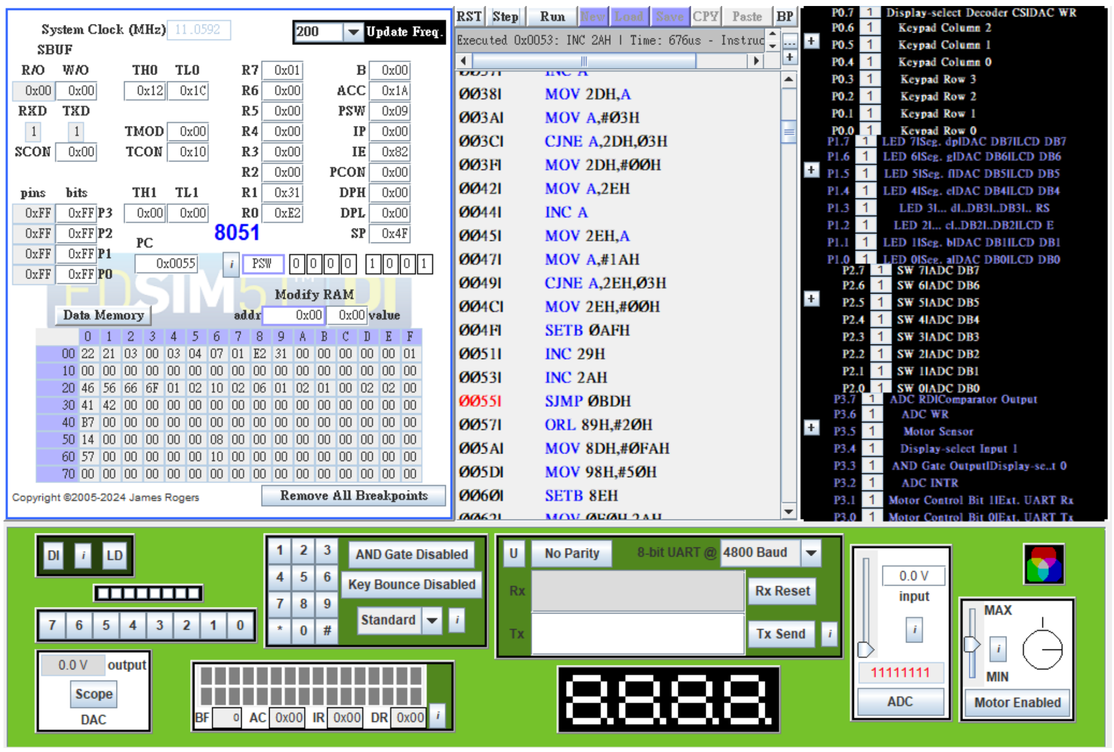
Data Memory — Modify RAM addr 0x00 value 0x00

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	22	21	03	00	03	04	07	01	E2	31	00	00	00	00	00	01
10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	46	56	66	6F	01	02	10	02	06	01	01	01	00	02	02	00
30	41	42	00	00	00	00	00	00	00	00	00	00	00	00	00	00
40	B7	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
50	14	00	00	00	00	00	08	00	00	00	00	00	00	00	00	00
60	57	00	00	00	00	00	10	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Copyright ©2005-2024 James Rogers

```
Executed 0x0051: INC 29H | Time: 675us - Instruc
0038|   MOV 2DH,A
003A|   MOV A,#03H
003C|   CJNE A,2DH,03H
003F|   MOV 2DH,#00H
0042|   MOV A,2EH
0044|   INC A
0045|   MOV 2EH,A
0047|   MOV A,#1AH
0049|   CJNE A,2EH,03H
004C|   MOV 2EH,#00H
004F|   SETB 0AFH
0051|   INC 29H
0053|   INC 2AH
0055|   SJMP 0BDH
0057|   ORL 89H,#20H
005A|   MOV 8DH,#0FAH
005D|   MOV 98H,#50H
0060|   SETB 8EH
```

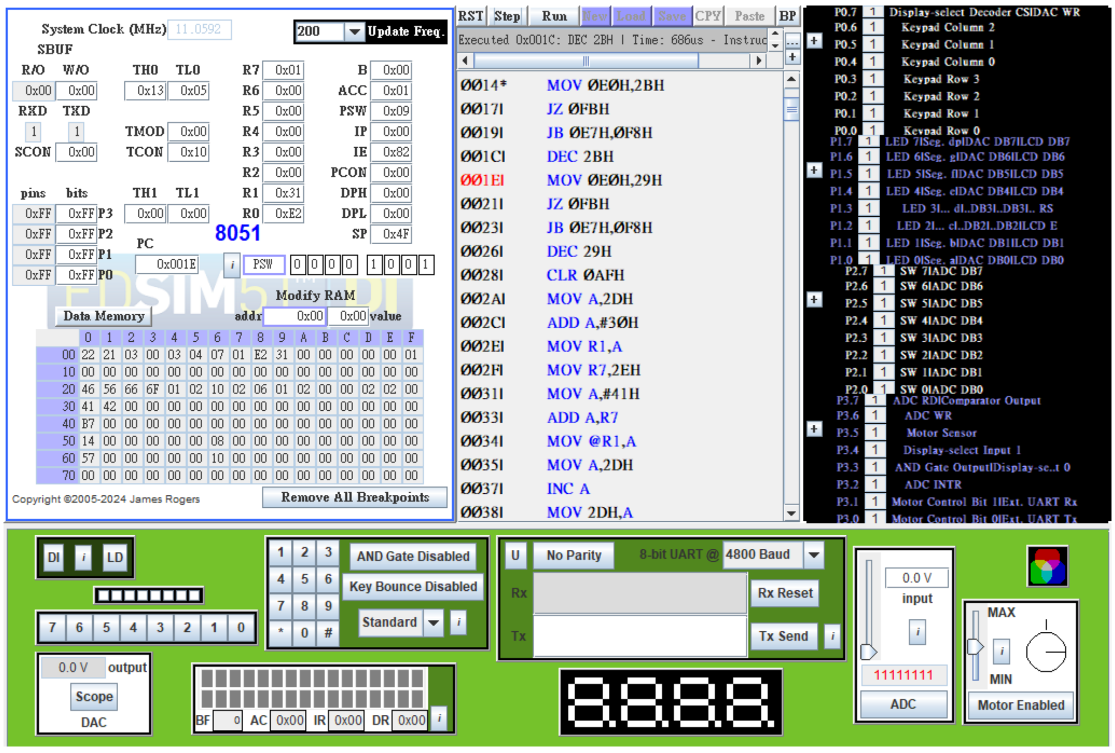
▲ After **`SemaphoreSignal(mutex);`** (mutex=1, full=1, empty=1).



```
Executed 0x0053: INC 2AH | Time: 676us - Instruc

0038|  MOV 2DH,A
003A|  MOV A,#03H
003C|  CJNE A,2DH,03H
003F|  MOV 2DH,#00H
0042|  MOV A,2EH
0044|  INC A
0045|  MOV 2EH,A
0047|  MOV A,#1AH
0049|  CJNE A,2EH,03H
004C|  MOV 2EH,#00H
004F|  SETB 0AFH
0051|  INC 29H
0053|  INC 2AH
0055|  SJMP 0BDH
0057|  ORL 89H,#20H
005A|  MOV 8DH,#0FAH
005D|  MOV 98H,#50H
0060|  SETB 8EH
```

```
System Clock (MHz) 11.0592        200  Update Freq.
SBUF
R/O   W/O     TH0   TL0     R7 0x01     B    0x00
0x00  0x00    0x12  0x1C    R6 0x00     ACC  0x1A
RXD   TXD                   R5 0x00     PSW  0x09
1     1       TMOD  0x00    R4 0x00     IP   0x00
SCON  0x00    TCON  0x10    R3 0x00     IE   0x82
                            R2 0x00     PCON 0x00
pins  bits    TH1   TL1     R1 0x31     DPH  0x00
0xFF  0xFF P3 0x00  0x00    R0 0xE2     DPL  0x00
0xFF  0xFF P2               8051        SP   0x4F
0xFF  0xFF P1 PC
0xFF  0xFF P0 0x0055   PSW 0 0 0 0 1 0 0 1
                       Modify RAM  addr 0x00  0x00 value
Data Memory
    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
00  22 21 03 00 03 04 07 01 E2 31 00 00 00 00 00 01
10  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
20  46 56 66 6F 01 02 10 02 06 01 02 01 00 02 02 00
30  41 42 00 00 00 00 00 00 00 00 00 00 00 00 00 00
40  B7 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
50  14 00 00 00 00 00 08 00 00 00 00 00 00 00 00 00
60  57 00 00 00 00 00 10 00 00 00 00 00 00 00 00 00
70  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Copyright ©2005-2024 James Rogers
```

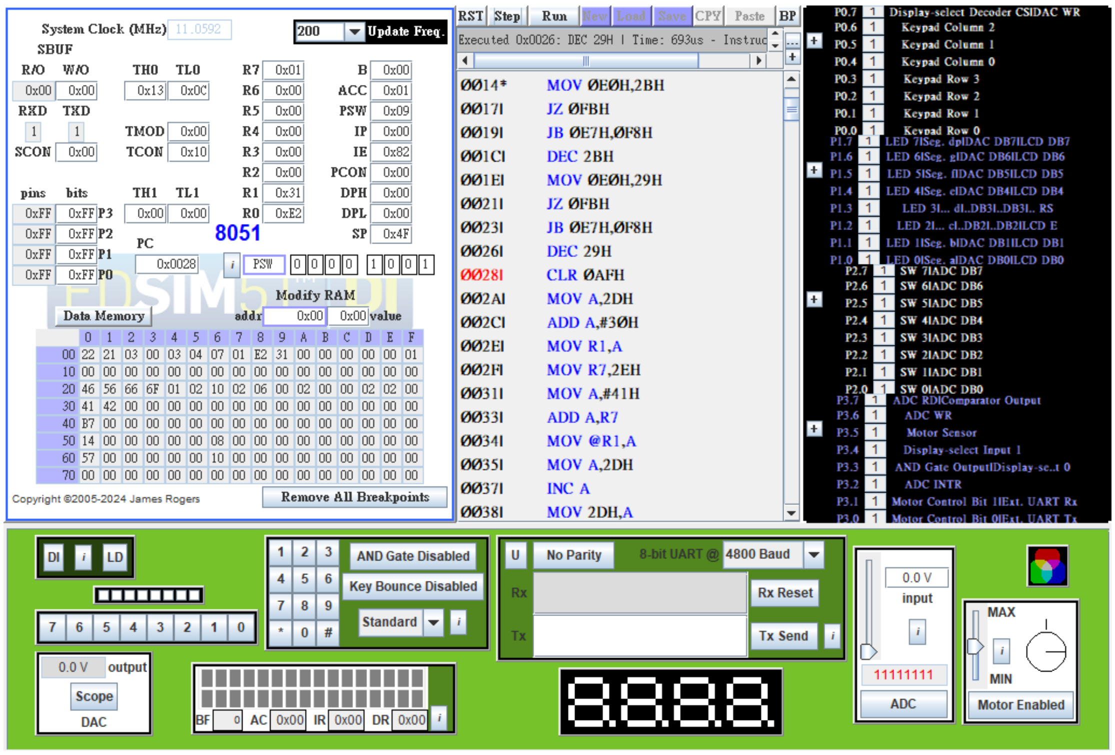
▲ After **`SemaphoreSignal(full)`**; (mutex=1, full=2, empty=1).



```
Executed 0x001C: DEC 2BH | Time: 686us - Instruc

0014*  MOV 0E0H,2BH
0017|  JZ 0FBH
0019|  JB 0E7H,0F8H
001C|  DEC 2BH
001E|  MOV 0E0H,29H
0021|  JZ 0FBH
0023|  JB 0E7H,0F8H
0026|  DEC 29H
0028|  CLR 0AFH
002A|  MOV A,2DH
002C|  ADD A,#30H
002E|  MOV R1,A
002F|  MOV R7,2EH
0031|  MOV A,#41H
0033|  ADD A,R7
0034|  MOV @R1,A
0035|  MOV A,2DH
0037|  INC A
0038|  MOV 2DH,A
```

```
System Clock (MHz) 11.0592        200  Update Freq.
SBUF
R/O   W/O     TH0   TL0     R7 0x01     B    0x00
0x00  0x00    0x13  0x05    R6 0x00     ACC  0x01
RXD   TXD                   R5 0x00     PSW  0x09
1     1       TMOD  0x00    R4 0x00     IP   0x00
SCON  0x00    TCON  0x10    R3 0x00     IE   0x82
                            R2 0x00     PCON 0x00
pins  bits    TH1   TL1     R1 0x31     DPH  0x00
0xFF  0xFF P3 0x00  0x00    R0 0xE2     DPL  0x00
0xFF  0xFF P2               8051        SP   0x4F
0xFF  0xFF P1 PC
0xFF  0xFF P0 0x001E   PSW 0 0 0 0 1 0 0 1
                       Modify RAM  addr 0x00  0x00 value
Data Memory
    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
00  22 21 03 00 03 04 07 01 E2 31 00 00 00 00 00 01
10  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
20  46 56 66 6F 01 02 10 02 06 01 02 00 00 02 02 00
30  41 42 00 00 00 00 00 00 00 00 00 00 00 00 00 00
40  B7 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
50  14 00 00 00 00 00 08 00 00 00 00 00 00 00 00 00
60  57 00 00 00 00 00 10 00 00 00 00 00 00 00 00 00
70  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Copyright ©2005-2024 James Rogers
```

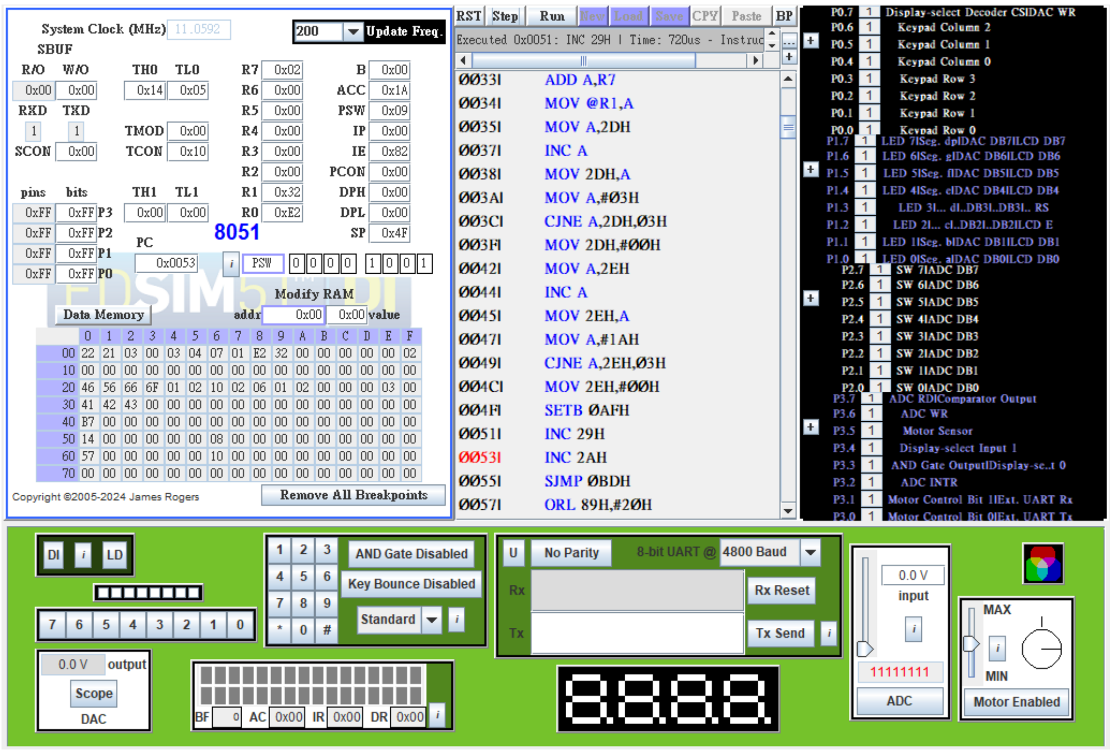
▲ After **`SemaphoreWait(empty)`** (mutex=1, full=2, empty=0).



```
System Clock (MHz) 11.0592        200  Update Freq.
SBUF
R/O   W/O      TH0   TL0     R7  0x01     B     0x00
0x00  0x00     0x13  0x0C    R6  0x00     ACC   0x01
RXD   TXD                    R5  0x00     PSW   0x09
1     1        TMOD  0x00    R4  0x00     IP    0x00
SCON  0x00     TCON  0x10    R3  0x00     IE    0x82
                             R2  0x00     PCON  0x00
pins  bits     TH1   TL1     R1  0x31     DPH   0x00
0xFF  0xFF P3  0x00  0x00    R0  0xE2     DPL   0x00
0xFF  0xFF P2                8051         SP    0x4F
0xFF  0xFF P1  PC
0xFF  0xFF P0  0x0028        PSW 0 0 0 0  1 0 0 1
                             Modify RAM
Data Memory                  addr 0x00  0x00 value

    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
00 22 21 03 00 03 04 07 01 E2 31 00 00 00 00 00 01
10 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
20 46 56 66 6F 01 02 10 02 06 00 02 00 00 02 02 00
30 41 42 00 00 00 00 00 00 00 00 00 00 00 00 00 00
40 B7 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
50 14 00 00 00 00 00 08 00 00 00 00 00 00 00 00 00
60 57 00 00 00 00 00 10 00 00 00 00 00 00 00 00 00
70 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Copyright ©2005-2024 James Rogers    Remove All Breakpoints
```

```
Executed 0x0026: DEC 29H | Time: 693us - Instruc
0014*   MOV 0E0H,2BH
0017|   JZ 0FBH
0019|   JB 0E7H,0F8H
001C|   DEC 2BH
001E|   MOV 0E0H,29H
0021|   JZ 0FBH
0023|   JB 0E7H,0F8H
0026|   DEC 29H
0028|   CLR 0AFH
002A|   MOV A,2DH
002C|   ADD A,#30H
002E|   MOV R1,A
002F|   MOV R7,2EH
0031|   MOV A,#41H
0033|   ADD A,R7
0034|   MOV @R1,A
0035|   MOV A,2DH
0037|   INC A
0038|   MOV 2DH,A
```

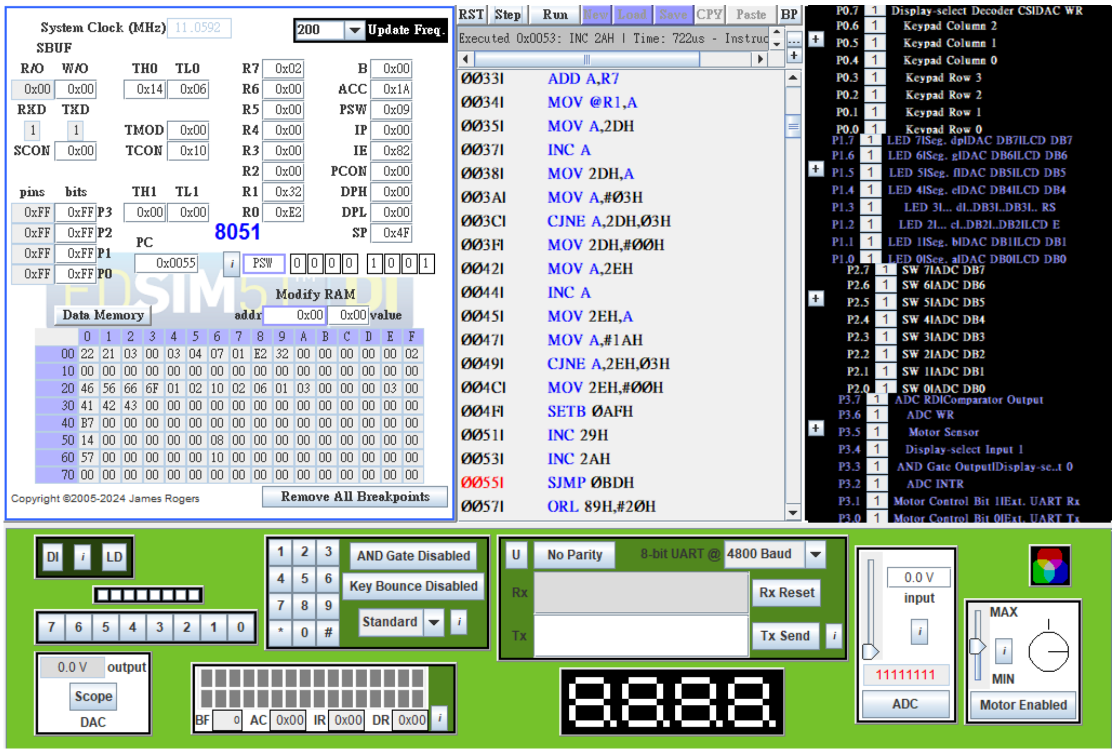
▲ After **`SemaphoreWait(mutex)`** (mutex=0, full=2, empty=0).



```
System Clock (MHz) 11.0592        200  Update Freq.
SBUF
R/O   W/O      TH0   TL0     R7  0x02     B     0x00
0x00  0x00     0x14  0x05    R6  0x00     ACC   0x1A
RXD   TXD                    R5  0x00     PSW   0x09
1     1        TMOD  0x00    R4  0x00     IP    0x00
SCON  0x00     TCON  0x10    R3  0x00     IE    0x82
                             R2  0x00     PCON  0x00
pins  bits     TH1   TL1     R1  0x32     DPH   0x00
0xFF  0xFF P3  0x00  0x00    R0  0xE2     DPL   0x00
0xFF  0xFF P2                8051         SP    0x4F
0xFF  0xFF P1  PC
0xFF  0xFF P0  0x0053        PSW 0 0 0 0  1 0 0 1
                             Modify RAM
Data Memory                  addr 0x00  0x00 value

    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
00 22 21 03 00 03 04 07 01 E2 32 00 00 00 00 00 02
10 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
20 46 56 66 6F 01 02 10 02 06 01 02 00 00 00 03 00
30 41 42 43 00 00 00 00 00 00 00 00 00 00 00 00 00
40 B7 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
50 14 00 00 00 00 00 08 00 00 00 00 00 00 00 00 00
60 57 00 00 00 00 00 10 00 00 00 00 00 00 00 00 00
70 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Copyright ©2005-2024 James Rogers    Remove All Breakpoints
```

```
Executed 0x0051: INC 29H | Time: 720us - Instruc
0033|   ADD A,R7
0034|   MOV @R1,A
0035|   MOV A,2DH
0037|   INC A
0038|   MOV 2DH,A
003A|   MOV A,#03H
003C|   CJNE A,2DH,03H
003F|   MOV 2DH,#00H
0042|   MOV A,2EH
0044|   INC A
0045|   MOV 2EH,A
0047|   MOV A,#1AH
0049|   CJNE A,2EH,03H
004C|   MOV 2EH,#00H
004F|   SETB 0AFH
0051|   INC 29H
0053|   INC 2AH
0055|   SJMP 0BDH
0057|   ORL 89H,#20H
```

▲ After **`SemaphoreSignal(mutex);`** (mutex=1, full=2, empty=0).



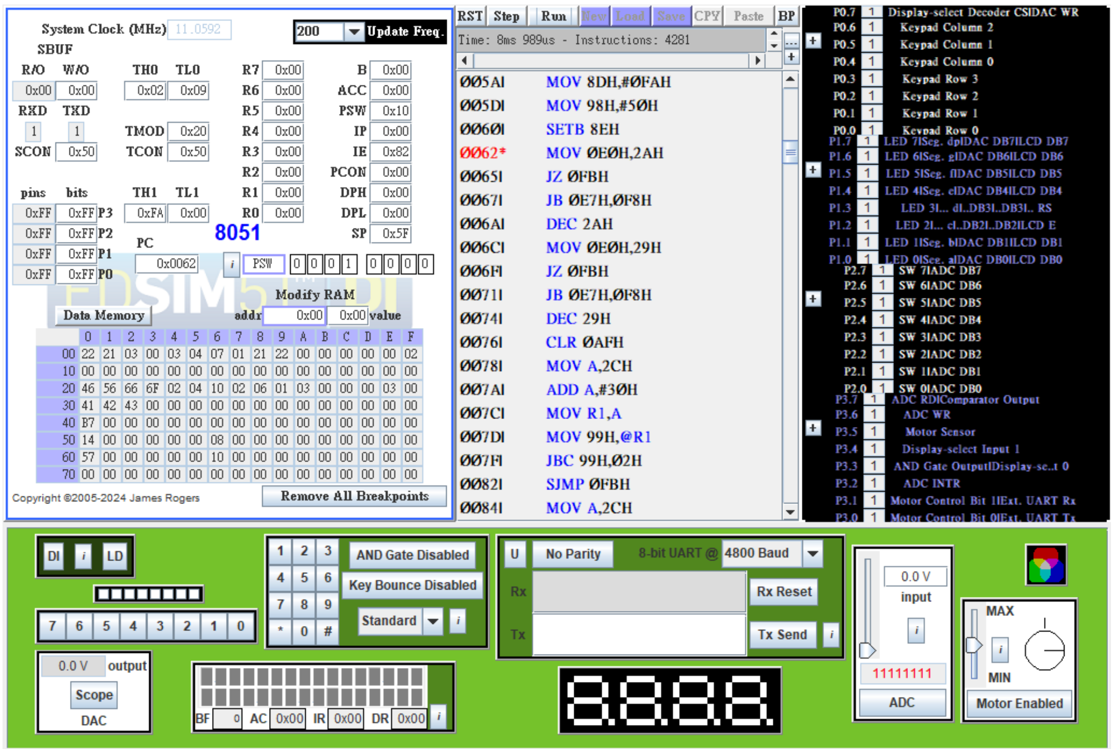
```
System Clock (MHz) 11.0592        200  Update Freq.
SBUF
R/O   W/O      TH0   TL0      R7 0x02      B    0x00
0x00  0x00     0x14  0x06     R6 0x00      ACC  0x1A
RXD   TXD                     R5 0x00      PSW  0x09
1     1        TMOD  0x00     R4 0x00      IP   0x00
SCON  0x00     TCON  0x10     R3 0x00      IE   0x82
                              R2 0x00      PCON 0x00
pins  bits     TH1   TL1      R1 0x32      DPH  0x00
0xFF  0xFF P3  0x00  0x00     R0 0xE2      DPL  0x00
0xFF  0xFF P2                 8051         SP   0x4F
0xFF  0xFF P1  PC
0xFF  0xFF P0  0x0055         PSW 0 0 0 0  1 0 0 1
                              Modify RAM
Data Memory                   addr 0x00  0x00 value
    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
00  22 21 03 00 03 04 07 01 E2 32 00 00 00 00 00 02
10  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
20  46 56 66 6F 01 02 10 02 06 01 03 00 00 00 03 00
30  41 42 43 00 00 00 00 00 00 00 00 00 00 00 00 00
40  B7 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
50  14 00 00 00 00 00 08 00 00 00 00 00 00 00 00 00
60  57 00 00 00 00 00 10 00 00 00 00 00 00 00 00 00
70  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Copyright ©2005-2024 James Rogers
```

```
Executed 0x0053: INC 2AH | Time: 722us - Instruc
0033|   ADD A,R7
0034|   MOV @R1,A
0035|   MOV A,2DH
0037|   INC A
0038|   MOV 2DH,A
003A|   MOV A,#03H
003C|   CJNE A,2DH,03H
003F|   MOV 2DH,#00H
0042|   MOV A,2EH
0044|   INC A
0045|   MOV 2EH,A
0047|   MOV A,#1AH
0049|   CJNE A,2EH,03H
004C|   MOV 2EH,#00H
004F|   SETB 0AFH
0051|   INC 29H
0053|   INC 2AH
0055|   SJMP 0BDH
0057|   ORL 89H,#20H
```

```
8-bit UART @ 4800 Baud   No Parity
```

▲ After **`SemaphoreSignal(full);`** (mutex=1, full=3, empty=0).

- Consumer:

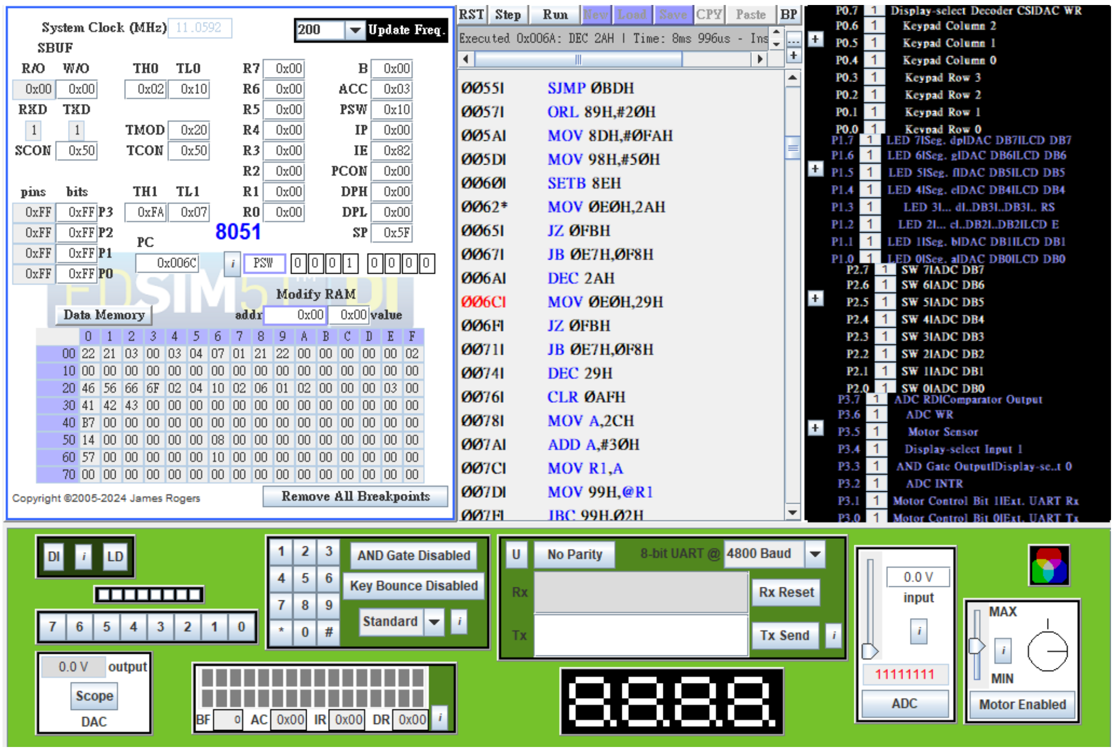


```
System Clock (MHz) 11.0592        200  Update Freq.
SBUF
R/O   W/O      TH0   TL0      R7 0x00      B    0x00
0x00  0x00     0x02  0x09     R6 0x00      ACC  0x00
RXD   TXD                     R5 0x00      PSW  0x10
1     1        TMOD  0x20     R4 0x00      IP   0x00
SCON  0x50     TCON  0x50     R3 0x00      IE   0x82
                              R2 0x00      PCON 0x00
pins  bits     TH1   TL1      R1 0x00      DPH  0x00
0xFF  0xFF P3  0xFA  0x00     R0 0x00      DPL  0x00
0xFF  0xFF P2                 8051         SP   0x5F
0xFF  0xFF P1  PC
0xFF  0xFF P0  0x0062         PSW 0 0 0 1  0 0 0 0
                              Modify RAM
Data Memory                   addr 0x00  0x00 value
    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
00  22 21 03 00 03 04 07 01 21 22 00 00 00 00 00 02
10  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
20  46 56 66 6F 02 04 10 02 06 01 03 00 00 00 03 00
30  41 42 43 00 00 00 00 00 00 00 00 00 00 00 00 00
40  B7 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
50  14 00 00 00 00 00 08 00 00 00 00 00 00 00 00 00
60  57 00 00 00 00 00 10 00 00 00 00 00 00 00 00 00
70  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Copyright ©2005-2024 James Rogers
```

```
Time: 8ms 989us - Instructions: 4281
005A|   MOV 8DH,#0FAH
005D|   MOV 98H,#50H
0060|   SETB 8EH
0062*   MOV 0E0H,2AH
0065|   JZ 0FBH
0067|   JB 0E7H,0F8H
006A|   DEC 2AH
006C|   MOV 0E0H,29H
006F|   JZ 0FBH
0071|   JB 0E7H,0F8H
0074|   DEC 29H
0076|   CLR 0AFH
0078|   MOV A,2CH
007A|   ADD A,#30H
007C|   MOV R1,A
007D|   MOV 99H,@R1
007F|   JBC 99H,02H
0082|   SJMP 0FBH
0084|   MOV A,2CH
```

```
8-bit UART @ 4800 Baud   No Parity
```

▲ Just enter, after finish UART init (mutex=1, full=3, empty=0).



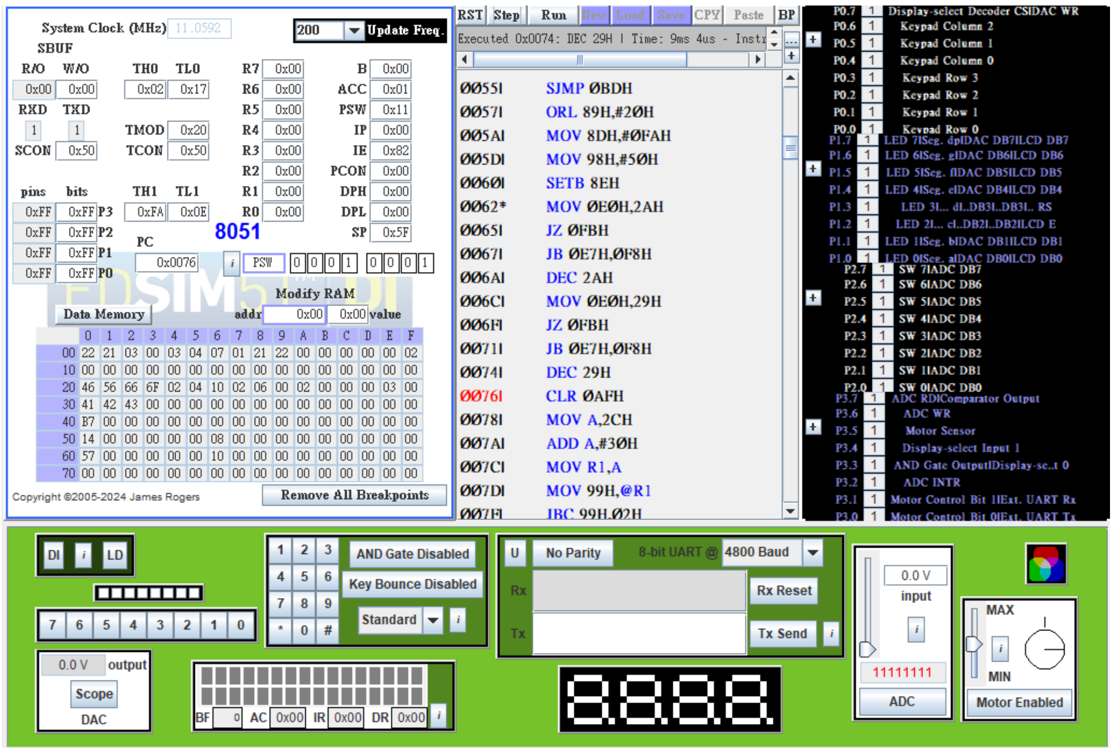
```
Executed 0x006A: DEC 2AH | Time: 8ms 996us - Ins

0055| SJMP 0BDH
0057| ORL 89H,#20H
005A| MOV 8DH,#0FAH
005D| MOV 98H,#50H
0060| SETB 8EH
0062* MOV 0E0H,2AH
0065| JZ 0FBH
0067| JB 0E7H,0F8H
006A| DEC 2AH
006C| MOV 0E0H,29H
006F| JZ 0FBH
0071| JB 0E7H,0F8H
0074| DEC 29H
0076| CLR 0AFH
0078| MOV A,2CH
007A| ADD A,#30H
007C| MOV R1,A
007D| MOV 99H,@R1
007F| JBC 99H,02H
```

```
System Clock (MHz) 11.0592        Update Freq. 200
SBUF R/O 0x00  W/O 0x00   TH0 0x02  TL0 0x10   R7 0x00   B    0x00
RXD 1  TXD 1                                   R6 0x00   ACC  0x03
SCON 0x50   TMOD 0x20  TCON 0x50               R5 0x00   PSW  0x10
                                               R4 0x00   IP   0x00
                                               R3 0x00   IE   0x82
                                               R2 0x00   PCON 0x00
pins  bits        TH1 0xFA  TL1 0x07           R1 0x00   DPH  0x00
0xFF  0xFF P3                                  R0 0x00   DPL  0x00
0xFF  0xFF P2                                            SP   0x5F
0xFF  0xFF P1     PC 0x006C    PSW 0 0 0 1  0 0 0 0
0xFF  0xFF P0     Modify RAM addr 0x00 value 0x00
```

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	22	21	03	00	03	04	07	01	21	22	00	00	00	00	00	02
10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	46	56	66	6F	02	04	10	02	06	01	02	00	00	00	03	00
30	41	42	43	00	00	00	00	00	00	00	00	00	00	00	00	00
40	B7	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
50	14	00	00	00	00	00	08	00	00	00	00	00	00	00	00	00
60	57	00	00	00	00	00	10	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Copyright ©2005-2024 James Rogers

▲ After **`SemaphoreWait(full);`** (mutex=1, full=2, empty=0).



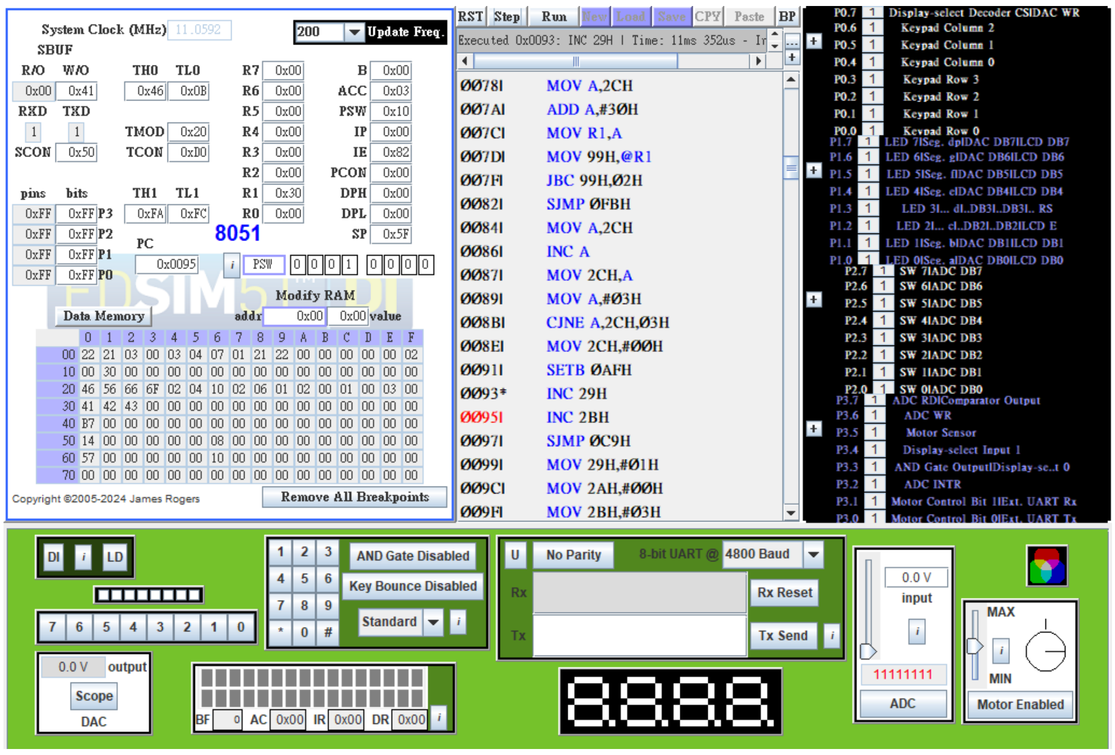
```
Executed 0x0074: DEC 29H | Time: 9ms 4us - Instr

0055| SJMP 0BDH
0057| ORL 89H,#20H
005A| MOV 8DH,#0FAH
005D| MOV 98H,#50H
0060| SETB 8EH
0062* MOV 0E0H,2AH
0065| JZ 0FBH
0067| JB 0E7H,0F8H
006A| DEC 2AH
006C| MOV 0E0H,29H
006F| JZ 0FBH
0071| JB 0E7H,0F8H
0074| DEC 29H
0076| CLR 0AFH
0078| MOV A,2CH
007A| ADD A,#30H
007C| MOV R1,A
007D| MOV 99H,@R1
007F| JBC 99H,02H
```

```
System Clock (MHz) 11.0592        Update Freq. 200
SBUF R/O 0x00  W/O 0x00   TH0 0x02  TL0 0x17   R7 0x00   B    0x00
RXD 1  TXD 1                                   R6 0x00   ACC  0x01
SCON 0x50   TMOD 0x20  TCON 0x50               R5 0x00   PSW  0x11
                                               R4 0x00   IP   0x00
                                               R3 0x00   IE   0x82
                                               R2 0x00   PCON 0x00
pins  bits        TH1 0xFA  TL1 0x0E           R1 0x00   DPH  0x00
0xFF  0xFF P3                                  R0 0x00   DPL  0x00
0xFF  0xFF P2                                            SP   0x5F
0xFF  0xFF P1     PC 0x0076    PSW 0 0 0 1  0 0 0 1
0xFF  0xFF P0     Modify RAM addr 0x00 value 0x00
```

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	22	21	03	00	03	04	07	01	21	22	00	00	00	00	00	02
10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	46	56	66	6F	02	04	10	02	06	00	02	00	00	00	03	00
30	41	42	43	00	00	00	00	00	00	00	00	00	00	00	00	00
40	B7	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
50	14	00	00	00	00	00	08	00	00	00	00	00	00	00	00	00
60	57	00	00	00	00	00	10	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Copyright ©2005-2024 James Rogers

▲ After **`SemaphoreWait(mutex);`** (mutex=0, full=2, empty=0).

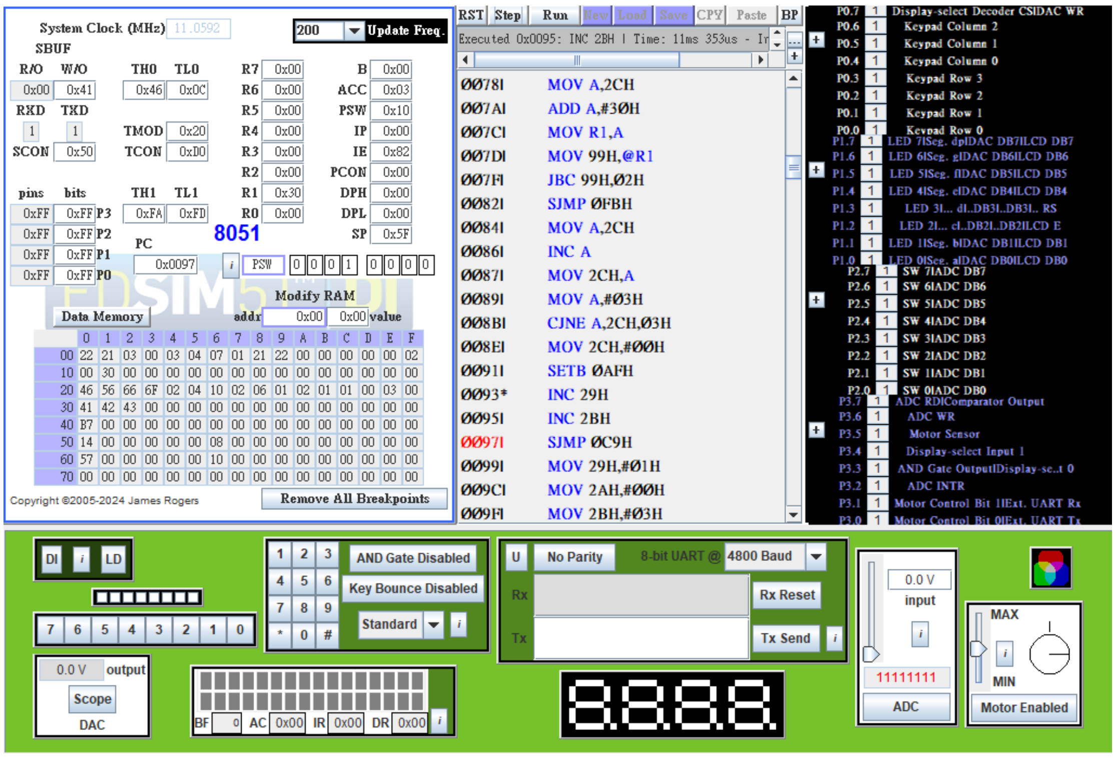


```
SBUF R/O 0x00  W/O 0x41   TH0 0x46  TL0 0x0B   R7 0x00   B    0x00
RXD 1  TXD 1              TMOD 0x20            R6 0x00   ACC  0x03
SCON 0x50                 TCON 0xD0            R5 0x00   PSW  0x10
pins  bits                TH1 0xFA  TL1 0xFC   R4 0x00   IP   0x00
0xFF  0xFF P3                                  R3 0x00   IE   0x82
0xFF  0xFF P2             PC 0x0095            R2 0x00   PCON 0x00
0xFF  0xFF P1             PSW 0 0 0 1  0 0 0 0 R1 0x30   DPH  0x00
0xFF  0xFF P0                                  R0 0x00   DPL  0x00
                                                         SP   0x5F
Modify RAM addr 0x00  0x00 value
```

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	22	21	03	00	03	04	07	01	21	22	00	00	00	00	00	02
10	00	30	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	46	56	66	6F	02	04	10	02	06	01	02	00	01	00	03	00
30	41	42	43	00	00	00	00	00	00	00	00	00	00	00	00	00
40	B7	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
50	14	00	00	00	00	00	08	00	00	00	00	00	00	00	00	00
60	57	00	00	00	00	00	10	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

```
Executed 0x0093: INC 29H | Time: 11ms 352us - Ir
ØØ78|    MOV A,2CH
ØØ7A|    ADD A,#3ØH
ØØ7C|    MOV R1,A
ØØ7D|    MOV 99H,@R1
ØØ7F|    JBC 99H,Ø2H
ØØ82|    SJMP ØFBH
ØØ84|    MOV A,2CH
ØØ86|    INC A
ØØ87|    MOV 2CH,A
ØØ89|    MOV A,#Ø3H
ØØ8B|    CJNE A,2CH,Ø3H
ØØ8E|    MOV 2CH,#ØØH
ØØ91|    SETB ØAFH
ØØ93*    INC 29H
ØØ95|    INC 2BH
ØØ97|    SJMP ØC9H
ØØ99|    MOV 29H,#Ø1H
ØØ9C|    MOV 2AH,#ØØH
ØØ9F|    MOV 2BH,#Ø3H
```

▲ After `SemaphoreSignal(mutex);` (mutex=1, full=2, empty=0).

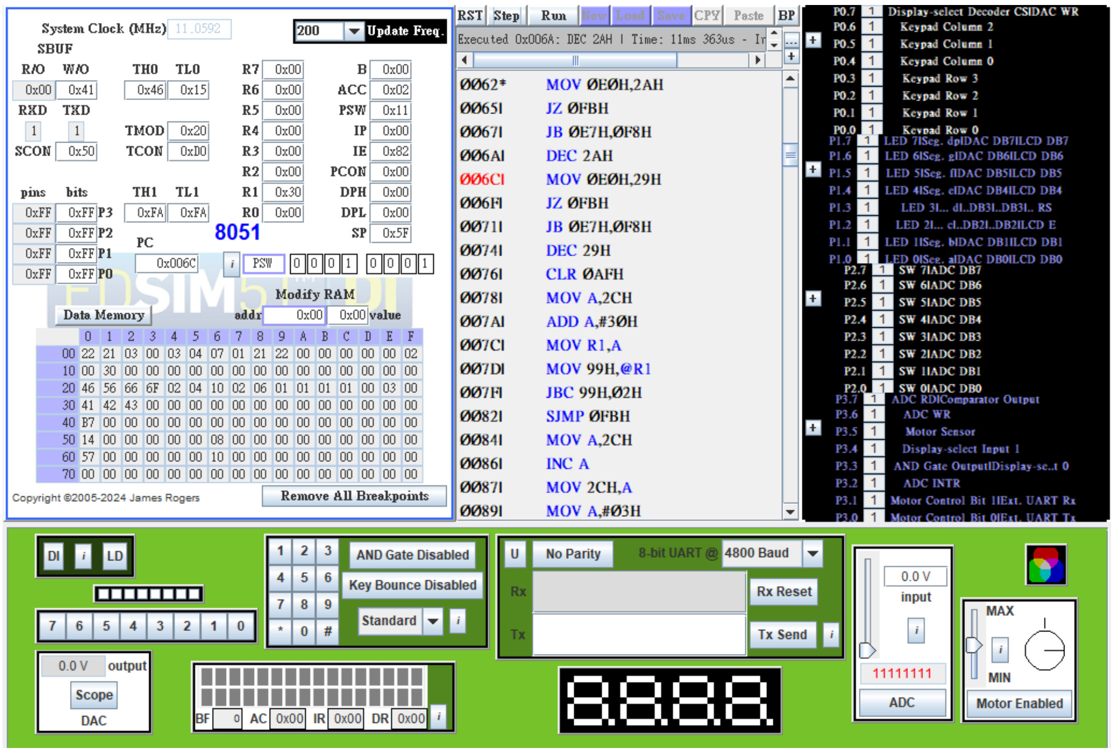


```
SBUF R/O 0x00  W/O 0x41   TH0 0x46  TL0 0x0C   R7 0x00   B    0x00
RXD 1  TXD 1              TMOD 0x20            R6 0x00   ACC  0x03
SCON 0x50                 TCON 0xD0            R5 0x00   PSW  0x10
pins  bits                TH1 0xFA  TL1 0xFD   R4 0x00   IP   0x00
0xFF  0xFF P3                                  R3 0x00   IE   0x82
0xFF  0xFF P2             PC 0x0097            R2 0x00   PCON 0x00
0xFF  0xFF P1             PSW 0 0 0 1  0 0 0 0 R1 0x30   DPH  0x00
0xFF  0xFF P0                                  R0 0x00   DPL  0x00
                                                         SP   0x5F
Modify RAM addr 0x00  0x00 value
```

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	22	21	03	00	03	04	07	01	21	22	00	00	00	00	00	02
10	00	30	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	46	56	66	6F	02	04	10	02	06	01	02	01	01	00	03	00
30	41	42	43	00	00	00	00	00	00	00	00	00	00	00	00	00
40	B7	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
50	14	00	00	00	00	00	08	00	00	00	00	00	00	00	00	00
60	57	00	00	00	00	00	10	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

```
Executed 0x0095: INC 2BH | Time: 11ms 353us - Ir
ØØ78|    MOV A,2CH
ØØ7A|    ADD A,#3ØH
ØØ7C|    MOV R1,A
ØØ7D|    MOV 99H,@R1
ØØ7F|    JBC 99H,Ø2H
ØØ82|    SJMP ØFBH
ØØ84|    MOV A,2CH
ØØ86|    INC A
ØØ87|    MOV 2CH,A
ØØ89|    MOV A,#Ø3H
ØØ8B|    CJNE A,2CH,Ø3H
ØØ8E|    MOV 2CH,#ØØH
ØØ91|    SETB ØAFH
ØØ93*    INC 29H
ØØ95|    INC 2BH
ØØ97|    SJMP ØC9H
ØØ99|    MOV 29H,#Ø1H
ØØ9C|    MOV 2AH,#ØØH
ØØ9F|    MOV 2BH,#Ø3H
```

▲ After `SemaphoreSignal(empty);` (mutex=1, full=2, empty=1).

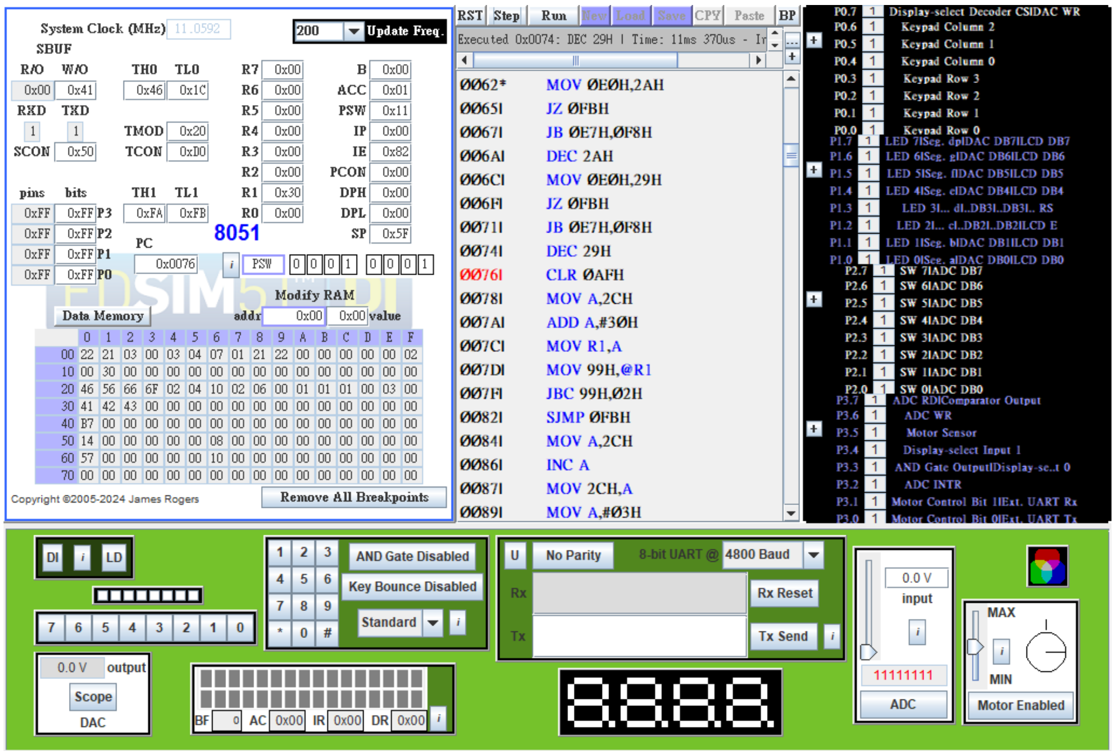


```
System Clock (MHz) 11.0592      200  Update Freq.
SBUF
R/O   W/O     TH0   TL0     R7 0x00      B    0x00
0x00  0x41    0x46  0x15    R6 0x00      ACC  0x02
RXD   TXD                   R5 0x00      PSW  0x11
1     1       TMOD  0x20    R4 0x00      IP   0x00
SCON  0x50    TCON  0xD0    R3 0x00      IE   0x82
                            R2 0x00      PCON 0x00
pins  bits    TH1   TL1     R1 0x30      DPH  0x00
0xFF  0xFF P3 0xFA  0xFA    R0 0x00      DPL  0x00
0xFF  0xFF P2                  8051      SP   0x5F
0xFF  0xFF P1   PC
0xFF  0xFF P0   0x006C      PSW  0 0 0 1  0 0 0 1

Data Memory          Modify RAM  addr 0x00  0x00 value
    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
00 22 21 03 00 03 04 07 01 21 22 00 00 00 00 00 02
10 00 30 00 00 00 00 00 00 00 00 00 00 00 00 00 00
20 46 56 66 6F 02 04 10 02 06 01 01 01 01 00 03 00
30 41 42 43 00 00 00 00 00 00 00 00 00 00 00 00 00
40 B7 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
50 14 00 00 00 00 00 08 00 00 00 00 00 00 00 00 00
60 57 00 00 00 00 00 10 00 00 00 00 00 00 00 00 00
70 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Copyright ©2005-2024 James Rogers     Remove All Breakpoints
```

```
Executed 0x006A: DEC 2AH | Time: 11ms 363us - Ir
ØØ62*   MOV ØEØH,2AH
ØØ65|   JZ ØFBH
ØØ67|   JB ØE7H,ØF8H
ØØ6A|   DEC 2AH
ØØ6C|   MOV ØEØH,29H
ØØ6F|   JZ ØFBH
ØØ71|   JB ØE7H,ØF8H
ØØ74|   DEC 29H
ØØ76|   CLR ØAFH
ØØ78|   MOV A,2CH
ØØ7A|   ADD A,#3ØH
ØØ7C|   MOV R1,A
ØØ7D|   MOV 99H,@R1
ØØ7F|   JBC 99H,Ø2H
ØØ82|   SJMP ØFBH
ØØ84|   MOV A,2CH
ØØ86|   INC A
ØØ87|   MOV 2CH,A
ØØ89|   MOV A,#Ø3H
```

```
P0.7 1 Display-select Decoder CS|DAC WR
P0.6 1 Keypad Column 2
P0.5 1 Keypad Column 1
P0.4 1 Keypad Column 0
P0.3 1 Keypad Row 3
P0.2 1 Keypad Row 2
P0.1 1 Keypad Row 1
P0.0 1 Keypad Row 0
P1.7 1 LED 7|Seg. dp|DAC DB7|LCD DB7
P1.6 1 LED 6|Seg. g|DAC DB6|LCD DB6
P1.5 1 LED 5|Seg. f|DAC DB5|LCD DB5
P1.4 1 LED 4|Seg. e|DAC DB4|LCD DB4
P1.3 1 LED 3|... d|..DB3|..DB3|.. RS
P1.2 1 LED 2|... c|..DB2|..DB2|LCD E
P1.1 1 LED 1|Seg. b|DAC DB1|LCD DB1
P1.0 1 LED 0|Seg. a|DAC DB0|LCD DB0
P2.7 1 SW 7|ADC DB7
P2.6 1 SW 6|ADC DB6
P2.5 1 SW 5|ADC DB5
P2.4 1 SW 4|ADC DB4
P2.3 1 SW 3|ADC DB3
P2.2 1 SW 2|ADC DB2
P2.1 1 SW 1|ADC DB1
P2.0 1 SW 0|ADC DB0
P3.7 1 ADC RD|Comparator Output
P3.6 1 ADC WR
P3.5 1 Motor Sensor
P3.4 1 Display-select Input 1
P3.3 1 AND Gate Output|Display-se..t 0
P3.2 1 ADC INTR
P3.1 1 Motor Control Bit 1|Ext. UART Rx
P3.0 1 Motor Control Bit 0|Ext. UART Tx
```

▲ After **`SemaphoreWait(full);`** (mutex=1, full=1, empty=1).

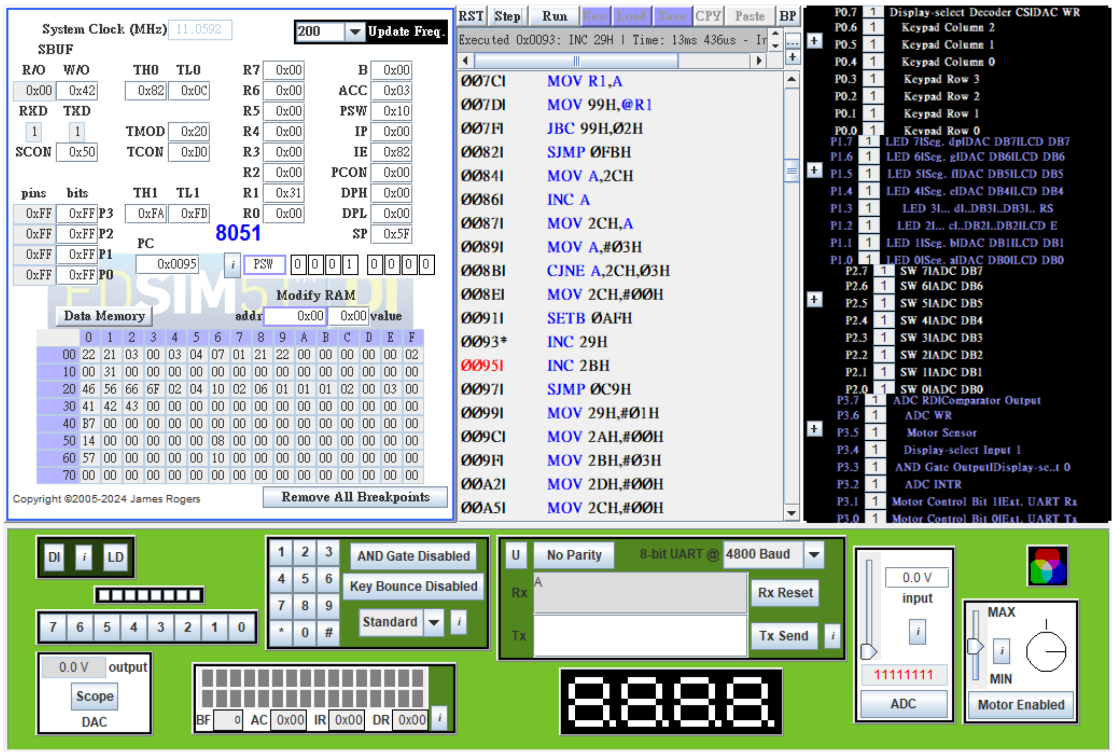


```
System Clock (MHz) 11.0592      200  Update Freq.
SBUF
R/O   W/O     TH0   TL0     R7 0x00      B    0x00
0x00  0x41    0x46  0x1C    R6 0x00      ACC  0x01
RXD   TXD                   R5 0x00      PSW  0x11
1     1       TMOD  0x20    R4 0x00      IP   0x00
SCON  0x50    TCON  0xD0    R3 0x00      IE   0x82
                            R2 0x00      PCON 0x00
pins  bits    TH1   TL1     R1 0x30      DPH  0x00
0xFF  0xFF P3 0xFA  0xFB    R0 0x00      DPL  0x00
0xFF  0xFF P2                  8051      SP   0x5F
0xFF  0xFF P1   PC
0xFF  0xFF P0   0x0076      PSW  0 0 0 1  0 0 0 1

Data Memory          Modify RAM  addr 0x00  0x00 value
    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
00 22 21 03 00 03 04 07 01 21 22 00 00 00 00 00 02
10 00 30 00 00 00 00 00 00 00 00 00 00 00 00 00 00
20 46 56 66 6F 02 04 10 02 06 00 01 01 01 00 03 00
30 41 42 43 00 00 00 00 00 00 00 00 00 00 00 00 00
40 B7 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
50 14 00 00 00 00 00 08 00 00 00 00 00 00 00 00 00
60 57 00 00 00 00 00 10 00 00 00 00 00 00 00 00 00
70 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Copyright ©2005-2024 James Rogers     Remove All Breakpoints
```

```
Executed 0x0074: DEC 29H | Time: 11ms 370us - Ir
ØØ62*   MOV ØEØH,2AH
ØØ65|   JZ ØFBH
ØØ67|   JB ØE7H,ØF8H
ØØ6A|   DEC 2AH
ØØ6C|   MOV ØEØH,29H
ØØ6F|   JZ ØFBH
ØØ71|   JB ØE7H,ØF8H
ØØ74|   DEC 29H
ØØ76|   CLR ØAFH
ØØ78|   MOV A,2CH
ØØ7A|   ADD A,#3ØH
ØØ7C|   MOV R1,A
ØØ7D|   MOV 99H,@R1
ØØ7F|   JBC 99H,Ø2H
ØØ82|   SJMP ØFBH
ØØ84|   MOV A,2CH
ØØ86|   INC A
ØØ87|   MOV 2CH,A
ØØ89|   MOV A,#Ø3H
```

```
P0.7 1 Display-select Decoder CS|DAC WR
P0.6 1 Keypad Column 2
P0.5 1 Keypad Column 1
P0.4 1 Keypad Column 0
P0.3 1 Keypad Row 3
P0.2 1 Keypad Row 2
P0.1 1 Keypad Row 1
P0.0 1 Keypad Row 0
P1.7 1 LED 7|Seg. dp|DAC DB7|LCD DB7
P1.6 1 LED 6|Seg. g|DAC DB6|LCD DB6
P1.5 1 LED 5|Seg. f|DAC DB5|LCD DB5
P1.4 1 LED 4|Seg. e|DAC DB4|LCD DB4
P1.3 1 LED 3|... d|..DB3|..DB3|.. RS
P1.2 1 LED 2|... c|..DB2|..DB2|LCD E
P1.1 1 LED 1|Seg. b|DAC DB1|LCD DB1
P1.0 1 LED 0|Seg. a|DAC DB0|LCD DB0
P2.7 1 SW 7|ADC DB7
P2.6 1 SW 6|ADC DB6
P2.5 1 SW 5|ADC DB5
P2.4 1 SW 4|ADC DB4
P2.3 1 SW 3|ADC DB3
P2.2 1 SW 2|ADC DB2
P2.1 1 SW 1|ADC DB1
P2.0 1 SW 0|ADC DB0
P3.7 1 ADC RD|Comparator Output
P3.6 1 ADC WR
P3.5 1 Motor Sensor
P3.4 1 Display-select Input 1
P3.3 1 AND Gate Output|Display-se..t 0
P3.2 1 ADC INTR
P3.1 1 Motor Control Bit 1|Ext. UART Rx
P3.0 1 Motor Control Bit 0|Ext. UART Tx
```

▲ After **`SemaphoreWait(mutex);`** (mutex=0, full=1, empty=1).



```
Executed 0x0093: INC 29H | Time: 13ms 436us - Ir
007C| MOV R1,A
007D| MOV 99H,@R1
007F| JBC 99H,02H
0082| SJMP 0FBH
0084| MOV A,2CH
0086| INC A
0087| MOV 2CH,A
0089| MOV A,#03H
008B| CJNE A,2CH,03H
008E| MOV 2CH,#00H
0091| SETB 0AFH
0093* INC 29H
0095| INC 2BH
0097| SJMP 0C9H
0099| MOV 29H,#01H
009C| MOV 2AH,#00H
009F| MOV 2BH,#03H
00A2| MOV 2DH,#00H
00A5| MOV 2CH,#00H
```

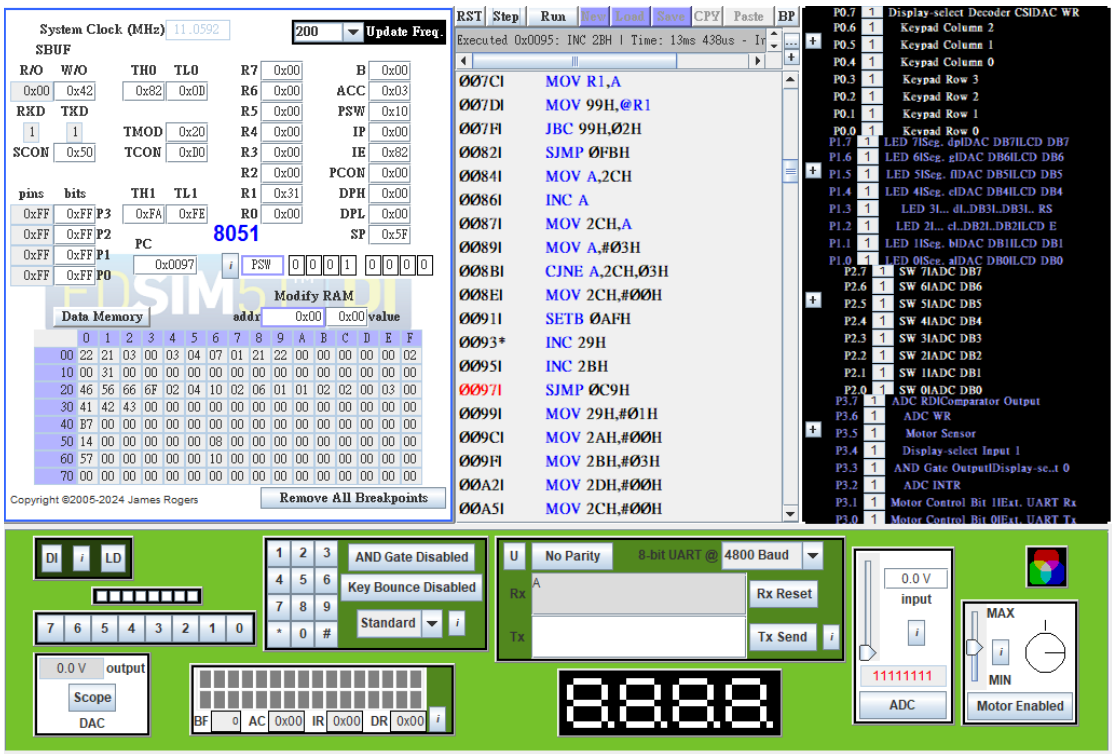
System Clock (MHz) 11.0592 · Update Freq. 200 · SBUF R/O 0x00 W/O 0x42 · RXD 1 TXD 1 · SCON 0x50 · TH0 0x82 TL0 0x0C · TMOD 0x20 · TCON 0xD0 · TH1 0xFA TL1 0xFD · P3 0xFF/0xFF · P2 0xFF/0xFF · P1 0xFF/0xFF · P0 0xFF/0xFF · PC 0x0095 · PSW 0 0 0 1 0 0 0 0

R7 0x00 · R6 0x00 · R5 0x00 · R4 0x00 · R3 0x00 · R2 0x00 · R1 0x31 · R0 0x00 · B 0x00 · ACC 0x03 · PSW 0x10 · IP 0x00 · IE 0x82 · PCON 0x00 · DPH 0x00 · DPL 0x00 · SP 0x5F

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	22	21	03	00	03	04	07	01	21	22	00	00	00	00	00	02
10	00	31	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	46	56	66	6F	02	04	10	02	06	01	01	01	02	00	03	00
30	41	42	43	00	00	00	00	00	00	00	00	00	00	00	00	00
40	B7	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
50	14	00	00	00	00	00	08	00	00	00	00	00	00	00	00	00
60	57	00	00	00	00	00	10	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Copyright ©2005-2024 James Rogers

▲ After **`SemaphoreSignal(mutex);`** (mutex=1, full=1, empty=1).



```
Executed 0x0095: INC 2BH | Time: 13ms 438us - Ir
007C| MOV R1,A
007D| MOV 99H,@R1
007F| JBC 99H,02H
0082| SJMP 0FBH
0084| MOV A,2CH
0086| INC A
0087| MOV 2CH,A
0089| MOV A,#03H
008B| CJNE A,2CH,03H
008E| MOV 2CH,#00H
0091| SETB 0AFH
0093* INC 29H
0095| INC 2BH
0097| SJMP 0C9H
0099| MOV 29H,#01H
009C| MOV 2AH,#00H
009F| MOV 2BH,#03H
00A2| MOV 2DH,#00H
00A5| MOV 2CH,#00H
```

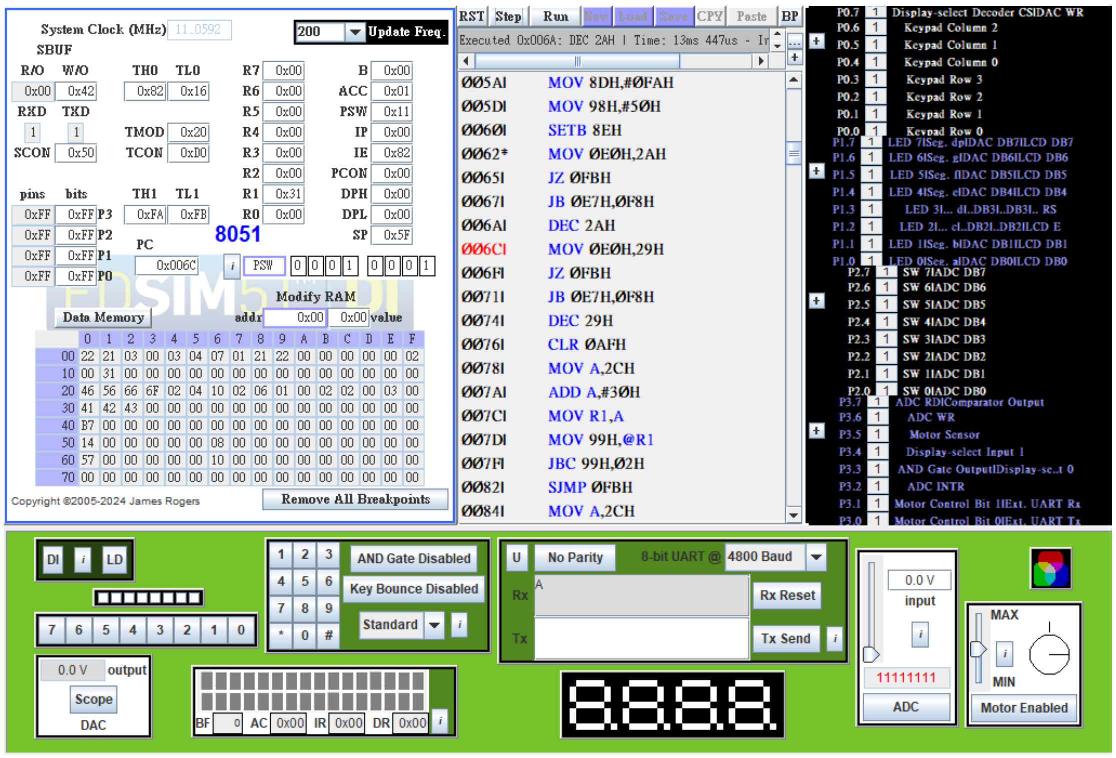
System Clock (MHz) 11.0592 · Update Freq. 200 · SBUF R/O 0x00 W/O 0x42 · RXD 1 TXD 1 · SCON 0x50 · TH0 0x82 TL0 0x0D · TMOD 0x20 · TCON 0xD0 · TH1 0xFA TL1 0xFE · P3 0xFF/0xFF · P2 0xFF/0xFF · P1 0xFF/0xFF · P0 0xFF/0xFF · PC 0x0097 · PSW 0 0 0 1 0 0 0 0

R7 0x00 · R6 0x00 · R5 0x00 · R4 0x00 · R3 0x00 · R2 0x00 · R1 0x31 · R0 0x00 · B 0x00 · ACC 0x03 · PSW 0x10 · IP 0x00 · IE 0x82 · PCON 0x00 · DPH 0x00 · DPL 0x00 · SP 0x5F

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	22	21	03	00	03	04	07	01	21	22	00	00	00	00	00	02
10	00	31	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	46	56	66	6F	02	04	10	02	06	01	01	02	02	00	03	00
30	41	42	43	00	00	00	00	00	00	00	00	00	00	00	00	00
40	B7	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
50	14	00	00	00	00	00	08	00	00	00	00	00	00	00	00	00
60	57	00	00	00	00	00	10	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

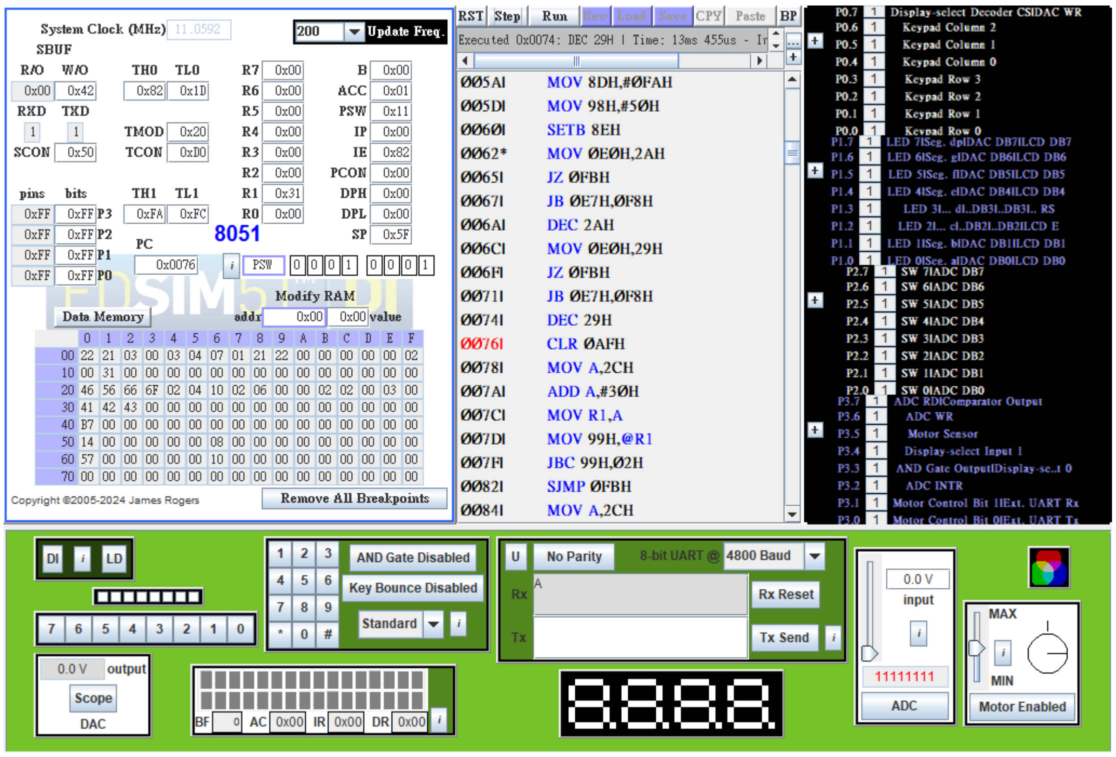
Copyright ©2005-2024 James Rogers

▲ After **`SemaphoreSignal(empty);`** (mutex=1, full=1, empty=2).



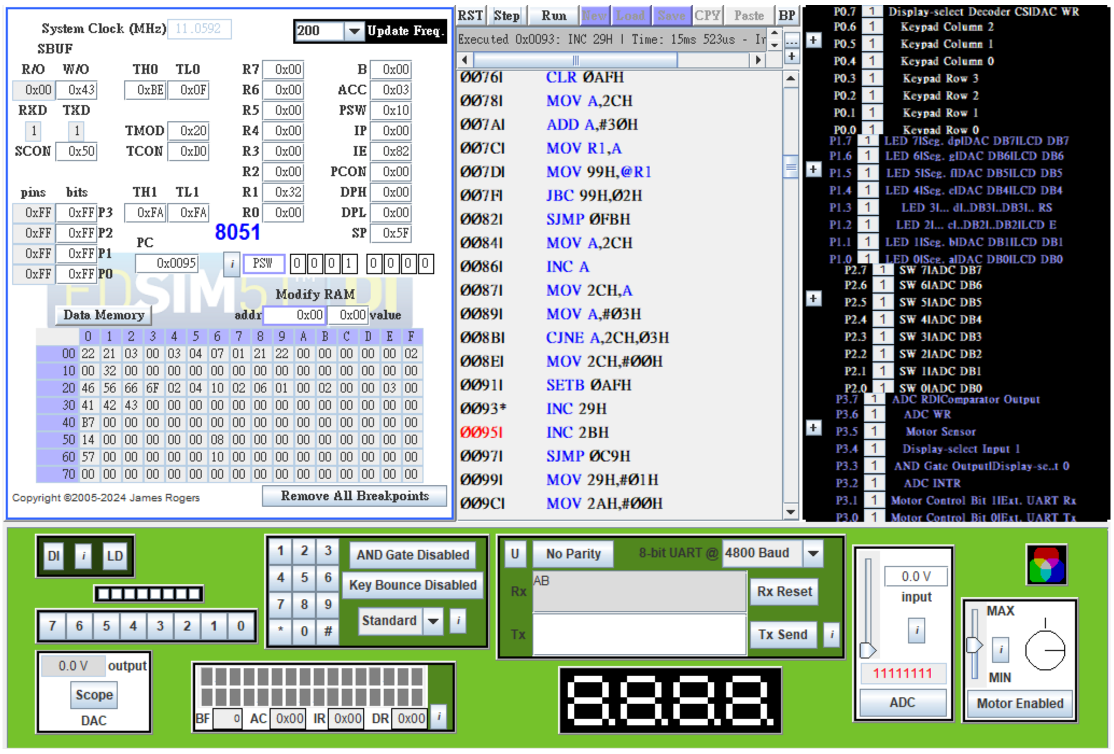
```
System Clock (MHz) 11.0592      200   Update Freq.
SBUF
R/O   W/O     TH0   TL0     R7  0x00    B    0x00
0x00  0x42    0x82  0x16    R6  0x00    ACC  0x01
RXD   TXD                   R5  0x00    PSW  0x11
1     1       TMOD  0x20    R4  0x00    IP   0x00
SCON  0x50    TCON  0xD0    R3  0x00    IE   0x82
                            R2  0x00    PCON 0x00
pins  bits    TH1   TL1     R1  0x31    DPH  0x00
0xFF  0xFF P3 0xFA  0xFB    R0  0x00    DPL  0x00
0xFF  0xFF P2         8051              SP   0x5F
0xFF  0xFF P1   PC
0xFF  0xFF P0   0x006C   PSW 0 0 0 1 0 0 0 1
                Modify RAM
Data Memory     addr 0x00  0x00 value
    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
00 22 21 03 00 03 04 07 01 21 22 00 00 00 00 00 02
10 00 31 00 00 00 00 00 00 00 00 00 00 00 00 00 00
20 46 56 66 6F 02 04 10 02 06 01 00 02 02 00 03 00
30 41 42 43 00 00 00 00 00 00 00 00 00 00 00 00 00
40 B7 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
50 14 00 00 00 00 08 00 00 00 00 00 00 00 00 00 00
60 57 00 00 00 00 00 10 00 00 00 00 00 00 00 00 00
70 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Copyright ©2005-2024 James Rogers    Remove All Breakpoints

RST Step Run New Load Save CPY Paste BP
Executed 0x006A: DEC 2AH | Time: 13ms 447us
005A|  MOV 8DH,#0FAH
005D|  MOV 98H,#50H
0060|  SETB 8EH
0062*  MOV 0E0H,2AH
0065|  JZ 0FBH
0067|  JB 0E7H,0F8H
006A|  DEC 2AH
006C|  MOV 0E0H,29H
006F|  JZ 0FBH
0071|  JB 0E7H,0F8H
0074|  DEC 29H
0076|  CLR 0AFH
0078|  MOV A,2CH
007A|  ADD A,#30H
007C|  MOV R1,A
007D|  MOV 99H,@R1
007F|  JBC 99H,02H
0082|  SJMP 0FBH
0084|  MOV A,2CH

P0.7 1 Display-select Decoder CS|DAC WR
P0.6 1 Keypad Column 2
P0.5 1 Keypad Column 1
P0.4 1 Keypad Column 0
P0.3 1 Keypad Row 3
P0.2 1 Keypad Row 2
P0.1 1 Keypad Row 1
P0.0 1 Keypad Row 0
P1.7 1 LED 7|Seg. dp|DAC DB7|LCD DB7
P1.6 1 LED 6|Seg. g|DAC DB6|LCD DB6
P1.5 1 LED 5|Seg. f|DAC DB5|LCD DB5
P1.4 1 LED 4|Seg. e|DAC DB4|LCD DB4
P1.3 1 LED 3|... d|...DB3|...DB3|.. RS
P1.2 1 LED 2|... c|...DB2|...DB2|LCD E
P1.1 1 LED 1|Seg. b|DAC DB1|LCD DB1
P1.0 1 LED 0|Seg. a|DAC DB0|LCD DB0
P2.7 1 SW 7|ADC DB7
P2.6 1 SW 6|ADC DB6
P2.5 1 SW 5|ADC DB5
P2.4 1 SW 4|ADC DB4
P2.3 1 SW 3|ADC DB3
P2.2 1 SW 2|ADC DB2
P2.1 1 SW 1|ADC DB1
P2.0 1 SW 0|ADC DB0
P3.7 1 ADC RD|Comparator Output
P3.6 1 ADC WR
P3.5 1 Motor Sensor
P3.4 1 Display-select Input 1
P3.3 1 AND Gate Output|Display-se..t 0
P3.2 1 ADC INTR
P3.1 1 Motor Control Bit 1|Ext. UART Rx
P3.0 1 Motor Control Bit 0|Ext. UART Tx

DI  i  LD     7 6 5 4 3 2 1 0
0.0 V output  Scope  DAC
1 2 3  4 5 6  7 8 9  * 0 #   AND Gate Disabled   Key Bounce Disabled   Standard
BF 0  AC 0x00  IR 0x00  DR 0x00
U  No Parity  8-bit UART @ 4800 Baud
Rx A   Rx Reset
Tx     Tx Send
0.0 V input  11111111  ADC
MAX  MIN  Motor Enabled
```

▲ After `SemaphoreWait(full);` (mutex=1, full=0, empty=2).



```
System Clock (MHz) 11.0592      200   Update Freq.
SBUF
R/O   W/O     TH0   TL0     R7  0x00    B    0x00
0x00  0x42    0x82  0x1D    R6  0x00    ACC  0x01
RXD   TXD                   R5  0x00    PSW  0x11
1     1       TMOD  0x20    R4  0x00    IP   0x00
SCON  0x50    TCON  0xD0    R3  0x00    IE   0x82
                            R2  0x00    PCON 0x00
pins  bits    TH1   TL1     R1  0x31    DPH  0x00
0xFF  0xFF P3 0xFA  0xFC    R0  0x00    DPL  0x00
0xFF  0xFF P2         8051              SP   0x5F
0xFF  0xFF P1   PC
0xFF  0xFF P0   0x0076   PSW 0 0 0 1 0 0 0 1
                Modify RAM
Data Memory     addr 0x00  0x00 value
    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
00 22 21 03 00 03 04 07 01 21 22 00 00 00 00 00 02
10 00 31 00 00 00 00 00 00 00 00 00 00 00 00 00 00
20 46 56 66 6F 02 04 10 02 06 01 00 02 02 00 03 00
30 41 42 43 00 00 00 00 00 00 00 00 00 00 00 00 00
40 B7 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
50 14 00 00 00 00 08 00 00 00 00 00 00 00 00 00 00
60 57 00 00 00 00 00 10 00 00 00 00 00 00 00 00 00
70 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Copyright ©2005-2024 James Rogers    Remove All Breakpoints

RST Step Run New Load Save CPY Paste BP
Executed 0x0074: DEC 29H | Time: 13ms 455us
005A|  MOV 8DH,#0FAH
005D|  MOV 98H,#50H
0060|  SETB 8EH
0062*  MOV 0E0H,2AH
0065|  JZ 0FBH
0067|  JB 0E7H,0F8H
006A|  DEC 2AH
006C|  MOV 0E0H,29H
006F|  JZ 0FBH
0071|  JB 0E7H,0F8H
0074|  DEC 29H
0076|  CLR 0AFH
0078|  MOV A,2CH
007A|  ADD A,#30H
007C|  MOV R1,A
007D|  MOV 99H,@R1
007F|  JBC 99H,02H
0082|  SJMP 0FBH
0084|  MOV A,2CH

P0.7 1 Display-select Decoder CS|DAC WR
P0.6 1 Keypad Column 2
P0.5 1 Keypad Column 1
P0.4 1 Keypad Column 0
P0.3 1 Keypad Row 3
P0.2 1 Keypad Row 2
P0.1 1 Keypad Row 1
P0.0 1 Keypad Row 0
P1.7 1 LED 7|Seg. dp|DAC DB7|LCD DB7
P1.6 1 LED 6|Seg. g|DAC DB6|LCD DB6
P1.5 1 LED 5|Seg. f|DAC DB5|LCD DB5
P1.4 1 LED 4|Seg. e|DAC DB4|LCD DB4
P1.3 1 LED 3|... d|...DB3|...DB3|.. RS
P1.2 1 LED 2|... c|...DB2|...DB2|LCD E
P1.1 1 LED 1|Seg. b|DAC DB1|LCD DB1
P1.0 1 LED 0|Seg. a|DAC DB0|LCD DB0
P2.7 1 SW 7|ADC DB7
P2.6 1 SW 6|ADC DB6
P2.5 1 SW 5|ADC DB5
P2.4 1 SW 4|ADC DB4
P2.3 1 SW 3|ADC DB3
P2.2 1 SW 2|ADC DB2
P2.1 1 SW 1|ADC DB1
P2.0 1 SW 0|ADC DB0
P3.7 1 ADC RD|Comparator Output
P3.6 1 ADC WR
P3.5 1 Motor Sensor
P3.4 1 Display-select Input 1
P3.3 1 AND Gate Output|Display-se..t 0
P3.2 1 ADC INTR
P3.1 1 Motor Control Bit 1|Ext. UART Rx
P3.0 1 Motor Control Bit 0|Ext. UART Tx

DI  i  LD     7 6 5 4 3 2 1 0
0.0 V output  Scope  DAC
1 2 3  4 5 6  7 8 9  * 0 #   AND Gate Disabled   Key Bounce Disabled   Standard
BF 0  AC 0x00  IR 0x00  DR 0x00
U  No Parity  8-bit UART @ 4800 Baud
Rx A   Rx Reset
Tx     Tx Send
0.0 V input  11111111  ADC
MAX  MIN  Motor Enabled
```

▲ After `SemaphoreWait(mutex);` (mutex=0, full=0, empty=2).



```
System Clock (MHz) 11.0592        200  Update Freq.
SBUF
R/O   W/O      TH0   TL0      R7 0x00      B    0x00
0x00  0x43     0xBE  0x0F     R6 0x00      ACC  0x03
RXD   TXD                     R5 0x00      PSW  0x10
1     1        TMOD  0x20     R4 0x00      IP   0x00
SCON  0x50     TCON  0xD0     R3 0x00      IE   0x82
                              R2 0x00      PCON 0x00
pins  bits     TH1   TL1      R1 0x32      DPH  0x00
0xFF  0xFF P3  0xFA  0xFA     R0 0x00      DPL  0x00
0xFF  0xFF P2                              SP   0x5F
0xFF  0xFF P1  PC 0x0095      PSW 0 0 0 1  0 0 0 0
0xFF  0xFF P0
                              Modify RAM
Data Memory                   addr 0x00  0x00 value
```

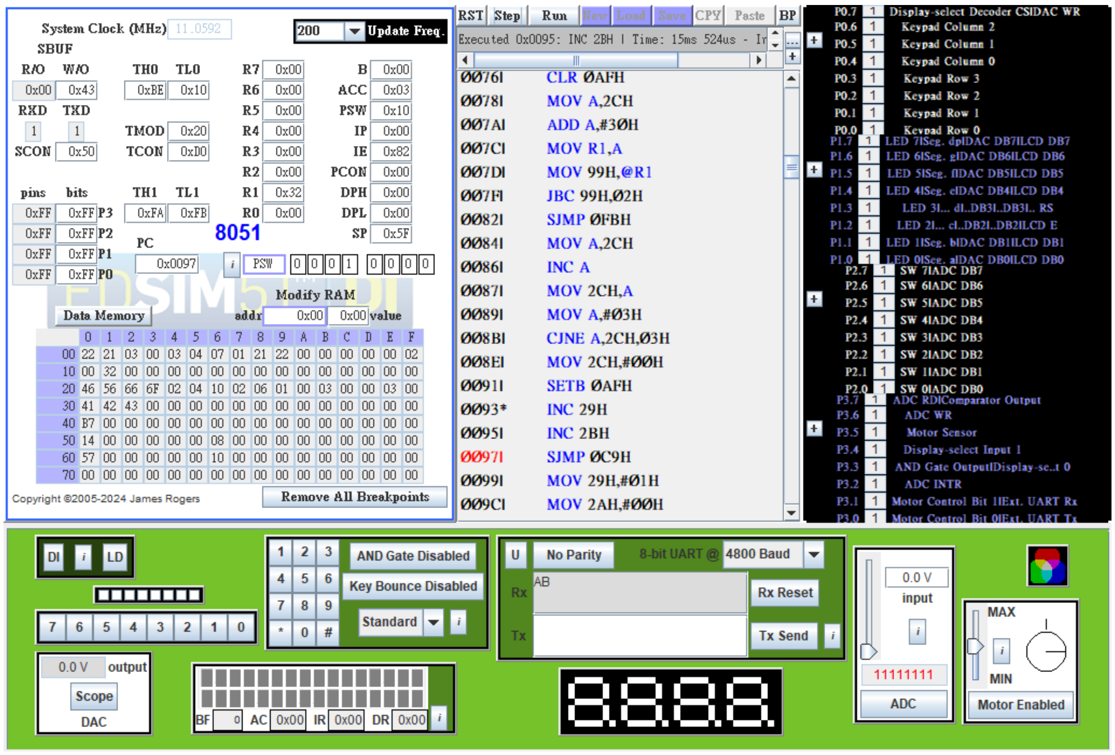
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	22	21	03	00	03	04	07	01	21	22	00	00	00	00	00	02
10	00	32	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	46	56	66	6F	02	04	10	02	06	01	00	02	00	00	03	00
30	41	42	43	00	00	00	00	00	00	00	00	00	00	00	00	00
40	B7	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
50	14	00	00	00	00	00	08	00	00	00	00	00	00	00	00	00
60	57	00	00	00	00	00	10	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Copyright ©2005-2024 James Rogers

```
Executed 0x0093: INC 29H | Time: 15ms 523us - Ir
0076|   CLR 0AFH
0078|   MOV A,2CH
007A|   ADD A,#30H
007C|   MOV R1,A
007D|   MOV 99H,@R1
007F|   JBC 99H,02H
0082|   SJMP 0FBH
0084|   MOV A,2CH
0086|   INC A
0087|   MOV 2CH,A
0089|   MOV A,#03H
008B|   CJNE A,2CH,03H
008E|   MOV 2CH,#00H
0091|   SETB 0AFH
0093*   INC 29H
0095|   INC 2BH
0097|   SJMP 0C9H
0099|   MOV 29H,#01H
009C|   MOV 2AH,#00H
```

```
No Parity   8-bit UART @ 4800 Baud
Rx  AB
```

▲ After **`SemaphoreSignal(mutex);`** (mutex=1, full=0, empty=2).



```
System Clock (MHz) 11.0592        200  Update Freq.
SBUF
R/O   W/O      TH0   TL0      R7 0x00      B    0x00
0x00  0x43     0xBE  0x10     R6 0x00      ACC  0x03
RXD   TXD                     R5 0x00      PSW  0x10
1     1        TMOD  0x20     R4 0x00      IP   0x00
SCON  0x50     TCON  0xD0     R3 0x00      IE   0x82
                              R2 0x00      PCON 0x00
pins  bits     TH1   TL1      R1 0x32      DPH  0x00
0xFF  0xFF P3  0xFA  0xFB     R0 0x00      DPL  0x00
0xFF  0xFF P2                              SP   0x5F
0xFF  0xFF P1  PC 0x0097      PSW 0 0 0 1  0 0 0 0
0xFF  0xFF P0
                              Modify RAM
Data Memory                   addr 0x00  0x00 value
```

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	22	21	03	00	03	04	07	01	21	22	00	00	00	00	00	02
10	00	32	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	46	56	66	6F	02	04	10	02	06	01	00	03	00	00	03	00
30	41	42	43	00	00	00	00	00	00	00	00	00	00	00	00	00
40	B7	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
50	14	00	00	00	00	00	08	00	00	00	00	00	00	00	00	00
60	57	00	00	00	00	00	10	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Copyright ©2005-2024 James Rogers

```
Executed 0x0095: INC 2BH | Time: 15ms 524us - Ir
0076|   CLR 0AFH
0078|   MOV A,2CH
007A|   ADD A,#30H
007C|   MOV R1,A
007D|   MOV 99H,@R1
007F|   JBC 99H,02H
0082|   SJMP 0FBH
0084|   MOV A,2CH
0086|   INC A
0087|   MOV 2CH,A
0089|   MOV A,#03H
008B|   CJNE A,2CH,03H
008E|   MOV 2CH,#00H
0091|   SETB 0AFH
0093*   INC 29H
0095|   INC 2BH
0097|   SJMP 0C9H
0099|   MOV 29H,#01H
009C|   MOV 2AH,#00H
```

```
No Parity   8-bit UART @ 4800 Baud
Rx  AB
```

▲ After **`SemaphoreSignal(empty);`** (mutex=1, full=0, empty=3).