EE343 CMOS Mixed Signal Design
Lab 3: Charge Redistribution DAC Layout and Simulation

Jeffrey Cool 006442018
Dr. M. Wagdy

10-29-2015

Contents

1 Introduction

Presented here is a detailed account of the design, layout and simulation of a 4 bit serial DAC within the Microwind and DSCH environments. Figure 1 shows the charge redistribution circuit which provides 4 bit serial digital to analog conversion. Table 1 summarizes the required switching signals. The integrated circuit presented is laid out in $0.12\mu m$ CMOS technology, and consists of the switched capacitor circuit and a control unit which provides parallel to serial data conversion and sequential control of the switches.

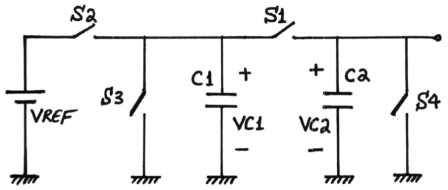

Figure 1: Charge Redistribution Circuit

Table 1: Control Signals

PHASE 1	$S_1 = 0$ $S_2 = bit$ $S_3 = \overline{bit}$ $S_4 = 0(1)^*$
$^*S_4 = 1$ only during clock cycle 1	
PHASE 2	$S_1 = 1$ $S_2 = 0$ $S_3 = 0$ $S_4 = 0$

2 Parallel to Serial Data Conversion

An easy way to accomplish parallel to serial conversion is to use a multiplexer. The 4 bit DAC requires a 4 to 1 MUX, which can be realized with 10 transistors using pass gates, as shown in Figure 2. The two inverters are used to restore the logic levels (NPGs pass logic 1 as $V_{DD} - V_{TN}$ and PPGs pass logic zero as V_{TP}) and to provide logical inversion.

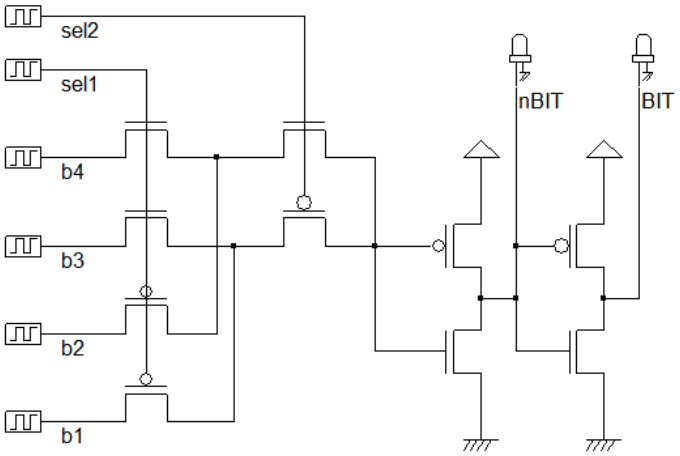

Figure 2: 4 to 1 MUX schematic

The layout for the MUX was done manually in Microwind. The aspect ratios of the NMOS and PMOS transistors are 5 and 10 respectively, with $L = 2\lambda$. Note the dotted line around the transistors–this is the option mask which is used here to specify high speed (low threshold voltage) devices to minimize the negative effects of the pass transistors and to speed up the conversion.

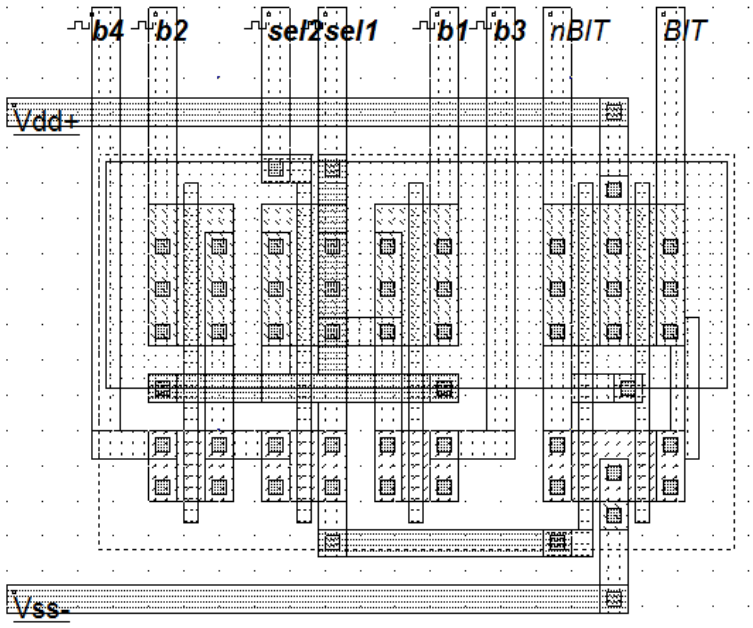

Figure 3: 4 to 1 MUX Layout

Proper operation of the multiplexer is verified in the timing diagram below:

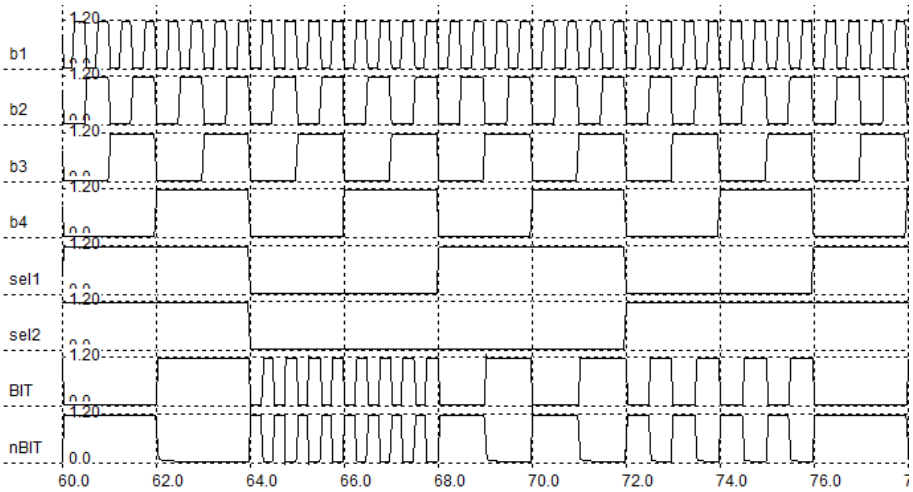

Figure 4: 4 to 1 MUX timing diagram

3 Controlling the MUX: A 2 Bit Dynamic Counter

As seen in Table 1, switches S_2 and S_3 are logically determined by the current input bit. Since the DAC must input the LSB (b_4) first, the control inputs to the multiplexor can be generated using a two bit down counter (3 to 0).

3.1 Edge Detector Circuit

Since a dynamic D latch will be used for the storage elements, an edge detector circuit is needed. Figure 5 shows a logic diagram for an edge detector. The output is high when the two inputs are the same, and

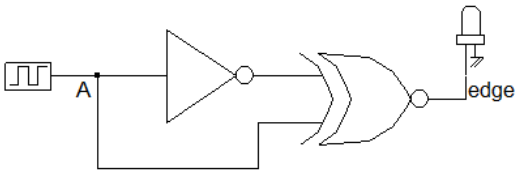

Figure 5: Edge Detector Logic Diagram

this only occurs during a small interval due to the short delay of the inverter. A simple NXOR gate can be realized using pass gates and two inverters.

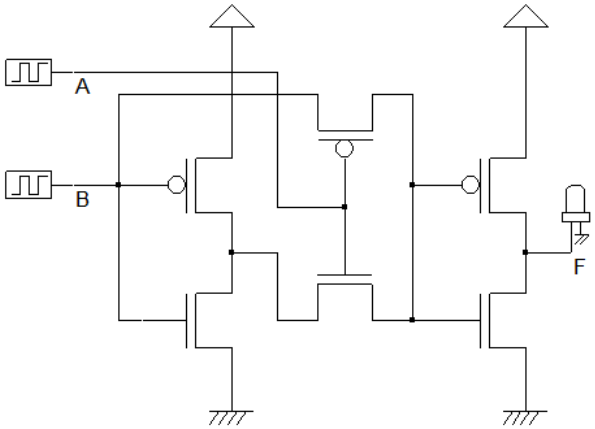

Figure 6: NXOR Gate CMOS Realization

Realizing the edge detector is simply a matter of adding another inverter. The delay inverter shown Figure 7 must have long channel MOS devices in order to provide sufficient delay.

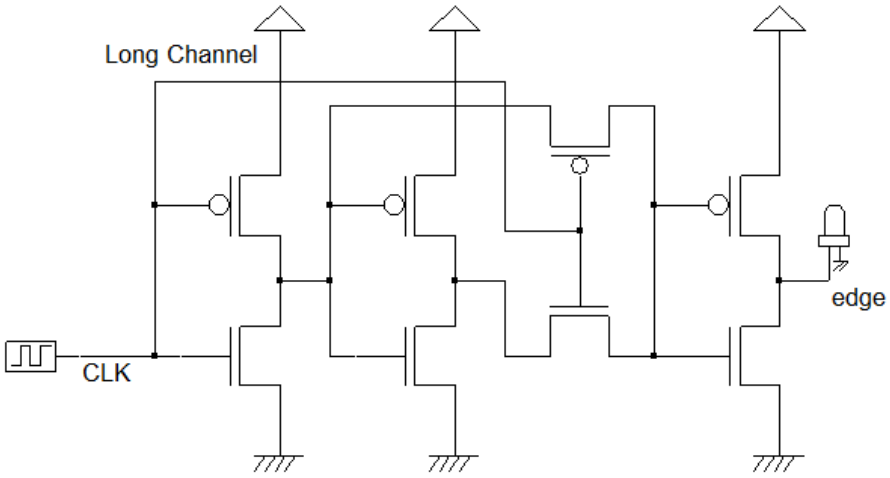

Figure 7: CMOS Edge Detector Schematic

The edge detector circuit was laid out manually to allow for fine control over MOS characteristics. The

delay inverter has twice the length of the others, and it is specified as a low leakage device (slower). The other transistors are specified as low threshold voltage devices using the option layer–this has the effect of reducing delay in the inverters and allowing the PGs to pass better logic levels. It would seem that

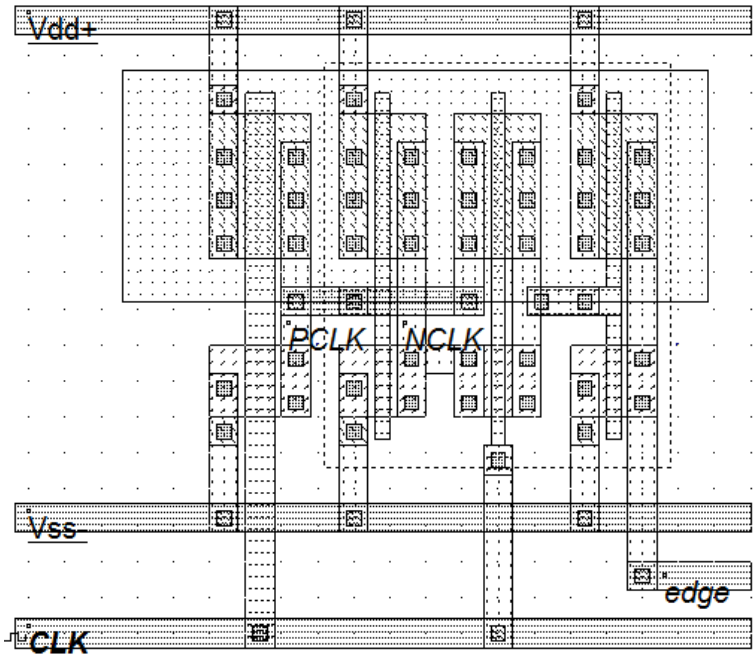

Figure 8: Edge Detector Layout

this circuit should detect both positive and negative edges, which is not desirable since an additional latch would be needed for the counter; however, the circuit will act as a positive edge detector with a very good noise margin if the input into the NMOS PG (NCLK) has a faster edge than the signal going into the PMOS PG (PCLK). This was the goal of the layout design shown in Figure 8. Result of BSIM4 simulation is shown below.

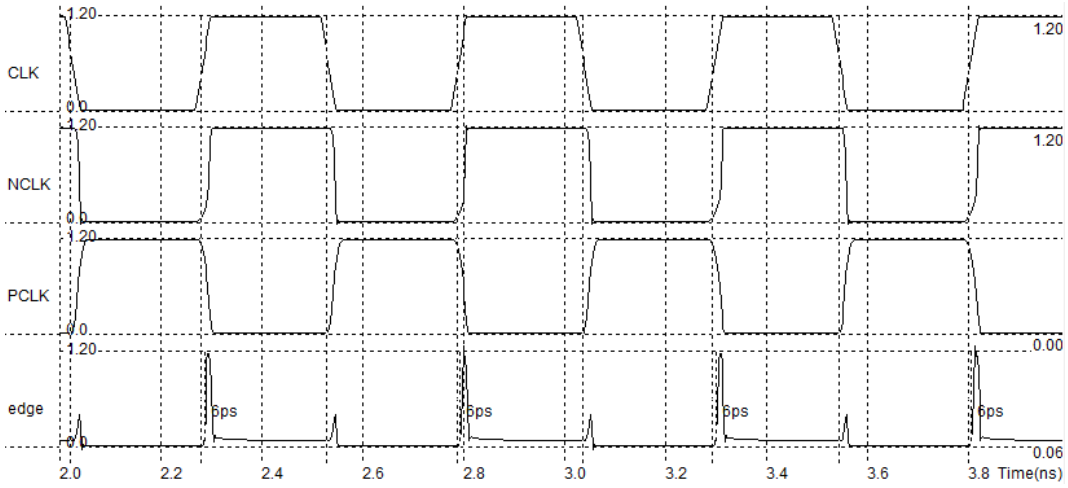

Figure 9: Edge Detector Layout

3.2 Dynamic D-Latch

The dynamic D-latch is an attractive option because it only requires five transistors: 1 NMOS PG and 2 inverters (a buffer). The layout is shown below.

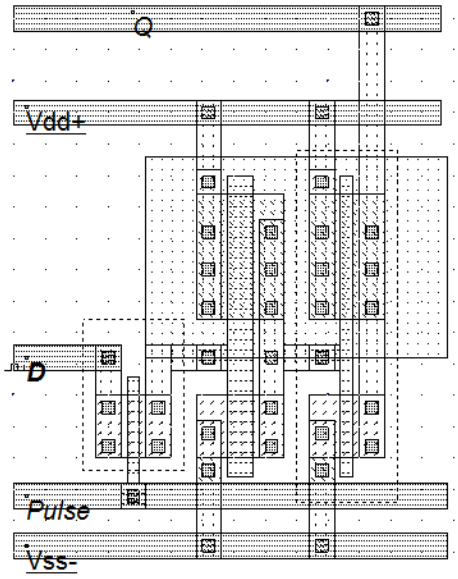

Figure 10: Dynamic D Latch Layout

Notice that the options mask does not surround the the first inverter. The gate of the first inverter is the storage node, so it is made to be a low leakage type, while the pass gate benefits from lower threshold voltage, as does the output inverter.

3.3 Synchronous Counter

The complete counter is shown in Figure 11, and the BSIM4 simulation results are shown in figure 12

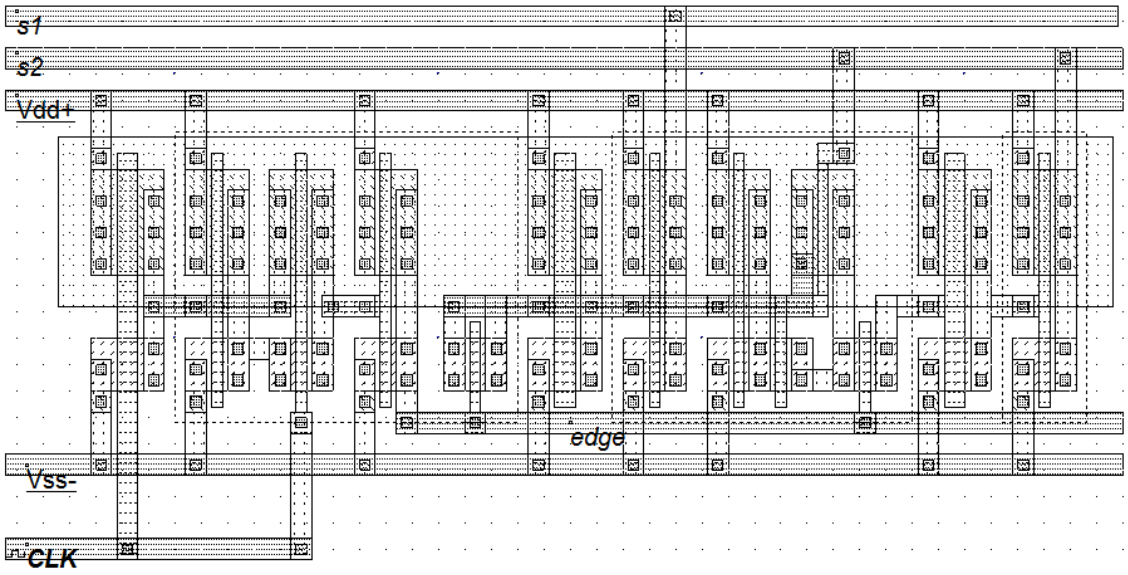

Figure 11: Synchronous Counter Layout

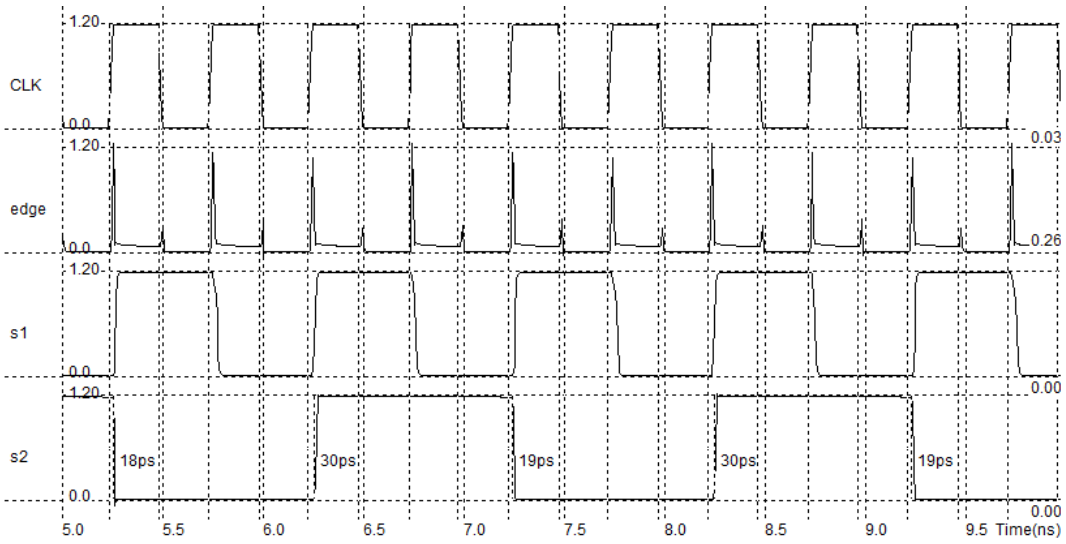

Figure 12: Counter Timing Diagram

4 Switching Control Logic

The four switches S_i must be properly controlled to give D to A conversion. using the outputs of the counter and the multiplexer, and table 1, the logic for the control signals are summarized below, and the layout for this logic is shown in Figure 13.

$$S_1 = \overline{CLK}$$
$$S_2 = CLK \cdot Bit = \overline{\overline{CLK} + \overline{Bit}}$$
$$S_3 = CLK \cdot \overline{Bit} = \overline{\overline{CLK} + Bit}$$
$$S_4 = CLK \cdot Sel_1 \cdot Sel_2$$

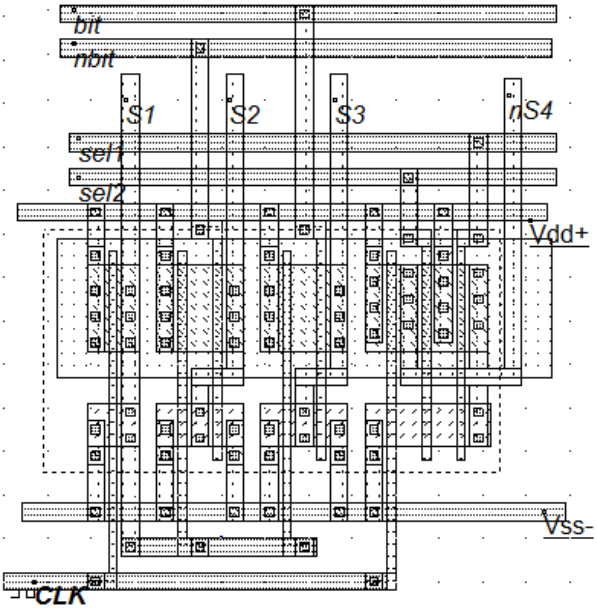

Figure 13: Control Logic For Switches

The layout for the whole control circuit is shown in figure 14.

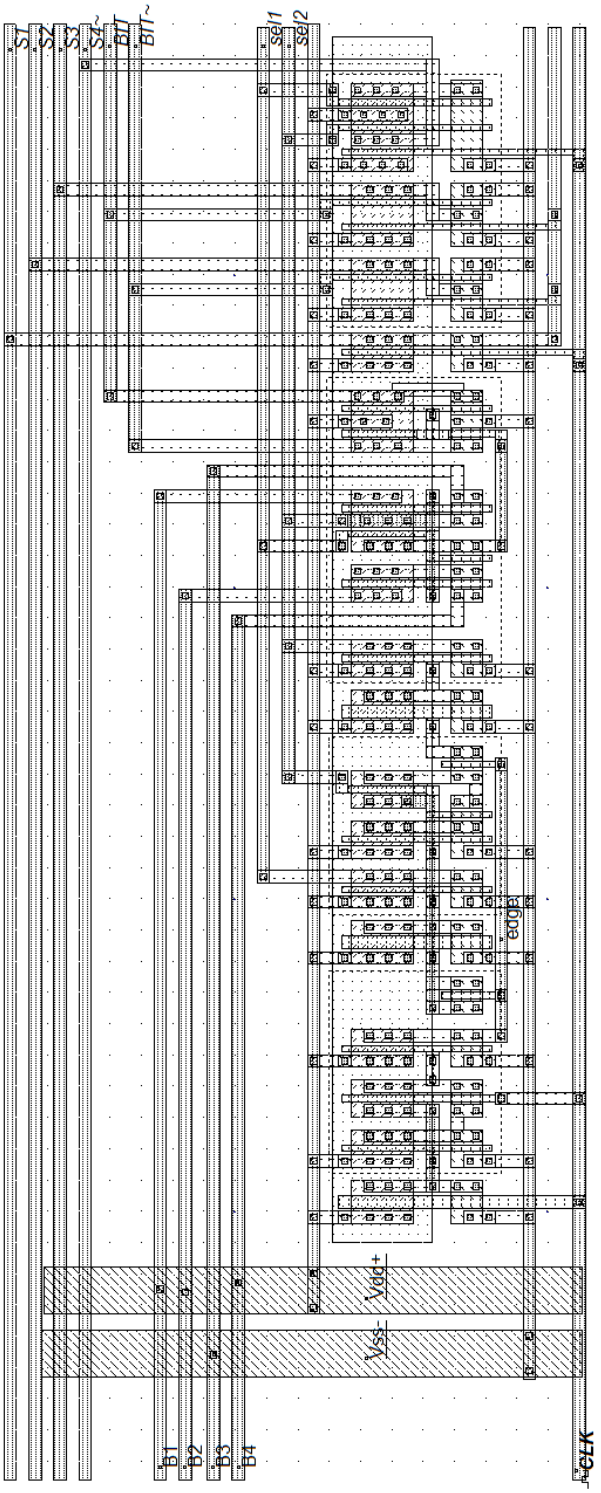

Figure 14: Complete Controller layout

Special attention must be payed to delays in the design so that the operation complies with table 1. Consider the timing diagram in figure 15. The test signal 1101 is applied to the input. The control signals are as they should be, except for the presence of narrow spikes which are the result of delay in the multiplexer and in the overall circuit as compared with the clock signal.

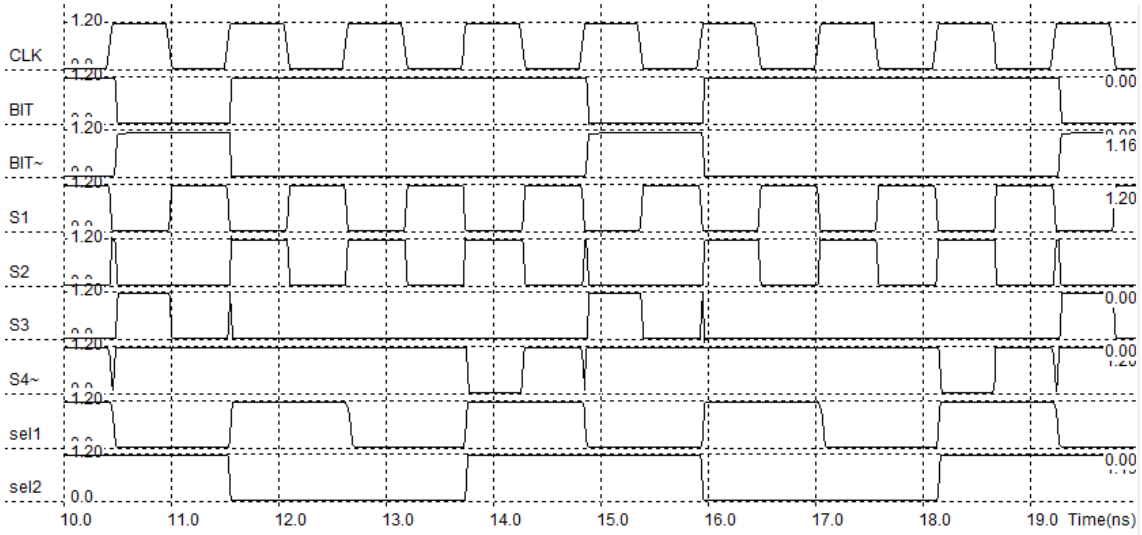

Figure 15: Response of switching signals to test input 1101

One simple solution to this problem is to use switches that have a delay long enough so that these spikes are ignored. A better way to do it is to use a second clock signal for the logic of S_i which is delayed by a small amount.

5 Charge Redistribution Circuit

The switches used are simple pass gates: the layout is shown below.

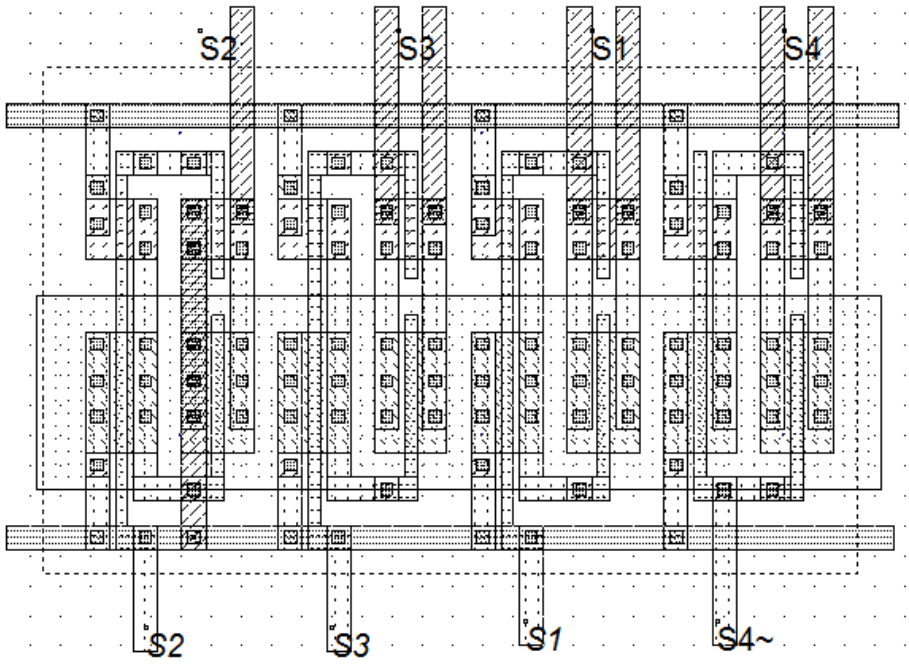

Figure 16: TG Switch Layout

The capacitor design chosen is based on NFETs, using the gate oxide capacitance. The design philosophy is that the capacitors should be large enough so that the narrow spikes have minimal effect on the conversion. Figure 17 shows the design.

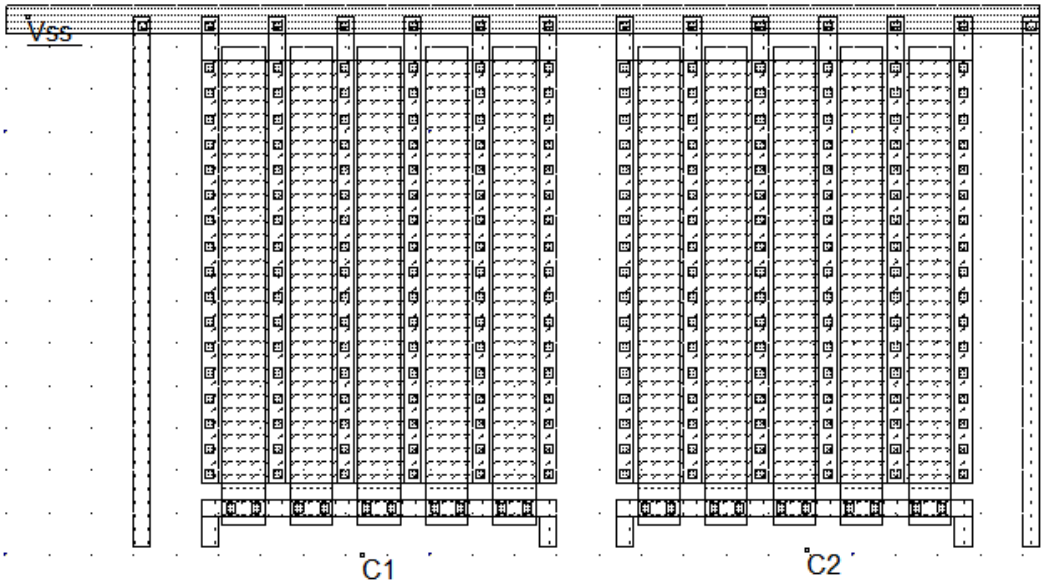

Figure 17: MOS Capacitors

6 Complete DAC

Figure **??** shows The complete DAC layout is shown in figure **??** on a subsequent page.