REV	CHANGE DESCRIPTION	NAME	DATE
A	Release		9-15-06
B	Added External Pull-down Resistor to Pin 75 (RXD0)		3-22-07
C	Added VDD_REF (pin 8) Decoupling Cap		3-30-07
D	Added EECLK (pin 69) Special Instruction		7-19-07

Document Description

Schematic Checklist for the LAN9215I, 100-pin TQFP Package

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Document Number	Revision
SC471197	D

Schematic Checklist for LAN9215I

Information Particular for the 100-pin TQFP Package

LAN9215I TQFP Phy Interface:

1. TPO+ (pin 79); This pin is the transmit twisted pair output positive connection from the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD_A (created from +3.3V). This pin also connects to the transmit channel of the magnetics.

2. TPO- (pin 78); This pin is the transmit twisted pair output negative connection from the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD_A (created from +3.3V). This pin also connects to the transmit channel of the magnetics.

3. For Transmit Channel connection and termination details, refer to Figure 1.

4. TPI+ (pin 83); This pin is the receive twisted pair input positive connection to the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD_A (created from +3.3V). This pin also connects to the receive channel of the magnetics.

5. TPI- (pin 82); This pin is the receive twisted pair input negative connection to the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD_A (created from +3.3V). This pin also connects to the receive channel of the magnetics.

6. For Receive Channel connection and termination details, refer to Figure 2.

VDD_A (+3.3V)

LAN9215I

R3 49.9 Ohms 1.0%
R4 49.9 Ohms 1.0%
R5 10.0 Ohms 1.0%

TPO+ 79
TPO- 78

I Temp Magnetics Module

Transmit Channel

TD+   TX+
TCT   TCMT
TD-   TX-

Connect TX
Center Tap to RX
Center Tap
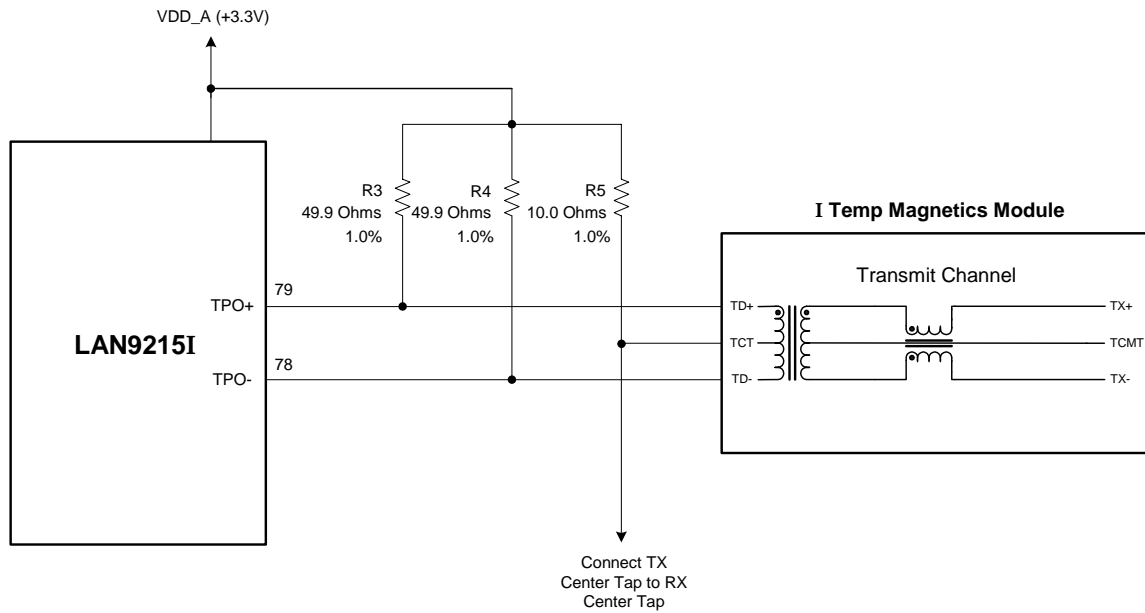
Figure 1 – Transmit Channel Connections and Terminations

Connect RX
Center Tap to TX
Center Tap

VDD_A (+3.3V)

R1 49.9 Ohms 1.0%
R2 49.9 Ohms 1.0%

LAN9215I

TPI+ 83
TPI- 82

I Temp Magnetics Module

Receive Channel

RD+   RX+
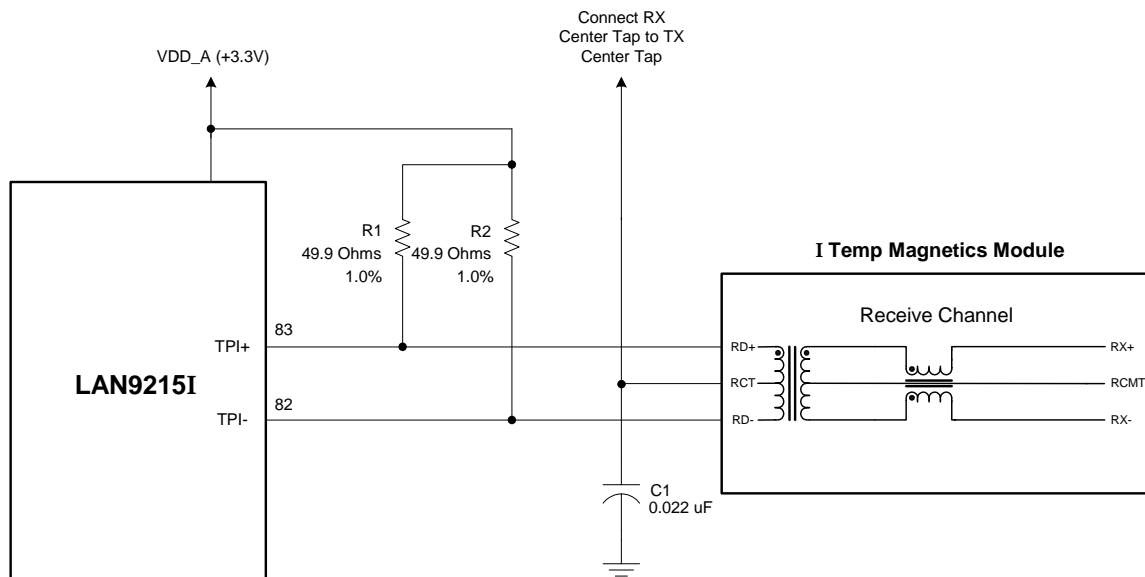RCT   RCMT
RD-   RX-

C1 0.022 uF

Figure 2 - Receive Channel Connections and Terminations

LAN9215I TQFP Magnetics:

1. The center tap connection on the LAN9215I side for the transmit channel must be connected to VDD_A (created from +3.3V) through a 10.0Ω series resistor. This resistor must have a tolerance of 1.0%. The transmit channel center tap of the magnetics also connects to the receive channel center tap of the magnetics.

2. The center tap connection on the LAN9215I side for the receive channel is connected to the transmit channel center tap on the magnetics. In addition, a 0.022 μF capacitor is required from the receive channel center tap of the magnetics to digital ground.

3. The center tap connection on the cable side (RJ45 side) for the transmit channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

4. The center tap connection on the cable side (RJ45 side) for the receive channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

5. Only one 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground is required. It is shared by both TX & RX center taps.

6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to TPO+ (pin 79) of the LAN9215I TQFP.

7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to TPO- (pin 78) of the LAN9215I TQFP.

8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to TPI+ (pin 83) of the LAN9215I TQFP.

9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to TPI- (pin 82) of the LAN9215I TQFP.

10. When using the SMSC LAN921x Family of parts in the HP Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required. Please refer to the SMSC Applications Note 8.13 "Suggested Magnetics" for proper magnetics.

11. In order to guarantee IEEE compliancy over the entire temperature range of operation, the magnetics used in conjunction with the LAN9215I must be rated for Industrial Temperature use.

RJ45 Connector:

1. Pins 4 & 5 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 4 & 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

2. Pins 7 & 8 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 7 & 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

3. The RJ45 shield should be attached directly to chassis ground.

Power Supply Connections:

1. The digital supply (VDD_IO) pins on the LAN9215I TQFP are 20, 28, 35, 42, 48, 55, 61 & 97. They require a connection to +3.3V.

2. Each power pin should have one .01 μF (or smaller) capacitor to decouple the LAN9215I. The capacitor size should be SMD_0603 or smaller.

3. The analog supply (VDD_A) pins on the LAN9215I TQFP are 81, 85 & 89. They require a connection to +3.3V through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

4. Each VDD_A pin should have one .01 μF (or smaller) capacitor to decouple the LAN9215I. The capacitor size should be SMD_0603 or smaller.

5. Pin 2 (VREG_3.3) is a supply voltage for the two separate internal +1.8V regulators. This pin must be connected to +3.3V.

6. The VREG_3.3 pin should have one .01 μF (or smaller) capacitor to decouple the LAN9215I. The capacitor size should be SMD_0603 or smaller.

7. VDD_REF (pin 8), this pin serves as the voltage supply for the internal PLL of the LAN9215I. This pin must always be at the same potential as the VDD_IO (+3.3V) power supply pins.

8. The VDD_REF pin should have one .01 μF (or smaller) capacitor to decouple the LAN9215I. The capacitor size should be SMD_0603 or smaller.

Ground Connections:

1. The digital ground pins (GND_IO) on the LAN9215I TQFP are 19, 27, 34, 41, 47, 54, 60 & 96. They need to be connected directly to a solid, contiguous ground plane.

2. The analog ground pins (VSS_A) on the LAN9215I TQFP are 77, 80, 86 & 88. They also need to be connected directly to the same solid, contiguous ground plane.

3. We recommend that the Digital Ground pins and the AVSS pins be tied together to the same ground plane. We do not recommend running separate ground planes for any of our LAN products.

4. There are two core grounds on the LAN9215I. These grounds are pins 1 & 66 (GND_CORE). They also need to be connected to the same solid, contiguous ground plane as above.

5. There is one PLL ground on the LAN9215I. This ground is pin 4 (VSS_PLL). Again, this pin must be connected to the same digital ground plane as above.

Voltage Reference Inputs:

1. ATEST (pin 9), this pin serves as a plus voltage reference input to the LAN9215I. This pin must always be at the same potential as the VDD_REF pin (pin 8,+3.3V).

Ground Reference Inputs:

1. VSS_REF (pin 11), this pin serves as a ground reference for the internal PLL (in conjunction with the VDD_REF pin). This pin must be connected directly the digital ground plane.

VDD_CORE_1.8V:

1. VDD_CORE (pins 3 & 65), these two pins are used to provide bypassing for the +1.8V core regulator. Each pin requires a 0.01 μF decoupling capacitor. Each capacitor should be located as close as possible to its pin without using vias. In addition, pin 3 requires a bulk capacitor placed as close as possible to pin 3. The bulk capacitor must have a value of at least 10 μF, and have an ESR (equivalent series resistance) of no more than 2.0 Ω. SMSC recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended.

Caution: Even though both are +1.8V levels, **Do Not Connect** VDD_CORE_1.8V to VDD_PLL_1.8V.

Caution: This +1.8V supply is for internal logic only. **Do Not** power other circuits or devices with this supply.

VDD_PLL_1.8V:

1. VDD_PLL (pin 7), this pin is used to provide an external supply decoupling capacitor to the internal +1.8V PLL regulator. A 0.01 μF decoupling capacitor must be attached to this pin. The capacitor should be located as close as possible to pin 7, and must be attached without using vias. In addition, a bulk capacitor must also be attached to this pin. The bulk capacitor must have a value of at least 10 μF, and must have a very low ESR (equivalent series resistance) of less than 2.0 Ω. SMSC recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended.

Caution: Even though both are +1.8V levels, **Do Not Connect** VDD_PLL_1.8V to VDD_CORE_1.8V.

Caution: This +1.8V supply is for internal logic only. **Do Not** power other circuits or devices with this supply.
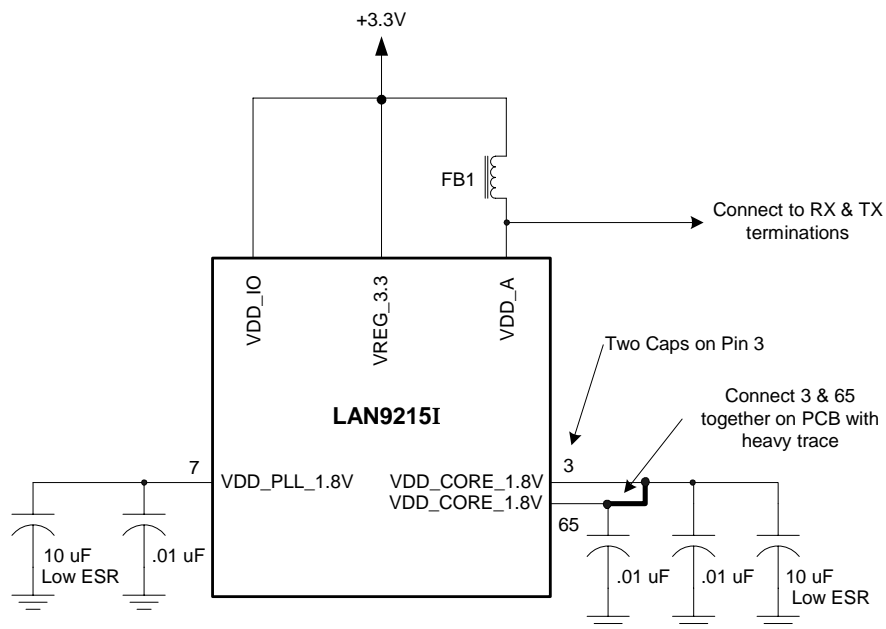

Figure 3 - LAN9215I Power Connections

Crystal Connections:

1. A 25.000 MHz crystal must be used with the LAN9215I TQFP. For exact specifications and tolerances refer to the latest revision LAN9215I data sheet.

2. XTAL1 (pin 6) on the LAN9215I TQFP is the clock circuit input. This pin requires a 15 – 33 ρF capacitor to digital ground. One side of the crystal connects to this pin.

3. XTAL2 (pin 5) on the LAN9215I TQFP is the clock circuit output. We recommend placing a 0Ω resistor in series with this pin to the crystal for future EMI considerations. The other side of the resistor can then connect to a matching 15 – 33 ρF capacitor to ground and the other side of the crystal.

4. Since every system design is unique, the value for the series resistor and the capacitor values are system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

5. For proper operation, an additional 1.0M Ω resistor needs to be added to the crystal circuit. This resistor needs to be placed in parallel with the crystal.

6. In order to guarantee IEEE compliancy over the entire temperature range of operation, the crystal used in conjunction with the LAN9215I must be rated for Industrial Temperature use.

EEPROM Interface:

1. EECS (pin 68) on the LAN9215I TQFP connects to the external EEPROM's CS pin.

2. EECLK (pin 69) on the LAN9215I TQFP connects to the external EEPROM's serial clock pin.

   Caution: To ensure normal device operation, the EECLK pin must be high during any power-up and/or hardware reset event. Do not add any type of external pull-down or grounding connection to this pin as this will result in configuring the device disabled.

3. EEDIO (pin 67) on the LAN9215I TQFP connects to the external EEPROM's Data In pin. This pin on the LAN9215I is a bi-directional pin and it also connects to the EEPROM's Data Out pin through a 1.0K Ω resistor.

4. Be sure to select a 3-wire style 1K EEPROM that is organized for 128 x 8-bit or the ability to be strapped for 128 x 8-bit operation. Recommended EEPROMs can be found in our LAN9118 Designing with the LAN9118 - Getting Started design guide, application note AN 12.5.

RBIAS Resistor:

1. RBIAS (pin 10) on the LAN9215I TQFP should connect to digital ground through a 12.0K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the internal PLL of the LAN9215I.

EXRES1 Resistor:

1. EXRES1 (pin 87) on the LAN9215I TQFP should connect to digital ground through a 12.4K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded 10/100 Ethernet Physical device.

MII Interface:

1. When utilizing either an external MII Phy or an MII Connector, the following table indicates the proper connections for the 17 signals.

From:	Connects To:	
LAN9215I TQFP	MII Physical Device	MII Connector
RXD0 (pin 75)	RXD<0>	RXD<0> (contact 7)
RXD1 (pin 22)	RXD<1>	RXD<1> (contact 6)
RXD2 (pin 23)	RXD<2>	RXD<2> (contact 5)
RXD3 (pin 24)	RXD<3>	RXD<3> (contact 4)
RX_DV (pin 29)	RX_DV	RX_DV (contact 8)
RX_ER (pin 25)	RX_ER	RX_ER (contact 10)
RX_CLK (pin 26)	RX_CLK	RX_CLK (contact 9)
TXD0 (pin 39)	TXD<0>	TXD<0> (contact 14)
TXD1 (pin 38)	TXD<1>	TXD<1> (contact 15)
TXD2 (pin 37)	TXD<2>	TXD<2> (contact 16)
TXD3 (pin 36)	TXD<3>	TXD<3> (contact 17)
TX_EN (pin 21)	TX_EN	TX_EN (contact 13)
TX_CLK (pin 40)	TX_CLK	TX_CLK (contact 12)
CRS (pin 32)	CRS	CRS (contact 19)
COL (pin 33)	COL	COL (contact 18)
MDIO (pin 30)	MDIO	MDIO (contact 2)
MDC (pin 31)	MDC	MDC (contact 3)

2. If the MII interface is not used by the system, do not terminate on the board level. These pins have the proper internal terminations and should be left as no-connects.

Required External Pull-ups/Pull-downs:

1. IRQ (pin 72) may require an external pull-up resistor if this output is programmed as an Open Drain type.

2. PME (pin 70) may require an external pull-up resistor if this output is programmed as an Open Drain type.

3. GPIO0/nLED1 (pin 98) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed for LED functionality, this pin indicates what speed (10/100) the Ethernet phy is currently set for. A pull-up resistor would also be required if this pin is programmed as an Open Drain Output.

4. GPIO1/nLED2 (pin 99) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed for LED functionality, this pin indicates Link & Activity status of the Ethernet phy. A pull-up resistor would also be required if this pin is programmed as an Open Drain Output.

5. GPIO2/nLED3 (pin 100) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed for LED functionality, this pin indicates what duplex mode (half/full) the Ethernet phy is currently set for. A pull-up resistor would also be required if this pin is programmed as an Open Drain Output.

6. When using the MII interface of the LAN9215I TQFP with an external Physical device on board, a pull-up resistor on the signal MDIO must be incorporated. A pull-up resistor of 1.5KΩ to +5V is required for this application. If the LAN9215I TQFP is used with the industry standard MII connector, the 1.5KΩ is not required as this pull-up will be on the plug-in MII PCB.

7. RXD0 (pin 75) must be pulled or driven to a valid state at all times. An external 10KΩ pull-down resistor is required on this pin.

CPU Interface:

1. A1 – A7 Address Bus: Please refer to the latest revision of the LAN9215I Application Note for exact implementation of the CPU interface selected.

2. D0 – D15 Data Bus: Please refer to the latest revision of the LAN9215I Application Note for exact implementation of the CPU interface selected.

3. Control Signals: Please refer to the latest revision of the LAN9215I Application Note for exact implementation of the CPU interface selected.

4. The LAN9215I is a Little Endian LAN device. It is the designers' responsibility to ensure that the selected CPU has compatible Endianess, as this may affect Data Bus connections to the LAN9215I. For example, if a Big Endian processor is used in conjunction with the LAN9215I, it may be necessary to swap data bus byte lanes in order to ensure proper system operation. Please refer to the latest LAN9215I data sheet and design guides to determine compatibility.

Miscellaneous:

1. There are four No-Connect pins on the LAN9215I. It is very important that these pins remain as no-connects. These pins are 71, 84, 90 & 91.

2. EEDIO (pin 67), 16-bit operation is hardwired into the LAN9215I device. No external means are necessary to enable 16-bit operation.

    However, to maintain backwards compatibility with the LAN9218I device, the designer may consider including the following pull-up/pull-down options to select 32-bit/16-bit operation. In addition to this pin's function as the bi-directional data path for the EEPROM, this pin has a secondary function during reset. Upon the deassertion of reset, this pin selects the Data Bus Width depending upon what state it is in. This pin cannot be left as a no-connect in the LAN9218I device.

    When this pin is high, 32-bit data bus width operation is selected. For 32-bit operation, this pin must be pulled high with an external 10.0K Ω pull-up resistor.

    When this pin is low, 16-bit data bus width operation is selected. A 10.0KΩ pull-down resistor should be used to select this mode.

3. SPEED_SEL (pin 74), upon deassertion of reset, the Default Ethernet Settings are established.

    If this pin is high, the LAN9215I will default to 100BASE-TX, Half Duplex mode with Auto Negotiation enabled. This pin has a weak internal pull-up resistor, so, for this mode, this pin can be left as a no-connect.

    With this pin low, the default setting will be 10BASE-T, Half Duplex with Auto Negotiation disabled. A 1.0K Ω pull-down resistor should be used for this purpose.

4. FIFO_SEL (pin 76), when driven high, all accesses to the LAN9215I are to the RX or TX Data FIFOs. In this mode, the address input is ignored. Typical use will involve connecting an upper address line (A11 is recommended) to this pin to determine functionality. For normal operation (FIFO_SEL disabled), a 1.0K Ω external pull-down resistor must be attached to this pin.

5. MDIO / External Phy Detect (pin 30), this pin is used as a strap to indicate the presence of an external phy. The level of this pin is latched upon power-up or hard reset. This pin has no effect on the internal logic of the LAN9215I. It is only intended to provide a mechanism to the system designer to inform the software application that an external phy is present. The MII functionality (enable & disable) is completely register based. See the LAN9215I Data Sheet, HW_CFG – Hardware Configuration Register, Bit 3 for specific details.

6. nRESET (pin 95), this pin is an active-low reset input. This signal resets all logic and registers within the LAN9215I. This signal is pulled high with a weak internal pull-up resistor. If nRESET is left unconnected the LAN9215I will rely on its internal power-on reset circuitry.

7. AMDIX_EN (pin 73), this pin enables the HP Auto MDIX feature of the LAN9215I. To take advantage of the Auto MDIX feature (Auto MDIX enabled), a 1.0K Ω external pull-up resistor must be attached to this pin. This pin has a weak internal pull-down, so this pin can be left as a no-connection in order to disable the Auto MDIX feature (default mode of operation).

8. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.

9. Be sure to incorporate enough bulk capacitors (4.7 - 22μF caps) for each power plane.

10. In order to guarantee IEEE compliancy over the entire temperature range of operation, all components used in the customer's application must be rated for Industrial Temperature use. Processors, crystals, oscillators, magnetics and all integrated circuits must be rated properly to avoid operational inconsistencies.

LAN9215I TQFP QuickCheck Pinout Table:

Use the following table to check the LAN9215I TQFP shape in your schematic.

| table |
| LAN9215I TQFP |

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	GND_CORE	26	RX_CLK	51	D9	76	FIFO_SEL
2	VREG	27	GND_IO	52	D8	77	VSS_A
3	VDD_CORE	28	VDD_IO	53	D7	78	TPO-
4	VSS_PLL	29	RX_DV	54	GND_IO	79	TPO+
5	XTAL2	30	MDIO	55	VDD_IO	80	VSS_A
6	XTAL1	31	MDC	56	D6	81	VDD_A
7	VDD_PLL	32	CRS	57	D5	82	TPI-
8	VDD_REF	33	COL	58	D4	83	TPI+
9	ATEST	34	GND_IO	59	D3	84	NC
10	RBIAS	35	VDD_IO	60	GND_IO	85	VDD_A
11	VSS_REF	36	TXD3	61	VDD_IO	86	VSS_A
12	A7	37	TXD2	62	D2	87	EXRES1
13	A6	38	TXD1	63	D1	88	VSS_A
14	A5	39	TXD0	64	D0	89	VDD_A
15	A4	40	TX_CLK	65	VDD_CORE	90	NC
16	A3	41	GND_IO	66	GND_CORE	91	NC
17	A2	42	VDD_IO	67	EEDIO	92	nRD
18	A1	43	D15	68	EECS	93	nWR
19	GND_IO	44	D14	69	EECLK	94	nCS
20	VDD_IO	45	D13	70	PME	95	nRESET
21	TX_EN	46	D12	71	NC	96	GND_IO
22	RXD1	47	GND_IO	72	IRQ	97	VDD_IO
23	RXD2	48	VDD_IO	73	AMDIX_EN	98	nLED1
24	RXD3	49	D11	74	SPEED_SEL	99	nLED2
25	RX_ER	50	D10	75	RXD0	100	nLED3

Notes:

Reference Material:

1. SMSC LAN9215I Data Sheet; check web site for latest revision.

2. SMSC LAN9215I EVB Schematic, Assembly No. xxxx ; check web site for latest revision.

3. SMSC LAN9215I EVB PCB, Assembly No. xxxx ; order PCB from web site.

4. SMSC LAN9215I EVB PCB Bill of Materials, Assembly No. xxxx ; check web site for latest revision.

5. SMSC LAN9118 Design Guide, Designing with the LAN9118I – Getting Started, Application Note AN 12.5; check web site for latest revision.

6. SMSC LAN9118 Programmers Reference Guide, Application Note AN 12.12; check web site for latest revision.

7. Migrating from the LAN9118 to the LAN9218I, Application Note AN 14.10; check web site for latest revision.

8. SMSC Suggested Magnetics Application Note 8-13; check web site for latest revision.