


LAN9218 Reference Schematic

Schematic Revision 1.0

ITEM	Page
Title Page	1
LAN9218 Reference Schematic	2

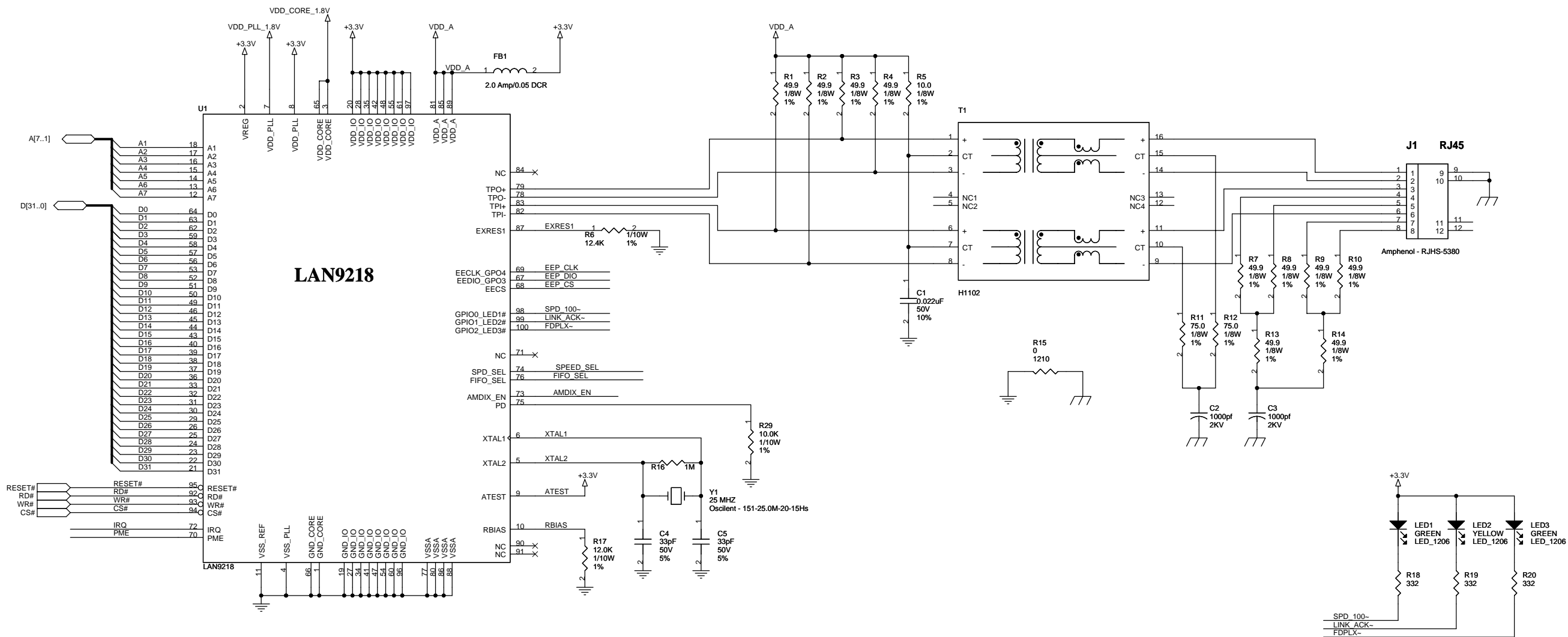
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Title

LAN9218 Reference Schematic

Size	Engineer	Assembly No.	Rev
C	N/A	N/A	1.0
Date: Tuesday, July 10, 2007		Sheet 1 of 2	



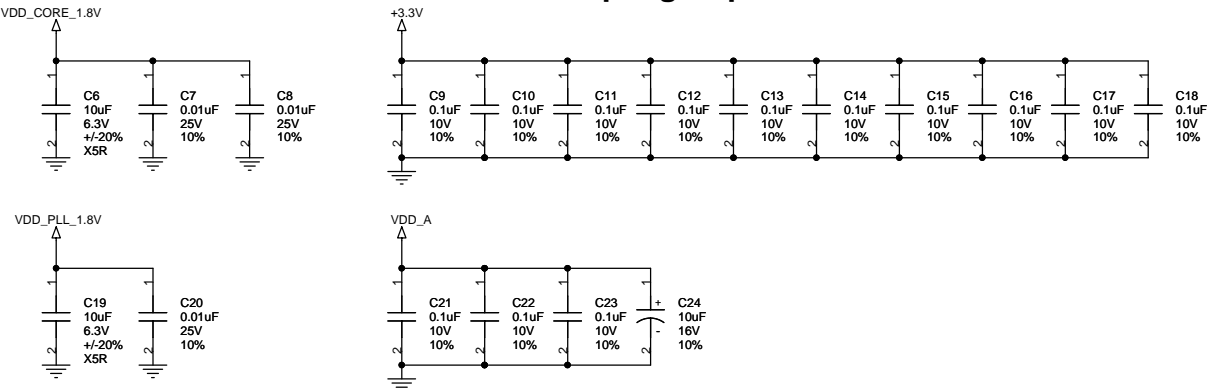
LAN9218

NOTE:
FIFO_SEL can be driven dynamically and is not pulled internally to either state. This pin has the same timing as the Address Bus and can be driven by upper address bits not used by the LAN9218. Refer to datasheet.

NOTE:
IN = Auto-MDIX Functionality Enabled
OUT = Auto-MDIX Functionality Disabled

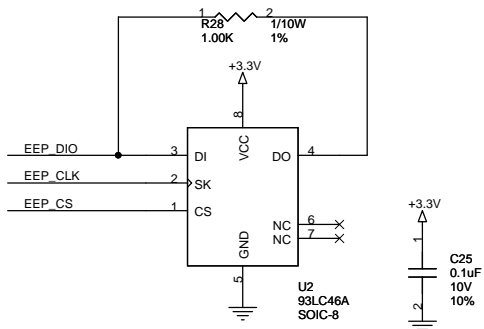
NOTE:
EE_DIO is the D32/D16# Strap
1 - 2 = 32 Bit Mode
2 - 3 = 16 Bit Mode

LAN9218 Decoupling Capacitors



NOTE:
C6 and C19 must be low ESR capacitors. Ceramic is recommended.

MAC EEPROM (Optional)



NOTE:
IN = 10Mbps, Half-Duplex, Auto Neg. Disabled
OUT = 100Mbps, Half-Duplex, Auto Neg. Enabled



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C	N/A	N/A	1.0
Date: Tuesday, July 10, 2007		Sheet 2 of 2	