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DOCUMENT DESCRIPTION

Routing Checklist for the LAN9215, 100-pin TQFP Package

SMSC®
SUCCESS BY DESIGN

SMSC
80 Arkay Drive
Hauppauge, New York 11788

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Routing Checklist for LAN9215

Information Particular for the 100-pin TQFP Package

LAN9215 TQFP Phy Interface:

1. The traces connecting the transmit outputs (TPO+, pin 79) & (TPO-, pin 78) to the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.

2. The traces connecting the receive inputs (TPI+, pin 83) & (TPI-, pin 82) from the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.

3. For differential traces running from the LAN controller to the magnetics, SMSC recommends routing these traces on the component side of the PCB with a contiguous digital ground plane on the next layer. This will minimize the use of vias and avoid impedance mismatches by switching PCB layers.

4. The VDD_A power supply should be routed as a mini-plane and can be routed on an internal power plane layer.

5. The union of the 10.0Ω resistor supplying VDD_A to the Transmit & Receive Channel center taps of the magnetics and the 0.022 µF capacitor, should be routed as a mini-plane.

LAN9215 TQFP Magnetics:

1. The traces connecting the transmit outputs from the magnetics to pins 1 & 2 on the RJ45 connector must be run as differential pairs. Again, the differential impedance should be 100 ohms.

2. The traces connecting the receive inputs on the magnetics from pins 3 & 6 on the RJ45 connector must be run as differential pairs. Again, the differential impedance should be 100 ohms.

3. For differential traces running from the magnetics to the RJ45 connector, SMSC recommends routing these traces on the component side of the PCB with all power planes (including chassis ground) cleared out from under these traces. This will minimize the use of vias and minimize any unwanted noise from coupling into the differential pairs. The plane clear out boundary is usually halfway through the magnetics.

RJ45 Connector:

1. Try to keep all other signals out of the Ethernet front end (RJ45 through the magnetics to the LAN chip). Any noise from other traces may couple into the Ethernet section and cause EMC problems.

2. Also recommended, is the construction of a separate chassis ground that can be easily connected to digital ground at one point. This plane provides the lowest impedance path to earth ground.

Power Supply Connections:

1. Route the (8) VDD_IO pins of the LAN9215 TQFP directly into a solid, +3.3V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.

2. In addition, route the (8) VDD_IO decoupling capacitors for the LAN9215 TQFP power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for each cap.

3. Route the (3) VDD_A pins of the LAN9215 TQFP directly into a solid, +3.3V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.

4. In addition, route the (3) VDD_A decoupling capacitors for the LAN9215 TQFP power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for each cap.

5. Route the (1) VREG_3.3 pin of the LAN9215 TQFP directly into a solid, +3.3V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.

6. In addition, route the (1) VREG_3.3 decoupling capacitor for the LAN9215 power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for the cap.

7. Route the (1) VDD_REF pin of the LAN9215 TQFP directly into a solid, +3.3V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.

8. In addition, route the (1) VDD_REF decoupling capacitor for the LAN9215 TQFP power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for the cap.

Ground Connections:

1. The (8) digital ground pins (GND_IO) on the LAN9215 TQFP should be routed directly into a solid, contiguous, internal ground plane. The pin-to-plane trace should be as short and as wide as possible.

2. The (4) analog ground pins (VSS_A) on the LAN9215 TQFP should be routed directly into the same solid, contiguous, internal ground plane. The pin-to-plane trace should be as short and as wide as possible.

3. We recommend that the Digital Ground pins (GND_IO) and the VSS_A pins be tied together to the same ground plane. We do not recommend running separate ground planes for any of our LAN products.

4. The (2) core ground pins (GND_CORE) on the LAN9215 TQFP should be routed directly into the same solid, contiguous, internal ground plane. The pin-to-plane trace should be as short and as wide as possible.

5. The (1) VSS_PLL ground connection on the LAN9215 TQFP should be routed directly into a solid, contiguous, internal ground plane. The pin-to-plane trace should be as short and as wide as possible. Again, these pins must be connected to the same digital ground plane as above.

Voltage Reference Inputs:

1. Route the (1) ATEST pin of the LAN9215 directly into a solid, +3.3V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.

Ground Reference Inputs:

1. Route the (1) VSS_REF pin of the LAN9215 directly into a solid, contiguous, internal ground plane. The pin-to-plane trace should be as short as possible and as wide as possible. Again, this pin must be connected to the same digital ground plane as above.

VDD_CORE_1.8V:

1. The VDD_CORE_+1.8V pin 65 must be routed with a heavy, wide trace with multiple vias to the single decoupling cap associated with it.

2. The VDD_CORE_+1.8V pin 3 must be routed with a heavy, wide trace with multiple vias to the single decoupling cap and the single bulk capacitor associated with it.

3. The two VDD_CORE_+1.8V pins 3 & 65 must then be connected together with a short, heavy, wide trace on the PCB. Be sure to use multiple vias as necessary.

VDD_PLL_1.8V:

1. The VDD_PLL_+1.8V pin 7 must be routed with a heavy, wide trace with multiple vias to the single decoupling cap and the single bulk capacitor associated with it.

2. **Do Not**, under any circumstances, connect VDD_CORE_+1.8V to VDD_PLL_+1.8V. Even though they are both +1.8V potentials, they must remain separate, as they are two independent, internal voltage regulators of the LAN9215.

3. **Do Not**, under any circumstances, use either VDD_CORE_+1.8V or VDD_PLL_+1.8V to supply other circuits or devices. These two separate, internal voltage regulators are designed to supply internal logic of the LAN9215 only.

Crystal Connections:

1. The routing for the crystal or clock circuitry should be kept as small as possible and as short as possible.

2. A small ground flood routed under the crystal package on the component layer of PCB may improve the emissions signature. Stitch the flood with multiple vias into the digital ground plane directly below it.

EEPROM Interface:

1. There are no critical routing instructions for the EEPROM interface. Since it is a relatively slow interface, normal board routing measures should suffice.

RBIAS Resistor:

1. The RBIAS resistor (pin 10) should be routed with a short, wide trace. Any noise induced onto this trace may cause system failures. Do not run any traces under the RBIAS resistor.

EXRES1 Resistor:

1. The EXRES1 resistor (pin 87) should be routed with a short, wide trace. Any noise induced onto this trace may cause system failures. Do not run any traces under the EXRES1 resistor.

MII Interface:

1. The MII interface on the LAN9215 should be constructed using 68-ohm traces.

Required External Pull-ups/Pull-downs:

1. There are no critical routing instructions for the Required External Pull-ups/Pull-down connections.

CPU Interface

1. Good, general design practices should be adhered to ensure proper operation.

2. Follow recommended processor design guidelines to ensure proper operation.

3. Follow recommended interpair spacing guidelines within data bus byte lanes, address bus and control group signals.

4. Follow recommended intrapair spacing guidelines between data bus byte lanes, address bus and control group signals.

5. As with any high-speed design interface, it is the design engineer’s responsibility to review the PCB routing for specification adherence. The design engineer should review all timing relationships as put forth in the selected processor’s data sheet and the LAN9215 TQFP data sheet and make certain that any PCB routing does not add significant timing delays. These timing relationships can be found in the Host Bus System Timing section of the LAN9215 TQFP data sheet.

Miscellaneous:

1. SMSC recommends utilizing at least a four-layer design for boards for the LAN9215 TQFP device. The design engineer should be aware, however, as tighter EMC standards are applied to his product and as faster signal rates are utilized by his design, the product design may benefit by utilizing up to eight layers for the PCB construction.

2. As with any high-speed design, the use of series resistors and AC terminations is very application dependant. Buffer impedances should be anticipated and series resistors added to ensure that the board impedance matches the driver. Any critical clock lines should be evaluated for the need for AC terminations. Prototype validation will confirm the optimum value for any series and/or AC terminations.

3. Bulk capacitors for each power plane should be routed immediately into power planes with traces as short as possible and as wide as possible.

4. Following these guidelines and other general design rules in PCB construction should ensure a clean operating system.

5. Trace impedance depends upon many variables (PCB construction, trace width, trace spacing, etc.). The electrical engineer needs to work with the PCB designer to determine all these variables.