CIRRUS LOGIC

PRELIMINARY DATA SHEET
July, 1988

FEATURES

- Hardware implementation of VGA, EGA, CGA, MDA and Hercules® HGC
- Fast host access to video memory
- 32-bit video memory RAM access
- Automatic mode switching in hardware
- 800 x 600 resolution
- Scan line doubling
- 256 Kbytes memory configuration
- Up to 40 MHz dot clock
- Hardware support for both Hercules graphics and text modes on IBM PS/2 color or monochrome monitors, using 70 Hz vertical scan for flicker-free display
- 4 pages of memory in 256-color mode (13H)
- S/LA™ Design Technology
- Advanced double metal CMOS technology

CL – GD 510A/520A

Enhanced VGA Compatible Graphics Chip Set

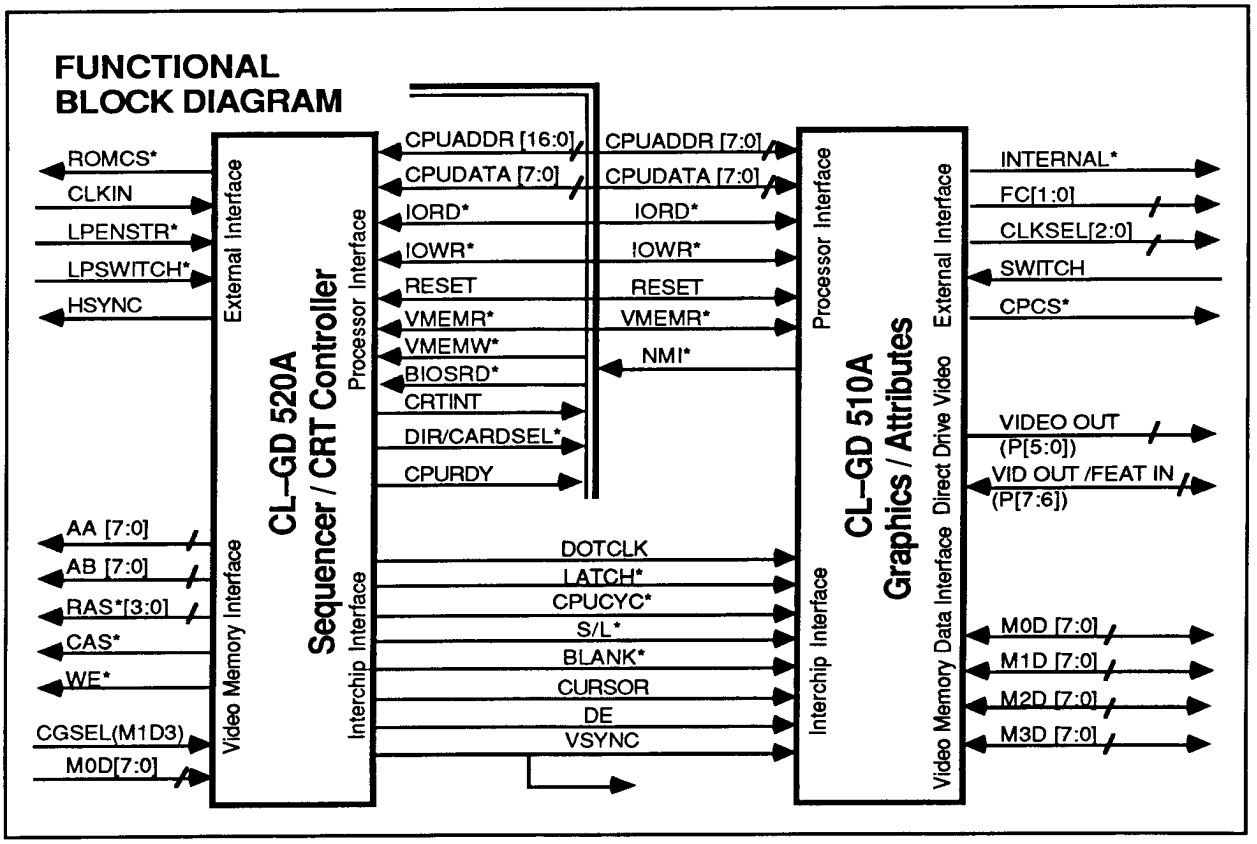
OVERVIEW

The CL-GD510A Graphics/Attributes chip and the CL-GD520A Sequencer/CRT Controller chip are hardware- compatible with the IBM® VGA, EGA, CGA, and MDA standards, as well as with the Hercules® HGC, and provide improved performance and additional functionality.

Operating at dot clock rates up to 40 MHz, the CL-GD510A/520A chip set supports high resolution graphics and alphanumeric display modes for both monochrome and color, and for high resolution variable frequency and PS/2 monitors. Video outputs are provided in 4 bits per pixel (all resolutions) and 8 bits per pixel (320 x 200). Using analog video output and an external palette, selection may be made from 256K colors.

(cont'd on next page)

FUNCTIONAL BLOCK DIAGRAM



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OVERVIEW (cont'd)

The CL-GD510A/520A implements all control and data registers in the current graphics standards, including those of the 6845 CRT Controller. The chip set also implements all data manipulation capabilities and data paths, providing complete hardware and software compatibility.

The sequencer design provides more video memory cycles for the CPU during the normal video refresh/display cycle. Memory cycles not used to refresh the display or video memory can be allocated to process CPU memory requests.

The hardware supports a mouse/graphics cursor, and a blinking insertion point text cursor. Additional text cursor controls include blink disable and replace/invert mode control. The hardware supports simultaneous and independent smooth scrolling of two separate text screens.

The CL-GD510A/520A is designed for minimum external circuitry support and is ideal for integrated systems. Support circuitry may include bus buffers, timing sources, memory/port address block decoders, and video drivers.

ADVANTAGES

Unique Features	Benefits
• Hardware compatibility with VGA, EGA, CGA, MDA, and HGC standards.	True backward compatibility for installed software base.
• Automatic Mode Switching in hardware.	Allows user to switch video modes without running an emulation program.
• Improved sequencer design for fast host access to video memory.	Applications run faster without modification.
• Makes use of full capabilities of variable frequency monitors.	Up to 800 x 600 lines allows thirty percent more information displayed with popular software (e.g. Microsoft® Windows®).
• Light pen support in VGA modes	IBM VGA does not support light pen.
• Enhanced split screen capability	Simplifies driver software while improving performance.
• Hardware graphics cursor	Dramatically reduces software overhead for mouse pointer. Graphics applications and environments (e.g. Microsoft® Windows® and DRI™ GEM™) run faster.
• Hardware insertion point caret	Allows cursor emulation when text is used in Graphics modes.
• Non intrusive software ID of devices	Simplifies installation of device-specific drivers and applications.
• 4 pages of memory for mode 13h (320 x 200 resolution mode)	Permits 256 color images to be switched rapidly to produce color animation.
• All control registers have read-back	Eliminates need for shadow registers, and allows graphics controller state-save for multi-tasking applications.

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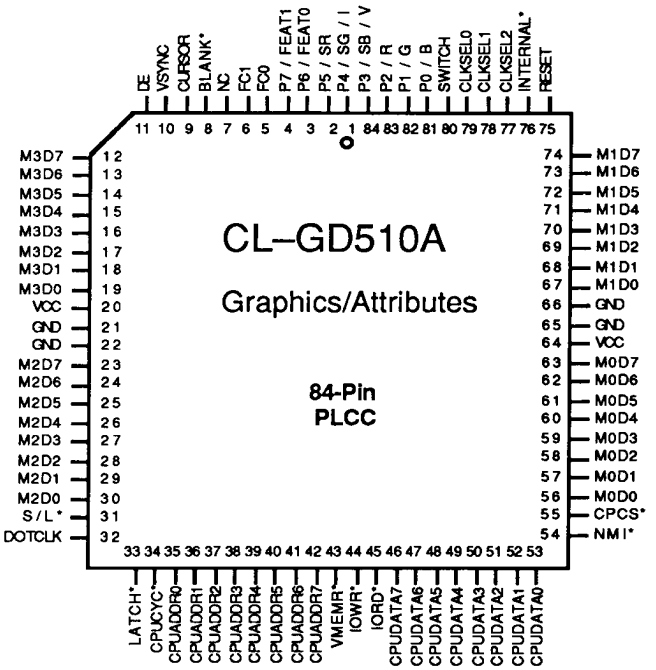
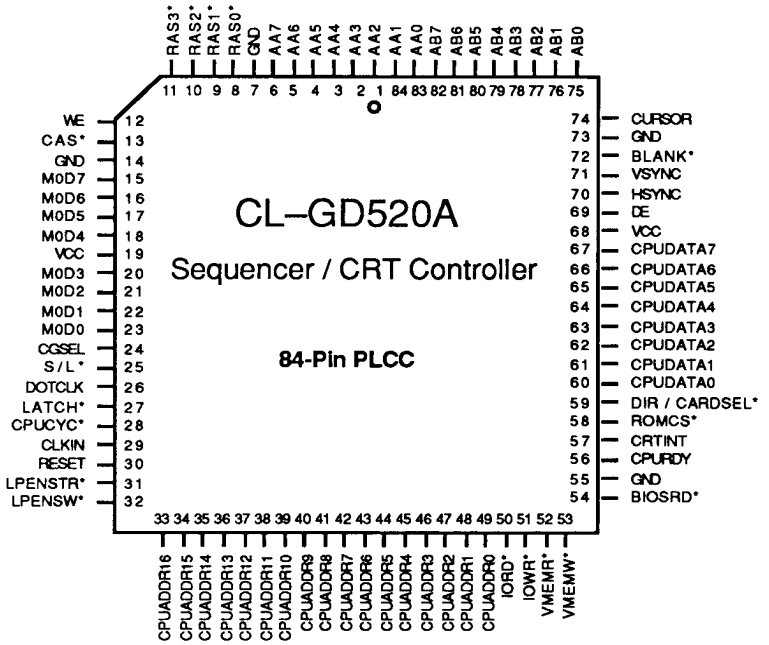
1. PIN INFORMATION

1.1 Pin Diagram





(*) Denotes negative true signal

1.2 Pin Assignment Table

NAME	GD510A PIN NO.	GD520A PIN NO.	TYPE	FUNCTION
PROCESSOR INTERFACE				
BIOSRD*		54	I	BIOS Read Strobe
VMEMR*,VMEMW*	43	52,53	I	CPU read/write of video memory
IORD*,IOWR*	44,45	50,51	I	I/O R/W Strobes
CPUDATA [7:0]	46-53	60,67	I/O	Bidirectional data to/from host CPU
CPUADDR [16:0]	35-42	33-49	I	17 low order CPU bus address bits
NMI*	54		O	Non Maskable Interrupt request
RESET	75	30	I	System Reset
CPURDY		56	O	Data available signal for wait-state logic
CRTINT		57	O	Display retrace interrupt
DIR / CARDSEL*		59	O	Bidirectional CPU data bus transceiver control (also used as PC/XT slot-8 control)
VIDEO MEMORY DATA INTERFACE				
M0D[7:0]	56-63	15-18, 20-23	I/O	Byte wide bidirectional data bus to Plane 0
M1D[7:0]	67-74		I/O	Byte wide bidirectional data bus to Plane 1
M2D[7:0]	23-30		I/O	Byte wide bidirectional data bus to Plane 2
M3D[7:0]	12-19		I/O	Byte wide bidirectional data bus to Plane 3
VIDEO MEMORY ADDRESS INTERFACE				
AA[7:0]		1-6,83,84	O	Address bus to byte planes 0 and 1
AB[7:0]		75-82	O	Address bus to byte planes 2 and 3
RAS[3:0]*		8-11	O	Row address strobe to planes 3-0
CAS*		13	O	Column address strobe to all planes
WE*		12	O	Video memory write enable
EXTERNAL INTERFACE				
ROMCS*		58	O	BIOS ROM chip select
CPCS*	55		O	Color Palette chip select
CLKSEL [2:0]	77-79		O	Programmable clock/switch mux control
SWITCH	80		I	Input from external switch select mux
CLKIN		29	I	Input from external clock select mux
LPENSTR*		31	I	CPU readable, can latch display addr to lightpen reg
LPENSW*		32	I	CPU readable, usually connected to lightpen switch
INTERNAL*	76		O	Selects internal vs. external video drivers
FC [1:0]	5,6		O	Programmable, normally drive feature connectors
HSYNC		70	O	Horizontal Sync output

GD510A / 520 INTERCONNECT				
DOTCLK	32	26	GD520A to GD510A	Video clock (40 MHz max)
LATCH*	33	27	GD520A to GD510A	Latches video RAM data on CPU or CRT reads
CPUCYC*	34	28	GD520A to GD510A	Indicates CPU read/write cycle to display memory
S/L*	31	25	GD520A to GD510A	Syncs loading shift registers with CRTC char clock
VSYNC	10	71	GD520A to GD510A	Vertical Sync signal
BLANK*	8	72	GD520A to GD510A	Video blanking signal
CURSOR	9	74	GD520A to GD510A	Cursor valid signal
DE	11	69	GD520A to GD510A	Display enable
CGSEL (Attr bit 3, M1D3)		24	DRAM to GD520A	Selects alpha map

VIDEO INTERFACE					Analog	ECD	CD	MD
P7/FEAT1	4		I/O	Pixel Data MSB / Feature Bit 1	P7			
P6/FEAT0	3		I/O	Pixel Data 6 / Feature Bit 0	P6			
P5/SR	2		O	Pixel Data 5 / Secondary Red	P5	SR		
P4/SG/I	1		O	Pixel Data 4 / Secondary Green / Intensity	P4	SG	I	I
P3/SB/V	84		O	Pixel Data 3 / Secondary Blue / Video	P3	SB		V
P2/R	83		O	Pixel Data 2 / Primary Red	P2	R	R	
P1/G	82		O	Pixel Data 1 / Primary Green	P1	G	G	
P0/B	81		O	Pixel Data LSB / Primary Blue	P0	B	B	

2. DETAILED SIGNAL DESCRIPTION

2.1 Processor Interface

NAME	GD510A	GD520A	DESCRIPTION
CPUADDR [16:0]	INPUT	INPUT	The GD520A utilizes the lower 16 of 17 address lines to direct video memory accesses to the proper location within the selected 64KByte bank. The last bit (CPUADDR-16) is used to decode between address AxxxxH and BxxxxH. The GD510A is only connected to CPUADDR bits 0 - 7 in order to qualify the least significant 8 bits of an I/O address. (I/O address MSBs must be decoded and ANDed externally with -IOR or -IOW to fully decode the I/O addressing to the chip). I/O accesses to the GD520A work in an identical manner.
CPUDATA [7:0]	I/O	I/O	Bi-directional flow between the CPU and the chip set for video for video memory and I/O data .
CPURDY		OUTPUT	This signal is inactive (tri-state) when no video memory CPU request is pending. The request may be either VMEMR* or VMEMW*. At the beginning of a CPU access to video memory, CPURDY drops low, putting the CPU in a wait-state. This condition is held until the video memory sequencer fits the memory request into the next available "slot". At completion of the sequencers' CPU memory cycle, CPURDY is driven high for CLKIN period and then returns to the tri-state condition.
CRTINT		OUTPUT	This signal is enabled by clearing Bit 5 of the Vertical Retrace End Register and cleared by resetting Bit 4 of the Vertical Retrace End Register. When enabled, the CRTINT pin will go high at the start of the vertical retrace interval and remain high until cleared by a write of "0"to Bit 4 of the Vertical Retrace End Register (CR11). CRTINT is enabled by: • Clearing bit 5 of CR11 • Setting bit 4 of CR11 If bit 4 is not reset to a "1" after clearing the initial CRTINT , interrupts will cease. The CR11 of the GD520A is also readable. This feature simplifies greatly the task of ORing in the proper value for the remaining bits of the CR11 register (this is not the case for an IBM-EGA or VGA controller).
DIR/CARDSEL*		OUTPUT	Controls the direction of the data flow on the bi-directional CPUDATA bus. Driven low when the CPU is performing an I/O or memory read cycle. This signal can also be used for PC XT slot-8 control.

(*) Denotes negative true signal.

2.1 Processor Interface (cont'd)

NAME	GD510A	GD520A	DESCRIPTION
IORD*, IOWR*	INPUT	INPUT	When low, these signals indicate that an IORD* or IOWR* cycle is taking place within the proper I/O address range. This requires that the required partial decoding of the MSBs of the I/O address range be ANDed with the CPUs' -IOR and -IOW signals to produce IORD* and IOWR* for the GD510A/520A chips.
NMI*	OUTPUT		A low on this signal will cause a non-maskable interrupt to the CPU . The NMI output is enabled by the NMI mask registers NMI 1 and NMI 2 (extension registers A8H and A9H). NMI* returns to the inactive state upon reading the NMI Status Registers (NSTAT 1/2).
RESET	INPUT	INPUT	This input is normally connected to the system reset bus signal and is used as a hardware reset of the GD510A/520A chips. An identical reset state can be accomplished via software by setting SR0-bit 0 low.
VMEMR* VMEMW*	INPUT	INPUT INPUT	Video memory read and write strobes. These inputs are driven low on CPU memory read/write access to video memory,thus, these signals are the result of ANDing the CPU read/write signals with the partial decode of the MSB addresses of the CPU address bus for the AxxxxH or BxxxxH range. The GD510A chip is not connected to VMEMW* signal. It decodes this operation if a valid CPU cycle is in progress, (CPUCYC*=0) and a read is not occurring (VMEMR*=1).

(*) Denotes negative true signal.

2.2 Video Memory Interface

NAME	GD510A	GD520A	DESCRIPTION
AA [7:0]		OUTPUT	Multiplexed video memory address bus A. This bus contains the row/column address information required by the DRAMS in the video memory for 64k memory planes 0 and 1.
AB [7:0]		OUTPUT	Multiplexed video memory address bus B. This bus contains the row/column address information required by the DRAMS in the video memory for 64k memory planes 2 and 3.
CAS*		OUTPUT	Video memory DRAM column address strobe. A low going edge on this signal latches the column address (contained on the AA and AB address busses) into the video memory DRAMs.
CGSEL		INPUT	Enabled by the sequencer character map select register, this bit (normally connected to M1D3 of the attribute memory plane in text mode) can be used to access 1 of 8 secondary character sets (instead of the normal intensity function), to give a total of 512 active display characters from a total of 2048.
M3D [7:0]	I/O		This bi-directional video memory data bus is controlled by the GD510A for read/write operations into video memory Plane 3 which stores graphic data for color plane #3.
M2D [7:0]	I/O		This bi-directional video memory data bus is controlled by the GD510A for read/write operations into video memory Plane 2 which stores graphic data for color plane #2 or character generator font tables in the text modes.
M1D [7:0]	I/O		Bi-directional video memory data bus controlled by GD510A for read/write operations into video memory Plane 1 which stores graphic data for color plane #1 or attribute codes in text modes.
M0D [7:0]	I/O	INPUT	This bi-directional video memory data bus is controlled by the GD510A for read/write operations into video memory Plane 0 which stores graphic data for color plane #0 or attribute codes in the text modes. The GD520A uses these character codes in text mode to produce the proper address on the memeory AB bus to access the character generator fonts.
RAS [3:0]*		OUTPUT	Video memory DRAM row address strobe. A low going edge on this signal latches the row address (contained on the AA and AB address busses) into the video memory DRAMs.
WE*		OUTPUT	When low, this signal enables a video memory write to the bank selected by the appropriate RAS* signal(s). The actual write occurs on the falling edge of CAS*.

(*) Denotes negative true signal.

2.3 Video Interface

The PIXEL DATA bits drive the analog or digital inputs of color or monochrome displays. P0-P5 bits are always "on" if video out is enabled by AR-12 (Attribute register 12) bit-4. P6 and P7 are also enabled by AR-12, bit-4 but are ANDed with the 8-bit Video Enable bit (Extension Index 87, bit 4). P0-P7 pins are described more fully in the following table:

NAME	DESCR.	Analog RAM DAC Interface	ECD 64-Color Digital	CD 16-Color Digital	MD Mono-chrome	GD510A/520A
P7 / FEAT1	Tertiary Red Feature Bit 1†	P7	0	0	0	OUTPUT INPUT
P6 / FEAT0	Tertiary Green Feature Bit 0†	P6	0	0	0	OUTPUT INPUT
P5 / SR	Secondary Red	P5	SR	I	Note	OUTPUT
P4 / SG / I	Secondary Green/ Intensity	P4	SG	I	Note	OUTPUT
P3 / SB / V	Secondary Blue/ Video	P3	SB	I	Note	OUTPUT
P2 / R	Primary Red	P2	R	R	Note	OUTPUT
P1 / G	Primary Green	P1	G	G	Note	OUTPUT
P0 / B	Primary Blue	P0	B	B	Note	OUTPUT

† FEAT1 and FEAT0 (Feature Bits 1 and 0) are programmable as inputs to the FC Register (Feature Control), and can be read at port address 3CA.

Note:
In Monochrome modes, video outputs are driven from GD510A Palette Registers 0, 7, 8, 15 as follows:

Intensity	Video	Palette Register Selected	Mode
0	0	0	Mono Text or HGC Graphics
0	1	7	Mono Text or HGC Graphics
1	0	8	Mono Text Only
1	1	15	Mono Text Only

Intensity = Text mode attribute byte bit 3
Video = Normal output to the monochrome display

2.3 Video Interface (cont'd)

NAME	GD510A	GD520A	DESCRIPTION
HSYNC		OUTPUT	Horizontal Sync. The active polarity of this signal can be selected by bit 6 of the miscellaneous output register (I/O address 3C2hex) or bit 6 of the timing control register (extension address 85H).
VSYNC	INPUT	OUTPUT	Vertical Sync. The active polarity of this signal can be selected by bit 7 of the miscellaneous output register (I/O address 3C2H) or bit 7 of the timing control register (extension address 85H).

2.4 External Interface

NAME	GD510A	GD520A	DESCRIPTION
BIOSRD*		INPUT	This pin is the decoded MSB address locations for the on-board ROM-BIOS. This is normally decoded for CPU address range (C0000H-C7FFFH) which decodes a 32Kbyte address range for EGA/VGA BIOS. This signal must be generated externally.
CLKIN		INPUT	From external clock select mux. The clock selected is controlled by the setting of the CLKSEL[2:0] outputs of the GD510A.
CLKSEL [2:0]	OUTPUT		These programmable output pins are used to select 1 of 8 clocks (via an external mux) to provide the proper frequencies required for VGA/EGA modes and various other user specified screen formats. During power-on or warm-boot conditions,these outputs can be used to select configuration switch settings (see description of SWITCH input below).
CPCS*	OUTPUT		Color Palette chip select. This pin decodes a valid I/O read or write to port addresses xC6-xC9H. The Most Significant I/O address must be decoded externally.
FC[1:0]	OUTPUT		Programmable output pins, normally used to drive feature connector.
INTERNAL*	OUTPUT		Programmable output pin,normally driving tri-state control pins of video drivers for internal or external (feature connector) video operation.

(*) Denotes negative true signal.

2.4 External Interface (cont'd)

NAME	GD510A	GD520A	DESCRIPTION
LPENSTR*		INPUT	Latches the current address being displayed into the light pen registers and sets the light pen flip-flop. The state of the light pen flip-flop can be read by the CPU at bit 1 of the display status register (3BAH).
LPENSW*		INPUT	This pin is usually connected to the light pen switch to indicate that the lightpen is activated. This signal can be read by the CPU through bit 2 of the display status register (3BAH).
ROMCS*		OUTPUT	This signal selects an on board BIOS ROM if the BIOSRD* signal is active and the ROM control register bit 7 is cleared.
SWITCH	INPUT		This input can be used in conjunction with the CLKSEL output pins and an external mux, to read up to 8 external inputs for switch position settings and other user defined inputs. This is normally performed at power-up time when the monitor is not yet activated, thus, the CLKSEL outputs can be used for this function.

(*) Denotes negative true signal.

2.5 CL-GD510A / 520A Interconnect Signals

NAME	GD510A	GD520A	DESCRIPTION
BLANK* / DE	INPUT	OUTPUT	Video Blanking signal / Display Enable. These signals function as follows: BLANK* DE FUNCTION 0 – OFF (Screen is black) 1 0 Border display 1 1 Active Screen (ie: text / graphics area)
CPUCYC*	INPUT	OUTPUT	Active low during an actual CPU Video RAM read or write cycles. This signal brackets the LATCH* signal during a read operation. The GD510A also uses this signal to differentiate between CPU and CRT write cycles.
CURSOR	INPUT	OUTPUT	Active during valid cursor position.
DOTCLOCK	INPUT	OUTPUT	Derived from CLKIN, this is the clock used to produce all of the signals in the GD510A AND GD520A. This signal should be used for any timing reference for video or CRT control.
LATCH*	INPUT	OUTPUT	Latches data to and from the video RAM in the GD510A.
S/L*	INPUT	OUTPUT	Shift / Load. Synchronizes the loading of the shift registers in the GD510A.
VSYNC	INPUT	OUTPUT	See description under video interface.

(*) Denotes negative true signal.

3. FUNCTIONAL DESCRIPTION

3.1 Functional Operation

The CIRRUS LOGIC GD510A Graphics/ Attributes chip and CIRRUS LOGIC GD520A Sequencer/CRT Controller chip are tightly coupled and interface with the host processor, video memory, the monitor and other external I/O.

The four major operations supported by the CL-GD510A / 520A are:

- Host access to CL-GD510A / 520A registers
- Host access to video memory
- Memory refresh
- Display access to video memory

Host Access to Registers

The host (typically an 8088/80286/80386 processor in an IBM PC/XT/AT bus compatible environment) can access CL-GD510A / 520A registers by setting up 20 bit addresses and generating IOR* / IOW* / MEMR* / MEMW* signals to read or write 8-bit data.

DRAM and screen refresh activities occur concurrently and independently (unless display parameters are being changed by the host CPU's actions on CL-GD510A / 520A registers).

The registers that may be accessed by the host are listed in sections 4 and 5. They include the registers of the IBM VGA, EGA, CGA, MDA, and Hercules HGC, including those of the 6845 CRT controller. Non-VGA registers have also been made host-readable in order to allow BIOS and driver software to determine the state of the graphics adapter.

Host Access to Video Memory

Host access to video memory is channelled via the CL-GD510A / 520A. The host must set up the proper address/data/timing parameters in CL-GD510A / 520A registers, then handshake with the CL-GD510A / 520A in order to connect the host data bus to one of the 4 video memory byte plane buses. For example, consider VGA/EGA operation:

Byte planes 0 and 1 share address bus A; planes 2 and 3 share the address bus B. The GD520A Sequencer/CRT Controller chip takes 17-bit addresses from the host, and transforms them according to the selected addressing mode and address space mappings, finally issuing multiplexed addresses to the different planes via the A and B address buses. The CAS* signal, four RAS* signals, and WE* are also generated.

Note that the GD520A Sequencer/CRT Controller chip also contains an intelligent address sequencer that allocates video memory cycles not only to the host, as just described, but also to the DRAM refresh controller and the display CRT controller.

Memory Refresh

Memory bandwidth is allocated to each process according to the actual realtime needs of the process, ensuring efficient use of the available bandwidth. The display is blanked during horizontal and vertical retrace intervals, freeing up memory bandwidth for host access and/or memory refresh. The CL-GD510A / 520A, unlike early VGA implementations that gave the host only 14% of memory cycles, can give the host from 25-50% access to video memory (1 out of 2 memory cycles), largely due to the sequencing strategy.

Display Access to Video Memory

The GD520A Sequencer/CRT Controller chip works very closely with the GD510A Graphics/Attributes chip in all video modes, as the GD510A actually contains the video memory data interface as well as the video outputs to the monitor. Thus the display data is latched in the GD510A after the GD520A determines where it is. Note that due to the 32-bit memory data interface, character data and attribute data can be pipelined. The GD510A contains the video shift registers to interface to the monitor. The GD520A works

with the GD510A in order to fetch scan line data from the font bitmaps, separately controlling the A and B address buses.

Foreground and background attributes are specified for each character in alphanumeric mode. Cursors and borders are also controlled by the GD510A in alpha modes.

In bit-mapped graphics (All Points Addressable) modes, pixel data is latched into the GD510A Graphics/Attributes chip, transferred to shift registers, and shifted out upon translation through the color palette registers, which are also contained in the GD510A.

The GD520A Sequencer/CRT Controller chip supplies the video clock to the GD510A Graphics/Attributes chip, as well as display memory read strobe (LATCH*), CPU read/write cycle (CPUCYC*), and shift register load (S/L*)

The GD520A Sequencer/CRT Controller chip keeps track of the active and unused areas of the screen and cursor positions and consequently supplies screen control signals (VSYNC, BLANK, Display Enable DE, and CURSOR) to the GD510A Graphics/ Attributes chip.

3.2 Compatibility Modes

The CL-GD510A / 520A includes all registers and data paths required for VGA/EGA, CGA, MDA, and HGC controllers. VGA enhancements to baseline EGA functionality include 320x200 eight-bit/pixel mode and support for an external color palette, 8 simultaneously loadable text fonts, write mode 3, and readable registers.

The GD510A / 520A includes a comprehensive mode switching feature that automatically detects application requirements and switches from VGA/EGA into CGA or HGC modes.

The high video clock speeds of these devices provide support for new extended resolution display mode.

Extended graphics resolutions beyond the 640x480 IBM VGA standard are also possible using either multiple frequency monitors such as the NEC MultiSync™ or Sony MultiScan™ or single frequency PS/2 monitors such as the IBM 8512. These include a 720 x 540 mode which has a 4:3 aspect ratio (square pixels on typical monitors). This mode is supported on both PS/2 monitors as well as multi-frequency displays. In addition there is an 800 x 600 mode which has a 4:3 aspect ratio (the same as 640 x 480 and 720 x 540). This mode requires a multi-frequency display. There are also high resolution text modes from 100 columns by 30 rows up to 132 columns by 60 rows.

The chip set also supports an extended mode 13 where 4 pages of 64K blocks of memory can be switched and displayed instead of the IBM VGA's single page. This will allow for animation using 256 displayable colors without requiring a large amount of data to be manipulated (64K maximum size per image).

The extended resolution capabilities of the CL-GD510A / 520A are listed on the next page following the listing of the standard screen formats.

3.3 Supported Screen Formats

PS/2 (Single Frequency Analog Display, IBM 85xx series-compatible)

Mode No.	No. of Colors	Char. x Row	Char. Cell	Video Mode	Display Mode	Screen Format	Buffer Start	CRT H/V Sync.	Dot Clock
0	4/256K	40x25	8x8	CGA	Text	320x200	B8000	31.5KHz/70Hz	25.172MHz
0*	16/256K	40x25	8x14	EGA	Text	320x350	B8000	31.5KHz/70Hz	25.172MHz
0/1+	16/256K	40x25	9x16	VGA	Text	360x400	B8000	31.5KHz/70Hz	28.332MHz
1	4/256K	40x25	8x8	CGA	Text	320x200	B8000	31.5KHz/70Hz	28.332MHz
1*	16/256K	40x25	8x14	EGA	Text	320x350	B8000	31.5KHz/70Hz	25.172MHz
2	4/256K	80x25	8x8	CGA	Text	640x200	B8000	31.5KHz/70Hz	25.172MHz
2*	16/256K	80x25	8x14	EGA	Text	640x350	B8000	31.5KHz/70Hz	25.172MHz
2/3+	16/256K	80x25	9x16	VGA	Text	720x400	B8000	31.5KHZ/70Hz	28.332MHZ
3	4/256K	80x25	8x8	CGA	Text	640x200	B8000	31.5KHz/70Hz	25.172MHz
3*	16/256K	80x25	8x14	EGA	Text	640x350	B8000	31.5KHz/70Hz	25.172MHz
4	4/256K			CGA	Graphics	320x200	A0000	31.5Khz/70Hz	12.586MHz
5	4/256K			CGA	Graphics	320x200	A0000	31.5KHz/70Hz	12.586MHz
6	2/256K			CGA	Graphics	640x200	A0000	31.5KHz/70Hz	25.172MHz
7	4	80x25	9x14	HGC/MDA	Text	720x350	B0000	31.5KHz/70Hz	28.332MHz
7+	4	80x25	9x16	VGA	Text	720x400	B0000	31.5KHz/70Hz	28.332MHz
10*	16x256K			EGA	Graphics	640x350	A0000	31.5KHz/70Hz	25.172MHz
11	2/256K			VGA	Graphics	640x480	A0000	31.5KHz/60Hz	25.172MHz
12	16/256K			VGA	Graphics	640x480	A0000	31.5KHz/60Hz	25.172MHz
13	256/256K			VGA	Graphics	320x200	A0000	31.5KHz/70Hz	25.172MHz
40	16/256K	100x30	8x13	Extended	Text	800x390	B8000	31.5KHz/70Hz	32.514MHz
41	16/256K	100x50	8x8	Extended	Text	800x400	B8000	31.5KHz/70Hz	32.514MHz
42	16/256K	100x60	8x8	Extended	Text	800x536	B8000	31.5KHz/56.2Hz	32.514MHz
53	16/256K	80x60	8x8	Extended	Text	640x480	B8000	31.5KHz/70Hz	32.514MHz
63	16/256K			Extended	Graphics	720x540	A0000	31.6KHz/56.5Hz	32.514MHz
D	16/256K			EGA	Graphics	320x200	A0000	31.5KHz/70Hz	12.586MHz
E	16/256K			EGA	Graphics	640x200	A0000	31.6KHz/70Hz	25.172MHz
F*	4			EGA	Graphics	640x350	A0000	31.5KHz/70Hz	25.172MHz
HGC	2			HGC	Graphics	720x348	A0000	31.5KHz/70Hz	28.332MHz

Note: Modes 40-52 and 63-64 require at least a 32.514 MHz dot clock and 100ns DRAM or faster. In monochrome modes, 4 colors is defined as Black, White, "Blinking" White, and "Intensified " White.
Note that "*" and "+" are part of the IBM mode names.

IBM Enhanced Color Display (Model 5154) or Compatible

Mode No.	No. of Colors	Char. x Row	Char. Cell	Video Mode	Display Mode	Screen Format	Buffer Start	CRT H/V Sync.	Dot Clock
0	4	40x25	8x8	CGA	Text	320x200	B8000	15.75KHz/60Hz	14.318MHz
0*	16/64	40x25	8x14	EGA	Text	320x350	B8000	21.85KHz/60Hz	16.257MHz
1	4	40x25	8x8	CGA	Text	320x200	B8000	15.75KHz/60Hz	14.318MHz
1*	16/64	40x25	8x14	EGA	Text	320x350	B8000	21.85KHz/60Hz	16.257MHz
2	4	80x25	8x8	CGA	Text	640x200	B8000	15.75KHz/60Hz	14.318MHz
2*	16/64	80x25	8x14	EGA	Text	640x350	B8000	21.85KHz/60Hz	16.257MHz
3	4	80x25	8x8	CGA	Text	640x200	B8000	15.75KHz/60Hz	14.318MHz
3*	16/64	80x25	8x14	EGA	Text	640x350	B8000	21.85KHz/60Hz	16.257MHz
4	4			CGA	Graphics	320x200	A0000	15,75KHz/60Hz	14.318MHz
5	4			CGA	Graphics	320x200	A0000	15.75KHz/60Hz	14.318MHz
6	2			CGA	Graphics	640x200	A0000	15.75KHz/60Hz	14.318MHz
10*	16/64			EGA	Graphics	640x350	A0000	21.85KHz/60Hz	16.257MHz
D	16/64			EGA	Graphics	320x200	A0000	21.85KHz/60Hz	16.257MHz
E	16/64			EGA	Graphics	640x200	A0000	21.85KHz/60Hz	16.257MHz
F*	4			EGA	Graphics	640x350	A0000	21.85KHz/60Hz	16.257MHz

3.3 Supported Screen Formats (cont'd)

IBM Color Display (Model 5153) or Compatible

Mode No.	No. of Colors	Char. x Row	Char. Cell	Video Mode	Display Mode	Screen Format	Buffer Start	CRT H/V Sync.	Dot Clock
0	4	40x25	8x8	CGA	Text	320x200	B8000	15.75KHz/60Hz	14.318MHz
1	4	40x25	8x8	CGA	Text	320x200	B8000	15.75KHz/60Hz	14.318MHz
2	4	80x25	8x8	CGA	Text	640x200	B8000	15.75KHz/60Hz	14.318MHz
3	4	80x25	8x8	CGA	Text	640x200	B8000	15.75KHz/60Hz	14.318MHz
4	4			CGA	Graphics	320x200	A0000	15.75KHz/60Hz	14.318MHz
5	4			CGA	Graphics	320x200	A0000	15.75KHz/60Hz	14.318MHz
6	2			CGA	Graphics	640x200	A0000	15.75KHz/60Hz	14.318MHz
D	16/64			EGA	Graphics	320x200	A0000	15.75KHz/60KHz	14.318MHz
E	16/64			EGA	Graphics	640x200	A0000	15.75KHz/60Hz	14.318MHz

Note: In monochrome modes, 4 colors is defined as Black, White, "Blinking" White, and "Intensified" White.

IBM Monochrome Display (Model 5151) or Compatible

Mode No.	No. of Colors	Char. x Row	Char. Cell	Video Mode	Display Mode	Screen Format	Buffer Start	CRT H/V Sync.	Dot Clock
7	4	80x25	9x14	HGC/MDA	Text	720x350	B0000	18.4KHz/50Hz	16.257MHz
F*	4			EGA	Graphics	640x350	A0000	18.4KHz/50Hz	16.257MHz
HGC	2			HGC	Graphics	720x348	B0000	18,4KHz/50Hz	16.257MHz

Note: In monochrome modes,4 colors means Black, White, "Blinking" White, and "Intensified" White.

Multi-Frequency Display (NEC Multisync™, SonyMultiscan™, or compatible)

Mode No.	No. of Colors	Char. x Row	Char. Cell	Video Mode	Display Mode	Screen Format	Buffer Start	CRT H/V Sync.†	Dot Clock†
0	4/256K	40x25	8x8	CGA	Text	320x200	B8000	–	–
0*	16/256K	40x25	8x14	EGA	Text	320x350	B8000	–	–
0/1+	16/256K	40x25	9x16	VGA	Text	360x400	B8000	–	–
1	4/256K	40x25	8x8	CGA	Text	320x200	B8000	–	–
1*	16/256K	40x25	8x14	EGA	Text	320x350	B8000	–	–
2	4/256K	80x25	8x8	CGA	Text	640x200	B8000	-	–
2*	16/256K	80x25	8x14	EGA	Text	640x350	B8000	-	–
2/3+	16/256K	80x25	9x16	VGA	Text	720x400	B8000	–	–
3	4/256K	80x25	8x8	CGA	Text	640x200	B8000	–	–
3*	16/256K	80x25	8x14	EGA	Text	640x350	B8000	–	–
4	4/256K			CGA	Graphics	320x200	A0000	–	–
5	4/256K			CGA	Graphics	320x200	A0000	–	–
6	2/256K			CGA	Graphics	640x200	A0000	–	–
7	4	80x25	9x14	HGC/MDA	Text	720x350	B0000	–	–
7+	4	80x25	9x16	VGA	Text	720x400	B0000	–	–
10*	16/256K			EGA	Graphics	640x350	A0000	–	–
11	2/256K			VGA	Graphics	640x480	A0000	–	–
12	16/256K			VGA	Graphics	640x480	A0000	–	–
13	256/256K			VGA	Graphics	320x200	A0000	–	–
40	16/256K	100x30	9x13	Extended	Text	900x390	B8000	–	–
41	16/256K	100x50	8x8	Extended	Text	800x400	B8000	–	–
42	16/256K	100x60	8x8	Extended	Text	800x480	B8000	–	–
43	16/256K	100x75	8x8	Extended	Text	800x600	B8000	–	–
50	16/256K	132x30	8x13	Extended	Text	1056x390	B8000	–	–
51	16/256K	132x50	8x8	Extended	Text	1056x400	B8000	–	–
52	16/256K	132x60	8x8	Extended	Text	1056x480	B8000	–	–
53	16/256K	80x60	8x8	Extended	Text	640x480	B8000	–	–
63	16/256K			Extended	Graphics	720x540	A0000	–	–
64	16/256K			Extended	Graphics	800x600	A0000	–	–
D	16/256K			EGA	Graphics	320x200	A0000	–	–
E	16/256K			EGA	Graphics	640x200	A0000	–	–
F*	4			EGA	Graphics	640x350	A0000	–	–
HGC	2			HGC	Graphics	720x348	A0000	–	–

Note: Modes 40h-52h and 63h-64h require at least a 32.514 MHz dot clock and 100ns DRAM or faster. In monochrome modes, 4 colors is defined as Black, White, "Blinking" White, and "Intensified " White.
Note that "*" and "+" are part of the IBM mode names.
† These values will vary depending upon which monitor and which monitor parameters are used in the BIOS.

4. VGA, EGA, CGA, AND HGC REGISTER PORT MEMORY MAP

Address	VGA/EGA Port	CGA Port	HGC Port
2B0 / 3B0	CRTC Index (R/W) (EGA Only)		6845 Index (R/W)
2B1 / 3B1	CRTC Data (R/W) (EGA Only)		6845 Data (R/W)
2B2 / 3B2	CRTC Index (R/W) (EGA Only)		6845 Index (R/W)
2B3 / 3B3	CRTC Data (R/W) (EGA Only)		6845 Data (R/W)
2B4 / 3B4	CRTC Index (R/W) (EGA Only)		6845 Index (R/W)
2B5 / 3B5	CRTC Data (R/W)		6845 Data (R/W)
2B6 / 3B6	CRTC Index (R/W) (EGA Only)		6845 Index (R/W)
2B7 / 3B7	CRTC Data (R/W) (EGA Only)		6845 Data (R/W)
2B8 / 3B8			Mode Control (R/W)
2B9 / 3B9			Set Light Pen Flip Flop (W)
2BA / 3BA	Feature Control(W), Display Status(R)		Display Status (R)
2BB / 3BB	Clear Light Pen Flip Flop (W)		Clear Light Pen Flip Flop (W)
2BC / 3BC	Set Light Pen Flip Flop (W)		
2BD / 3BD			
2BE / 3BE			
2BF / 3BF			Configuration (R/W)

2C0 / 3C0	Attribute Controller Index/Data (R/W)		
2C1 / 3C1	Attribute Controller Index/Data (R/W)		
2C2 / 3C2	Misc Output (W), Feature (R)		
2C3 / 3C3	Misc Output (W), Feature (R)		
2C4 / 3C4	Sequencer/Extensions Index (R/W)		
2C5 / 3C5	Sequencer/Extensions Data (R/W)		
2C6 / 3C6	Palette Pixel Mask (R/W)		
2C7 / 3C7	Palette Address Register R Mode (R/W)		
2C8 / 3C8	Palette Address Register W Mode (R/W)		
2C9 / 3C9	Palette Data (R/W)		
2CA / 3CA	G. Pos. 2 (W) (EGA Only)		
2CB / 3CB	(Reserved)		
2CC / 3CC	G. Pos. 1(W)(EGA Only) Misc Output (R)		
2CD / 3CD	(Reserved)		
2CE / 3CE	Graphics Controller Index (R/W)		
2CF / 3CF	Graphics Controller Data (R/W)		

2D0 / 3D0	CRTC Index (R/W) (EGA Only)	6845 Index (R/W)	
2D1 / 3D1	CRTC Data (R/W) (EGA Only)	6845 Data (R/W)	
2D2 / 3D2	CRTC Index (R/W) (EGA Only)	6845 Index (R/W)	
2D3 / 3D3	CRTC Data (R/W) (EGA Only)	6845 Data (R/W)	
2D4 / 3D4	CRTC Index (R/W) (EGA Only)	6845 Index (R/W)	
2D5 / 3D5	CRTC Data (R/W)	6845 Data (R/W)	
2D6 / 3D6	CRTC Index (R/W) (EGA Only)	6845 Index (R/W)	
2D7 / 3D7	CRTC Data (R/W) (EGA Only)	6845 Data (R/W)	
2D8 / 3D8		Mode Control (R/W)	
2D9 / 3D9		Color Select (R/W)	
2DA / 3DA	Feature Control(W), Display Status(R)	Display Status (R)	
2DB / 3DB	Clear Light Pen Flip Flop (W)	Clear Light Pen Flip Flop (W)	
2DC / 3DC	Set Light Pen Flip Flop (W)	Set Light Pen Flip Flop (W)	
2DD / 3DD			
2DE / 3DE			
2DF / 3DF			

5. CGA, MDA, AND HGC REGISTERS

5.1 Color Graphics Adapter (CGA) Compatible Registers

ABBREV	CGA REGISTER NAME	BITS	REG TYPE	READ/ WRITE	REG/ INDEX	PORT ADDRESS
MODE	Mode Control	7	GD510A/GD520A‡	R/W	--	3D8
COLOR	Color Select	6	GD510A	R/W	--	3D9
STAT	Display Status	7	GD510A/GD520A‡	R	--	3DA
CLPEN	Clear Light Pen Flip Flop	0	GD520A	W	--	3DB
SLPEN	Set Light Pen Flip Flop	0	GD520A	W	--	3DC
CRX	6845 Index	5	GD520A	R/W	--	3D4 (3D0,3D2,3D6)†
R0	Horizontal Total	8	GD520A	R/W	00	3D5 (3D1,3D3,3D7)†
R1	Horizontal Displayed	8	GD520A	R/W	01	3D5 (3D1,3D3,3D7)†
R2	Horizontal Sync Position	8	GD520A	R/W	02	3D5 (3D1,3D3,3D7)†
R3	Sync Width	4+4††	GD520A	R/W	03	3D5 (3D1,3D3,3D7)†
R4	Vertical Total	7	GD520A	R/W	04	3D5 (3D1,3D3,3D7)†
R5	Vertical Total Adjust	5	GD520A	R/W	05	3D5 (3D1,3D3,3D7)†
R6	Vertical Displayed	7	GD520A	R/W	06	3D5 (3D1,3D3,3D7)†
R7	Vertical Sync Position	7	GD520A	R/W	07	3D5 (3D1,3D3,3D7)†
R8	Interlace Mode	2	GD520A	R/W	08	3D5 (3D1,3D3,3D7)†
R9	Character Cell Height	5	GD520A	R/W	09	3D5 (3D1,3D3,3D7)†
RA	Cursor Start	5+2††	GD520A	R/W	0A	3D5 (3D1,3D3,3D7)†
RB	Cursor End	5	GD520A	R/W	0B	3D5 (3D1,3D3,3D7)†
CRC	Start Address High	8	GD520A	R/W	0C	3D5 (3D1,3D3,3D7)†
CRD	Start Address Low	8	GD520A	R/W	0D	3D5 (3D1,3D3,3D7)†
CRE	Cursor Address High	8	GD520A	R/W	0E	3D5 (3D1,3D3,3D7)†
CRF	Cursor Address Low	8	GD520A	R/W	0F	3D5 (3D1,3D3,3D7)†
LPENH	Light Pen High	8	GD520A	R	10	3D5 (3D1,3D3,3D7)†
LPENL	Light Pen Low	8	GD520A	R	11	3D5 (3D1,3D3,3D7)†

5.2 Monochrome Display Adapter (MDA) and Hercules Graphics Adapter (HGC) Compatible Registers

ABBREV	MDA/HGC REGISTER NAME	BITS	REG TYPE	READ/ WRITE	REG/ INDEX	PORT ADDRESS
MODE	Mode Control	7	GD510A/GD520A‡	R/W	--	3B8
STAT	Display Status	7	GD510A/GD520A‡	R	--	3BA
CONFIG	Configuration	2	GD510A/GD520A‡	R/W	--	3BF
CLPEN	Clear Light Pen Flip Flop	0	GD520A	W	--	3BB
SLPEN	Set Light Pen Flip Flop	0	GD520A	W	--	3B9
CRX	6845 Index	5	GD520A	R/W	--	3B4 (3B0,3B2,3B6)†
R0	Horizontal Total	8	GD520A	R/W	00	3B5 (3B1,3B3,3B7)†
R1	Horizontal Displayed	8	GD520A	R/W	01	3B5 (3B1,3B3,3B7)†
R2	Horizontal Sync Position	8	GD520A	R/W	02	3B5 (3B1,3B3,3B7)†
R3	Sync Width	4+4††	GD520A	R/W	03	3B5 (3B1,3B3,3B7)†
R4	Vertical Total	7	GD520A	R/W	04	3B5 (3B1,3B3,3B7)†
R5	Vertical Total Adjust	5	GD520A	R/W	05	3B5 (3B1,3B3,3B7)†
R6	Vertical Displayed	7	GD520A	R/W	06	3B5 (3B1,3B3,3B7)†
R7	Vertical Sync Position	7	GD520A	R/W	07	3B5 (3B1,3B3,3B7)†
R8	Interlace Mode	2	GD520A	R/W	08	3B5 (3B1,3B3,3B7)†
R9	Character Cell Height	5	GD520A	R/W	09	3B5 (3B1,3B3,3B7)†
RA	Cursor Start	5+2††	GD520A	R/W	0A	3B5 (3B1,3B3,3B7)†
RB	Cursor End	5	GD520A	R/W	0B	3B5 (3B1,3B3,3B7)†
CRC	Start Address High	8	GD520A	R/W	0C	3B5 (3B1,3B3,3B7)†
CRD	Start Address Low	8	GD520A	R/W	0D	3B5 (3B1,3B3,3B7)†
CRE	Cursor Address High	8	GD520A	R/W	0E	3B5 (3B1,3B3,3B7)†
CRF	Cursor Address Low	8	GD520A	R/W	0F	3B5 (3B1,3B3,3B7)†
LPENH	Light Pen High	8	GD520A	R	10	3B5 (3B1,3B3,3B7)†
LPENL	Light Pen Low	8	GD520A	R	11	3B5 (3B1,3B3,3B7)

‡ Physical readback chip is underlined for split/duplicated registers
† Valid alternate register addresses are presented in parenthesis
†† Split-field registers are denoted by 'X+Y'

5.3 MDA, CGA, and HGC Bit Summary

Bit	MODE Register		CONFIG Register (HGC only)
7	Page	(HGC only)	–
6	–		–
5	Blink Enable		–
4	High-Res Graphics	(CGA only)	–
3	Video Enable		–
2	Monochrome	(CGA only)	–
1	Graphics		Page 1 Enable
0	High-Res Text	(CGA only)	Graphics Mode Enable

Bit	COLOR Register
7	
6	
5	Color Set #
4	Intensity
3	Color bit-3 (I)
2	Color bit-2 (R)
1	Color bit-1 (G)
0	Color bit-0 (B)

Color Set	Pixel = 0	Pixel = 1	Pixel = 2	Pixel = 3
Set 0:	Color specified in bits 0-3	Green	Red	Brown
Set 1:	Color specified in bits 0-3	Cyan	Magenta	White

Text Mode: Intensified Background
320x200: Intensified Color 0-3
640x200: Ignored

Text Mode: Border Color
320x200: Background Color (color when pixel value is 0)
(foreground color: see bit 5)
640x200: Foreground Color (color when pixel value is 1)
(background color: black)

5.4 Decode for Attribute Byte in Video Memory

Text Attribute Byte		Interpretation
b000	i000	HGC Black
bxxx	i001	HGC Underline
b111	i000	HGC Reverse Video
bBBB	iFFF	CGA Color Select
b000	s001	EGA Underline
bBBB	sFFF	EGA Color Select

b = Character blink (CGA BG intensity if Mode [5]=0)
(EGA BG intensity if AR10[3]=0)
B = Background Color
F = Foreground Color
i = Character intensity
s = Character set select and foreground color msb

5.5 6845 CRT Controller Bit Summary

Bit	R0	R1	R2	R3	R4	R5	R6
7	H Total 7	H Disp 7	H Sync Pos 7	V Sync Width 3	–	–	–
6	H Total 6	H Disp 6	H Sync Pos 6	V Sync Width 2	V Total 6	–	V Disp 6
5	H Total 5	H Disp 5	H Sync Pos 5	V Sync Width 1	V Total 5	–	V Disp 5
4	H Total 4	H Disp 4	H Sync Pos 4	V Sync Width 0	V Total 4	V Total Adj 4	V Disp 4
3	H Total 3	H Disp 3	H Sync Pos 3	H Sync Width 3	V Total 3	V Total Adj 3	V Disp 3
2	H Total 2	H Disp 2	H Sync Pos 2	H Sync Width 2	V Total 2	V Total Adj 2	V Disp 2
1	H Total 1	H Disp 1	H Sync Pos 1	H Sync Width 1	V Total 1	V Total Adj 1	V Disp 1
0	H Total 0	H Disp 0	H Sync Pos 0	H Sync Width 0	V Total 0	V Total Adj 0	V Disp 0

Bit	R7
7	–
6	V Sync Pos 6
5	V Sync Pos 5
4	V Sync Pos 4
3	V Sync Pos 3
2	V Sync Pos 2
1	V Sync Pos 1
0	V Sync Pos 0

R8

–
–
–
–
–
–

Interlace Mode:
Non-interlace
Interlace Sync
Non-interlace
Interlace Sync and Video

Interlace Mode 1: 0 0 1 1
Interlace Mode 0: 0 1 0 1

Bit	R9	RA	RB
7	–	–	–
6	–	Cursor Display Mode 1: 0 0 1 1	–
5	–	Cursor Display Mode 0: 0 1 0 1	–
4	Cell Height 4	Cursor Start 4	Cursor End 4
3	Cell Height 3	Cursor Start 3	Cursor End 3
2	Cell Height 2	Cursor Start 2	Cursor End 2
1	Cell Height 1	Cursor Start 1	Cursor End 1
0	Cell Height 0	Cursor Start 0	Cursor End 0

Cursor Display Mode:
Slow Blink
No Cursor
No Cursor Display
Fast Blink

6. VGA / EGA REGISTERS

6.1 Video Graphics Array/Enhanced Graphics Adapter Compatible Register Table

ABBREV PORT	EGA REGISTER NAME	BITS	REG TYPE	R/W	REG/NDX	MONO PORT	COLOR
MISC	Miscellaneous Output	8	GD510A/GD520A‡	W	--	3C2	3C2
FEAT	Input Status 0 (Feature Read)	4	GD510A/GD520A‡	R	--	3C2	3C2
STAT	Input Status 1 (Display Status)	7	GD510A/GD520A‡	R	--	3BA	3DA
FC	Feature Control	3	GD510A	W	--	3BA	3DA
GPOS1/MISC	Graphics 1 Pos (W), Misc (R)	2,8	GD510A, GD510A/GD520A‡	R/W	--	3CC	3CC
GPOS2/FC	Graphics 2 Pos (W), FeatCtrl (R)	2,3	GD510A,GD510A	R/W	--	3CA	3CA
GRX	Graphics Controller Index	4	GD510A	R/W	--	3CE	3CE
GR0	Set/Reset	4	GD510A	R/W	00	3CF	3CF
GR1	Enable Set/Reset	4	GD510A	R/W	01	3CF	3CF
GR2	Color Compare	4	GD510A	R/W	02	3CF	3CF
GR3	Data Rotate	5	GD510A	R/W	03	3CF	3CF
GR4	Read Map Select	3	GD510A	R/W	04	3CF	3CF
GR5	Mode	7	GD510A	R/W	05	3CF	3CF
GR6	Miscellaneous	4	GD520A	R/W	06	3CF	3CF
GR7	Color Don't Care	4	GD510A	R/W	07	3CF	3CF
GR8	Bit Mask	8	GD510A	R/W	08	3CF	3CF
ARX	Attribute Controller Index	6	GD510A/GD520A‡	R/W	--	3C0	3C0
AR0-F	Color Palette Regs 0-15	8	GD510A	R/W	00-0F	3C0	3C0
AR10	Mode Control	7	GD510A	R/W	10	3C0	3C0
AR11	Overscan Color	8	GD510A	R/W	11	3C0	3C0
AR12	Color Plane Enable	6	GD510A	R/W	12	3C0	3C0
AR13	Horizontal Pixel Panning	4	GD510A	R/W	13	3C0	3C0
AR14	Color Select	4	GD510A	R/W	14	3C0	3C0
CLPEN	Clear Light Pen Flip Flop	0	GD520A	W	--	3BB	3DB
SLPEN	Set Light Pen Flip Flop	0	GD520A	W	--	3BC / 3B9	3DC
SERX	Sequencer / Extension Reg. Index	7	GD520A	R/W	--	3C4	3C4
SR0	Reset	2	GD520A	R/W	00	3C5	3C5
SR1	Clocking Mode	6	GD520A	R/W	01	3C5	3C5
SR2	Plane Mask	4	GD520A	R/W	02	3C5	3C5
SR3	Character Map Select	6	GD520A	R/W	03	3C5	3C5
SR4	Memory Mode	3	GD520A	R/W	04	3C5	3C5
SR6	Extensions Control (see Ext. Table)	1	GD510A/GD520A‡	R/W	06	3C5	3C5
SR7	Reset H. Character Counter	1	GD520A	W	07	3C5	3C5
CRX	CRTC Index	6/5	GD520A	R/W	--	3B4	3D4
CR0	Horizontal Total	8	GD520A	R/W	00	3B5	3D5
CR1	Horizontal Display End	8	GD520A	R/W	01	3B5	3D5
CR2	Horizontal Blanking Start	8	GD520A	R/W	02	3B5	3D5
CR3	Horizontal Blanking End	5+2+1††	GD520A	R/W	03	3B5	3D5
CR4	Horizontal Retrace Start	8	GD520A	R/W	04	3B5	3D5
CR5	Horizontal Retrace End	5+2+1††	GD520A	R/W	05	3B5	3D5
CR6	Vertical Total	8	GD520A	R/W	06	3B5	3D5
CR7	Overflow	8	GD520A	R/W	07	3B5	3D5
CR8	Screen A Preset Row Scan	7	GD520A	R/W	08	3B5	3D5
CR9	Character Cell Height	5+1+1+1	GD520A	R/W	09	3B5	3D5
CRA	Cursor Start	6	GD520A	R/W	0A	3B5	3D5
CRB	Cursor End	5+2††	GD520A	R/W	0B	3B5	3D5
CRC	Screen A Start Address High	8	GD520A	R/W	0C	3B5	3D5
CRD	Screen A Start Address Low	8	GD520A	R/W	0D	3B5	3D5
CRE	Cursor Location High	8	GD520A	R/W	0E	3B5	3D5
CRF	Cursor Location Low	8	GD520A	R/W	0F	3B5	3D5
LPENH	Light Pen High	8	GD520A	R	10	3B5	3D5
LPENL	Light Pen Low	8	GD520A	R	11	3B5	3D5
CR10	Vertical Retrace Start	8	GD520A	W	10	3B5	3D5
CR11	Vertical Retrace End	4+2+1+1††	GD520A	W	11	3B5	3D5
CR12	Vertical Display End	8	GD520A	R/W	12	3B5	3D5
CR13	Offset	8	GD520A	R/W	13	3B5	3D5
CR14	Underline Location	5+2††	GD520A	R/W	14	3B5	3D5
CR15	Vertical Blanking Start	8	GD520A	R/W	15	3B5	3D5
CR16	Vertical Blanking End	8	GD520A	R/W	16	3B5	3D5
CR17	CRT Mode Control	7	GD520A	R/W	17	3B5	3D5
CR18	Line Compare	8	GD520A	R/W	18	3B5	3D5
CR22	Readback CRT Latches	8	GD510A	R	22	3B5	3D5
CR24	Attribute Index Toggle	7	GD510A	R	24	3B5	3D5
CR30-CR3F	Frame Blank	1	GD520A	W	3X	3B5	3D5

‡ Physical readback chip is underlined for split/duplicated registers
†† Split-field registers are denoted by 'X+Y' or "X+Y+Z" or 'X+Y+Z+M.'
Note: EGA supports sparce decoding. VGA does not.

6.2 VGA/EGA Bit Summary

General Registers

Bit	MISC		FEAT	STAT	FC
7	EGA V Retrace Polarity‡	(0=pos,1=neg)	CRT Interrupt Pending	Not Vertical Retrace	--
6	EGA H Retrace Polarity‡	(0=pos,1=neg)	Feature Code 1	--	--
5	Page Bit for Odd/Even Mode		Feature Code 0	Diagnostic 1	--
4	Disable External Video Driver		Switch	Diagnostic 0	--
3	Clock Select 1‡	(0=14/25, 1=16/28,	--	Vertical Retrace	-reserved-
2	Clock Select 0‡	2=25/39, 3=32/x)†	--	Light Pen Switch	--
1	RAM Enable		--	Light Pen Flip Flop	Feature Control 1
0	CRTC I/O Address	(0=2Bx/3Bx, 1=2Dx/3Dx)	--	Display Enabled	Feature Control 0

‡ Indicates write protected with WRC register bit 0 (write control)

† See CLOCK SELECT Register in section 6.5, bit 4 (EGA/VGA) or bit 7 (CGA/HGC),work as a "page" select for clock

VGA/EGA Graphics Controller

Bit	GR0	GR1	GR2	GR3	GR4
7	--	--	--	--	--
6	--	--	--	--	--
5	--	--	--	--	--
4	--	--	--	Function Select 1	--
3	Set/Reset Plane 3	Enable Set/Reset Plane 3	Color Compare Plane 3	Function Select 0	--
2	Set/Reset Plane 2	Enable Set/Reset Plane 2	Color Compare Plane 2	Rotate Count 2	Map Select 2
1	Set/Reset Plane 1	Enable Set/Reset Plane 1	Color Compare Plane 1	Rotate Count 1	Map Select 1
0	Set/Reset Plane 0	Enable Set/Reset Plane 0	Color Compare Plane 0	Rotate Count 0	Map Select 0

Bit	GR5	GR6	GR7	GR8
7	--	--	--	Write Enable Data 7
6	Shift 256	--	--	Write Enable Data 6
5	Shift Register	--	--	Write Enable Data 5
4	Odd/Even	--	--	Write Enable Data 4
3	Read Mode	Memory Map 1	Color Plane 3 Don't Care	Write Enable Data 3
2	Test Condition	Memory Map 0	Color Plane 2 Don't Care	Write Enable Data 2
1	Write Mode 1	Chain Odd Maps to Even	Color Plane 1 Don't Care	Write Enable Data 1
0	Write Mode 0	Graphics Mode	Color Plane 0 Don't Care	Write Enable Data 0

VGA/EGA Attribute Controller

Bit	ARX	AR0-F	AR10	AR11	AR12	AR13	AR14
7	Index 0, Data 1	Tertiary Green	AR14 Enable	Tertiary Green	--	--	--
6	--	Tertiary Blue	Pixel Double	Tertiary Blue	--	--	--
5	Video Enable	Secondary Red	Pixel Pan Comp.	Secondary Red	Video Status Mux 1	--	--
4	Index 4	Secondary Green	--	Secondary Green	Video Status Mux 0	--	--
3	Index 3	Secondary Blue	Blink Enable	Secondary Blue	Ena Color Plane 3	Shift Count 3	Video 7
2	Index 2	Primary Red	Line Graphics Enable	Primary Red	Ena Color Plane 2	Shift Count 2	Video 6
1	Index 1	Primary Green	Mono Graph Attr Ena	Primary Green	Ena Color Plane 1	Shift Count 1	Video 5
0	Index 0	Primary Blue	Graphics Mode	Primary Blue	Ena Color Plane 0	Shift Count 0	Video 4

Note: Writing or reading 3C0 or 3C1 toggles between Index and Data; Index may be read at extensions Index 83 (3C5)
Toggle is cleared by reading 3BA/3DA (Display Status Register)
State of toggle may be read as MSB of Index when read at extensions Index 83; Index MSB reads 0 when read at 3C0.

VGA/EGA Sequencer

Bit	SR0	SR1	SR2	SR3	SR4	SR7
7	--	--	--	--	--	--
6	--	--	--	--	--	--
5	--	Full Bandwidth/blank	--	Secondary Font Select 0	--	--
4	--	Shift load 32	--	Primary Font Select 0	--	--
3	--	Divide Dot Clock by 2	Enable Plane 3	Secondary Font Select 2	Double Odd/Even	--
2	--	Shift Load (0=8-bits, 1=16-bits)	Enable Plane 2	Secondary Font Select 1	Odd/Even	--
1	Sync Reset	Bandwidth (0=1:4, 1=3:2)	Enable Plane 1	Primary Font Select 2	Extended Memory	--
0	Async Reset	Character Width (0=9, 1=8)	Enable Plane 0	Primary Font Select 1	--	H.Cntr Reset

6.3 VGA / EGA CRT Controller Bit Summary

Bit	CR0	CR1	CR2	CR3	CR4	CR5
7	H Total 7	H Disp End 7	H Blank Start 7	LP Compat. Read	H Retrace Start 7	H. Blank End 5†
6	H Total 6	H Disp End 6	H Blank Start 6	DE Skew Control 1	H Retrace Start 6	H Retrace Delay 1
5	H Total 5	H Disp End 5	H Blank Start 5	DE Skew Control 0	H Retrace Start 5	H Retrace Delay 0
4	H Total 4	H Disp End 4	H Blank Start 4	H Blank End 4	H Retrace Start 4	H Retrace End 4
3	H Total 3	H Disp End 3	H Blank Start 3	H Blank End 3	H Retrace Start 3	H Retrace End 3
2	H Total 2	H Disp End 2	H Blank Start 2	H Blank End 2	H Retrace Start 2	H Retrace End 2
1	H Total 1	H Disp End 1	H Blank Start 1	H Blank End 1	H Retrace Start 1	H Retrace End 1
0	H Total 0	H Disp End 0	H Blank Start 0	H Blank End 0	H Retrace Start 0	H Retrace End 0

Bit	CR6	CR7	CR8	CR9	CRA	CRB
7	V Total 7	V. Retrace Start 9	--	Scan Double	--	--
6	V Total 6	V. Display End 9	Screen A Byte Pan Control 1	Line Compare 9	--	Cursor Skew 1
5	V Total 5	V. Total 9	Screen A Byte Pan Control 0	V. Blank Start 9	Cursor Disable	Cursor Skew 0
4	V Total 4	Line Compare 8	Screen A Preset Row Scan 4	Cell Height 4	Cursor Start 4	Cursor End 4
3	V Total 3	V Blank Start 8	Screen A Preset Row Scan 3	Cell Height 3	Cursor Start 3	Cursor End 3
2	V Total 2	V Retrace 8	Screen A Preset Row Scan 2	Cell Height 2	Cursor Start 2	Cursor End 2
1	V Total 1	V Disp End 8	Screen A Preset Row Scan 1	Cell Height 1	Cursor Start 1	Cursor End 1
0	V Total 0	V Total 8	Screen A Preset Row Scan 0	Cell Height 0	Cursor Start 0	Cursor End 0

Bit	CRC	CRD	CRE	CRF
7	Screen A Start Address 15	Screen A Start Address 7	Cursor Location 15	Cursor Location 7
6	Screen A Start Address 14	Screen A Start Address 6	Cursor Location 14	Cursor Location 6
5	Screen A Start Address 13	Screen A Start Address 5	Cursor Location 13	Cursor Location 5
4	Screen A Start Address 12	Screen A Start Address 4	Cursor Location 12	Cursor Location 4
3	Screen A Start Address 11	Screen A Start Address 3	Cursor Location 11	Cursor Location 3
2	Screen A Start Address 10	Screen A Start Address 2	Cursor Location 10	Cursor Location 2
1	Screen A Start Address 9	Screen A Start Address 1	Cursor Location 9	Cursor Location 1
0	Screen A Start Address 8	Screen A Start Address 0	Cursor Location 8	Cursor Location 0

Bit	CR10	CR11	CR12	CR13	CR14
7	V Retrace Start 7	VGA Write Protect	V Disp End 7	Offset 7	--
6	V Retrace Start 6	Refresh Cycle Select	V Disp End 6	Offset 6	Doubleword
5	V Retrace Start 5	0 = Enable V Intrpt	V Disp End 5	Offset 5	Count by 4
4	V Retrace Start 4	0 = Clear V Intrpt	V Disp End 4	Offset 4	Underline 4
3	V Retrace Start 3	V Retrace End 3	V Disp End 3	Offset 3	Underline 3
2	V Retrace Start 2	V Retrace End 2	V Disp End 2	Offset 2	Underline 2
1	V Retrace Start 1	V Retrace End 1	V Disp End 1	Offset 1	Underline 1
0	V Retrace Start 0	V Retrace End 0	V Disp End 0	Offset 0	Underline 0

Bit	CR15	CR16	CR17	CR18
7	V Blank Start 7	V. Blank End 7	Hardware Reset	Line Compare 7
6	V Blank Start 6	V. Blank End 6	Mode (0=word, 1=byte)	Line Compare 6
5	V Blank Start 5	V. Blank End 5	Address Wrap	Line Compare 5
4	V Blank Start 4	V Blank End 4	–	Line Compare 4
3	V Blank Start 3	V Blank End 3	Count by Two	Line Compare 3
2	V Blank Start 2	V Blank End 2	H Retrace Select	Line Compare 2
1	V Blank Start 1	V Blank End 1	Select Row Scan Counter	Line Compare 1
0	V Blank Start 0	V Blank End 0	Compatibility Mode Support	Line Compare 0

Bit	CR22	CR24	CR30-CR3F
7	CRT Latch Readback 7	Attribtue Toggle bit ††	–
6	CRT Latch Readback 6	–	–
5	CRT Latch Readback 5	Video Enable	–
4	CRT Latch Readback 4	Attribute Index 4	–
3	CRT Latch Readback 3	Attribute Index 3	–
2	CRT Latch Readback 2	Attribute Index 2	–
1	CRT Latch Readback 1	Attribute Index 1	–
0	CRT Latch Readback 0	Attribute Index 0	Frame Blank

† In EGA mode this is Start Odd Memory address.
†† 0= Attribute Index, 1= Data

6.4 Extension Register Table

ABBREV	EXTENSION REGISTER	BITS	REG TYPE	READ/WRITE	REG/INDEX	PORT ADDR
SERX	Sequencer Extensions Register Index	7	GD510A/GD520A‡	R/W	–	3C4
SR6	Extension Control	1	GD510A/GD520A‡	R/W	06	3C5
CR7F	Identification	8	GD520A	R	7F	3B5/3D5
MC1	Misc. Control 1	8	GD520A	R/W	80	3C5
GPOS1	Graphics 1 Position	2	GD510A	R/W	81	3C5
GPOS2	Graphics 2 Position	2	GD510A	R/W	82	3C5
ARX	Attribute Controller Index	7	GD510A	R/W	83	3C5
WRC	Write Control	8	GD510A/GD520A‡	R/W	84	3C5
TC	Timing Control	7	GD520A	R/W	85	3C5
BWC	Bandwidth Control	6	GD520A	R/W	86	3C5
MC2	Misc. Control 2	8	GD520A	R/W	87	3C5
HSS	H. Sync Skew	4	GD520A	R/W	88	3C5
FONTC	CGA, HGC Font Control	4	GD520A	R/W	89	3C5
	-reserved-	0	–	–	8A	3C5
SBPR	Screen B Preset Row Scan	5	GD520A	R/W	8B	3C5
SBSH	Screen B Start Address High	8	GD520A	R/W	8C	3C5
SBSL	Screen B Start Address Low	8	GD520A	R/W	8D	3C5
GAVER	GD510A Version Code	8	GD510A	R	8E	3C5
SCVER	GD520A Version Code	8	GD520A	R	8F	3C5
CR10	Vertical Retrace Start	8	GD520A	R/W	90	3C5
CR11	Vertical Retrace End	8	GD520A	R/W	91	3C5
LPENH	Light Pen High	8	GD520A	R/W	92	3C5
LPENL	Light Pen Low	8	GD520A	R/W	93	3C5
PPAH	Pointer Pattern Address High	8	GD520A	R/W	94	3C5
CADJ	Cursor Height Adjust	5	GD520A	R/W	95	3C5
CW	Caret Width	8	GD510A	R/W	96	3C5
CH	Caret Height	8	GD510A	R/W	97	3C5
CXH	Caret Horizontal Position High	3	GD510A	R/W	98	3C5
CXL	Caret Horizontal Position Low	8	GD510A	R/W	99	3C5
CYH	Caret Vertical Position High	2	GD510A	R/W	9A	3C5
CYL	Caret Vertical Position Low	8	GD510A	R/W	9B	3C5
PXH	Pointer Horizontal Position High	3	GD510A	R/W	9C	3C5
PXL	Pointer Horizontal Position Low	8	GD510A	R/W	9D	3C5
PYH	Pointer Vertical Position High	2	GD520A	R/W	9E	3C5
PYL	Pointer Vertical Position Low	8	GD520A	R/W	9F	3C5
GRL0	Graphics Ctrlr Memory Latch 0	8	GD510A	R/W	A0	3C5
GRL1	Graphics Ctrlr Memory Latch 1	8	GD510A	R/W	A1	3C5
GRL2	Graphics Ctrlr Memory Latch 2	8	GD510A	R/W	A2	3C5
GRL3	Graphics Ctrlr Memory Latch 3	8	GD510A	R/W	A3	3C5
CLK	Clock Select	6	GD510A	R/W	A4	3C5
CURS	Cursor Attributes	8	GD510A/GD520A‡	R/W	A5	3C5
ISS	Internal Switch Source	8	GGD510A	R/W	A6	3C5
NMI1	NMI Mask 1	8	GD510A	R/W	A8	3C5
NMI2	NMI Mask 2	8	GD510A	R/W	A9	3C5
	-reserved-	0	–	–	AA	3C5
SWITCH	State Switch Control	8	GD510A/GD520A‡	R/W	A7	3C5
CACHE	NMI Data Cache‡‡	4x24	GD510A	R	AE	3C5
NSTAT1	NMI Status 1	8	GD510A	R	AB	3C5
NSTAT2	NMI Status 2	8	GD510A	R	AC	3C5
256 CPC	256 Color Page Control	4	GD520A	R/W	AD	3C5
STATE	Active Adapter State	7	GD510A/GD520A‡	R/W	AF	3C5
SCR0-F	Scratch Register 0-F	8	GD510A	R/W	B0-BF	3C5
	-reserved-	0	–	–	C0-FF	3C5

‡ Physical readback chip is underlined for split/duplicated registers
‡‡ NMI Data Cache consists of four 24-bit words.

6.5 Extension Bit Summary

Bit	GAVER (SERX 8E)	SCVER (SERX 8F)	CR7F (SERX 7F)
7	GD510A Version MSB	GD520A Version MSB	CRTC Register C bit 7 XOR 1
6	GD510A Version	GD520A Version	CRTC Register C bit 6 XOR 1
5	GD510A Version	GD520A Version	CRTC Register C bit 5 XOR 0
4	GD510A Version	GD520A Version	CRTC Register C bit 4 XOR 0
3	GD510A Version	GD520A Version	CRTC Register C bit 3 XOR 1
2	GD510A Version	GD520A Version	CRTC Register C bit 2 XOR 0
1	GD510A Version	GD520A Version	CRTC Register C bit 1 XOR 1
0	GD510A Version LSB	GD520A Version LSB	CRTC Register C bit 0 XOR 0

Bit	SR6 (SERX 06)	ARX (SERX 83)	Timing Controls (SERX 85)
7	0	0 = Index / 1 = Data	CGA, HGC VRTC Polarity Reversal
6	0	–	CGA, HGC HRTC Polarity Reversal
5	0	Video Enable	Force CGA Text Display Enable
4	0	Attribute Index	Scan Doubling Enable 6845
3	0	Attribute Index	Analog Monitor
2	0	Attribute Index	Reserved (set this bit to 0)
1	0	Attribute Index	Character Width: 0 0 1 1
0	Extensions Write Enable	Attribute Index	Character Width: 0 1 0 1

Character Width: 0 1 0 1
- Reserved
- 6
- 8
- 9

Note: Write 0CAH to Extensions Control port to enable writes to Extension Registers (all other values ignored).
Write 0ACH to Extensions Control port to disable writes to Extension Registers (all other values ignored).

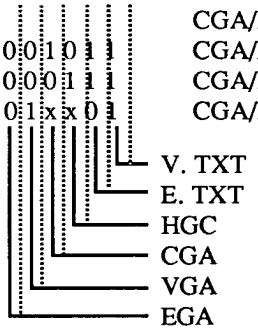
Bit	Bandwidth Control (SERX 86)
7	–
6	–
5	6845 BWI: 0 0 1 1
4	6845 BW0: 0 1 0 1
3	Skip CRT
2	Bandwidth 2: 0 0 0 0 1 1 1 1
1	Bandwidth 1: 0 0 1 1 0 0 1 1
0	Bandwidth 0: 0 1 0 1 0 1 0 1

- 1:1 All 40 column text modes and all graphics modes
- reserved
- 1:7 (HGC text + CGA high-res text) or 3:2 (HGC graphics + CGA graphics + CGA low-res text)
- 1:4 (HGC text + CGA high-res text) or 3:2 (HGC graphics + CGA graphics + CGA low-res text)

Bandwidth 0: 0 1 0 1 0 1 0 1
- Reserved
- Reserved
- 3:1 (7MHz, Monochrome graphics)
- 1:4 (24 MHz / 32 MHz 9 dot)
- 1:7 (32 MHz 8 dot)
- 1:2 (16MHz 6 dot)
- 1:1 (16MHz 8/9 dot)
- Use SR1 bit 1 (0 = 1:4, 1 = 3:2)

6.5 Extension Bit Summary (cont'd)

Bit	STATE (SERX AF)	FONTC (SERX 89)	Misc. Control 2 (SERX 87)
7	State Change Occurred	–	ROM Disabled
6	Previous Adapter State 2: 0 0 1 0 1 1	–	ARMVSE
5	Previous Adapter State 1: 0 0 0 1 1 1	Reserved	8 Bit Video
4	Previous Adapter State 0: 0 1 x x 0 1	Reserved	AR14 Bypass*
3	–	CGA/HGC Font Position	Palette Bypass
2	Current Adapter State 2: 0 0 1 0 1 1	CGA/HGC Font Number bit 2	PS2 Mon
1	Current Adapter State 1: 0 0 0 1 1 1	CGA/HGC Font Number bit 1	Switch Source
0	Current Adapter State 0: 0 1 x x 0 1	CGA/HGC Font Number bit 0	Enable VGA Sparce



Bit	WRC (SERX 84)	Registers Protected
7	Disable Write of Non-6845 CMGA Registers	Mode, Config, Color
6	Disable Write of Non-6845 Regs Common to EGA/CGA/HGC	Set/Clear Light Pen
5	Disable Write of 6845 Display Timing Registers	R1, R6, R9-B
4	Disable Write of 6845 Monitor Timing Registers	R0, R2-5, R7-8
3	Disable Write of Non-CRTC EGA Registers	GPOS1-2, GR0-8, SR0-4, AR0-13, ARX b5, FC, Misc b0-1,4-5
2	Disable Write of Registers Common to CRTC & 6845	CRC-CRF
1	Disable Write of CRTC Display Timing Registers	CR1, CR8-B, CR12-14, CR18, CR7 b1,4
0	Disable Write of CRTC Monitor Timing Registers	CR0, CR2-6, CR10-11, CR15-17, CR7 b0, 2, 3, Misc b2-3, 6-7

Note: Setting WRC (Write Control) register to FF(H) write protects all registers except index and extension registers. Index fields of index registers are always write enabled to allow register readback any time. Extension registers are separately write protected by the Extensions Control register (EXTC).

(*) Denotes negative true bit.

Bit	Cursor Attr. (SERX A5)
7	Pointer Enable
6	Caret Enable
5	Caret Color (0 = Black / 1 = White)
4	Caret Mode (0 = Replace / 1 = Invert)
3	Cursor Mode (0 = Replace / 1 = Invert)
2	Caret / Cursor Blink Rate (0 = fast / 1 = slow)
1	Caret Blink Disable
0	Cursor Blink Disable

ISS (SERX A6)

Bit positions will be gated to switch status (3C2 Bit 4) when MC2 [1] is set. Bit select will be controlled by clock select [4:2].

6.5 Extension Bit Summary (cont'd)

Bit	Clock Select (SERX A4)		
7	6845 CLK Sel 2:	0 0 0 0 1 1 1 1	
6	6845 CLK Sel 1:	0 0 1 1 0 0 1 1	
5	6845 CLK Sel 0:	0 1 0 1 0 1 0 1	
4	CLK Sel 2:	0 0 0 0 1 1 1 1	Reserved
3	CLK Sel 1:	0 0 1 1 0 0 1 1	39 MHz
2	CLK Sel 0:	0 1 0 1 0 1 0 1	28.332MHz
1	–		25.172MHz
0	–		32.514MHz
			25.172MHz
			16.257MHz
			14.318MHz

Bit	256 Color Page Control (SERX AD)
7	CRTC AM 13
6	CRTC AM 12
5	CPA 15
4	CPA 14
3	–
2	–
1	–
0	–

Note: Clock Select bit-2 is the same as Misc Output register bit-2
Clock Select bit-3 is the same as Misc Output register bit-3

Bit	HSS (SERX 88)
7	–
6	--
5	--
4	–
3	HSP Skew 3
2	HSP Skew 2
1	HSP Skew 1
0	HSP Skew 0

Note: Max skew is 11.
Any higher value will
give a skew of 11.

Misc. Control 1 (SERX 80)
CGA/HGC HSS Bypass
En. State Change at Frame Boundary
En. Sync Reset at Line End
En. All-to-CPU
Force VGA Cursor
H. All-to-CPU Disable
Force EGA Light Pen Operation
All GD520A Reg. Readback

Notes:

7. ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Ambient Temperature Under Bias. .....0° C to 70° C
Storage Temperature. .....-65° C to 150° C
Voltage On Any Pin With Respect To Ground.....GND-0.5 to VCC+0.5 Volts
Power Dissipation (Per Chip).....0.300 Watt
Power Supply Voltage. .....7 Volts
Injection Current (Latch-up). .....25 mA

Note: Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

7.2 CL–GD510A / 520A D.C. Characteristics

(VCC=5V±5%, TA=0° to 70° C, unless otherwise specified)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
VCC	Power Supply Voltage	4.75	5.25	V	Normal Operations
VIL	Input Low Voltage	-0.5	0.8	V	
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VOL	Output Low Voltage		0.4	V	IOL = 2mA†
VOH	Output High Voltage	2.4		V	IOH = 400µA
ICC	Operating Supply Current		50	mA	@ 33MHz, 5V nominal
IL	Input Leakage	-10	10	µA	0 < VIN < VCC
CIN	Input Capacitance		10	pF	
COUT	Output Capacitance		10	pF	
VCC	Power Supply Voltage	4.75	5.25	V	Normal Operations
VIL	Input Low Voltage	-0.5	0.8	V	
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VOL	Output Low Voltage		0.4	V	IOL = 2mA††
VOH	Output High Voltage	2.4		V	IOH = 400µA
ICC	Operating Supply Current		50	mA	@ 33MHz, 5V nominal
IL	Input Leakage	-10	10	µA	0 < VIN < VCC
CIN	Input Capacitance		10	pF	
COUT	Output Capacitance		10	pF	

†**NOTE:** IOL max for GD510A = 12mA for NMI* (IOCHCK*) @ .4 Vol
= 16mA for NMI* (IOCHCK*) @ .5 Vol

††**NOTE:** IOL max for GD520A = 12mA for CPURDY, CRTINT
= 8mA for DIR / CRDSEL*, WE*, CAS*

7.3 A.C. Characteristics / Timing Information

The following timing information assumes that all outputs will drive one Schottky TTL load in parallel with 50 pF and all inputs are at TTL level. The MIN and MAX timings are those conforming to the operating ranges of a power supply voltage of 5V ± 5% and an ambient temparature of 0° C to 70° C.

Index of Timing Information

DRAM Memory Performance Table

DRAM ACCESS TIME (ns)	DOT CLOCK FREQ. (MHz)	MEMORY BAN CPU:CRT CYCLE INTERLEAVE
80	25	
100	20	1:1, 1:2
120	16	
150	13	
80	33	
100	30	3:2‡
120	25	
150	20	
80	37	
100	33	1:4 8 dot character clock
120	25	
150	20	
80	FcMax†	
100	FcMax†	1:7 8 dot character clock
120	30	1:4 9 dot character clock
150	26	

† FcMax = Maximum CLKIN frequency = 1/Tc = 40MHz

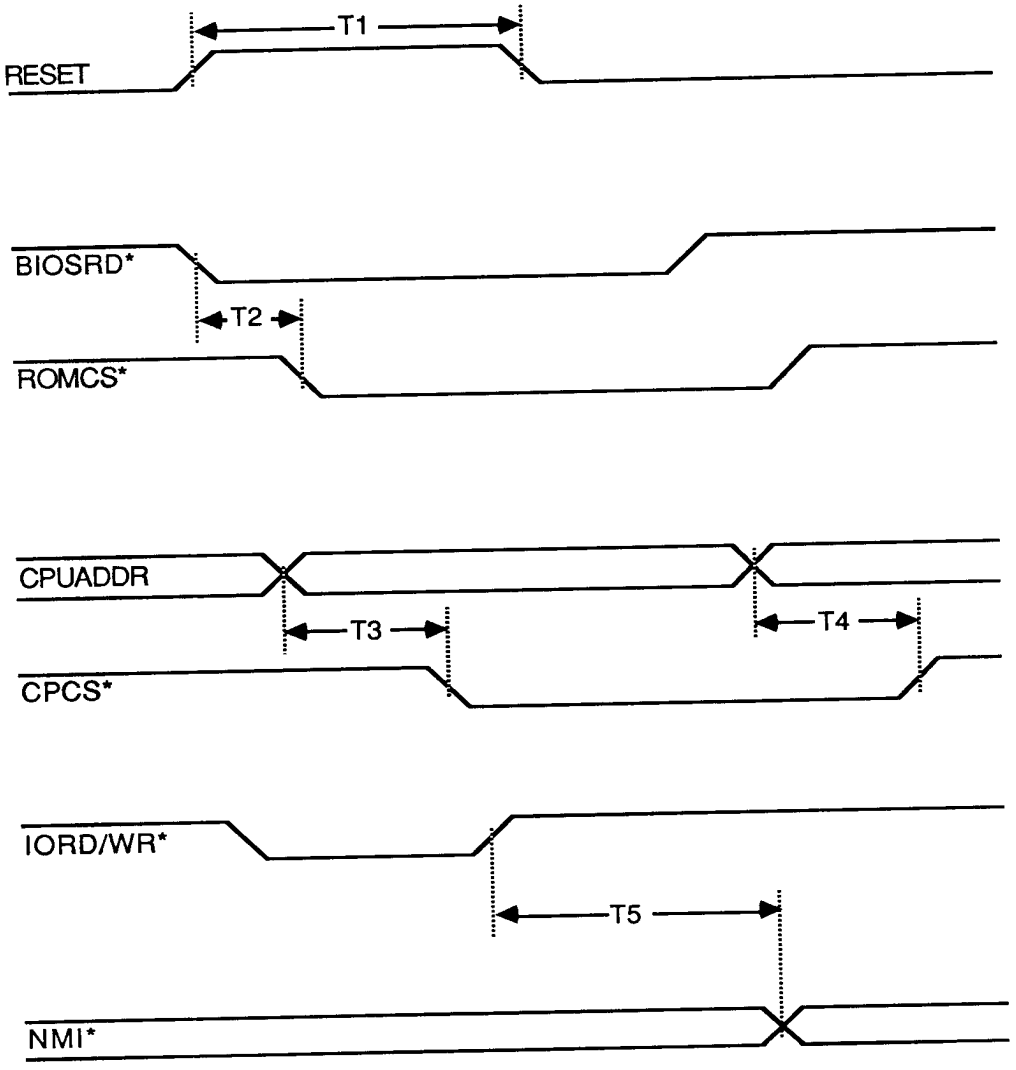
‡ Used when Dot Clock = Clock in/2

Note: 1 character clock is 8 dot clocks in graphics modes and either 8 or 9 dot clocks in text modes, depending upon the character width used.

I/O Bus Timing Table

SYMBOL	PARAMETER	MIN	MAX	UNITS
T1	RESET Pulse Width	100		ns
T2	BIOSRD* to ROMCS* Delay		25	ns
T3	CPCS* Low Delay from CPUADDR		25	ns
T4	CPCS* High Delay from CPUADDR		50	ns
T5	NMI* Delay from IORD/WR*		50	n s

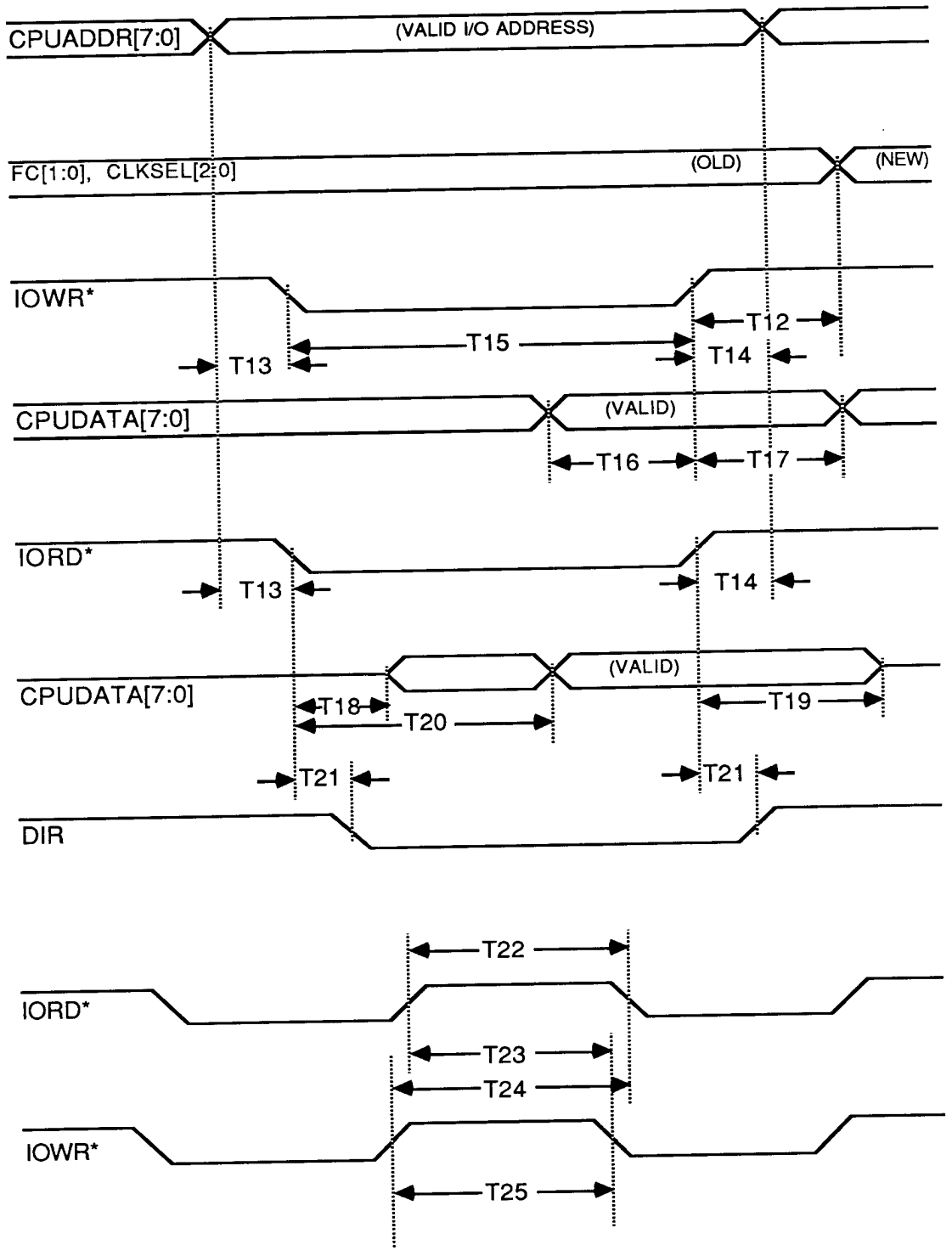
I/O Bus Timing:



I/O Port Timing Table

SYMBOL	PARAMETER	MIN	MAX	UNITS
T12	IOWR* To I/O Port (FC[1:0], CLKSEL[2:0]) Output Delay		30	ns
T13	CPUADDR[7:0] Setup to IOWR* Low	0		ns
T14	CPUADDR[7:0] Hold Time from IOWR* or IORD* High	5		ns
T15	IORD*, IOWR* Low Pulse Width	120		ns
T16	Data Setup Time to IOWR* High	100		ns
T17	Data Hold Time to IOWR* High	5		ns
T18	IORD* Low to CPUDATA[7:0] Driven Delay		15	ns
T19	IORD* High to CPUDATA[7:0] Tri-State Delay		15	ns
T20	IORD* Low to CPUDATA[7:0] Valid Delay		80	ns
T21	DIR Delay		25	ns
T22	IORD* High to IORD* Low	100		ns
T23	IORD* High to IOWR* Low	100		ns
T24	IOWR* High to IORD* Low	100		ns
T25	IOWR* High to IOWR* Low	100		ns

I/O Port Timing:



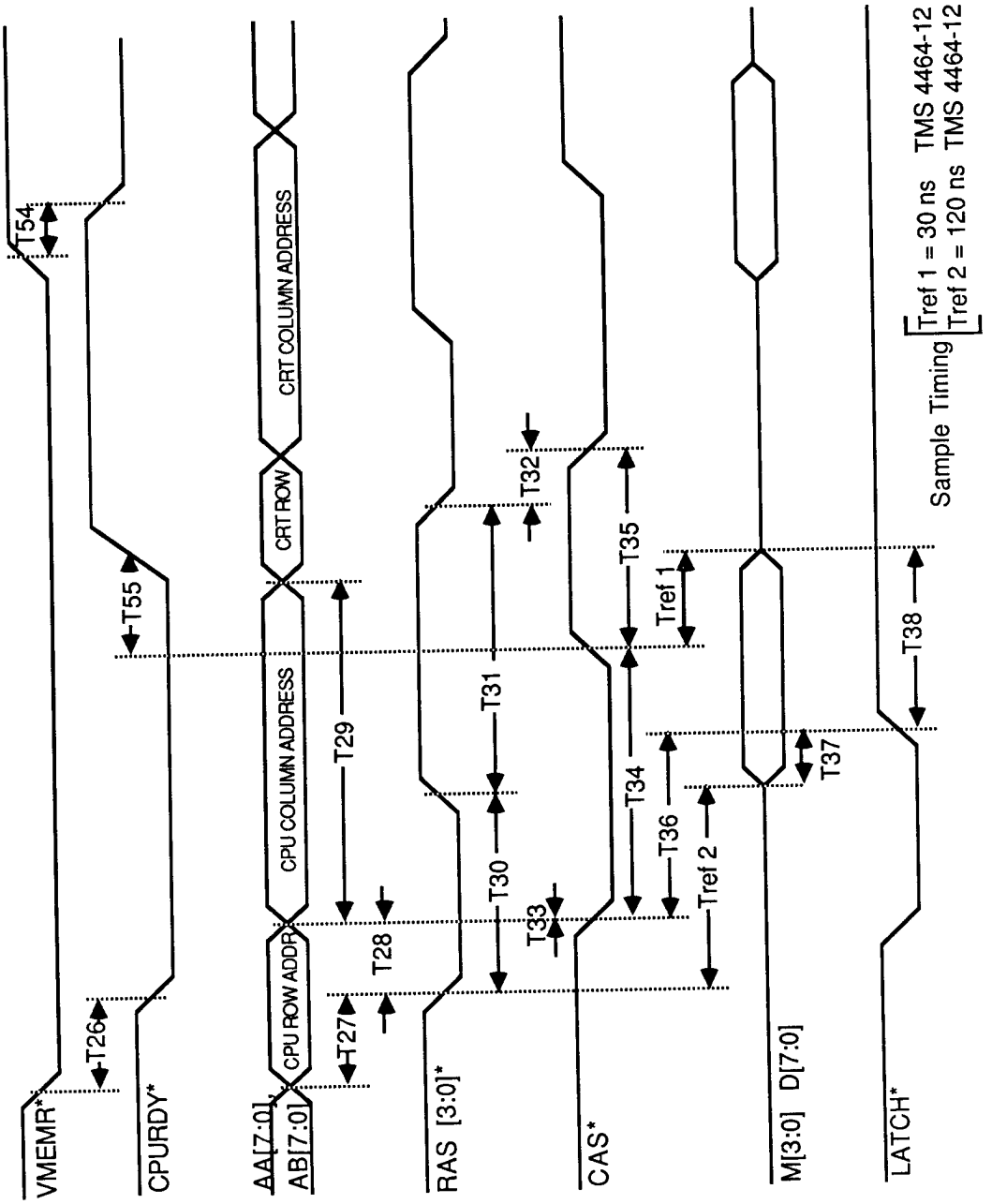
DRAM Read Timing Table

SYMBOL	PARAMETER	X:Y - Z † 1:4 - 9	1:4 - 8	1:7 - 8	3:2 - 8	1:2 - 6	1:1 - 8	1:1 - 9	Min/Max
Tc	CLKIN Cycle Time (100 ns DRAM)	25	30	25	30	50	50	50	Typ
T26	CPURDY Low from VMEMR*	15	15	15	15	15	15	15	Typ
T27	Row Address Setup Time	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	Typ
T28	Row Address Hold Time	0.5 Tc	0.5 Tc	0.5 Tc	0.5 Tc	15	15	15	Typ
T29	Column Address Hold Time	4 Tc	3 Tc	4 Tc	3 Tc	1.5 Tc	1.5 Tc	1.5 Tc	Typ
T30	RAS* Low Time	4 Tc	3 Tc	4 Tc	3 Tc	2 Tc	2 Tc	2 Tc	Typ
T31	RAS* Precharge	3 Tc	3 Tc	3 Tc	3 Tc	2 Tc	2 Tc	2 Tc	Typ
T32	RAS* to CAS* Delay	1 Tc	1 Tc	1 Tc	1 Tc	0.5 Tc	0.5 Tc	0.5 Tc	Typ
T33	Column Address Setup Time	5	5	5	5	5	5	5	Typ
T34	CAS* Low Time	5 Tc	4 Tc	5 Tc	4 Tc	2.5 Tc	2.5 Tc	2.5 Tc	Typ
T35	CAS* Precharge	2 Tc	2 Tc	2 Tc	2 Tc	1.5 Tc	1.5 Tc	1.5 Tc	Typ
T36	Data Sample From CAS*	3.5 Tc	3 Tc	3.5 Tc	3 Tc	1.5 Tc	1.5 Tc	1Tc	Typ
T37	Valid Data Hold Time (to LATCH*)	0	0	0	0	0	0	0	Typ
T38	Valid Data Hold Time (to LATCH*)	40	40	40	40	40	40	40	Typ
T54	VMEMR* Inactive to CPURDY* Tristate	15	15	15	15	15	15	15	Typ
T55	CPU Read Cycle End to CPURDY* Inactive	1 Tc	1 Tc	1 Tc	1 Tc	1 Tc	1 Tc	1 Tc	Typ

† **X:Y - Z** (X = CPU Cycles, Y = CRT Cycles, Z = Dots / Character)

NOTE: All times are in nanoseconds (ns) unless otherwise noted.
50 pf Load capacitance is assumed.
GD510A latches the video memory data on the rising edge of LATCH*. That is when the data is actually sampled (See T36, T37 and T38).

DRAM Read Timing



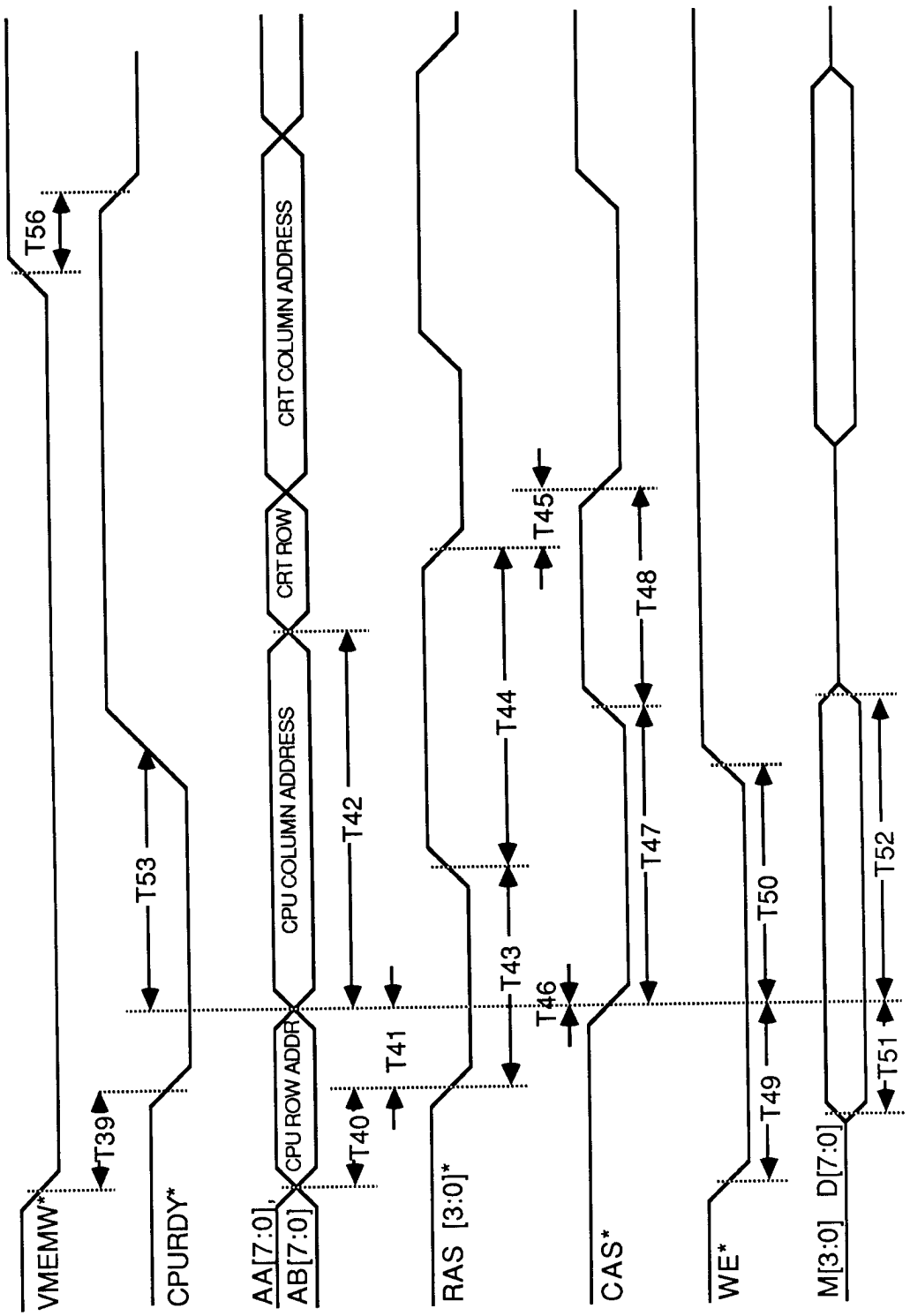
DRAM Write Timing Table

SYMBOL	PARAMETER	X:Y - Z † 1:4 - 9	1:4 - 8	1:7 - 8	3:2 - 8	1:2 - 6	1:1 - 8	1:1 - 9	Min/Max
Tc	CLKIN Cycle Time	25	30	25	30	50	50	50	Typ
T39	CPURDY Low from VMEMW*	15	15	15	15	15	15	15	Typ
T40	Row Address Setup Time	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	Typ
T41	Row Address Hold Time	0.5 Tc	0.5 Tc	0.5 Tc	0.5 Tc	15	15	15	Typ
T42	Column Address Hold Time	4 Tc	3 Tc	4 Tc	3 Tc	1.5 Tc	1.5 Tc	1.5 Tc	Typ
T43	RAS* Low Time	4 Tc	3 Tc	4 Tc	3 Tc	2 Tc	2 Tc	2 Tc	Typ
T44	RAS* Precharge	3 Tc	3 Tc	3 Tc	3 Tc	2 Tc	2 Tc	2 Tc	Typ
T45	RAS* to CAS* Delay	1 Tc	1 Tc	1 Tc	1 Tc	0.5 Tc	0.5 Tc	0.5 Tc	Typ
T46	Address Setup to CAS*	5	5	5	5	5	5	5	Typ
T47	CAS* Low Time	5 Tc	4 Tc	5 Tc	4 Tc	2.5 Tc	2.5 Tc	2.5 Tc	Typ
T48	CAS* Precharge	2 Tc	2 Tc	2 Tc	2 Tc	1.5 Tc	1.5 Tc	1.5 Tc	Typ
T49	WE* Setup to CAS*	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	1 Tc	1 Tc	1 Tc	Typ
T50	WE* Hold from CAS* (=T47)	5 Tc	4 Tc	5 Tc	4 Tc	2.5 Tc	2.5 Tc	2.5 Tc	Typ
T51	Data Setup to CAS*	5	5	5	5	10	10	10	Typ
T52	Data Hold from CAS* (=T47)	5Tc	4Tc	5 Tc	4Tc	2.5 Tc	2.5 Tc	2.5	Typ
T53	CPU Write Cycle End (=CAS* Low) to CPURDY* Inactive	2 Tc	2 Tc	2 Tc	2 Tc	2 Tc	2 Tc	2 Tc	Typ
T56	VMEMW* Inactive to CPURDY* Tristate	15	15	15	15	15	15	15	Typ

† **X:Y - Z** (X = CPU Cycles, Y = CRT Cycles, Z = Dots / Character)

NOTE: All times are in nanoseconds (ns) unless otherwise noted.

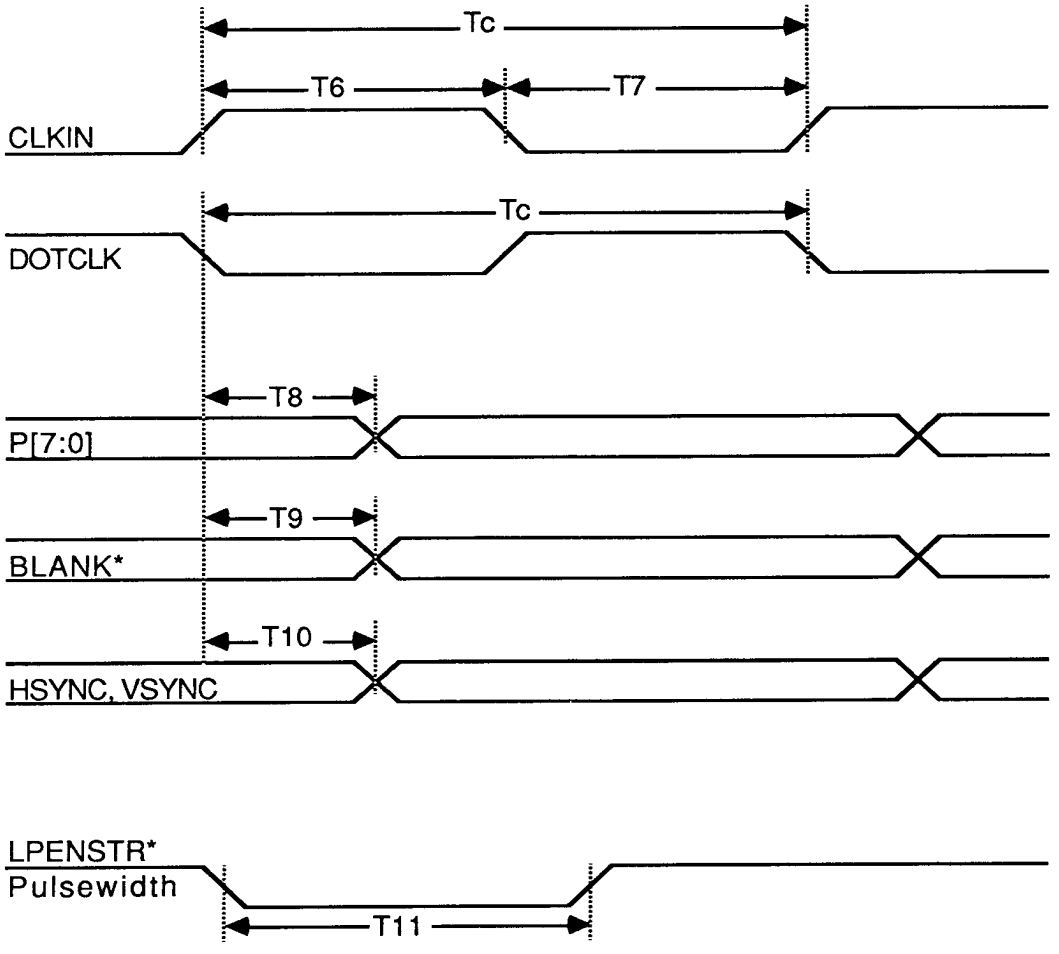
DRAM Write Timing



Video Timing Table

SYMBOL	PARAMETER	MIN	MAX	UNITS
Tc	CLKIN / DOTCLK Cycle	30		ns
T6	CLKIN High (measured @ 2.0v)	[Tc/2] - 5%		
T7	CLKIN Low (measured @ 0.4v)	[Tc/2] - 5%		
T8	P[7:0] Delay		15	ns
T9	BLANK* Delay		15	ns
T10	VSYNC, HSYNC Delay		15	ns
T11	LPENSTR* Pulse Width	160		ns

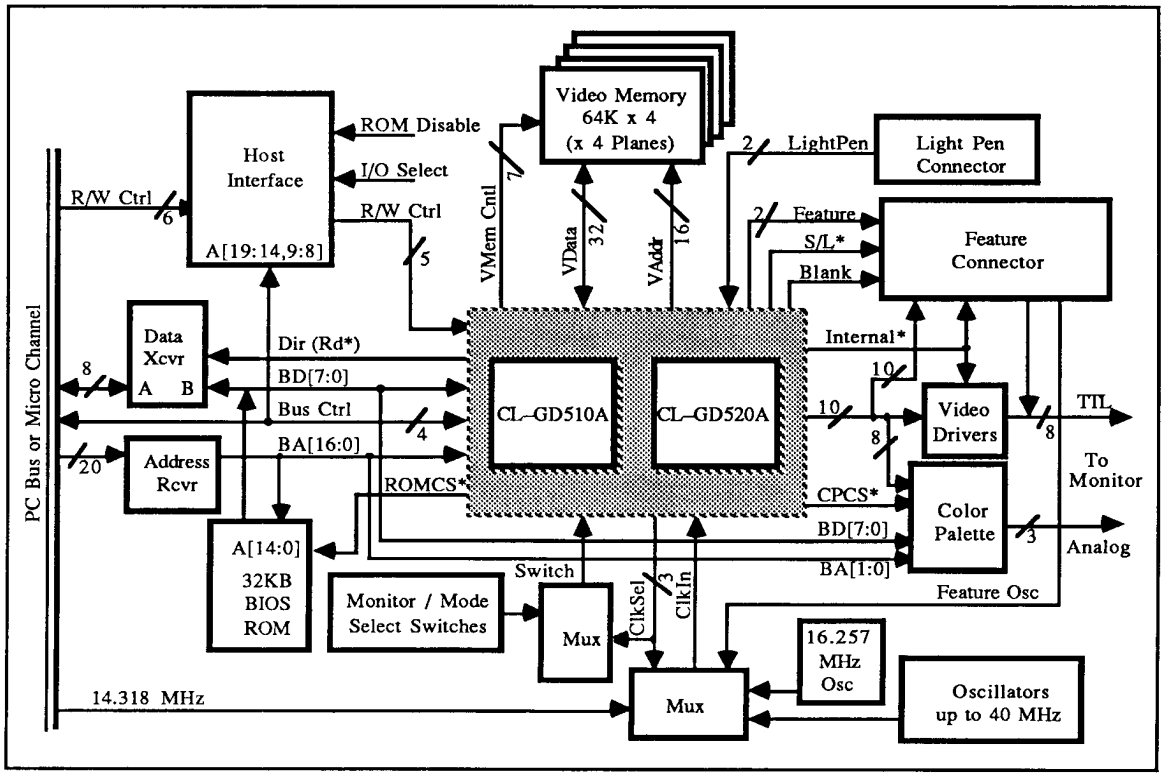
Video Timing:



Notes

8. TYPICAL APPLICATION

8.1 System Block Diagram

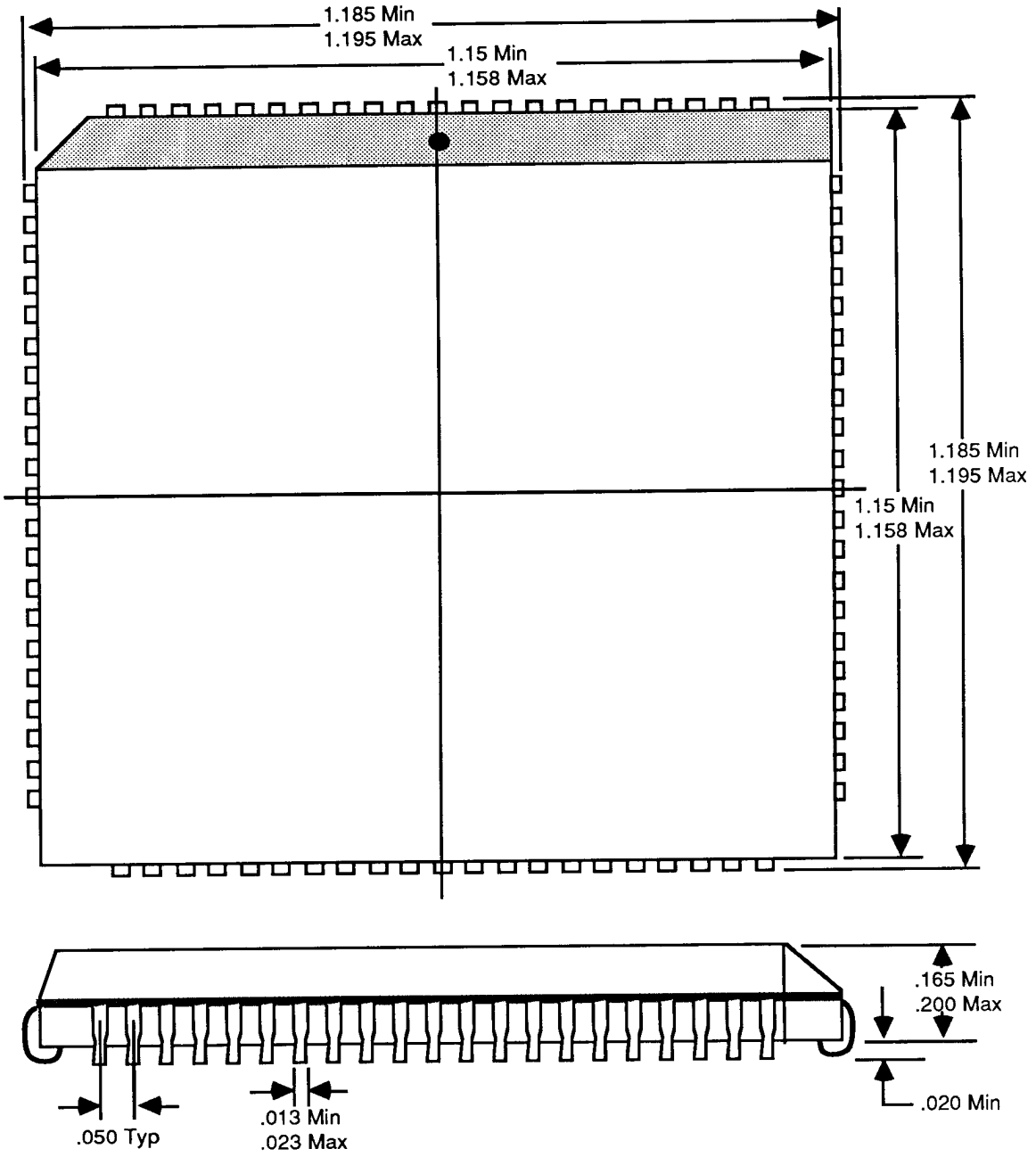


8.2 Parts List for VGA / EGA System

- CL–GD510A Graphics / Attributes chip
- CL–GD520A Sequencer / CRT Controller chip
- BIOS (16 KByte or 32 KByte ROM)
- Glue logic (PLD, Mux and Receiver, or one Gate Array)
- Video driver and PC Bus Data Transceiver (2 LSTTL parts)
- 256 KBytes Dynamic RAM (8 DRAM parts)
- Crystal(s) (16 MHz - 40 MHz)
- RAMDAC (for VGA only)

9. PACKAGE INFORMATION

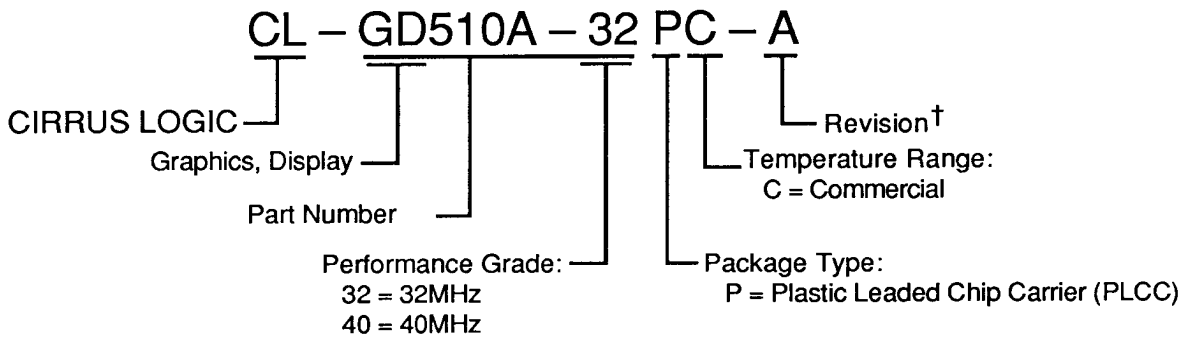
9.1 84-Pin PLCC



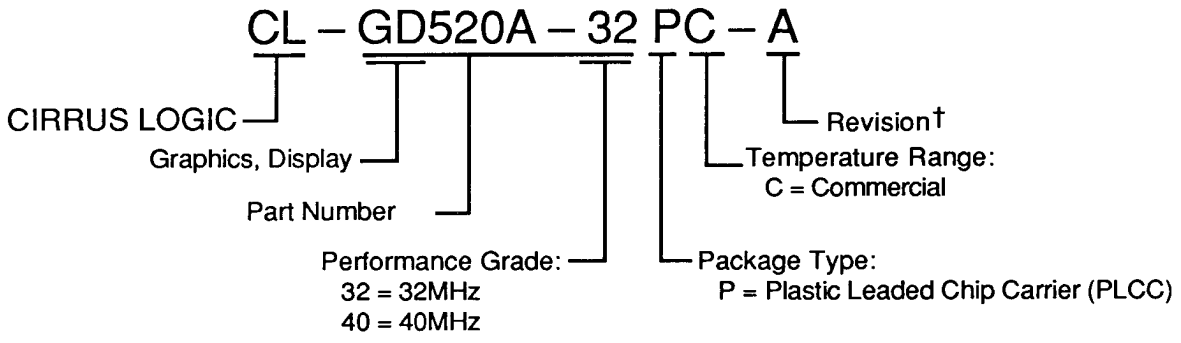
NOTE: All dimensions are in inches and are nominal unless otherwise stated.

10. ORDERING INFORMATION

10.1 Numbering Guide – Graphics / Attributes Chip:



10.2 Numbering Guide – Sequencer / CRT Controller:



† Contact CIRRUS LOGIC for up-to-date information on revisions.

Notes

ABOUT CIRRUS LOGIC

CIRRUS LOGIC makes proprietary VLSI circuits for peripheral controller applications. Current product lines include: data communications circuits, disk drive controllers, and graphics and display controllers.

A family of products are offered in each line. Each product provides a VLSI solution to a current system design requirement. You will find CIRRUS LOGIC to be different from other semiconductor companies in the way we respond to your needs, with VLSI products that are specific to your applications.

The CIRRUS LOGIC formula combines state-of-the-art IC design automation technology with an understanding of system requirements that is uncommon in the semiconductor industry. The result is better VLSI products, with richer features, brought to market in a time frame that allows you to lead your field. Our products help you compete.

Our internally developed, proprietary S/LA™ IC design automation technology is unique in the industry.† It gives us unparalleled capability in bringing highly complex, high performance logic circuits to market in less than half the time of other semiconductor companies. But design technology is only half of the story. It is our knowledge of system requirements, and our commitment to meeting the needs of the system design engineer that makes CIRRUS LOGIC a different kind of semiconductor company. CIRRUS LOGIC offers system level solutions in silicon.

So look at our products. Talk to our systems and applications specialists. Consider the system-specific solutions that we offer, and consider how your products can benefit from the capabilities of a new kind of semiconductor company ... CIRRUS LOGIC.

† U.S. Patent No. 4,293,783

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