SIEMENS

3.3V 2M x 64/72-Bit 1 BANK SDRAM Module   HYS64/72V2200GU-8
3.3V 4M x 64/72-Bit 2 BANK SDRAM Module   HYS64/72V4220GU-8

PC100-168 pin unbuffered DIMM Modules

Advanced Information

- 168 Pin PC100-compatible unbuffered 8 Byte Dual-In-Line SDRAM Modules

- 1 bank 2M x 64, 2M x 72 and 2 bank 4M x 64, 4M x 72 organisation

- Optimized for byte-write non-parity or ECC applications

- JEDEC standard Synchronous DRAMs (SDRAM)

- Fully PC board layout compatible to INTELś Rev. 1.0 module specification

- SDRAM Performance:

		PC100	Units
f_{CK}	Clock frequency (max.)	100	MHz
t_{AC}	Clock access time $\overline{CAS}$ latency = 2 & 3	6	ns

- Supported Latencies at 100 Mhz operation:

CL	tRCD	tRP	tRC	
3	2	2	8	CLK
2	2	2	7	CLK

- Single +3.3V($\pm$ 0.3V) power supply

- Programmable $\overline{CAS}$ Latency, Burst Length and Wrap Sequence (Sequential & Interleave)

- Auto Refresh (CBR) and Self Refresh

- Decoupling capacitors mounted on substrate

- All inputs, outputs are LVTTL compatible

- Serial Presence Detect with E^2PROM

- Utilizes 2M x 8 SDRAMs in TSOPII-44 packages

- 4096 refresh cycles every 64 ms

- Gold contact pad

- Card Size: 133,35 mm x 31.75 mm x 4,00 mm

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The HYS64(72)2200 and HYS64(72)4220 are industry standard 168-pin 8-byte Dual in-line Memory Modules (DIMMs) which are organised as 2M x 64, 2M x 72 in 1 bank and 4M x 64 and 4M x 72 in two banks high speed memory arrays designed with Synchronous DRAMs (SDRAMs) (with die revisions „B"& „C") for non-parity and ECC applications. The DIMMs use -8 speed sort 2M x 8 SDRAM devices in TSOP44 packages to meet the PC100 requirement. Decoupling capacitors are mounted on the PC board. The PC board design is according to INTELs PC 100 module specification.

The DIMMs have a serial presence detect, implemented with a serial E ^{2}PROM using the two pin I^{2}C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user.

All SIEMENS 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133,35 mm long footprint, with 1,25"(31,75 mm) height.

Ordering Information

Type	Ordering Code	Package	Descriptions	Module Height
HYS 64V2200GU-8	PC100-222-620	L-DIM-168-29	100 Mhz 2M x 64 1 bank SDRAM module	1,25"
HYS 72V2200GU-8	PC100-222-620	L-DIM-168-29	100 MHz 2M x 72 1 bank SDRAM module	1,25"
HYS 64V4220GU-8	PC100-222-620	L-DIM-168-29	100 Mhz 4M x 64 2 bank SDRAM module	1,25"
HYS 72V4220GU-8	PC100-222-620	L-DIM-168-29	100 Mhz 4M x 72 2 bank SDRAM module	1,25"

Pin Names

A0-A10	Address Inputs(RA0 ~ RA10 / CA0 ~ CA8)
BA	Bank Address
DQ0 - DQ63	Data Input/Output
CB0-CB7	Check Bits (x72 organisation only)
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read / Write Input
$\overline{CKE0}$, $\overline{CKE1}$	Clock Enable
CLK0 - CLK3	Clock Input
DQMB0 - DQMB7	Data Mask
$\overline{CS0}$ - $\overline{CS3}$	Chip Select
Vcc	Power (+3.3 Volt)
Vss	Ground
SCL	Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
N.C.	No Connection

Address Format:

	Part Number	Rows	Columns	Banks	Refresh	Period	Interval
2M x 64	HYS 64V2200GU	11	9	1	4k	64 ms	15,6 µs
2M x 72	HYS 72V2200GU	11	9	1	4k	64 ms	15,6 µs
4M x 64	HYS 64V4220GU	11	9	1	4k	64 ms	15,6 µs
4M x 72	HYS 72V4220GU	11	9	1	4k	64 ms	15,6 µs

Pin Configuration

PIN #	Symbol	PIN #	Symbol		PIN #	Symbol	PIN #	Symbol
1	VSS	43	VSS		85	VSS	127	VSS
2	DQ0	44	DU		86	DQ32	128	CKE0
3	DQ1	45	CS2		87	DQ33	129	CS3
4	DQ2	46	DQMB2		88	DQ34	130	DQMB6
5	DQ3	47	DQMB3		89	DQ35	131	DQMB7
6	VCC	48	DU		90	VCC	132	NC
7	DQ4	49	VCC		91	DQ36	133	VCC
8	DQ5	50	NC		92	DQ37	134	NC
9	DQ6	51	NC		93	DQ38	135	NC
10	DQ7	52	NC (CB2)		94	DQ39	136	CB6
11	DQ8	53	NC (CB3)		95	DQ40	137	CB7
12	VSS	54	VSS		96	VSS	138	VSS
13	DQ9	55	DQ16		97	DQ41	139	DQ48
14	DQ10	56	DQ17		98	DQ42	140	DQ49
15	DQ11	57	DQ18		99	DQ43	141	DQ50
16	DQ12	58	DQ19		100	DQ44	142	DQ51
17	DQ13	59	VCC		101	DQ45	143	VCC
18	VCC	60	DQ20		102	VCC	144	DQ52
19	DQ14	61	NC		103	DQ46	145	NC
20	DQ15	62	DU		104	DQ47	146	DU
21	NC (CB0)	63	CKE1		105	NC (CB4)	147	NC
22	NC (CB1)	64	VSS		106	NC (CB5)	148	VSS
23	VSS	65	DQ21		107	VSS	149	DQ53
24	NC	66	DQ22		108	NC	150	DQ54
25	NC	67	DQ23		109	NC	151	DQ55
26	VCC	68	VSS		110	VCC	152	VSS
27	WE	69	DQ24		111	CAS	153	DQ56
28	DQMB0	70	DQ25		112	DQMB4	154	DQ57
29	DQMB1	71	DQ26		113	DQMB5	155	DQ58
30	CS0	72	DQ27		114	CS1	156	DQ59
31	DU	73	VCC		115	RAS	157	VCC
32	VSS	74	DQ28		116	VSS	158	DQ60
33	A0	75	DQ29		117	A1	159	DQ61
34	A2	76	DQ30		118	A3	160	DQ62
35	A4	77	DQ31		119	A5	161	DQ63
36	A6	78	VSS		120	A7	162	VSS
37	A8	79	CLK2		121	A9	163	CLK3
38	A10	80	NC		122	BA	164	NC
39	NC	81	WP		123	NC	165	SA0
40	VCC	82	SDA		124	VCC	166	SA1
41	VCC	83	SCL		125	CLK1	167	SA2
42	CLK0	84	VCC		126	NC	168	VCC

Note : Pinnames in brackets are for the x72 ECC versions

WE

CS0

DQMB0 — DQM, DQ(7:0) — DQ0-DQ7 — CS WE — D0

DQMB1 — DQM, DQ(15:8) — DQ0-DQ7 — CS WE — D1

CB(7:0) — DQ0-DQ7 — DQM — CS WE — D8

$\overline{CS2}$

DQMB2 — DQM, DQ(23:16) — DQ0-DQ7 — CS WE — D2

DQMB3 — DQM, DQ(31:24) — DQ0-DQ7 — CS WE — D3

DQMB4 — DQM, DQ(39:32) — DQ0-DQ7 — CS WE — D4

DQMB5 — DQM, DQ(47:40) — DQ0-DQ7 — CS WE — D5

DQMB6 — DQM, DQ(55:48) — DQ0-DQ7 — CS WE — D6

DQMB7 — DQM, DQ(63:56) — DQ0-DQ7 — CS WE — D7

A0-A10,BA → D0 - D7,(D8)

VCC → D0 - D7,(D8)

C0-C7,(C8)

VSS → D0 - D7,(D8)

$\overline{RAS}$ → D0 - D7,(D8)

$\overline{CAS}$ → D0 - D7,(D8)

CKE0 → D0 - D7,(D8)

Note: D8 is only used in the x72 ECC version

E^2PROM (256wordx8bit)

SA0 — SA0, SA1 — SA1, SA2 — SA2, SCL — SCL, SDA, WP, 47k

Clock Wiring		
	2M x 64	2M x 72
CLK0	4 SDRAM+3.3pF	5 SDRAM
CLK1	Termination	Termination
CLK2	4 SDRAM+3.3pF	4 SDRAM+3.3pF
CLK3	Termination	Termination

Block Diagram for 2M x 64/72 SDRAM DIMM modules (HYS64/72V2200GU)
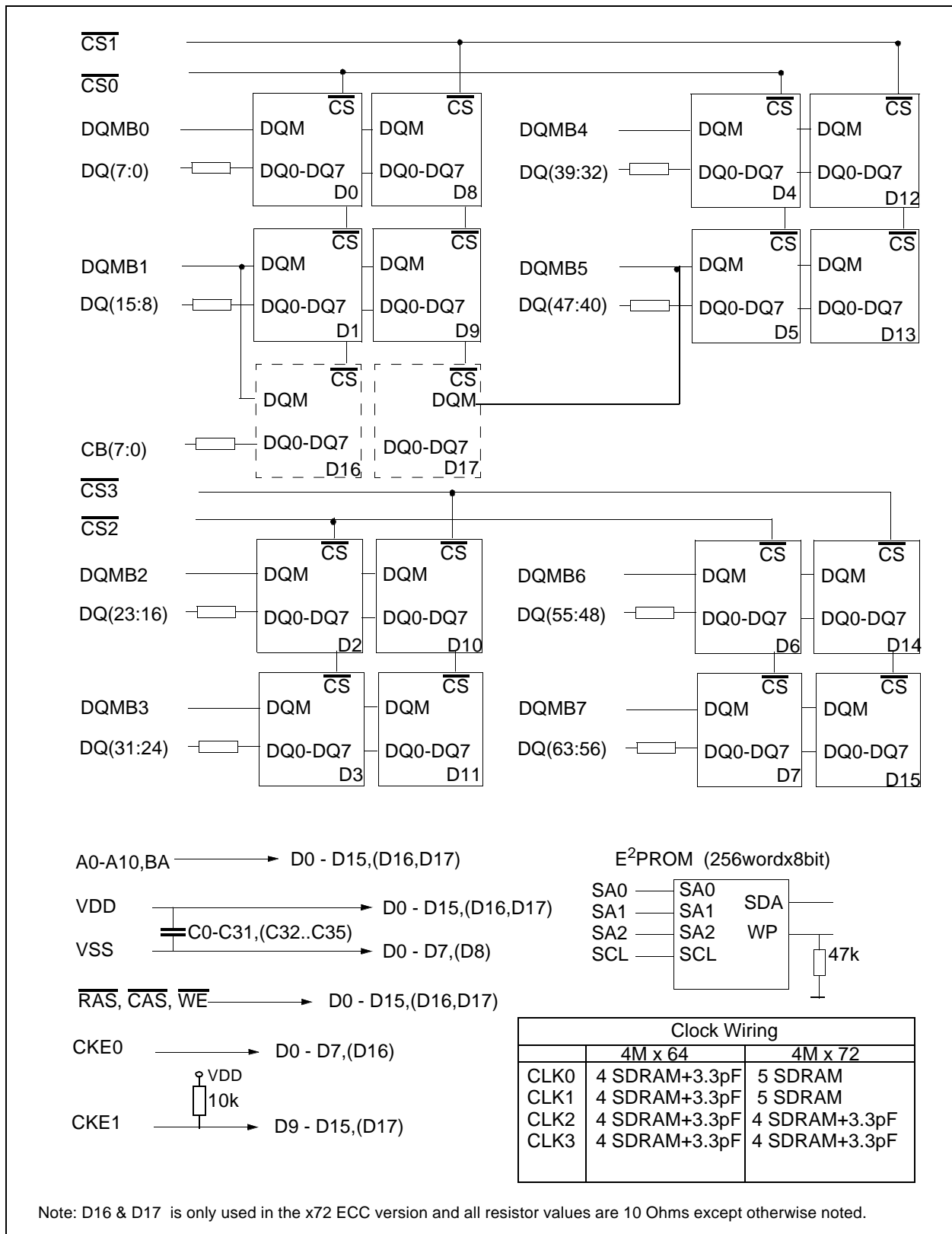
Block Diagram for 4M x 64/72 SDRAM DIMM modules (HYS64/72V4220GU)

The following signals are shown in the diagram:

- $\overline{CS1}$
- $\overline{CS0}$
- DQMB0, DQ(7:0) — D0, D8 / DQMB4, DQ(39:32) — D4, D12
- DQMB1, DQ(15:8) — D1, D9 / DQMB5, DQ(47:40) — D5, D13
- CB(7:0) — D16, D17
- $\overline{CS3}$
- $\overline{CS2}$
- DQMB2, DQ(23:16) — D2, D10 / DQMB6, DQ(55:48) — D6, D14
- DQMB3, DQ(31:24) — D3, D11 / DQMB7, DQ(63:56) — D7, D15

A0-A10,BA → D0 - D15,(D16,D17)

VDD → D0 - D15,(D16,D17)

VSS → D0 - D7,(D8)

C0-C31,(C32..C35)

$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ → D0 - D15,(D16,D17)

CKE0 → D0 - D7,(D16)

VDD 10k

CKE1 → D9 - D15,(D17)

E²PROM (256word x 8bit)

SA0 — SA0   SDA
SA1 — SA1
SA2 — SA2   WP
SCL — SCL   47k

Clock Wiring		
	4M x 64	4M x 72
CLK0	4 SDRAM+3.3pF	5 SDRAM
CLK1	4 SDRAM+3.3pF	5 SDRAM
CLK2	4 SDRAM+3.3pF	4 SDRAM+3.3pF
CLK3	4 SDRAM+3.3pF	4 SDRAM+3.3pF

Note: D16 & D17 is only used in the x72 ECC version and all resistor values are 10 Ohms except otherwise noted.

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD}, V_{DDQ} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input high voltage	V_{IH}	2.0	Vcc+0.3	V
Input low voltage	V_{IL}	− 0.5	0.8	V
Output high voltage (I_{OUT} = − 2.0 mA)	V_{OH}	2.4	–	V
Output low voltage (I_{OUT} = 2.0 mA)	V_{OL}	–	0.4	V
Input leakage current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	− 40	40	µA
Output leakage current (DQ is disabled, 0 V < V_{OUT} < V_{CC})	$I_{O(L)}$	− 40	40	µA

Capacitance

T_A = 0 to 70 °C; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values				Unit
		max. 2Mx64	max. 2Mx72	max. 4Mx64	max. 4Mx72	
Input capacitance (A0 to A10, BA, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{I1}	45	55	80	90	pF
Input capacitance (CS0 -CS3)	C_{I2}	20	25	30	35	pF
Input capacitance (CLK0 - CLK3)	C_{ICL}	22	38	22	38	pF
Input capacitance (CKE0, CKE1)	C_{I3}	22	38	50	55	pF
Input capacitance (DQMB0 - DQMB7)	C_{I4}	13	13	20	20	pF
Input / Output capacitance (DQ0-DQ63,CB0-CB7)	C_{IO}	13	12	20	20	pF
Input Capacitance (SCL,SA0-2)	C_{sc}	8	8	8	8	pF
Input/Output Capacitance	C_{sd}	10	10	10	10	pF

Standby and Refresh Currents (T_a = 0 to 70°C, VCC = 3.3V $\pm$ 0.3V) [1]

Parameter	Symbol	Test Condition	X64	X72		Note
			max.			
Operating Current	Icc1	Burst length = 4, CL=3 trc>=trc(min.), tck>=tck(min.), Io=0 mA 2 bank interleave operation	800	900	mA	1,2
Precharged Standby Current in Power Down Mode	Icc2P	CKE<=VIL(max), tck>=tck(min.)	24	27	mA	
	Icc2PS	CKE<=VIL(max), tck=infinite	16	18	mA	
Precharged Standby Current in Non-power Down Mode	Icc2N	CKE>=VIH(min), tck>=tck (min.), input changed once in 3 cycles	160	180	mA	$\overline{CS}$= High
	Icc2NS	CKE>=VIH(min), tck=infinite, no input change	80	90	mA	
Active Standby Current in Power Down Mode	Icc3P	CKE<=VIL(max), tck>=tck(min.)	24	27	mA	
	Icc3PS	CKE<=VIL(max), tck=infinite	16	18	mA	
Active Standby Current in Non-power Down Mode	Icc3N	CKE>=VIH(min), tck>=tck (min.) input changed one time	200	225	mA	$\overline{CS}$= High
	Icc3NS	CKE=>VIH(min),tck=infinite, no input change	120	135	mA	
Burst Operating Current	Icc4	Burst length = full page, trc = infinite, CL = 3, tck>=tck (min.), Io = 0 mA 2 banks activated	760	855	mA	1,2
Auto (CBR) Refresh Current	Icc5	trc>=trc(min)	720	810	mA	1,2
Self Refresh Current	Icc6	CKE=<0,2V	16	18	mA	1,2

AC Characteristics 3)4)

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values -8		Unit	Note
		min	max		

Clock and Clock Enable

Parameter	Symbol	min	max	Unit	Note
Clock Cycle Time	t_{CK}				
$\overline{CAS}$ Latency = 3		10		ns	
$\overline{CAS}$ Latency = 2		10		ns	
System Frequency	f_{CK}				
$\overline{CAS}$ Latency = 3		–	100	MHz	
$\overline{CAS}$ Latency = 2		–	100	MHz	
Clock Access Time	t_{AC}				4,5)
$\overline{CAS}$ Latency = 3		–	6	ns	
$\overline{CAS}$ Latency = 2		–	6	ns	
Clock High Pulse Width	t_{CH}	3	–	ns	6)
Clock Low Pulse Width	t_{CL}	3	–	ns	6)
Input Setup time	t_{CS}	2	–	ns	7)
Input Hold Time	t_{CH}	1	–	ns	7)
CKE Setup Time (Power down mode)	t_{CKSP}	2.5	–	ns	8)
CKE Setup Time (Self Refresh Exit)	t_{CKSR}	8	–	ns	9)
Transition time (rise and fall)	t_T	1	–	ns	

Common Parameters

Parameter	Symbol	min	max	Unit	Note
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{RCD}	20	–	ns	2 CLK
Cycle Time	t_{RC}	70	120k	ns	7 CLK
Active Command Period	t_{RAS}	45	–	ns	5 CLK
Precharge Time	t_{RP}	20	–	ns	2 CLK
Bank to Bank Delay Time	t_{RRD}	16	–	ns	2 CLK
$\overline{CAS}$ to $\overline{CAS}$ delay time (same bank)	t_{CCD}	1	–	CLK	

Refresh Cycle

Parameter	Symbol	min	max	Unit	Note
Self Refresh Exit Time	t_{SREX}	10	–	ns	9)
Refresh Period (4096 cycles)	t_{REF}	64	–	ms	8)

Parameter	Symbol	Limit Values		Unit	Note
		-8			
		min	**max**		
Read Cycle					
Data Out Hold Time	t_{OH}	3	–	ns	4)
Data Out to Low Impedance Time	t_{LZ}	0	–	ns	
Data Out to High Impedance Time	t_{HZ}	3	9	ns	10)
DQM Data Out Disable Latency	t_{DQZ}	2	–	CLK	
Write Cycle					
Data input to Precharge (write recovery)	t_{DPL}	2	–	CLK	
Data In to Active/refresh	t_{DAL}	5	–	CLK	11)
DQM Write Mask Latency	t_{DQW}	0	–	CLK	

Notes:

1. The specified values are valid when addresses are changed no more than once during tck(min.)
   and when No Operation commands are registered on every rising clock edge during tRC(min).
   Values are shown per module bank.
2. The specified values are valid when data inputs (DQs) are stable during tRC(min.).
3. All AC characteristics are shown for device level.
   An initial pause of 100µs is required after power-up, then a Precharge All Banks command must
   be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can
   begin.
4. AC timing tests have V_{il} = 0.4 V and V_{ih} = 2.4 V with the timing referenced to the 1.4 V crossover
   point. The transition time is measured between V_{ih} and V_{il}. All AC measurements assume t_T=1ns
   with the AC output load circuit show. Specified tac and toh parameters are measured with a 50
   pF only, without any resistive termination and with a input signal of 1V / ns edge rate between
   0.8V and 2.0 V.
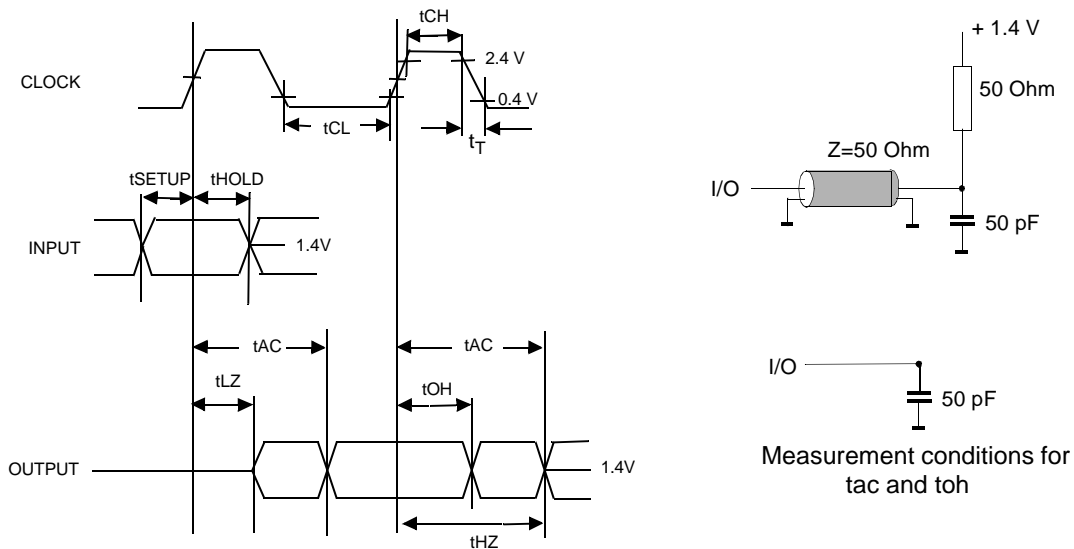

fig.1

5. If clock rising time is longer than 1ns, a time (t_T/2 -0.5) ns has to be added to this parameter.
6. Rated at 1.5 V
7. If t_T is longen than 1 ns, a time (t_T -1) ns has to be added to this parameter.
8. Any time that the refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh
   commands must be given to "wake-up"the device.
9. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after
   CKE returns high. Self Refresh Exit is not complete until a time period equal to tRC is satisfied
   once the Self Refresh Exit command is registered.
10. Referenced to the time which the output achieves the open circuit condition, not to output voltage
    levels.
11. t_{DAL} is equivalent to t_{DPL} + t_{RP}.

A serial presence detect storage device - E ^{2}PROM - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E ^{2}PROM device during module production using a serial presence detect protocol (I ^{2}C synchronous 2-wire bus)

PD-Table:

Byte#	Description	SPD Entry Value	Hex 2Mx64 -8	2Mx72 -8	4Mx64 -8	4Mx72 -8
0	Number of SPD bytes	128	80	80	80	80
1	Total bytes in Serial PD	256	08	08	08	08
2	Memory Type	SDRAM	04	04	04	04
3	Number of Row Addresses (without BS bits)	11	0B	0B	0B	0B
4	Number of Column Addresses (for x8 SDRAM)	9	09	09	09	09
5	Number of DIMM Banks	2	01	01	02	02
6	Module Data Width	64 / 72	40	48	40	48
7	Module Data Width (cont'd)	0	00	00	00	00
8	Module Interface Levels	LVTTL	01	01	01	01
9	SDRAM Cycle Time at CL=3	10.0 ns	A0	A0	A0	A0
10	SDRAM Access time from Clock at CL=3	6.0 ns	60	60	60	60
11	Dimm Config (Error Det/Corr.)	none / ECC	00	02	00	02
12	Refresh Rate/Type	Self-Refresh, 15.6µs	80	80	80	80
13	SDRAM width, Primary	x8	08	08	08	08
14	Error Checking SDRAM data width	n/a / x8	00	08	00	08
15	Minimum clock delay for back-to-back random column address	t_{ccd} = 1 CLK	01	01	01	01
16	Burst Length supported	1, 2, 4, 8 & full page	8F	8F	8F	8F
17	Number of SDRAM banks	2	02	02	02	02
18	Supported CAS Latencies	CAS lat. = 2 & 3	06	06	06	06
19	CS Latencies	CS latency = 0	01	01	01	01
20	WE Latencies	Write latency = 0	01	01	01	01
21	SDRAM DIMM module attributes	non buffered/non reg.	00	00	00	00
22	SDRAM Device Attributes :General	Vcc tol +/- 10%	06	06	06	06
23	Min. Clock Cycle Time at CAS Latency = 2	10.0 ns	A0	A0	A0	A0
24	Max. data access time from Clock for CL=2	6.0 ns	60	60	60	60
25	Minimum Clock Cycle Time at CL = 1	not supported	FF	FF	FF	FF
26	Maximum Data Access Time from Clock at CL=1	not supported	FF	FF	FF	FF
27	Minimum Row Precharge Time	20 ns	14	14	14	14
28	Minimum Row Active to Row Active delay tRRD	16 ns	10	10	10	10

SPD-Table (cont'd):

Byte#	Description	SPD Entry Value	Hex			
			2Mx64	2Mx72	4Mx64	4Mx72
29	Minimum RAS to CAS delay tRCD	20 ns	14	14	14	14
30	Minimum RAS pulse width tRAS	45 ns	2D	2D	2D	2D
31	Module Bank Density (per bank)	16 MByte	04	04	04	04
32	SDRAM input setup time	2 ns	20	20	20	20
33	SDRAM input hold time	1 ns	10	10	10	10
34	SDRAM data input setup time	2 ns	20	20	20	20
35	SDRAM data input hold time	1 ns	10	10	10	10
36-61	Superset information (may be used in future)		FF	FF	FF	FF
62	SPD Revision	Revision 1	12	12	12	12
63	Checksum for bytes 0 - 62		C9	DB	CA	DC
64-125	Manufactures's information (optional) (FFh if not used)		XX	XX	XX	XX
126	Frequency Specification	100 MHz	64	64	64	64
127	Details of 100 MHz Support		AF	AF	FF	FF
128+	Unused storage locations		FF	FF	FF	FF

**L-DIM-168-29
SDRAM DIMM Module package**

133,35

127,35

4,0

31,75

17,78

3,0

1 10 11 40 41 84

42,18

66,68

A B C

85 94 95 124 125 168

D

6,35 6,35 1,27 1,0 ± 0.5

3,125 3,125 2,54 min.

2,0 2,0 0,2 +0,15

Detail C

Detail A Detail B

DM168-29.WMF

4,45
2.26
8.25
RADIUS
1.27 + 0.10

Detail D

x) on ECC modules only