PC133 SDRAM Registered DIMM

Design Specification

Revision 1.1

August 1999

Prepared By IBM and Reliance Computer Corporation

Product Description

This specification defines the electrical and mechanical requirements for 168-pin, 3.3 Volt, 133MHz, 72-bit wide, Registered Synchronous DRAM Dual In-Line Memory Modules (SDRAM DIMMs).These SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations.

Reference design examples are included which provide an initial basis for Registered DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity and thermal requirements for 133MHz support. All registered DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

This specification largely follows the JEDEC defined 168-pin 8-Byte Registered SDRAM DIMM product. (Refer to JEDEC standard 21-C, Section 4.5.7, at www.jedec.org).

Product Family Attributes

DIMM Organization	x 72 ECC
DIMM Dimensions (nominal)	5.25" x 1.5"/1.7" x .157"/.320"
Pin Count	168
SDRAMs Supported	64Mb, 128Mb, 256Mb
Capacity	64MB, 128MB, 256MB, 512MB, 1GB
Serial PD	Consistent with JEDEC Rev. 2.0
Voltage Options	3.3 volt (V_{DD}/V_{DDQ})
Interface	LVTTL

Environmental Requirements

PC133 SDRAM Registered DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to +55	°C	1
H_{OPR}	Operating Humidity (relative)	10 to 90	%	1
T_{STG}	Storage Temperature	-50 to +100	°C	1
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1
	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1, 2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.

Architecture

Pin Description

CK(0:3)	Clock Inputs	DQ(0:63)	Data Input/Output
CKE(0:1)	Clock Enables	CB(0:7)	ECC Data Input/Output
$\overline{RAS}$	Row Address Strobe	DQMB(0:7)	Data Mask
$\overline{CAS}$	Column Address Strobe	V_{DD}	Power (3.3V)
$\overline{WE}$	Write Enable	V_{SS}	Ground
$\overline{S}$(0:3)	Chip Selects	NC	No Connect
A(0:9,11:12)	Address Inputs	SCL	Serial Presence Detect Clock Input
A10/AP	Address Input/Autoprecharge	SDA	Serial Presence Detect Data Input/Output
BA0-BA1	SDRAM Bank Address	SA(0:2)	Serial Presence Detect Address Inputs
REGE	Register Enable	WP	Write Protect for SPD on DIMM
DU	Don’t Use - leave as NC	NC	No Connect

Input/Output Functional Description

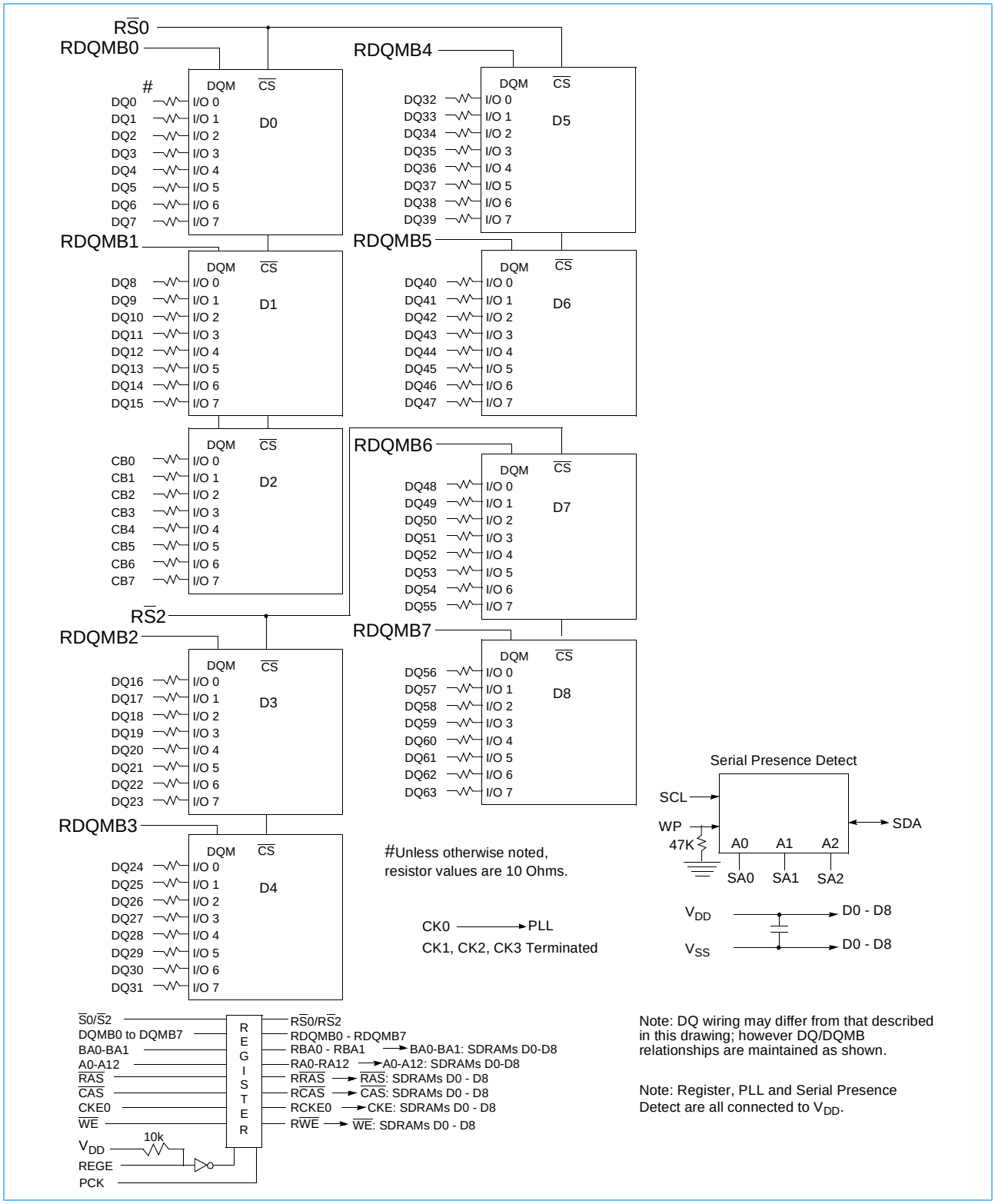
Symbol	Type	Polarity	Function
CK0 - CK3	Input	Positive Edge	The system clock inputs. All of the SDRAM inputs are sampled on the rising edge of their associated clock. CK0 drives the PLL. CK1, CK2 & CK3 are terminated.
CKE0,1	Input	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{S}$0 - $\overline{S}$3	Input	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Physical Bank 0 is selected by $\overline{S}$0 and $\overline{S}$2; Bank 1 is selected by $\overline{S}$1 and $\overline{S}$3.
$\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$	Input	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA0, 1	Input	—	Selects which SDRAM bank of four is activated.
A0 - A9, A11-12 A10/AP	Input	—	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A10 defines the column address (CA0-CA10) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, then BA0 and BA1 are used to define which bank to precharge.
DQ0 - DQ63, CB0 - CB7	Input Output	—	Data and Check Bit Input/Output pins.
DQMB0 - DQMB7	Input	Active High	The Data Input/Output masks, associated with one data byte, place the DQ buffers in a high impedance state when sampled high. In Read mode, DQMB has a latency of two clock cycles in Buffered mode or three clock cycles in Registered mode, and controls the output buffers like an output enable. In Write mode, DQMB has a zero clock latency in Buffered mode and a latency of one clock cycle in Registered mode. In this case, DQMB operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high.
V_{DD}, V_{SS}	Supply		Power and ground for the module.
REGE	Input	Active High (Register Mode Enable)	The Register Enable pin is used to permit the DIMM to operate in Buffered mode (inputs re-driven asynchronously) or Registered mode (signals re-driven to SDRAMs when clock rises, and held valid until next rising clock).
SA0 - 2	Input	—	These signals are tied at the system planar to either V_{SS} or V_{DD} to configure the SPD EEPROM.
SDA	Input Output	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus time to V_{DD} to act as a pull up.
SCL	Input	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pull up.
WP	Input	Active High	This signal is pulled low on the DIMM to enable data to be written into the last 128 bytes of the SPD EEPROM.

Registered SDRAM DIMM Pinout

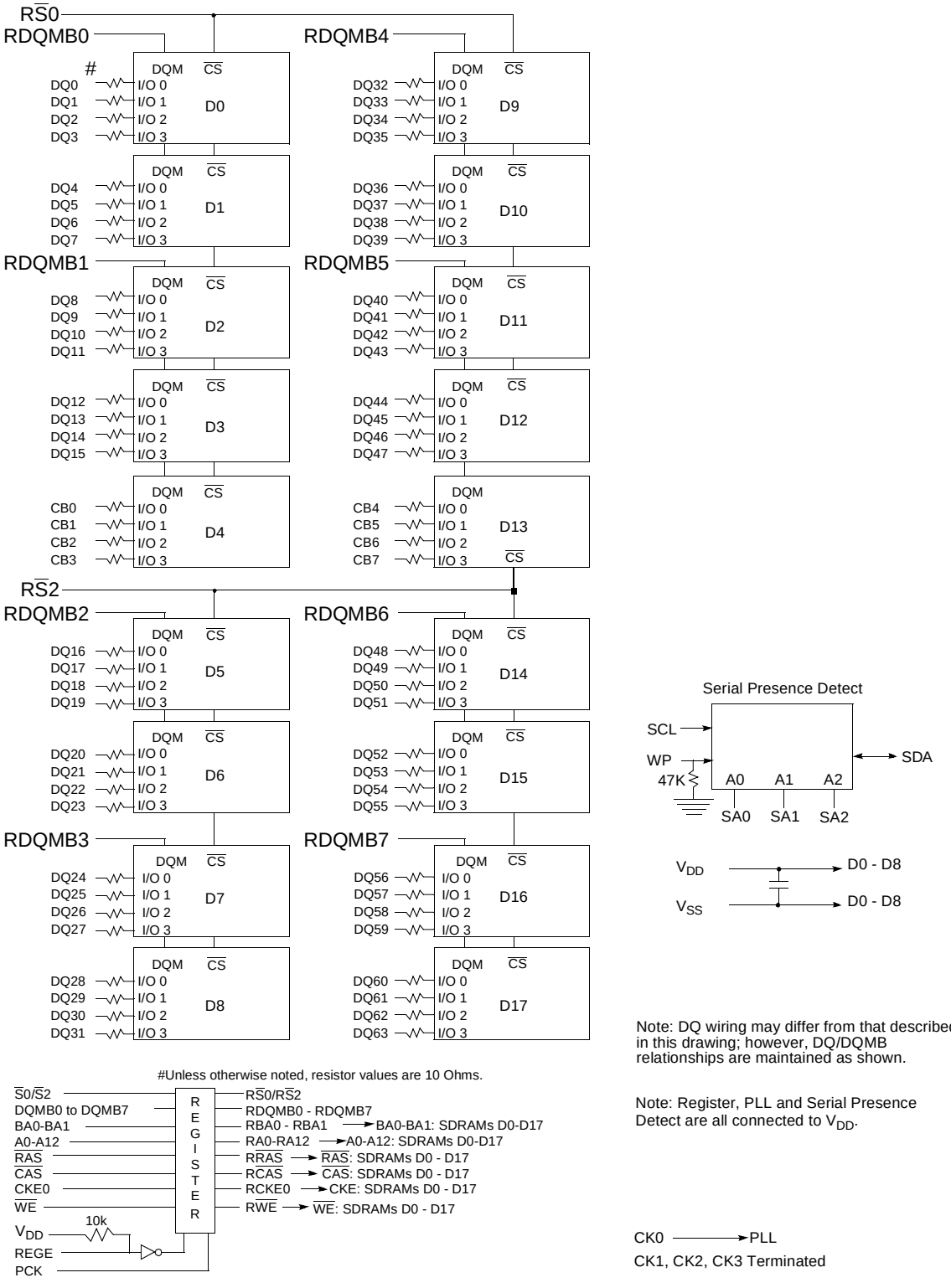
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	22	CB1	106	CB5	43	V_{SS}	127	V_{SS}	64	V_{SS}	148	V_{SS}
2	DQ0	86	DQ32	23	V_{SS}	107	V_{SS}	44	NC	128	CKE0	65	DQ21	149	DQ53
3	DQ1	87	DQ33	24	NC	108	NC	45	$\overline{S}2$	129	$\overline{S}3$	66	DQ22	150	DQ54
4	DQ2	88	DQ34	25	NC	109	NC	46	DQMB2	130	DQMB6	67	DQ23	151	DQ55
5	DQ3	89	DQ35	26	V_{DD}	110	V_{DD}	47	DQMB3	131	DQMB7	68	V_{SS}	152	V_{SS}
6	V_{DD}	90	V_{DD}	27	$\overline{WE}$	111	$\overline{CAS}$	48	NC	132	NC	69	DQ24	153	DQ56
7	DQ4	91	DQ36	28	DQMB0	112	DQMB4	49	V_{DD}	133	V_{DD}	70	DQ25	154	DQ57
8	DQ5	92	DQ37	29	DQMB1	113	DQMB5	50	NC	134	NC	71	DQ26	155	DQ58
9	DQ6	93	DQ38	30	$\overline{S}0$	114	$\overline{S}1$	51	NC	135	NC	72	DQ27	156	DQ59
10	DQ7	94	DQ39	31	NC	115	$\overline{RAS}$	52	CB2	136	CB6	73	V_{DD}	157	V_{DD}
11	DQ8	95	DQ40	32	V_{SS}	116	V_{SS}	53	CB3	137	CB7	74	DQ28	158	DQ60
12	V_{SS}	96	V_{SS}	33	A0	117	A1	54	V_{SS}	138	V_{SS}	75	DQ29	159	DQ61
13	DQ9	97	DQ41	34	A2	118	A3	55	DQ16	139	DQ48	76	DQ30	160	DQ62
14	DQ10	98	DQ42	35	A4	119	A5	56	DQ17	140	DQ49	77	DQ31	161	DQ63
15	DQ11	99	DQ43	36	A6	120	A7	57	DQ18	141	DQ50	78	V_{SS}	162	V_{SS}
16	DQ12	100	DQ44	37	A8	121	A9	58	DQ19	142	DQ51	79	CK2	163	CK3
17	DQ13	101	DQ45	38	A10/AP	122	BA0	59	V_{DD}	143	V_{DD}	80	NC	164	NC
18	V_{DD}	102	V_{DD}	39	BA1	123	A11	60	DQ20	144	DQ52	81	WP	165	SA0
19	DQ14	103	DQ46	40	V_{DD}	124	V_{DD}	61	NC	145	NC	82	SDA	166	SA1
20	DQ15	104	DQ47	41	V_{DD}	125	CK1	62	NC	146	NC	83	SCL	167	SA2
21	CB0	105	CB4	42	CK0	126	A12	63	CKE1/ NC	147	REGE	84	V_{DD}	168	V_{DD}

Note: All pin assignments are consistent with all 8-byte unbuffered versions.

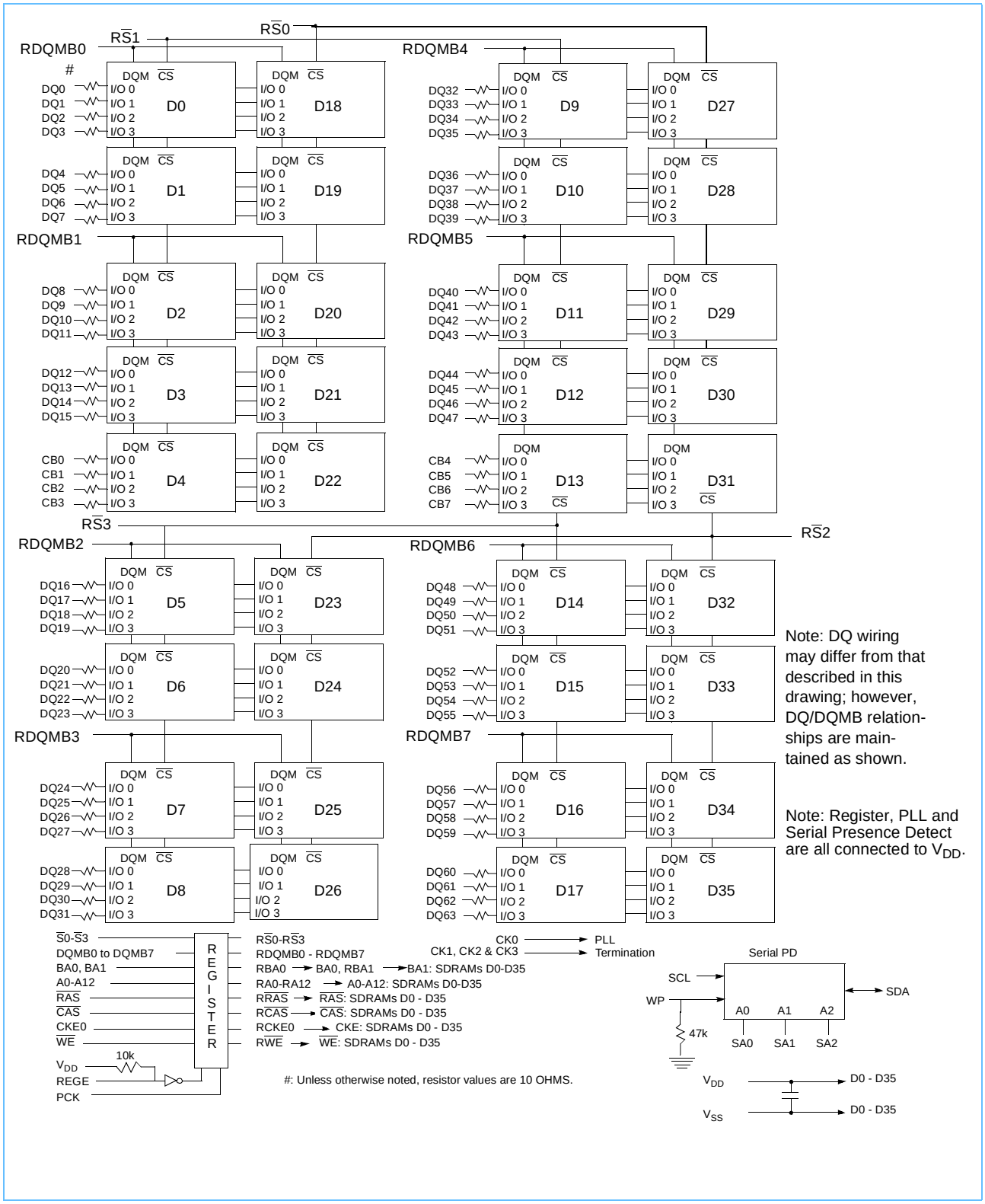
Block Diagram: Raw Card Version A (Populated as 1 physical bank of x8 SDRAMs)



Block Diagram: Raw Card Version B (Populated as 1 physical bank of x4 SDRAMs)



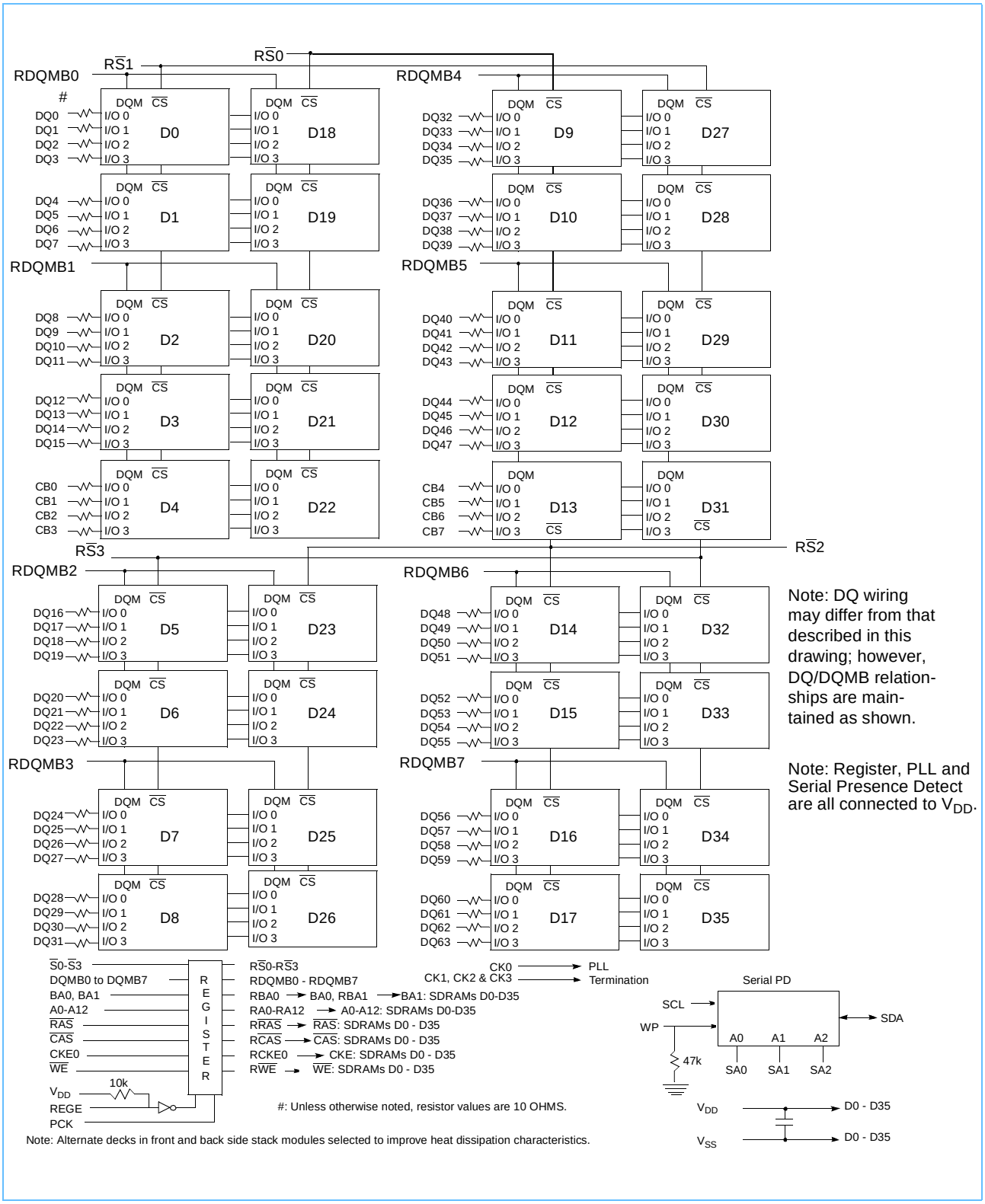
Block Diagram: Raw Card Version B (Populated as 2 physical banks of x4 SDRAMs)



Note: DQ wiring may differ from that described in this drawing; however, DQ/DQMB relationships are maintained as shown.

Note: Register, PLL and Serial Presence Detect are all connected to V_{DD}.

Block Diagram: Raw Card Versions C & D (Populated as 2 physical banks of x4 SDRAMs)

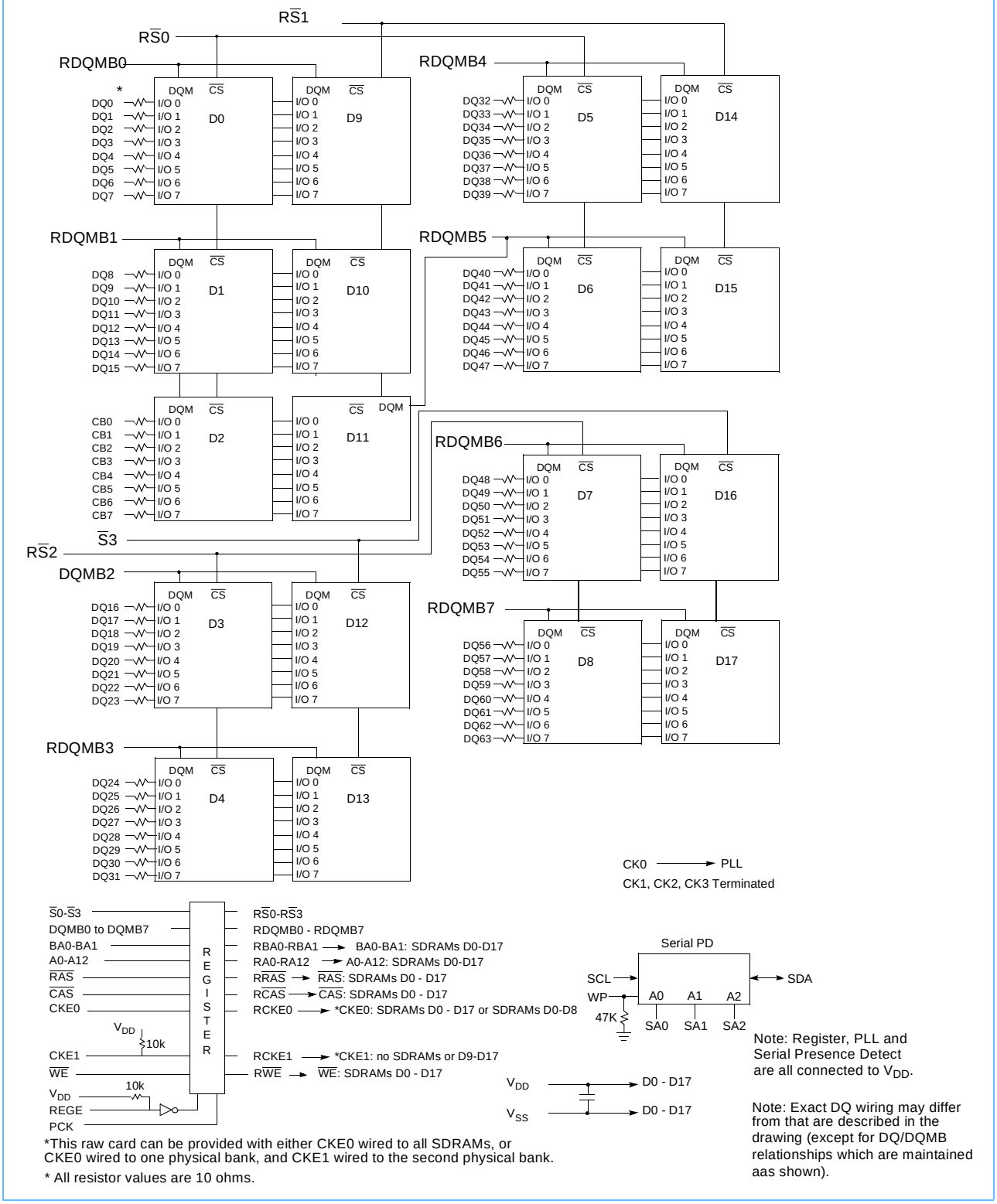


Note: Alternate decks in front and back side stack modules selected to improve heat dissipation characteristics.

Note: DQ wiring may differ from that described in this drawing; however, DQ/DQMB relationships are maintained as shown.

Note: Register, PLL and Serial Presence Detect are all connected to V_{DD}.

Block Diagram: Raw Card Version E (Populated as 2 physical bank of x8 SDRAMs)



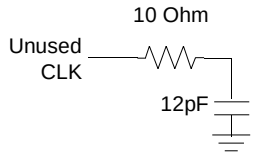
*This raw card can be provided with either CKE0 wired to all SDRAMs, or CKE0 wired to one physical bank, and CKE1 wired to the second physical bank.

* All resistor values are 10 ohms.

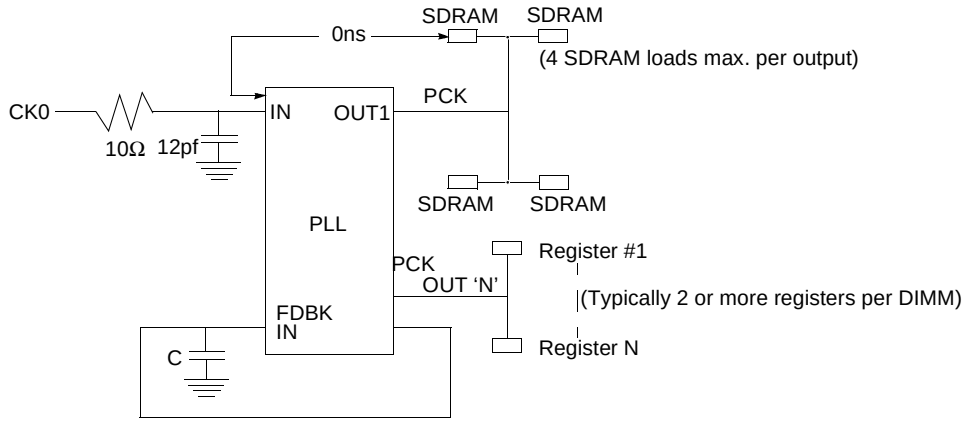
Note: Register, PLL and Serial Presence Detect are all connected to V_{DD}.

Note: Exact DQ wiring may differ from that are described in the drawing (except for DQ/DQMB relationships which are maintained aas shown).

Termination for Unused Clock Signals (CK1-CK3)



Clock Net Wiring (CK0)



Notes

1. PLL outputs (PCK) must be wired to assure tracking within ± 100ps at the load (any SDRAM to any SDRAM or any padding capacitor, or any register to any register).
2. Only one PLL output is shown per output type. Any additional PLL outputs will be wired in a similar manner.
3. A maximum of four SDRAM loads should be placed on each PLL output. If there are fewer than four loads, adjust line lengths and capacitive loading on PLL outputs to compensate for lighter loading.
4. Feedback capacitor value 'C' is to be determined based on the phase characteristics of the PLL, and should be selected and verified using the PC100/PC133 Clock Reference Board.

Register Functional Assignments

Raw Card Version A (Two Registers)				Raw Card Versions B, C, and D (Three Registers)					
Register 1		Register 2		Register 1		Register 2		Register 3	
In	Out	In	Out	In	Out	In	Out	In	Out
A0	RA0	DQMB2	RDQMB2	A0	RA0A	A0	RA0B	DQMB0	RDQMB0
A1	RA1	DQMB3	RDQMB3	A1	RA1A	A1	RA1B	DQMB1	RDQMB1
A2	RA2	DQMB6	RDQMB6	A2	RA2A	A2	RA2B	DQMB2	RDQMB2
A3	RA3	DQMB7	RDQMB7	A3	RA3A	A3	RA3B	DQMB3	RDQMB3
A4	RA4	$\overline{S}2$	R$\overline{S}2$	A4	RA4A	A4	RA4B	DQMB4	RDQMB4
A5	RA5	CKE0	RCKE0	A5	RA5A	A5	RA5B	DQMB5	RDQMB5
A6	RA6	BA0	RBA0	A6	RA6A	A6	RA6B	DQMB6	RDQMB6
A7	RA7	BA1	RBA1	A7	RA7A	A7	RA7B	DQMB7	RDQMB7
A8	RA8	A10	RA10	A8	RA8A	A8	RA8B	$\overline{S}0$	R$\overline{S}0$
A9	RA9	A11	RA11	A9	RA9A	A9	RA9B	$\overline{S}1$	R$\overline{S}1$
$\overline{S}0$	R$\overline{S}0$	A12[1]	RA12	A10	RA10A	A10	RA10B	$\overline{S}2$	R$\overline{S}2$
DQMB0	RDQMB0			A11	RA11A	A11	RA11B	$\overline{S}3$	R$\overline{S}3$
DQMB1	RDQMB1			BA0	RBA0A	BA0	RBA0B	$\overline{WE}$	R$\overline{WE}$A
DQMB4	RDQMB4			BA1	RBA1A	BA1	RBA1B	$\overline{WE}$	R$\overline{WE}$B
DQMB5	RDQMB5			$\overline{CAS}$	RCASA	$\overline{CAS}$	RCASB	A12[1]	RA12A
$\overline{CAS}$	RCAS			$\overline{RAS}$	RRASA	$\overline{RAS}$	RRASB	A12[1]	RA12B
$\overline{RAS}$	RRAS			CKE0	CKE0A				
$\overline{WE}$	R$\overline{WE}$			CKE0	CKE0B				

1. Only used with 256Mbit SDRAMs.

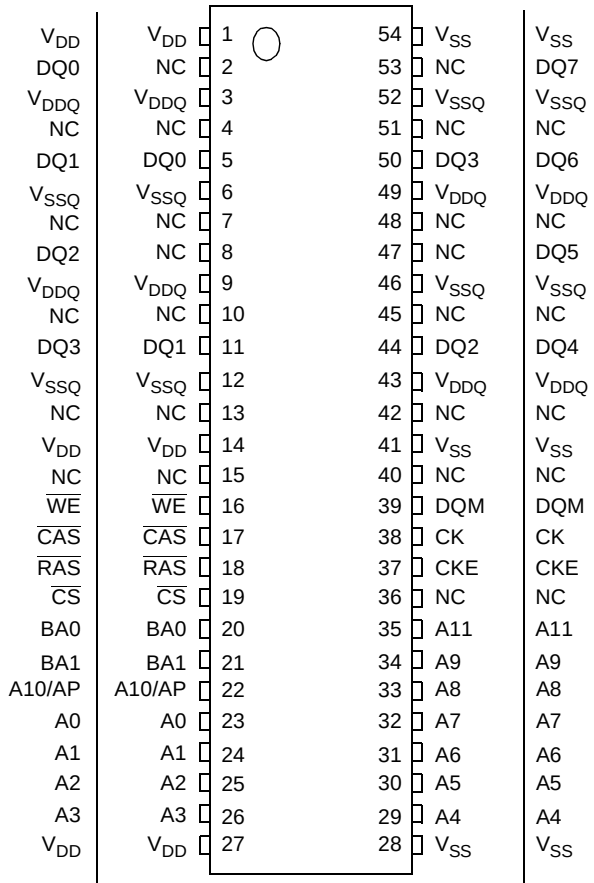
Register Functional Assignments (continued)

Raw Card Version E (Three Registers)					
Register 1		Register 2		Register 3	
In	Out	In	Out	In	Out
A0	RA0A	A0	RA0B	DQMB0	RDQMB0
A1	RA1A	A1	RA1B	DQMB1	RDQMB1
A2	RA2A	A2	RA2B	DQMB2	RDQMB2
A3	RA3A	A3	RA3B	DQMB3	RDQMB3
A4	RA4A	A4	RA4B	DQMB4	RDQMB4
A5	RA5A	A5	RA5B	DQMB5	RDQMB5
A6	RA6A	A6	RA6B	DQMB6	RDQMB6
A7	RA7A	A7	RA7B	DQMB7	RDQMB7
A8	RA8A	A8	RA8B	$\overline{S}0$	R$\overline{S}$0
A9	RA9A	A9	RA9B	$\overline{S}1$	R$\overline{S}$1
A10	RA10A	A10	RA10B	$\overline{S}2$	R$\overline{S}$2
A11	RA11A	A11	RA11B	$\overline{S}3$	R$\overline{S}$3
BA0	RBA0A	BA0	RBA0B	$\overline{WE}$	R$\overline{WE}$A
BA1	RBA1A	BA1	RBA1B	$\overline{WE}$	R$\overline{WE}$B
$\overline{RAS}$	R$\overline{RAS}$A	$\overline{RAS}$	R$\overline{RAS}$B	A12[1]	RA12A
$\overline{CAS}$	R$\overline{CAS}$A	$\overline{CAS}$	R$\overline{CAS}$B	A12[1]	RA12B
				CKE0	RCKE0
				CKE1[2]	RCKE1

1. Only used with 256Mbit SDRAMs.
2. R/C 'E' can be produced with either CKE0 wired to all SDRAMs (this pin would not be used), or CKE0 can be wired to one physical bank and CKE1 wired to the second physical bank.

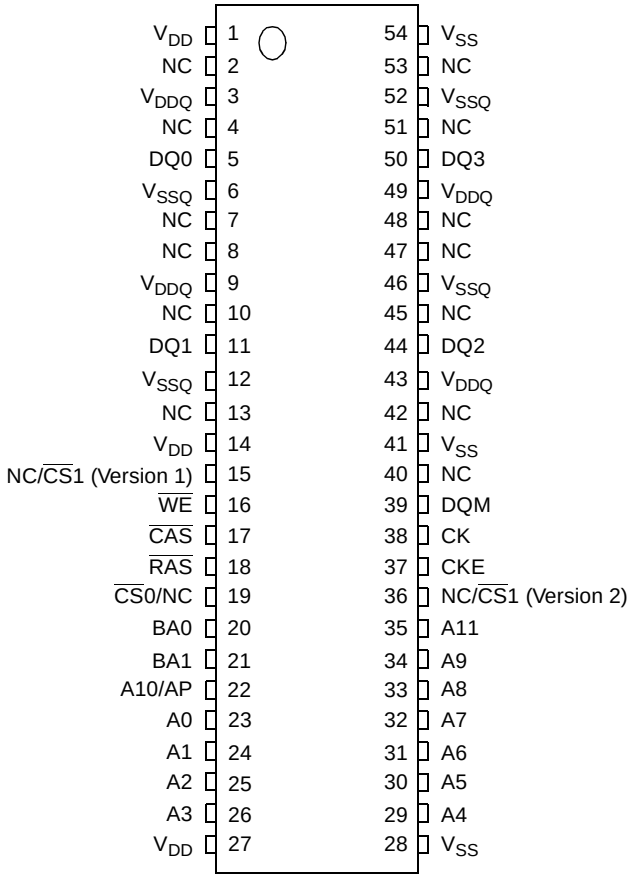
Component Details

Pin Assignments for 64Mb and 128Mb SDRAM Planar Components (Top View)



Note: Raw Card Versions ‘A’ and ‘B’ support the use of the above SDRAM pin assignments. These pin assignments are consistent with the JEDEC standard package definition.

Pin Assignments for 64Mb and 128Mb 54 pin SDRAM 2 High Stack Package (Dual $\overline{CS}$ Pin) (Top View)



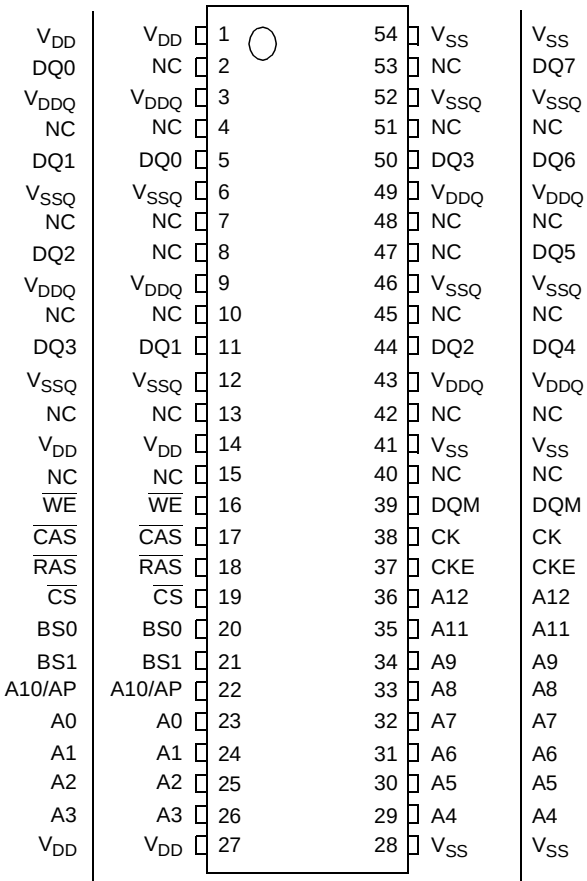
54-pin Plastic TSOP(II) or TSOJ(II) 400 mil

(4Mbit x 4 I/O x 4 Bank) x 2 High
(8Mbit x 4 I/O x 4 Bank) x 2 High

Version 1: Consistent with Staktek (TM) 2 High stacked package. Raw Card Version 'B' supports the use of this pin assignment.
Version 2: Consistent with IBM Microelectronics and JEDEC standard 2 High stacked package. Raw Card Version 'C' supports the use of this pin assignment.

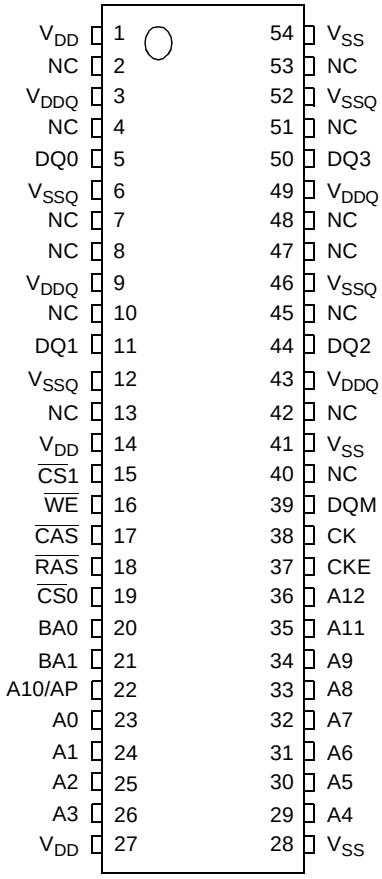
***** $\overline{CS}$0 selects the lower DRAM in the stack.
***** $\overline{CS}$1 selects the upper DRAM in the stack.

Pin Assignments for 256Mb 54 pin SDRAM Planar Components (Top View)



Note: Raw Card Version ‘B’ supports the use of the above SDRAM pin assignment. This pin assignment is consistent with the JEDEC standard package.

Pin Assignments for 256Mb 54 pin SDRAM 2 High Stack Package (Dual $\overline{CS}$ Pin) (Top View)



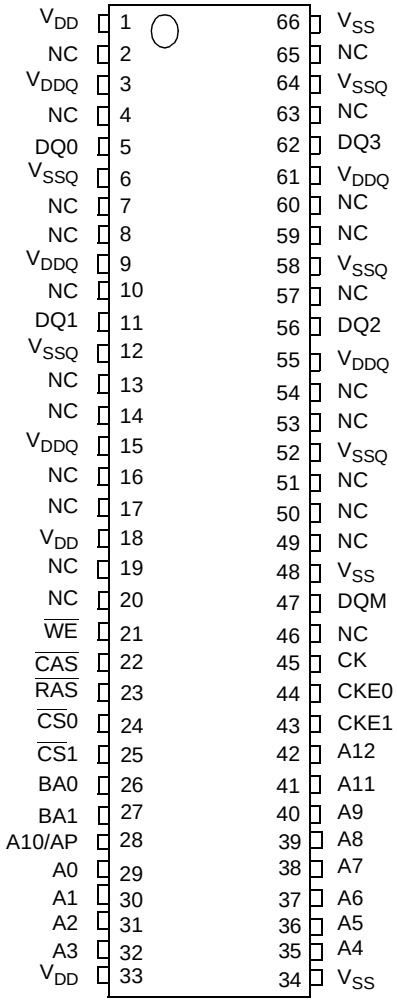
54-pin Plastic TSOP(II) or TSOJ(II) 400 mil

(16Mbit x 4 I/O x 4 Bank) x 2 High

Note: Raw Card Version ‘B’ supports the use of the above SDRAM pin assignment. This pin assignment is consistent with the Staktek (TM) 2 High stacked package.

* $\overline{CS0}$ selects the lower DRAM in the stack.
* $\overline{CS1}$ selects the upper DRAM in the stack.

Pin Assignments for 256Mb 66 pin SDRAM 2 High Stack Package (Dual $\overline{CS}$ Pin) (Top View)



66-pin Plastic TSOJ 400 mil

(16Mbit x 4 I/O x 4 Bank) x 2 High

Note: Raw Card Version ‘D’ supports the use of this SDRAM pin assignment. This pin assignment is consistent with IBM Microelectronics and JEDEC standard packages.

SDRAM Component Specifications

The 133MHz SDRAM components used with this DIMM design specification are intended to be consistent with the latest revision of the Intel “PC SDRAM” specification and the latest JEDEC SDRAM specification (located at www.jedec.org). However, the following information supersedes the equivalent data within the Intel PC100 SDRAM Specification. SDRAM component specification violations also violate 133MHz registered DIMM specifications.

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	3.0	3.6	V	
V_{DDQ}	I/O Supply Voltage	3. 0	3.6	V	
Ii_I	Input Leakage Current ($0 < V_{IN} < V_{DDQ}$)	-10	+10	µA	1, 2
I_{CCLP}	I_{cc} Low Power (CKE low, all banks closed)	-	2	ma	
V_{OH}	Output High Voltage (I_{OH} = -4mA)	2.4	-	V	
V_{OL}	Output Low Voltage (I_{OL} = 4mA)	-	0.4	V	
C_{IN}	Input Pin Capacitance (@1MHz, 23C T_J, 1.4V bias, 200mV swing, V_{DD} =3.3V)	2.5	3.8	pF	3
$C_{I/O}$	I/O Pin Capacitance(@1MHz, 23C T_J, 1.4V bias, 200mV swing, V_{DD} = 3.3V)	4.0	6.5	pF	4
C_{CK}	Pin Capacitance (@1MHz, 23C T_J, 1.4V bias, 200mV swing, V_{DD} = 3.3v)	2.5	3.5	pF	5
L_{PIN}	Pin Inductance		10	nH	
T_A	Ambient Temperature (No Airflow)	0	55	°C	

1. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.
2. No Activate or Precharge currents should be included in the Iccac value.
3. Target 3.15pF
4. Target 4.8pF
5. Target 3.0pF

AC Timing Parameters (T_A = 0-65×C; V_{DD} = 3.0V - 3.6V; CL= 2, 3) (Part 1 of 2)

Symbol	Parameter		Speed Grade 100MHz		Speed Grade 133MHz/100MHz		Units	Notes
			Min	Max	Min	Max		
t_{CK}	Clock Period		10		7.5		ns	
t_{CH}	Clock High Time Rated @1.5V		3		2.5		ns	
t_{CL}	Clock Low Time		3		2.5		ns	
t_{IS}	Input Setup Times	Address/ Command & CKE	2		1.5		ns	
		Data	2		1.5		ns	
t_{IH}	Input Hold Times	Address/Command & CKE	1		0.8		ns	
		Data	1		0.8		ns	
t_{AC}	Output Valid From Clock	$\overline{CAS}$ Latency = 2 limited application, 2 banks *all outputs switching*		7.0		N/A	ns	1
		$\overline{CAS}$ Latency = 2 LVTTL levels, Rated @50pF *all outputs switching*		6.0 (tco = 5.2)		5.4 (tco = 4.6)	ns	1
		$\overline{CAS}$ Latency = 3 LVTTL levels, Rated @50pF *all outputs switching*		6.0 (tco = 5.2)		5.4 (tco = 4.6)		1
t_{OH}	Output Hold From Clock Rated @ 50pF (1.8ns @ 0pf)		3		2.7		ns	
t_{OHZ}	Output Valid to Z		3	9	2.7	7	ns	
t_{CCD}	CAS to CAS Delay		1		1		t_{CK}	
t_{CBD}	CAS Bank Delay		1		1		t_{CK}	
t_{CKE}	CKE to Clock Disable		1		1		t_{CK}	
t_{RP}	RAS Precharge Time		20.0		20.0		ns	
t_{RAS}	RAS Active Time		50		45		ns	
t_{RCD}	Activate to Command Delay (RAS to CAS Delay)		20.0		20.0		ns	
t_{RRD}	RAS to RAS Bank Activate Delay		20		15		ns	
t_{RC}	RAS Cycle Time		70		67.5		ns	
t_{DQD}	DQM to Input Data Delay		0		0		t_{CK}	

1. Access times to be measured w/input signals of 1V/ns edge rate, 0.8V to 2.0V.
2. CL = CAS Latency
3. Data Masked on the same clock
4. Self refresh Exit is asynchronous, requiring 10ns to ensure initiation. Self refresh exit is complete in 10ns + t_{RC}.
5. Timing is asynchronous. If t_{set} is not met by rising edge of CK then CKE is assumed latched on next cycle.
6. If the clock is stopped during self refresh or power down, 200 clocks are required before CKE is high.
7. For 64Mbit SDRAM technology, 4096 refresh cycles. For 256Mbit SDRAM technology, 8192 refresh cycles.

AC Timing Parameters (T_A = 0-65×C; V_{DD} = 3.0V - 3.6V; CL= 2, 3) (Part 2 of 2)

Symbol	Parameter	Speed Grade 100MHz		Speed Grade 133MHz/100MHz		Units	Notes
		Min	Max	Min	Max		
t_{DWD}	Write Cmd. to Input Data Delay	0		0		t_{CK}	
t_{MRD}	Mode Register set to Active delay	3		3		t_{CK}	
t_{ROH}	Precharge to O/P in High Z		CL		CL	t_{CK}	2
t_{DQZ}	DQM to Data in High Z for read	2		2		t_{CK}	
t_{DQM}	DQM to Data mask for write	0		0		t_{CK}	3
t_{DPL}	Data-in to PRE Command Period	20		15		ns	
t_{DAL}	Data-in to ACT (PRE) Command period (Auto precharge)	5		5		t_{CK}	
t_{SB}	Power Down Mode Entry		1		1	t_{CK}	
t_{SRX}	Self Refresh Exit Time	10		10		ns	4
t_{PDE}	Power Down Exit Set up Time	1		1		t_{CK}	5
t_{CKSTP}	Clock Stop During Self Refresh or Power Down	200		200		t_{CK}	6
t_{REF}	Refresh Period		64		64	ms	7
t_{RFC}	Row Refresh Cycle Time	80.0		75.0		ns	

1. Access times to be measured w/input signals of 1V/ns edge rate, 0.8V to 2.0V.
2. CL = CAS Latency
3. Data Masked on the same clock
4. Self refresh Exit is asynchronous, requiring 10ns to ensure initiation. Self refresh exit is complete in 10ns + t_{RC}.
5. Timing is asynchronous. If t_{set} is not met by rising edge of CK then CKE is assumed latched on next cycle.
6. If the clock is stopped during self refresh or power down, 200 clocks are required before CKE is high.
7. For 64Mbit SDRAM technology, 4096 refresh cycles. For 256Mbit SDRAM technology, 8192 refresh cycles.

Register Component Specifications

Please refer to the vendor register data sheets for all technical specifications and requirements. Below is a chart explaining which possible registers may be used on each DIMM type.

DIMM Register Use

Raw Card Version	# of SDRAMs per output	Register Type[1]	Qty
A, AA	9	ALVC162835/4[2],AVC16835/4 or equiv.	2
B	9	ALVC162835/4[2],AVC16835/4 or equiv.	3
	18	ALVC162835/4[2],AVC16835/4 or equiv.	3
C	18	ALVC162835/4[2],AVC16835/4 or equiv.	3
D	18	ALVC162835/4[2],AVC16835/4 or equiv.	3
E	9	ALVC162835/4[2],AVC16835/4 or equiv.	3

1. Assemblies may use either ‘835 or ‘834 devices with Raw Card Version A,B,C,D or E. The inverter position must be populated when using ‘835 registers, whereas an inverter bypass jumper must be populated when using ‘834 registers.
2. A ‘fast’ version of this device is required for 133MHz operation.

The following specifications for the registers are critical for proper operation of PC133 registered DIMMs. These are meant to be a subset of the parameters for the device, but must be met if a different, but functionally equivalent, part is to be used.

Critical Register Specifications

Register	Parameter	From (input)	From (output)	Conditions	T_A = 0-70° C V_{DD} = 3.3V ± 0.3V			Units
					Min	Typ	Max	
ALVC162835/4, AVC16835/4 or equivalent	$t_{PD\ (9\ loads)}$[1]	Clock	Y	500 Ohm, 50pF	1.4	---	3.5	ns
	$t_{PD\ (18\ loads)}$[1]	Clock	Y	500 Ohms, 30pF	0.7	---	2.5	ns
	I_I	NA	NA	V_I = 0 to 3.6V			10	uA
	t_{setup}	NA	NA		1.0			ns
	t_{hold}	NA	NA		0.6			ns
	Clock Cin	NA	NA		3.3	4.0	6.0	pF

1. The t_{PD} value in this table would equate to the ‘Time-to Vm’ delay described in the post-register timings section of this document. The first value applies to DIMMs with nine SDRAM loads per register output, and the second to DIMMs with eighteen SDRAM loads per register output. These values should serve as only an initial starting point, as the critical timing closure is dependent on the DIMM net structure and the distributed load.

Register Sourcing

This document is not intended to be an approved vendor list for support chip components. Although it is recommended that all PC133 RDIMM registers meet the specifications documented above, it is up to each DIMM producer to select the registers and register vendors which meet these requirements, and to guarantee robustly operating DIMMs. For this reason all references to specific register sources have been removed. In addition, any use of a naming convention is only for reference; differently marked, functionally equivalent, registers are acceptable.

PLL Component Specifications

Please refer to the vendor PLL data sheets for all technical specifications and requirements. Below is a chart explaining which PLLs are used on each DIMM type.

DIMM PLL Use

Raw Card Version	# of SDRAMs per output	PLL Type[2]	Qty
A	3	CDC2509	1
AA[1]	3	CDC2510	1
B	2	CDC2510	1
	4	CDC2510	1
C	4	CDC2510	1
D	4	CDC2510	1
E	3	CDC2510	1

1. This DIMM design allows DIMM producers to utilize a common PLL part number for all of their PC133 RDIMM designs. This raw card design is optional and may be used in place of Raw Card Design A.
2. These are 133MHz versions of the PLLs utilized on 100MHz SDRAM Registered DIMMs.

The following specifications for the PLL are critical for proper operation of the PC133 Registered DIMMs. These are meant to be a subset of the parameters for the device.

Critical PLL Specifications

Device	Parameter	From	To	T_A = 70° C, V_{DD} = 3.3V ± 0.3V			Units
				Min	Typ	Max	
CDC2509/10	Operating Frequency	-----	-----	50	---	140	MHz
CDC2509/10	Jitter	Output in = CLK n	Output in = CLK n+1	-75	---	+75	ps
CDC2509/10	SSC Induced Skew[1, 2]	Output in = CLK n	Output in = CLK n+1	-----	---	+150	ps
CDC2509/10	Skew[2]	Output	Output	-----	---	+150	ps
CDC2509/10	Clock Input Capacitance	-----	----	-----	4	------	pF

1. SSC1 Induced Skew: SSC = Spread Spectrum Clock. The use of SSC synthesizers on the system motherboard will reduce EMI.
2. Skew is defined as the total clock skew between any two outputs and is therefore specified as a maximum only.

The PLL used on the registered DIMM needs to support SSC synthesizers with the following parameters:

Parameter	Min	Max
Modulation Frequency	30KHz	50KHz
Clock Frequency Deviation (ex. for 133 MHz: 132.3MHz to 133MHz range)		0.5%

PLL designs should target the following values to meet the 150ps maximum of SSC induced skew:

- Greater than 1.2MHz PLL loop bandwidth
- Less than -0.031 degrees of phase angle

PLL Sourcing

This document is not intended to be an approved vendor list for support chip components. Although it is recommended that all PC133 RDIMM PLLs meet the specifications documented above, it is up to each DIMM producer to select the PLL and PLL vendors which meet these requirements, and to guarantee robustly operating DIMMs. For this reason all references to specific PLL sources have been removed. In addition, any use of a naming convention is only for reference; differently marked, functionally equivalent, PLLs are acceptable.

Registered DIMM Details

SDRAM Module Configurations (Reference Designs)

Raw Card Version	DIMM Capacity	DIMM Organization	SDRAM Density	SDRAM Organization	# of SDRAMs	SDRAM Package Type	# of Physical Banks	# of Banks in SDRAM	# Address bits row/col/banks
A, AA	64MB	8Mx72	64Mbit	8Mx8	9	54 lead TSOP	1	4	12/9/2
	128MB	16Mx72	128Mbit	16Mx8	9	54 lead TSOP	1	4	12/10/2
	256MB	32Mx72	256Mbit	32Mx8	9	54 lead TSOP	1	4	13/10/2
B[1]	128MB	16Mx72	64Mbit	16Mx4	18	54 lead TSOP	1	4	12/10/2
	256MB	32Mx72	128Mbit	32Mx4	18	54 lead TSOP	1	4	12/11/2
	512MB	64Mx72	256Mbit	64Mx4	18	54 lead TSOP	1	4	13/11/2
	256MB	32Mx72	64Mbit	16Mx4	36	54 lead stack TSOP	2	4	12/10/2
	512MB	64Mx72	128Mbit	32Mx4	36	54 lead stack TSOP	2	4	12/11/2
	1GB	128Mx72	256Mbit	64Mx4	36	54 lead stack TSOP	2	4	13/11/2
C[1]	256MB	32Mx72	64Mbit	16Mx4	36	54 lead stack TSOJ	2	4	12/10/2
	512MB	64Mx72	128Mbit	32Mx4	36	54 lead stack TSOJ	2	4	12/11/2
D	1GB	128Mx72	256Mbit	64Mx4	36	66 lead stack TSOJ	2	4	13/11/2
E	128MB	16Mx72	64Mbit	8Mx8	18	54 lead TSOP	2	4	12/10/2
	256MB	32Mx72	128Mbit	16Mx8	18	54 lead TSOP	2	4	12/10/2
	512MB	64Mx72	256Mbit	32Mx8	18	54 lead TSOP	2	4	13/10/2

1. Raw Card Version ‘B’ and ‘C’ share the same topology information (with the exception of a few nets listed in the topology portion of this document), and vary in the location and size of the landing pads for the SDRAMs.

Input Loading Matrix

Signal Names	Input Device	R/C A Planar	R/C B		R/C C Stack	R/C D Stack	R/C E Planar
			Planar	Stack			
Clock (CK0)	PLL	1	1	1	1	1	1
CKE0	Register	1	2	2	2	2	1 or 2*
CKE1	Register	0	0	0	0	0	0 or 1*
Addr/RAS/CAS/BA/WE	Register	1	2	2	2	2	2
Chip Selects	Register	1	1	1	1	1	1
DQ/CB	SDRAM	1	1	2	2	2	1
DQMB	Register	1	1	1	1	1	1
REGE	*	1 or 2	1 or 3	1 or 3	1 or 3	1 or 3	1 or 3
SCL/SDA/SA/WP	EEPROM	1	1	1	1	1	1

*Raw Card Version E can be produced with either CKE0 wired to al of the SDRAMs, or CKE0 wired to the second physical bank (to permit selective bank depowering).

*REGE wires to an inverter (one load), or to all registers (if an '834 or equivalent register is utilized).

PC133 Gerber Releases

'Reference' Gerber file updates will be released as needed. This Registered DIMM specification will reflect the most recent Gerber files, but may also be updated to reflect clarifications to the specification only; in these cases the Gerber files will not be updated. The following table outlines the most recent Gerber file releases.

Note: Initial Gerber releases are identified in the 'read-me' file by their date. Future Gerber releases will include both a date and a revision label. All changes to the Gerber file are also documented within the 'read-me' file.

Raw Card Version	Specification Revision	Applicable Gerber File	Notes
A	1.1	2/1/99 (A1)	Original Release
AA[1]	1.1	5/28/99 (AA)	Original Release
B	1.1	12/14/98 (B2)	Second Release
C	1.1	2/19/98 (C1)	Original Release
D	1.1	5/12/99(D1)	Original Release
E	1.1	8/1/99 (E1)	Original Release

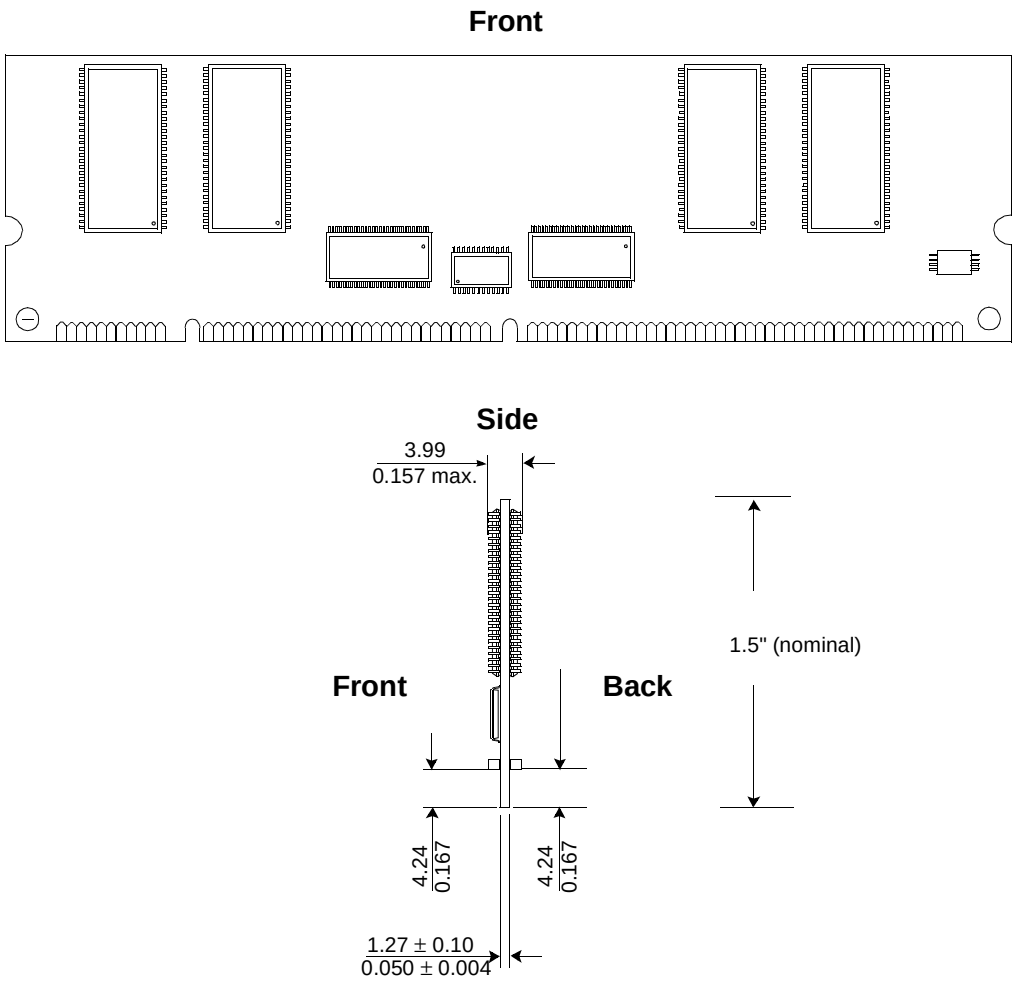
1. This DIMM design allows DIMM producers to utilize one PLL part number for all of their PC133 Registered DIMMs. This DIMM raw card is optional and may be selected by the DIMM producer. Any future revisions (although none are planned) will use raw card design 'AA' as the base design. It is important to note that there is no electrical difference between R/C Version 'A' and R/C Version 'AA'. All changes are clearly listed in the read me file associated with the Raw Card AA release.

Component Types and Placement

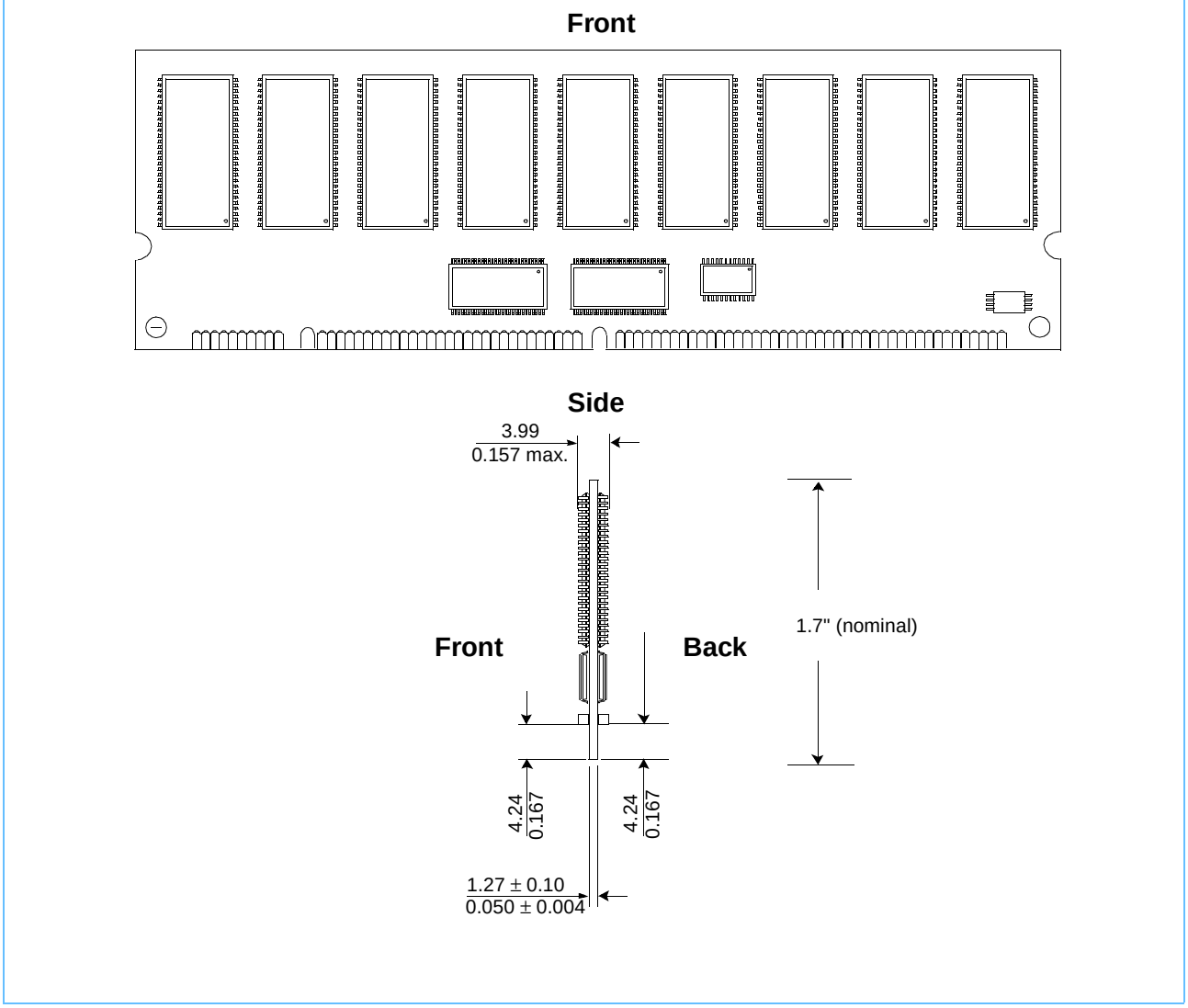
Components shall be surface mounted on both sides of the PCB and positioned on the PCB to meet the minimum and maximum trace lengths required for SDRAM signals. Bypass capacitors, for SDRAM devices, must be practically located near the device power pins. In two-bank SDRAM designs, the second SDRAM bank devices will be stacked on the first SDRAM bank devices.

The following layouts suggest placement for the Raw Card Versions A - E. Exact spacing is not provided, but should be based on manufacturing constraints and signal routing constraints imposed by this design guide.

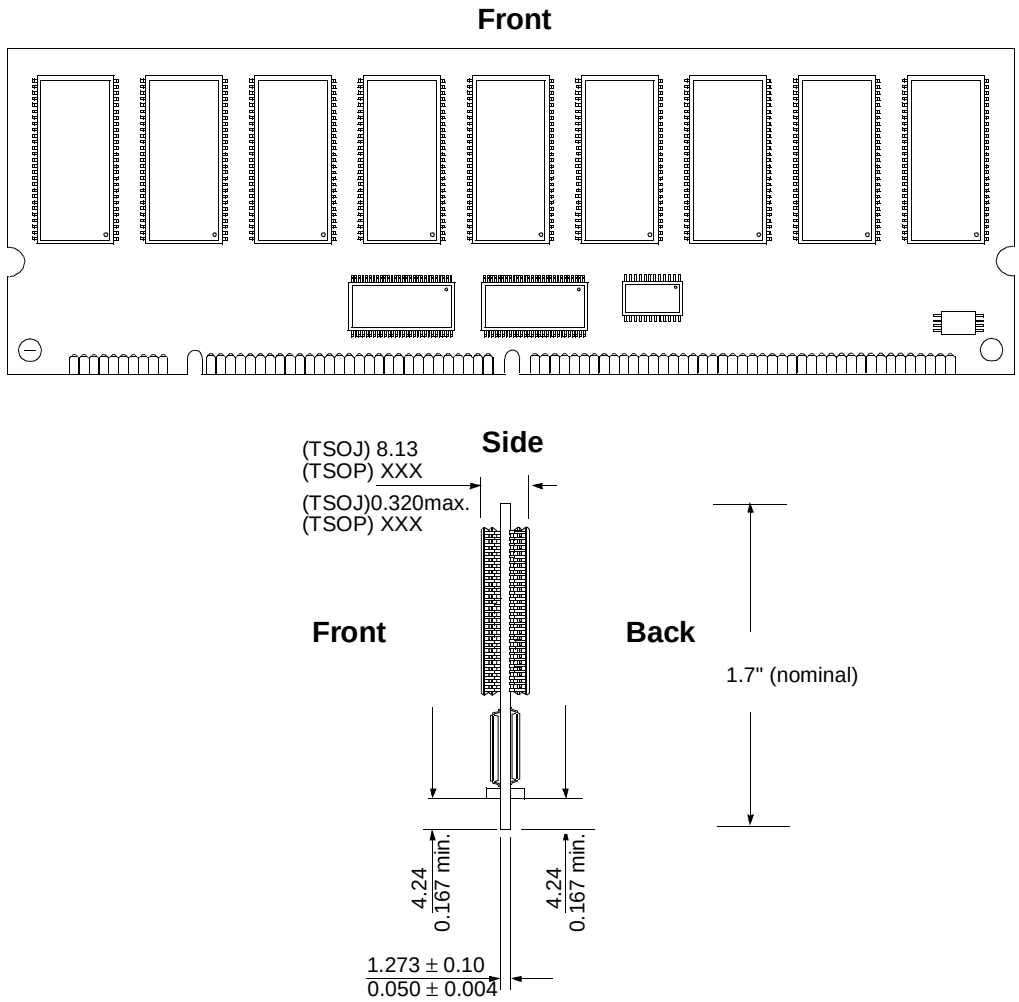
Example Raw Card Version A Component Placement



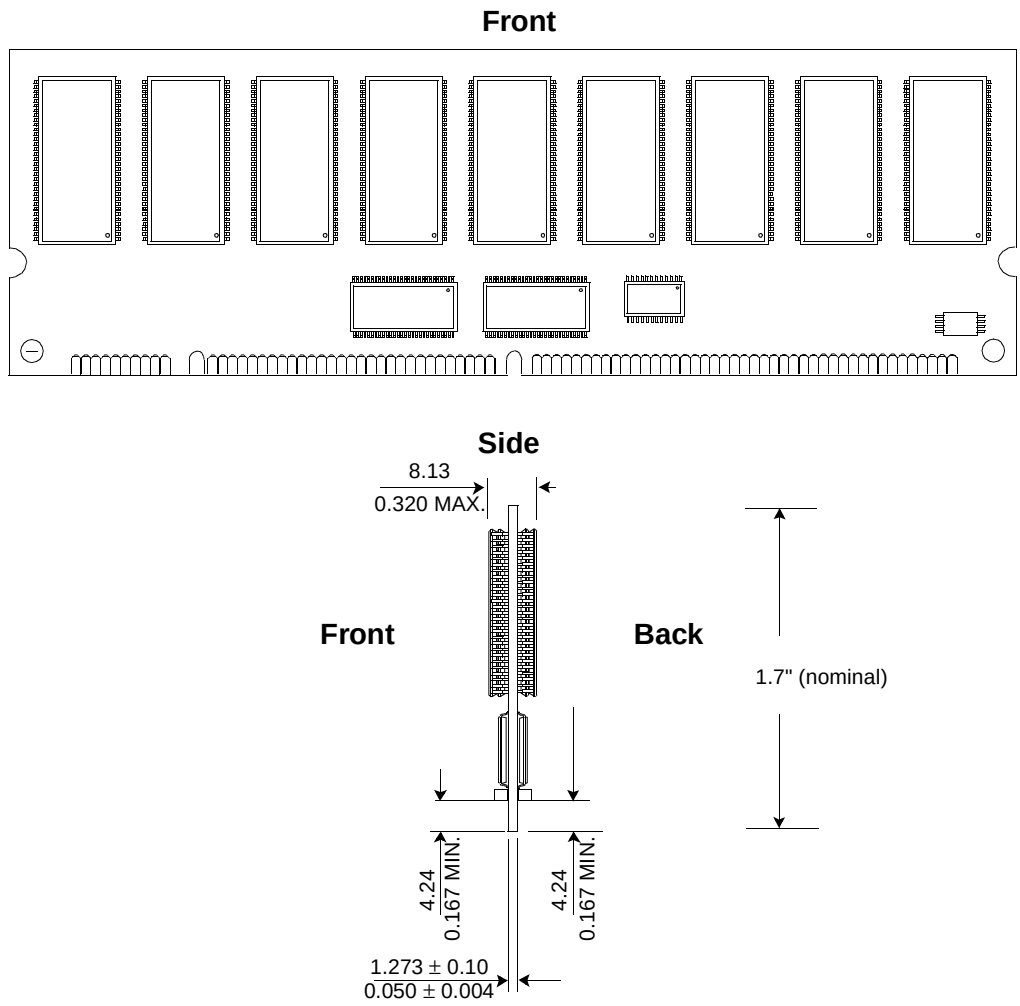
Example Raw Card Version B (Planar) and E Component Placement



Example Raw Card Versions B (Stacked) and C Component Placement



Example Raw Card Version D Component Placement



DIMM Wiring Details

Signal Groups

This specification categorizes SDRAM timing-critical signals into seven groups whose members have identical loadings and routings. The following table summarizes the signals contained in each group.

Signal Group	Signals In Group	Raw Card Version	Page
Clock (PLL input and output)	CK [3:0]	A, B, C, D	35
Data	DQ [63:0]; CB [7:0]	A, B, C, D	37
Data Mask (1, 2, or 4 loads)	DQMB[0, 2-7]	A	38
	DQMB [0, 2-4, 6-7]	B, C, D	
Data Mask (2, 3, or 6 loads)	DQMB [1]	A	39
	DQMB [1,5]	B, C, D	
Chip Select	CS [3:0]	A, B, C, D	40
Clock Enable	CKE [0,1]	A, B, C, D	43
Address/Control	Ax, BAx, RAS, CAS, WE	A	47
	A, BA, RAS, CAS	A	48
	WE	B, C, D	49

General Net Structure Routing Guidelines

Net structures and lengths must satisfy signal quality and setup/hold time requirements for the memory interface. Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace length table that lists the minimum and maximum allowable lengths for each trace segment and/or net.

The general routing requirements are as follows

- Route all signal traces except clocks using either 6/10 or 4/6 rules, i.e., 6 mil traces and 10 mil minimum spacing between adjacent traces.
- Route clocks using 4/12 or 6/18 rules.
- Route clocks using at least 90% of the total trace length in the inner layers.
- No test points are required.

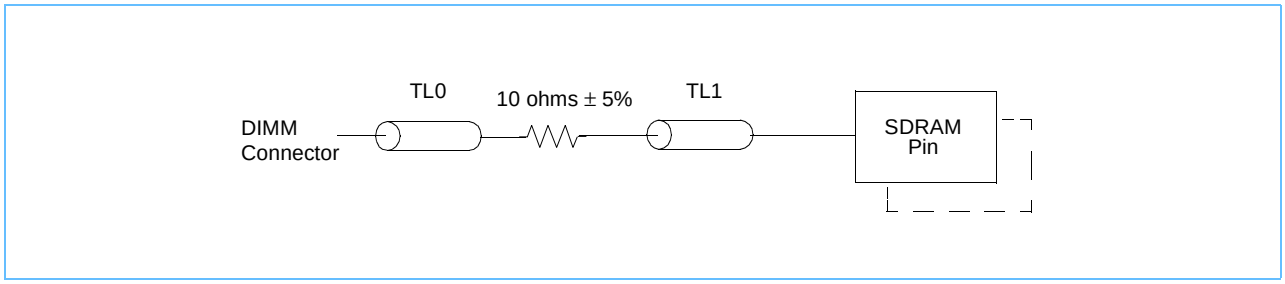
Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for registered DIMM designs. The diagrams should be used to determine individual signal wiring on a DIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators “TL”) represent physical trace segments. All other lines are zero in length. To verify DIMM functionality, a full simulation of all signal integrity and timing is required. The given net structures and trace lengths are not inclusive for all solutions.

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one SDRAM input. The net structure routing data in this document accurately represent reference Raw Card versions A, B, C, D, and E.

Net Structure Example

A 256MB double-sided ECC DIMM using 64Mbit 16Mx4 SDRAM devices would have a data net structure as shown in the following diagram.



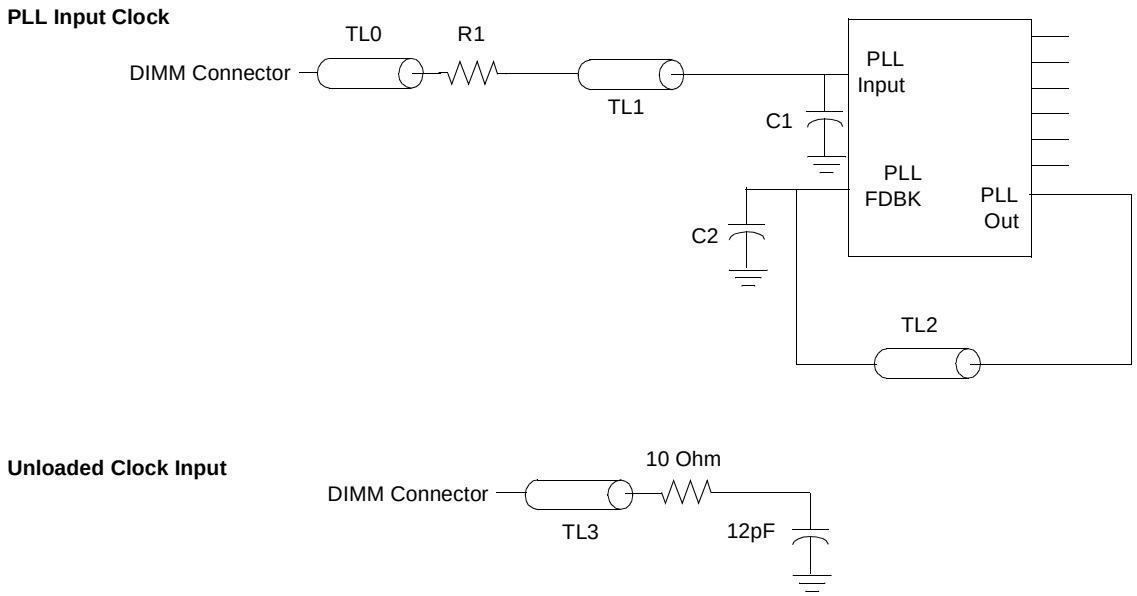
Clock Net Structures

CK[3:0]

SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality
- Rise/fall time
- SDRAM component edge skew
- Motherboard chipset clock edge skew
- Registered PC100 DIMM compatible delays (trace lengths and loads)

Net Structure Routing for PLL Clock Input

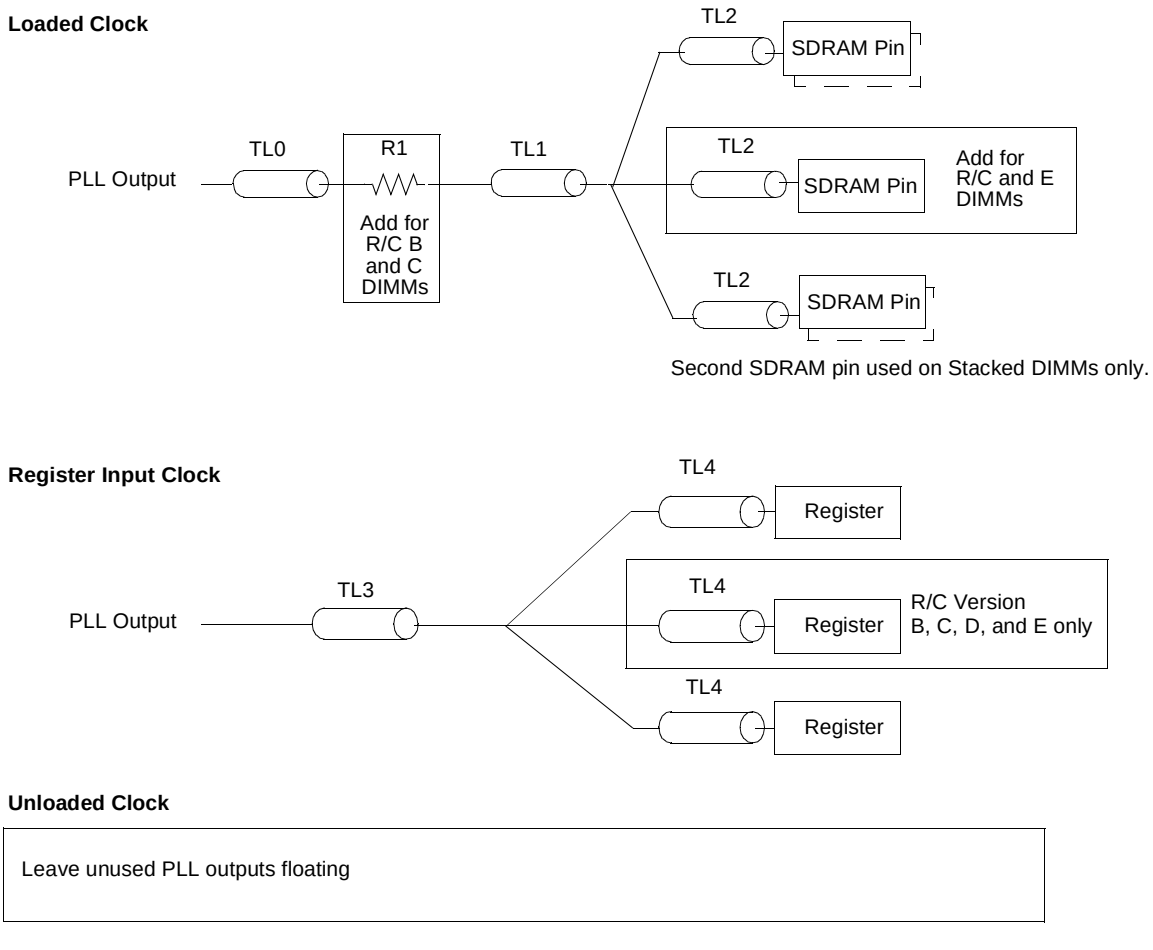


Clock Net Lengths for PLL Input Net Structures

Raw Card	TL0	TL1	TL2	TL3		R1 Ohms	C1	C2	Notes
				Min	Max				
A	0.177	2.661	3.003	0.221	0.291	10	12	12	1, 2, 3
B,&C	0.127	2.647	3.108	0.194	0.254	10	12	12	1, 2, 3
D	0.127	2.645	3.108	0.194	0.254	10	12	12	1, 2, 3
E	0.127	2.683	3.108	0.235	0.315	10	12	12	1, 2, 3

1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch.
2. All capacitances are given in pF and must be kept within a tolerance of ± 5%.
3. The value of C2 shall be determined based on the SDRAM capacitance and PLL phase characteristics of each suplier.

Net Structure Routing for PLL Clock Output



Trace Lengths for PLL Clock Output Net Structure

Raw Card	TL0		R1 Ohms	TL1		TL2		TL3	TL4		Notes
	Min	Max		Min	Max	Min	Max		Min	Max	
A	1.856	1.861	N/A	N/A	N/A	1.278	1.280	0.079	0.845	0.848	1, 2, 3
B planar	0.112	0.444	24.9	3.410	3.740	0.253	0.254	0.934	0.827	0.829	1, 2
B stacked & C	0.112	0.444	0	3.410	3.740	0.253	0.254	0.934	0.827	0.829	1, 2
D	3.417	3.453	N/A	N/A	N/A	0.227	0.228	0.934	0.827	0.829	1, 2, 3
E	3.549	3.558	N/A	N/A	N/A	0.369	0.371	0.934	0.827	0.829	1, 2, 3

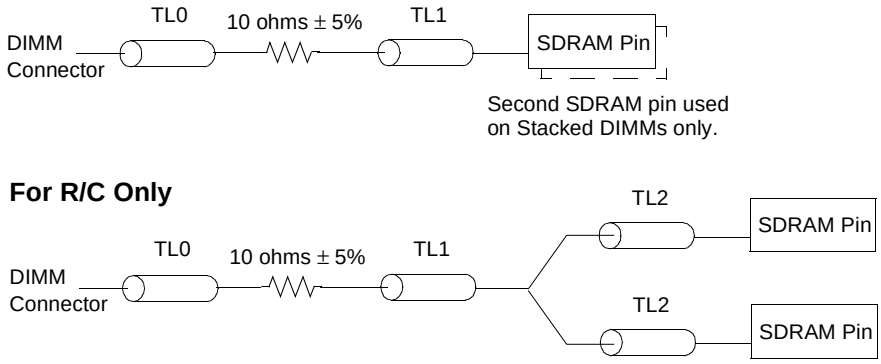
1. All distances are in inches and should be kept within a tolerance of ± 0.01 inch
2. All capacitances are given in pF and should be kept within a tolerance of ± 5%
3. R/C A, D, and E do not have R1, therefore TL0 in the table equals TL0 + TL1 in the diagram

Data Net Structures

DQ[63:0] and CB[7:0]

For specifying trace segment lengths, data lines have been grouped according to the location of their edge connector pins. These two data groups specify segment lengths that make the data lines connecting to the outside edge of the DIMM connector shorter in minimum and maximum length than those data lines on the inside edge of the DIMM connector. This allows the designer to pair longer data line traces on the mother-board with potentially shorter traces on DIMMs, and to pair longer DIMM traces with potentially shorter traces on the motherboard. Data Group 1 includes data line DQ [63-56, 39-24, 7-0]. Data Group 2 includes data lines DQ [55-40, 23-8] and CB [7-0].

Net Structure Routing for Data



Trace Lengths for Data Net Structure

Raw Card	Data Group	TL0		TL1		TL2		Total		Notes
		Min	Max	Min	Max	Min	Max	Min	Max	
A	I	0.136	0.176	0.799	0.869	N/A	N/A	0.838	1.040	1, 2
	II	0.134	0.312	0.787	1.018	N/A	N/A	0.942	1.285	1, 2
B & C	I	0.127	0.148	1.013	1.067	N/A	N/A	1.145	1.203	1, 2
	II	0.126	0.345	1.291	1.415	N/A	N/A	1.453	1.658	1, 2
D	I	0.128	0.148	1.014	1.020	N/A	N/A	1.143	1.163	1, 2
	II	0.126	0.344	1.292	1.380	N/A	N/A	1.429	1.645	1, 2
E	I	0.127	0.147	0.833	1.046	0.044	0.046	1.050	1.272	1, 2
	II	0.126	0.343	1.192	1.369	0.044	0.046	1.143	1.761	1, 2

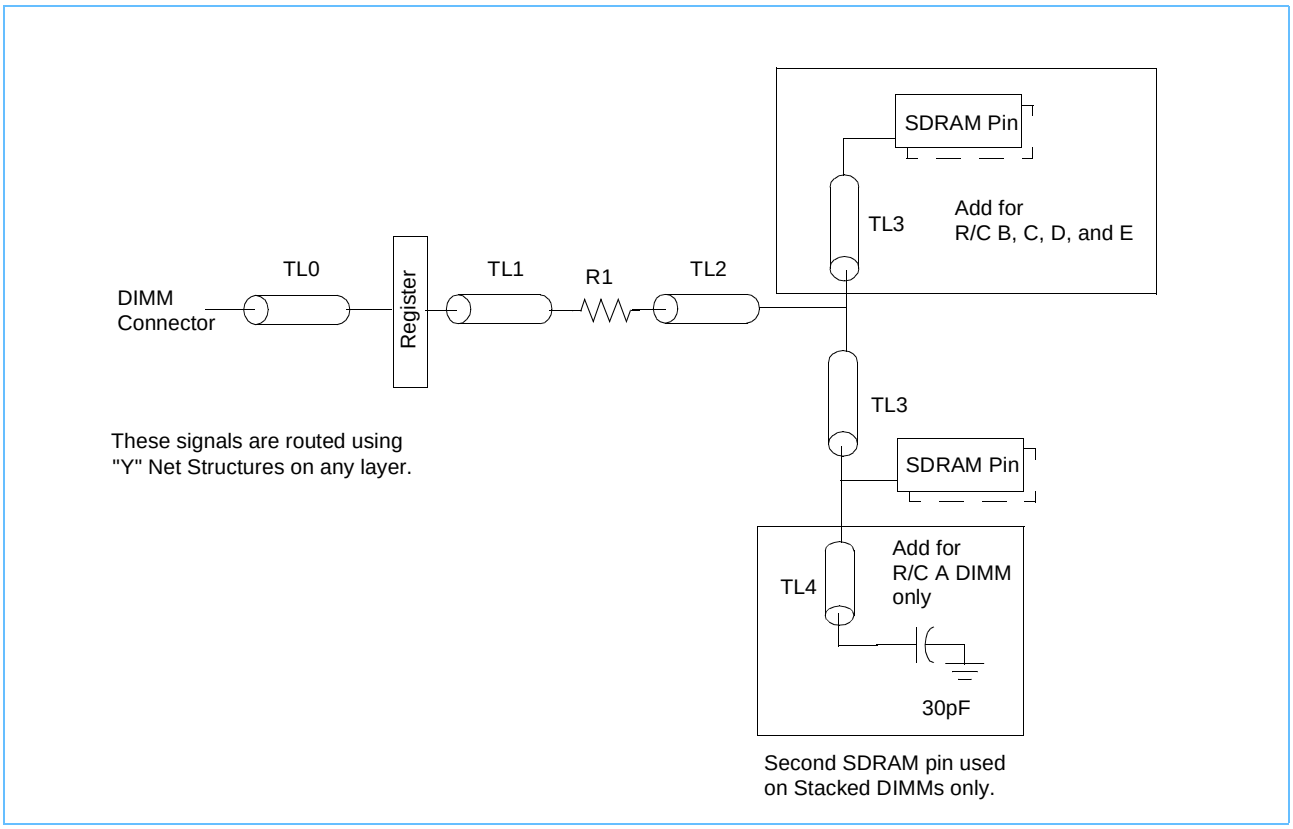
1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inch
2. Total Min and Total Max refer to the min and max respectively of L0 + L1.

Data Mask Net Structures

1/2/4 Loads: DQMB[0,2-7] for Raw Card Version A and DQMB[0,2-4,6-7] for Raw Card Versions B, C, D, and E.

Data Mask loading and net structures vary based on the specific DQMB pin, the card architecture, and DRAM organization. The following pages describe each of the net structures utilized on the reference designs.

Net Structure Routing for Data Mask (1/2/4 Loads)



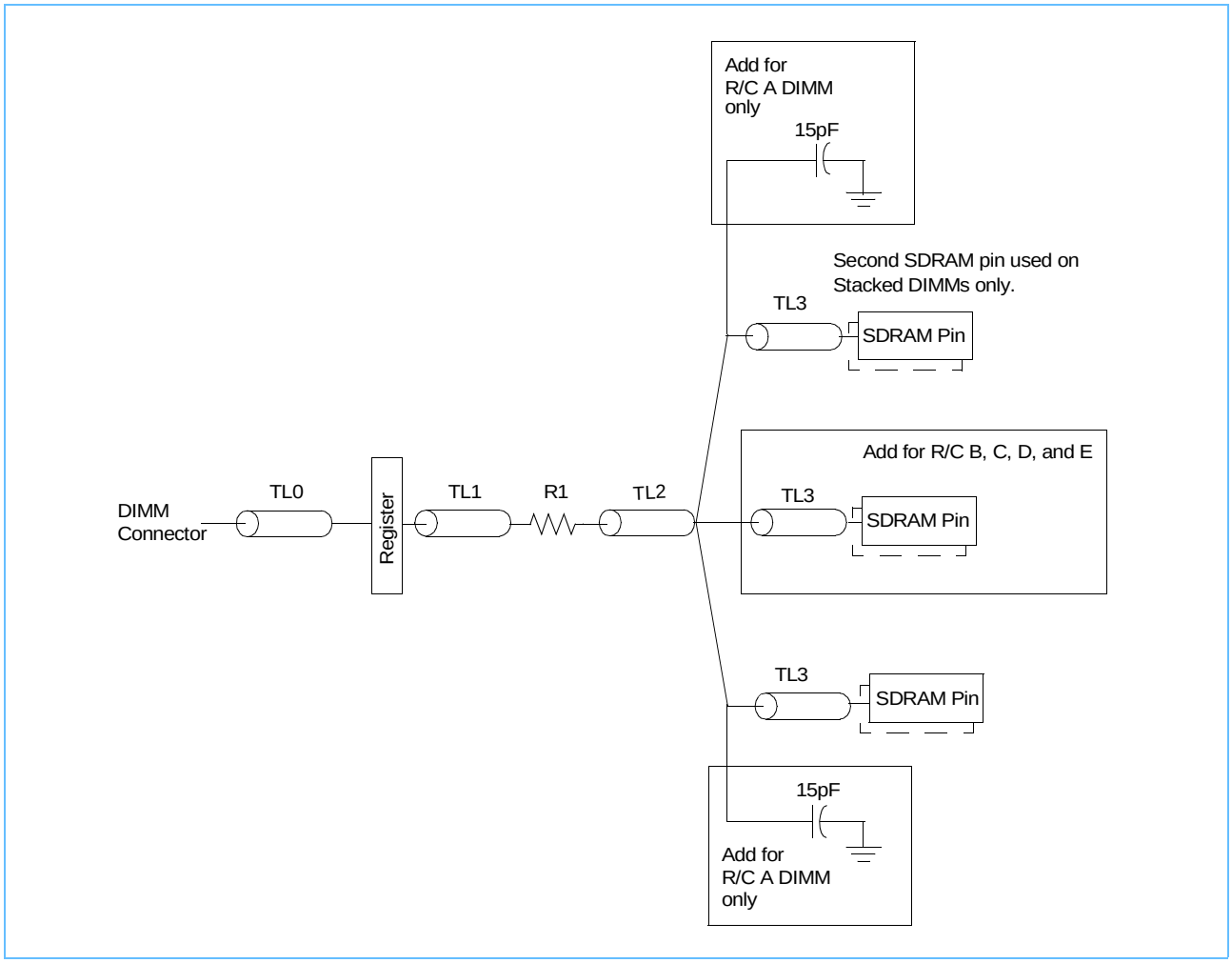
Trace Lengths for Data Mask Net Structures (1/2/4 Loads)

Raw Card	# of Loads	TL0		TL1		TL2		TL3		TL4		R1 Ohms	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
A	1	0.275	0.342	0.113	0.142	0.726	1.631	N/A	N/A	0.098	0.102	24.9	1, 2
B	2 or 4	0.199	0.991	0.170	0.259	2.710	2.783	0.729	0.885	N/A	N/A	49.9	1
C	4	0.198	0.989	0.169	0.259	2.714	3.069	0.700	0.825	N/A	N/A	49.9	1
D	4	0.199	0.990	0.170	0.259	2.882	3.500	0.384	0.385	N/A	N/A	30.0	1
E	2	0.199	0.990	0.170	0.259	2.697	3.084	0.803	0.872	N/A	N/A	49.9	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.
2. For Raw Card Version A, L2 = L2 + L3 as represented in the diagrm above.

2/3/6 Loads: DQMB[1] for Raw Card Version A and DQMB[1,5] for Raw Card Versions B,C, D, and E

Net Structure Routing for Data Mask (2/3/6 Loads)



Trace Lengths for Data Mask Net Structures (2/3/6 Loads)

Raw Card	# of Loads	TL0		TL1		TL2		TL3		R1 Ohms	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
A	6	0.887	1.167	0.101	0.124	3.101	3.108	0.081	0.664	30.0	1
B	3 or 6	0.887	1.070	0.101	0.125	2.767	2.780	0.770	0.892	49.9	1
C	6	0.885	1.069	0.101	0.125	2.766	2.779	0.740	0.862	49.9	1
D	6	0.887	1.167	0.101	0.124	3.101	3.108	0.081	0.664	30.0	1
E	3	0.886	0.970	0.102	0.124	2.676	2.721	0.814	0.899	49.9	1

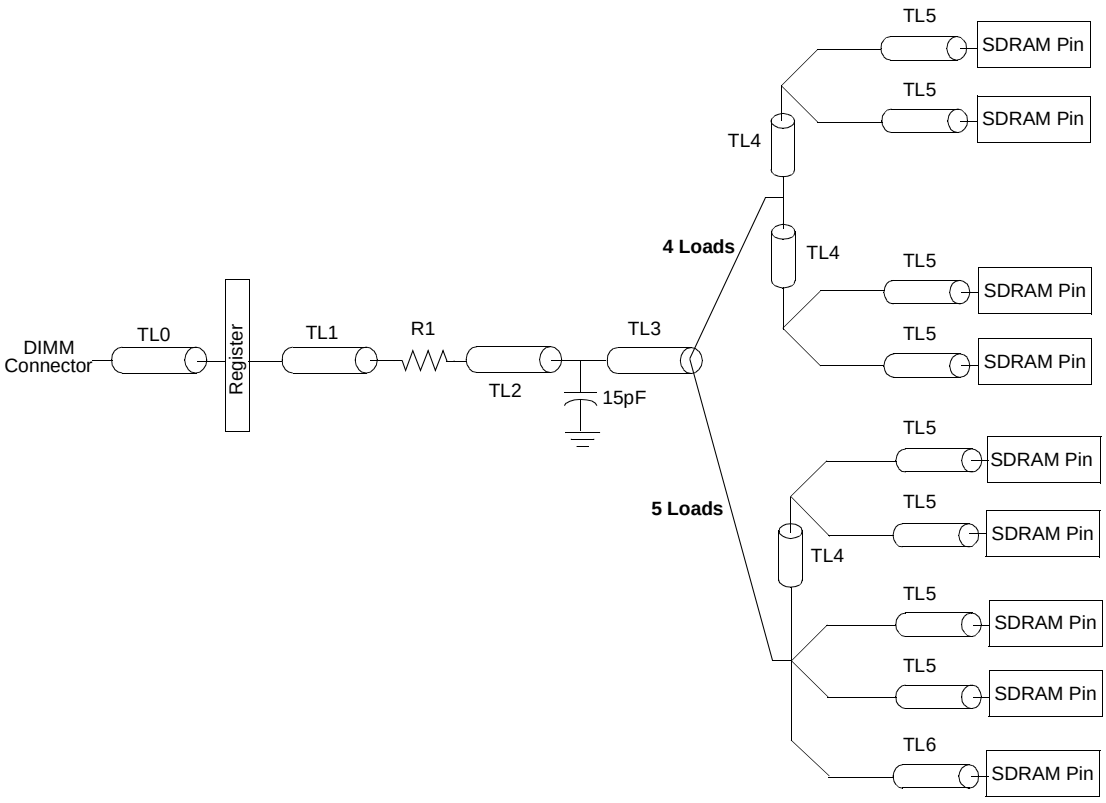
1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

Chip Select Net Structures

$\overline{CS}$ [3:0]

Two fundamental net structures are defined for Chip Selects, depending on whether x4 or x8 SDRAMs are used.

Net Structure Routing for Chip Select (Raw Card Version A)

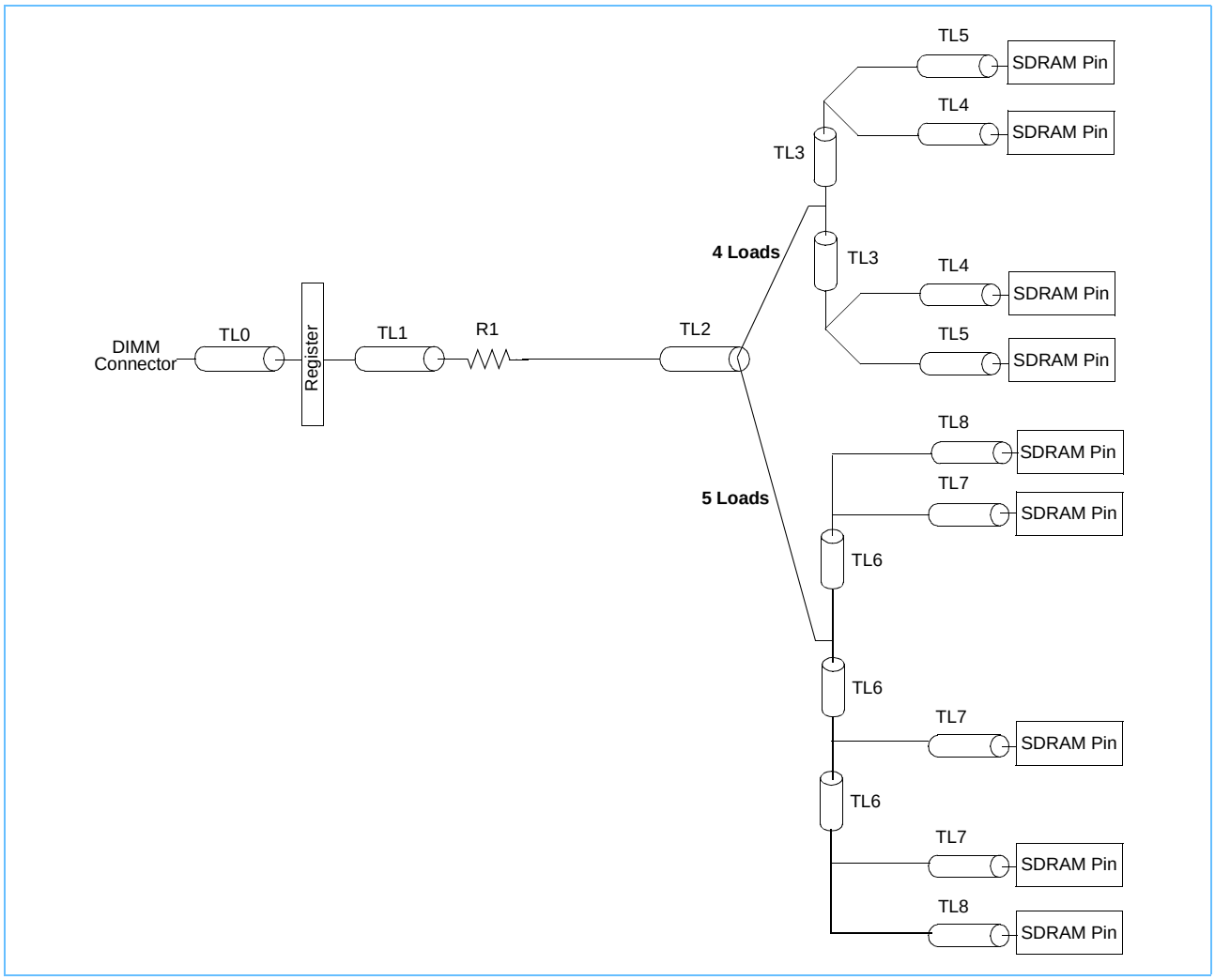


Trace Lengths for Chip Select Net Structures ($\overline{S0}$ - $\overline{S3}$, $\overline{S2}$)

Raw Card	# of Loads	TL0		TL1		TL2		TL3	TL4		TL5		TL6		R1 Ohms	Notes
		Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max		
A ($\overline{S0}$ Net)	5	N/A	0.329	N/A	0.10	N/A	0.416	0.672	N/A	0.684	0.134	0.368	N/A	1.312	20.0	1
A ($\overline{S2}$ Net)	4	N/A	0.293	N/A	0.120	N/A	1.039	0.370	0.238	0.461	0.134	0.370	N/A	N/A	24.9	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

Net Structure Routing for Chip Select (Raw Card Version E)

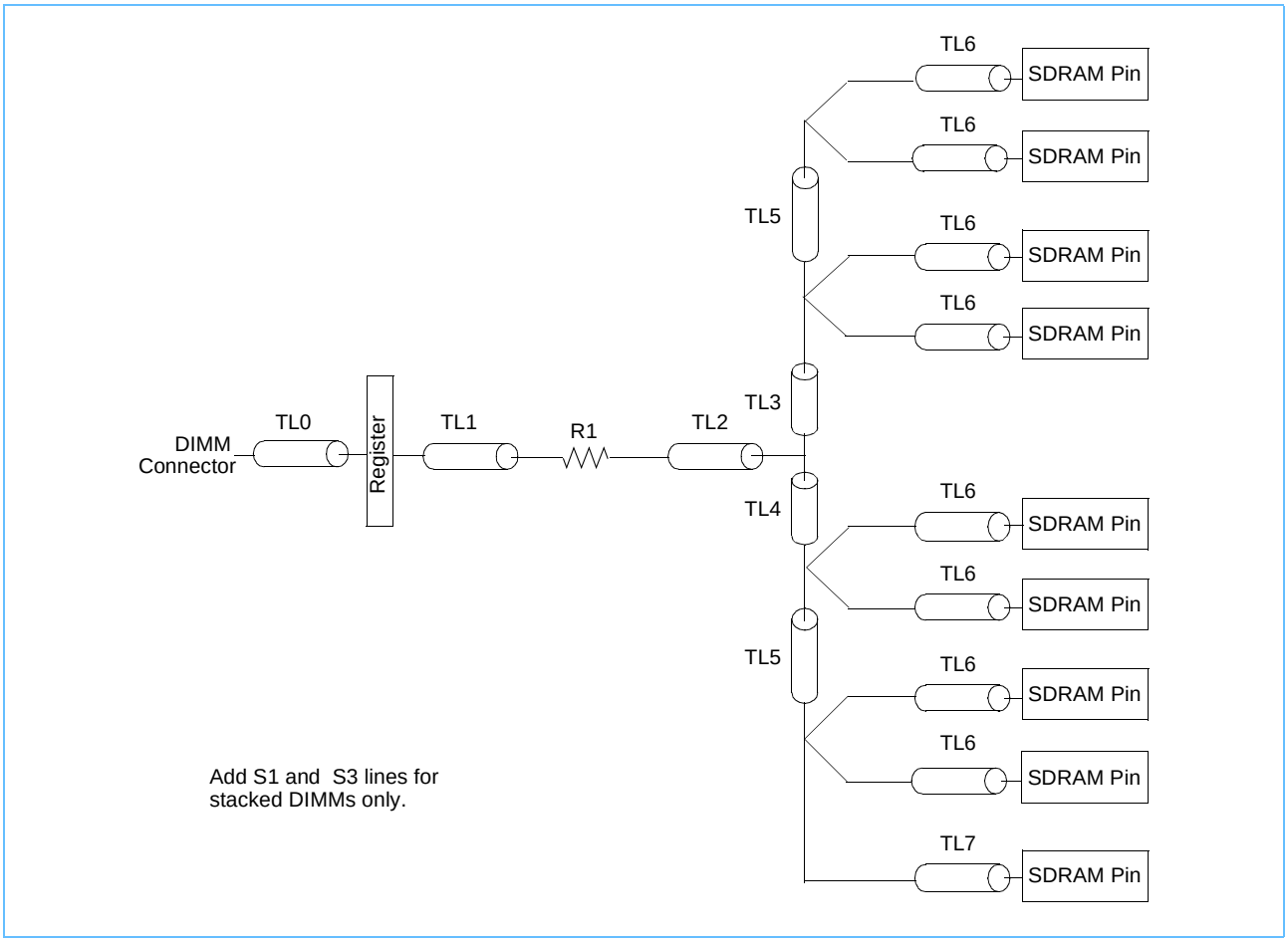


Trace Lengths for Chip Select Net Structures ($\overline{S0}$ - $\overline{S3}$)

Raw Card	# of Loads	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		R1 Ω	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
E	E($\overline{S0}$, $\overline{S1}$ Net)	5	0.923	1.089	0.171	0.206	3.017	3.086	N/A	N/A	N/A	N/A	N/A	N/A	0.591	0.624	0.061	0.062	0.062	0.672	0	1
E	E($\overline{S2}$, $\overline{S3}$ Net)	4	0.239	0.247	0.140	0.170	3.250	3.253	0.300	0.590	0.061	0.062	0.654	0.674	N/A	N/A	N/A	N/A	N/A	N/A	0	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

Net Structure Routing for Chip Select (Raw Card Versions B, C, D)



Trace Lengths for Chip Select Net Structures (S0, S1, S2, S3)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
B	0.232	1.336	0.140	0.206	2.760	2.868	0.389	0.580	0.148	0.152	0.527	0.617	0.173	0.311	0.781	0.874	0	1
C	0.232	1.122	0.140	0.206	2.636	2.775	0.389	0.533	0.147	0.585	0.430	0.616	0.158	0.253	0.514	0.827	0	1
D	0.214	1.195	0.153	0.206	2.268	2.707	0.100	0.561	0.084	0.514	0.477	0.679	0.148	0.356	0.749	0.856	0	1

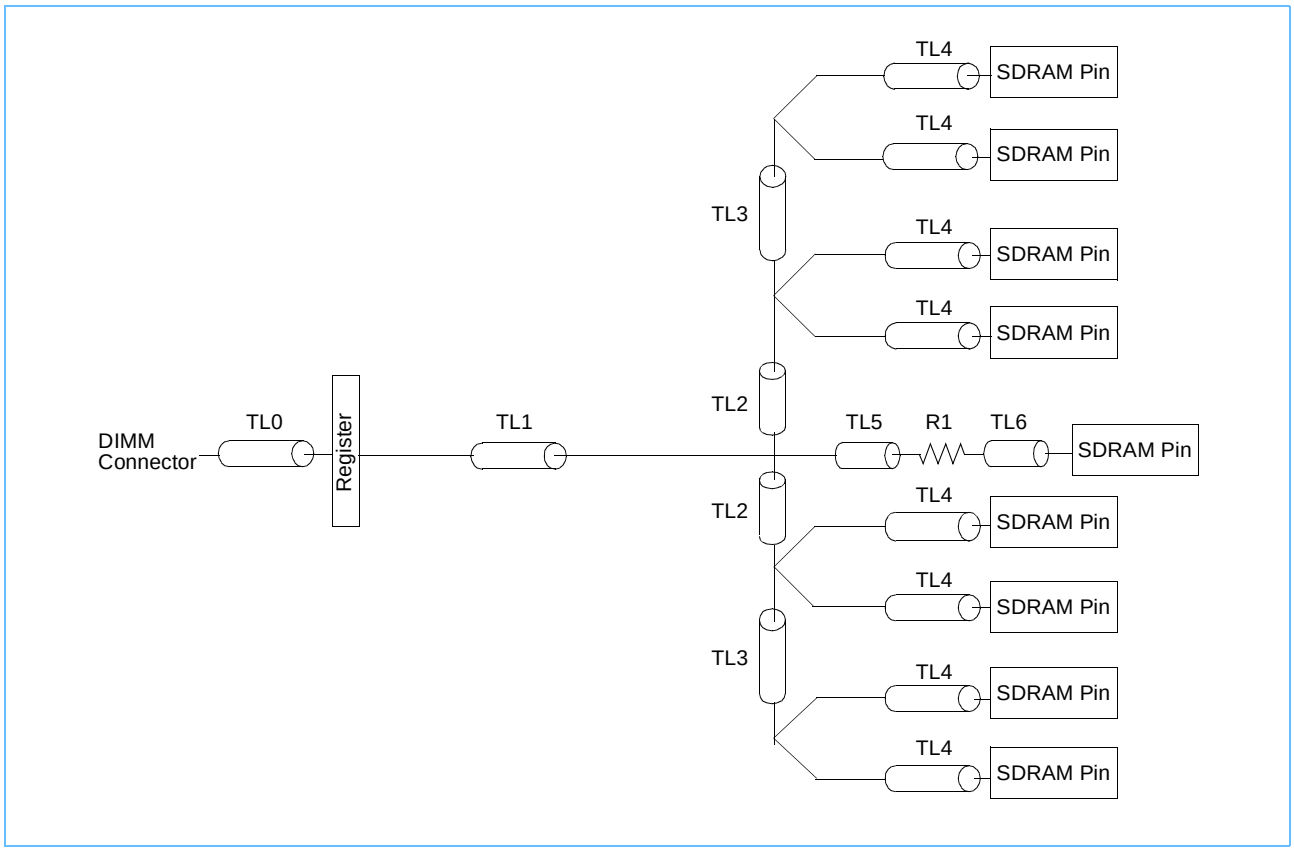
1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

Clock Enable Net Structures

CKE [0]

CKE0 is connected to all SDRAMs on the card, similar to an address. At this time, CKE1 is not uniquely wired on raw card versions A, B, and C or D. Raw Card E can be produced with either CKE0 wired to all of the SDRAMs, or CKE0 can be wired to one physical bank and CKE1 wired to the other physical bank.

Net Structure Routing for Clock Enable (Raw Card Version A)

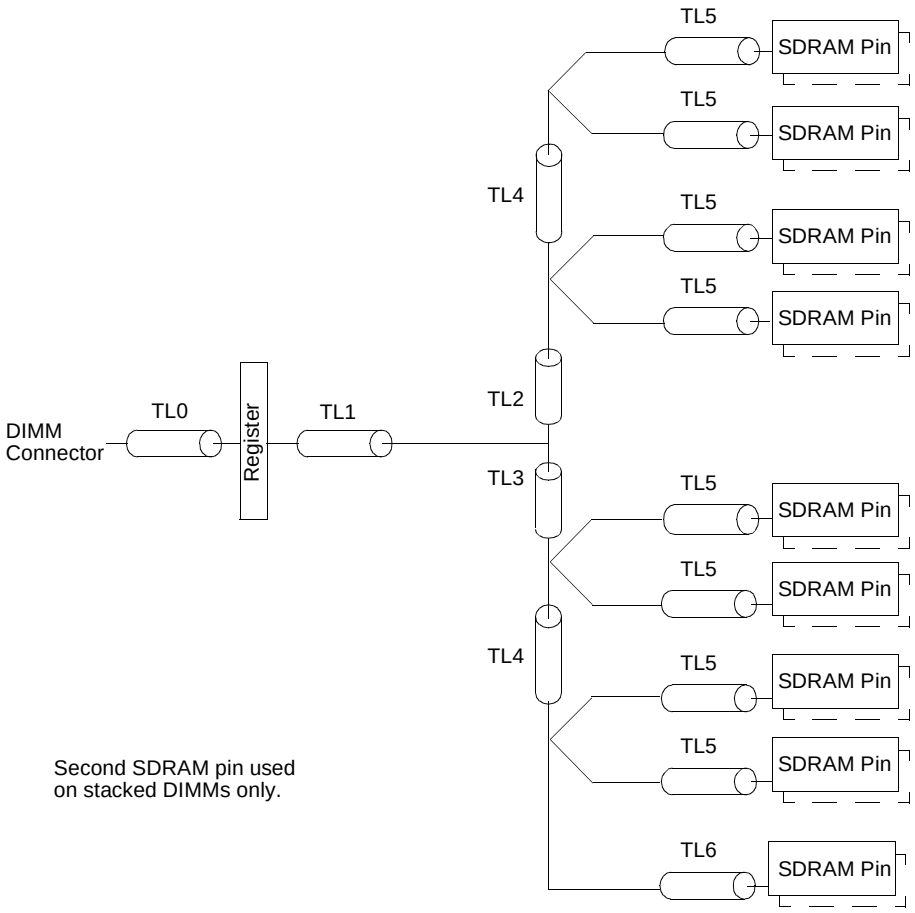


Trace Lengths for Clock Enable Net Structure (Raw Card A)

Raw Card	No. of loads	TL0	TL1	TL2	TL3	TL4		TL5	R1 Ohms	Notes
						Min	Max			
A	9	0.297	1.315	1.438	0.700	0.204	0.273	0.046	100	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

Net Structure Routing for Clock Enable (Raw Cards B, C, & D)



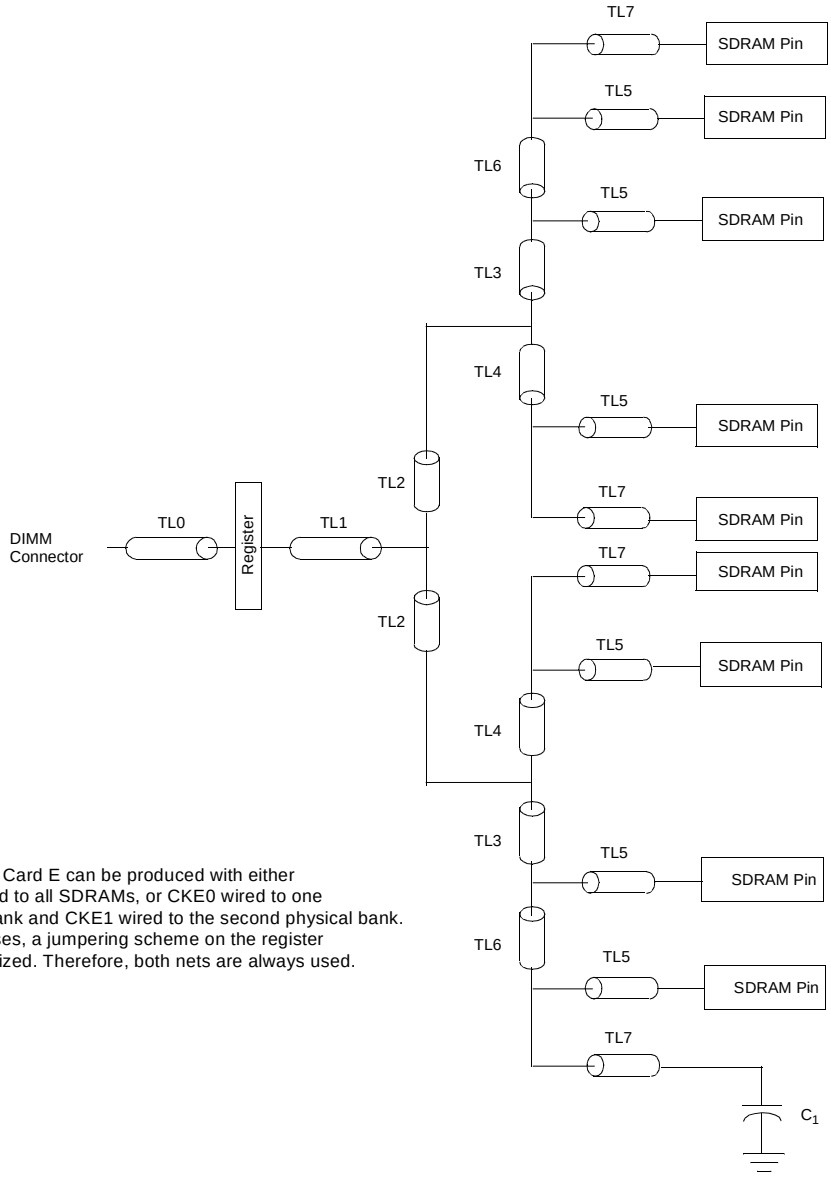
Note: These signals are double loaded on the input to the register so this net structure is repeated twice.

Trace Lengths for Clock Enable Net Structures (Raw Cards B, C, & D)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
B	0.784	1.03	2.844	2.899	0.459	0.530	0.145	0.150	0.527	0.630	0.210	0.286	0.535	0.662	1
C	0.782	0.819	2.880	2.897	0.458	0.476	0.144	0.149	0.527	0.564	0.193	0.260	0.505	0.529	1
D	N/A	0.702	1.900	2.322	N/A	0.463	0.150	0.153	N/A	0.555	0.114	0.137	0.652	0.711	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

Net Structure Routing for Clock Enable (Raw Cards E)



Note: Raw Card E can be produced with either CKE0 wired to all SDRAMs, or CKE0 wired to one physical bank and CKE1 wired to the second physical bank. In both cases, a jumpering scheme on the register input is utilized. Therefore, both nets are always used.

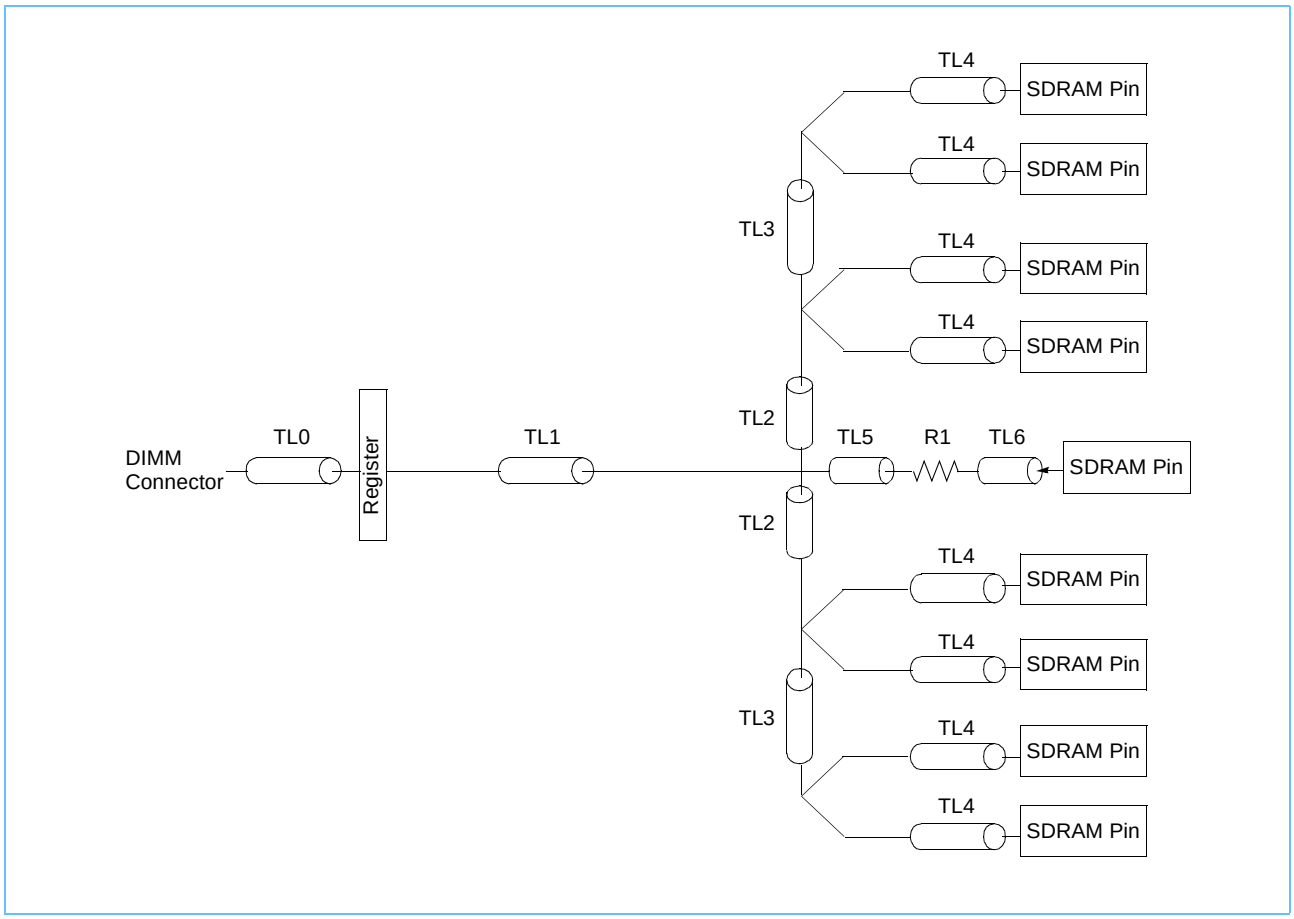
Trace Lengths for Clock Enable Net Structure (Raw Card E)

Raw Card	# of Loads	TL0	TL1	TL2		TL3		TL4		TL5		TL6		TL7		C_1pF
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
E (CKE0)	10	0.371	0.867	1.564	1.596	0.249	0.276	0.355	0.363	0.060	0.062	0.602	0.607	0.646	0.663	3.0
E (CKE1)	10	1.065	1.507	1.557	1.560	0.217	0.253	0.374	0.380	0.056	0.062	0.596	0.600	0.642	0.699	3.0
1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.																

Address/Control Net Structures

Ax, BAx, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ for Raw Card Version A

Net Structure Routing for Address and Control



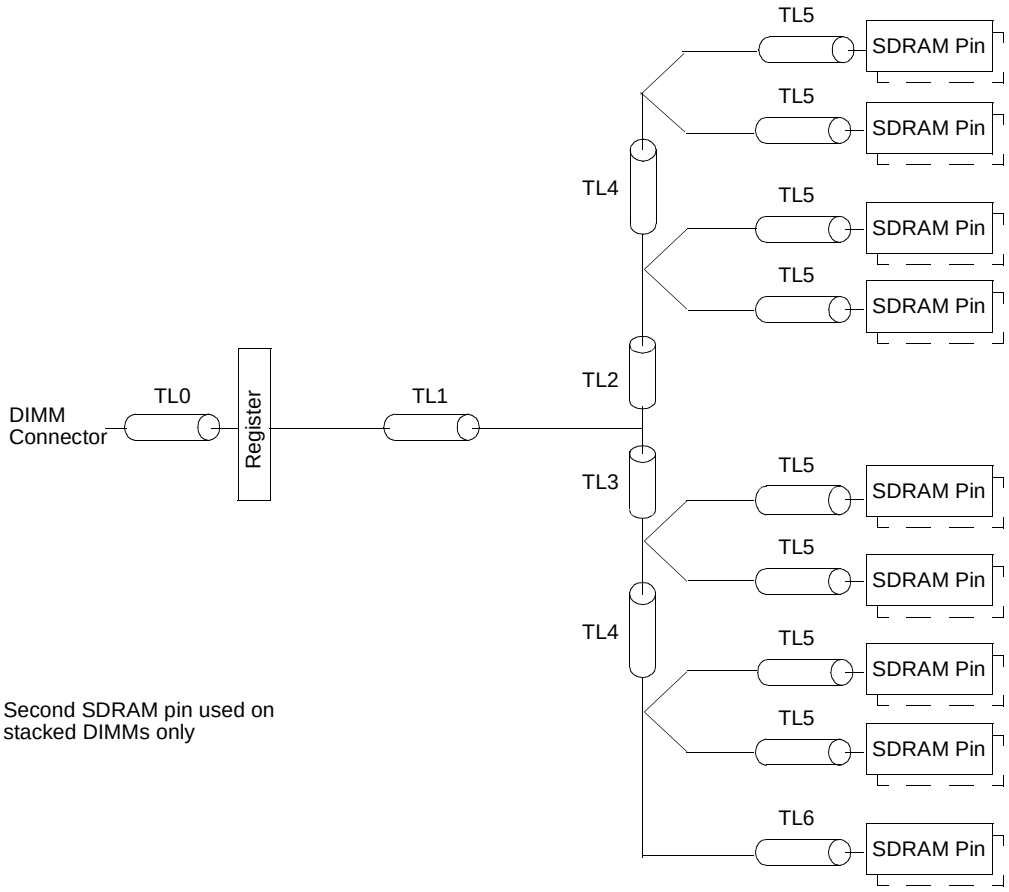
Trace Lengths for Address and Control Net Structures

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
A	0.328	0.686	1.295	1.329	1.256	1.405	0.661	0.704	0.125	0.375	0.058	0.182	0.127	0.272	100	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

A, BA, $\overline{RAS}$, $\overline{CAS}$ for Raw Card Versions B, C, D, and E

Net Structure Routing for Address and Control



Note: These signals are double loaded on the input to the register, so this net structure is repeated twice.

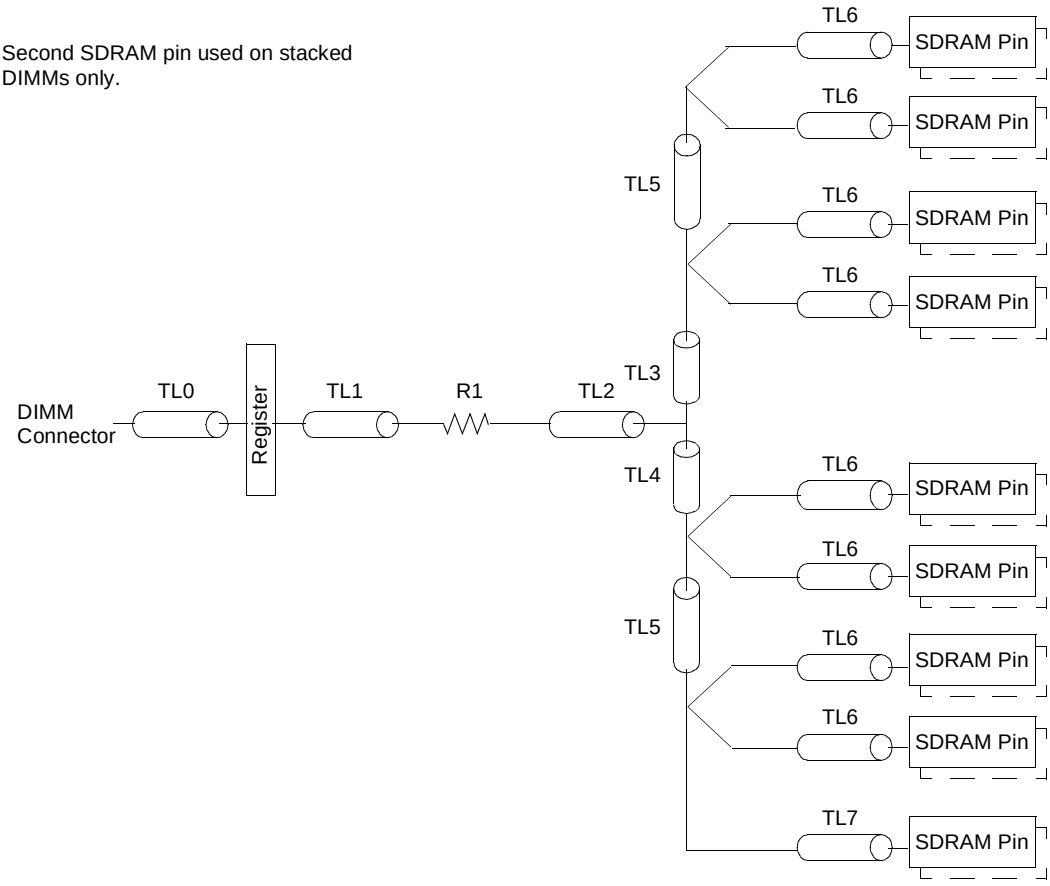
Trace Lengths for Address and Control Net Structures

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
B	0.254	0.583	2.454	3.535	0.389	0.492	0.145	0.150	0.527	0.625	0.201	0.287	0.538	0.704	1
C	0.254	0.441	2.483	3.535	0.389	0.492	0.145	0.154	0.527	0.625	0.172	0.287	0.533	0.704	1
D	0.224	0.527	0.222	0.345	0.358	0.576	0.125	0.211	0.470	0.577	0.169	0.275	0.634	0.846	1
E	0.209	0.526	2.456	3.611	0.126	0.499	0.097	0.463	0.528	0.708	0.196	0.330	0.540	0.805	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

$\overline{WE}$ for Raw Card Versions B, C, D, and E

Net Structure Routing for Write Enable



Note: These signals are double loaded on the input to the register, so this net structure is repeated twice.

Trace Lengths for Write Enable Net Structure

Raw Card	TL0	TL1		TL2		TL3		TL4		TL5		TL6		TL7		R1 Ohms	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
B	1.189	0.117	0.129	2.793	2.793	0.489	0.507	0.149	0.150	0.549	0.596	0.229	0.253	0.674	0.756	0	1
C	1.249	0.117	0.129	2.792	2.831	0.489	0.507	0.148	0.150	0.549	0.596	0.200	0.224	0.643	0.726	0	1
D	1.223	0.128	0.130	N/A	1.28	N/A	0.432	0.128	0.150	0.552	0.577	0.169	0.275	0.732	0.745	0	1
E	1.187	0.117	0.129	2.608	2.733	0.495	0.563	0.100	0.128	0.541	0.605	0.224	0.287	0.733	0.804	0	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

Cross Section Recommendations

The DIMM printed circuit board design uses six-layers of glass epoxy material. PCBs must contain full ground plane and full power plane layers. The PCB stackup must be designed with either 4 or 6 mil wide traces.

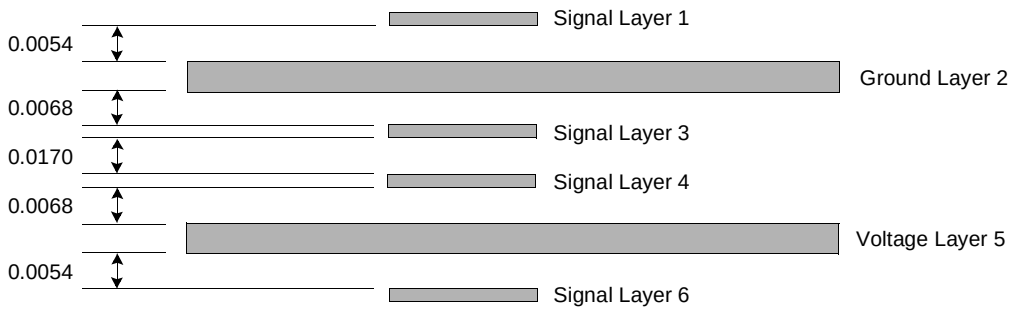
Note: The PCB edge connector contacts shall be gold-plated and not chamfered.

PCB Electrical Specifications

Parameter	Min	Max	Units
Trace velocity: S0 (outer layers)	1.6	2.2	ns/ft
Trace velocity: S0 (inner layers)	2.0	2.2	ns/ft
Trace impedance: Z0 (all layers)	58.5	71.5	Ohms

Example Layer Stackup for 6 mil Traces

Example Layer Stackup for 4 mil Traces



Timing Budget

The post-register timings on the Registered DIMMs are critical. The following table describes the post-register timing budget for a typical PC133 Registered DIMM, under these conditions:

- Raw Card Version ‘B’, Planar Configuration
- SDRAM Input Capacitance range of 2.6pF to 3.1pF
- IDT Register- P/N ALVCF162835A
- Worst Case Transition (High to Low or Low to High)
- ‘t_{CO}’ (no load) timing methodology

DIMM Post-Register Timing

Symbol	Parameter	Time (ns) Set-up	Time (ns) Hold	Notes
t_{CLK}	Clock cycle time	7.50	7.50	1
t_{CO}	Maximum time for the signal to exit the register. This is measured into a 0pF load.	–2.11	1.31	1, 2
t_{PD}	Maximum time for the signal to propagate from the register to any SDRAM. The switching point for a rising edge is 1.6Volts, and 1.2Volts for a falling edge.	–2.66	0.77	1, 2
t_{REG}	Shift in the register clock in relationship to the SDRAM. The input clocks to the registers and the SDRAM are purposely skewed to aid in the setup time of the signals into the SDRAM.	0.35	–0.55	1
t_{IS}	Setup time required for the SDRAM inputs	–1.50	NA	1
t_{IH}	Hold time required for the SDRAM inputs	NA	–0.80	1
t_{Skew}^{*}	Clock jitter and skew on the DIMM	–0.325	-0.25	1
t_{SS}	Simultaneous Switch adder	–0.35	NA	1, 2
Margin		**0.91**	**0.48**	1

Note:

1. The timing values shown are consistent with registers available at the time this specification was written. All registers must meet the combined delay values and ensure positive margin, although the specific delay value for each term may vary.
2. The timing values for t_{CO}, t_{PD}, and t_{SS}, when added together, define the overall delay from clock at the register to the time when the last re-driven signal arrives at the SDRAM (setup time), or earliest re-driven signal changes state after clock (hold time).

*DIMM Clock Contributions (t_{Skew})

t_{Skew} for Setup		Units
DIMM PLL JItter	0.75	ns
DIMM PLL Skew	0.150	ns
DIMM Clock Net Skew	0.10	ns
Total	0.325	ns

t_{Skew} for Hold		Units
DIMM PLL Skew	0.150	ns
DIMM Clock Net Skew	0.10	ns
Total	0.250	ns

Other methods can be used to evaluate post-register timings. One such method is ‘Time to Vm’ that uses the register timing into its specified test load (instead of t_{CO}, open circuit) and adds or subtracts the timing into the SDRAM net and loads. Both of these timing methods were used in the design of the ‘reference DIMMs’. The same overall timing budget must be maintained, regardless of the timing method used.

Serial PD Definition

The Serial Presence Detect function MUST be implemented on the PC SDRAM Registered DIMM. The component used and the data contents must adhere to the most recent version of the JEDEC SDRAM Serial Presence Detect Specifications. Please refer to this document for all technical specifications and requirements of the serial presence detect devices.

The following table is intended to be an **example** of a typical PC133 DIMM programmed for 3/3/3 (CL/tRP/tRCD), 133MHz operation. This SPD table is also programmed with 100MHz and 66MHz operation in order to maintain compatibility with these other frequency range operations. SPD values indicating different DIMM performance characteristics, such as CL = 2 operation at 133MHz, will be utilized based on a specific DIMMs' characteristics.

Serial Presence Detect Data EXAMPLE Raw Card Version 'B', 16Mx72 Registered DIMM (Part 1 of 2)

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
0	Number of Serial PD Bytes Written during Production	128	80	
1	Total Number of Bytes in Serial PD device	256	08	
2	Fundamental Memory Type	SDRAM	04	
3	Number of Row Addresses on Assembly	12	0C	
4	Number of Column Addresses on Assembly	10	0A	
5	Number of DIMM Banks	1	01	
6 - 7	Data Width of Assembly	x72	4800	
8	Assembly Voltage Interface Levels	LVTTL	01	
9	SDRAM Device Cycle Time (CL = 3)	7.5ns	75	1, 2
10	SDRAM Device Access Time from Clock at CL= 3	5.4ns	54	
11	Assembly Error Detection/Correction Scheme	ECC	02	
12	Assembly Refresh Rate/Type	SR/1X(15.625µs)	80	
13	SDRAM Device Width	x4	04	
14	Error Checking SDRAM Device Width	x4	04	
15	SDRAM Device Attr: Min Clk Delay, Random Col Access	1 Clock	01	
16	SDRAM Device Attributes: Burst Lengths Supported	1, 2, 4, 8, Full Page	8F	
17	SDRAM Device Attributes: Number of Device Banks	4	04	
18	SDRAM Device Attributes: $\overline{\text{CAS}}$ Latency	2, 3	06	
19	SDRAM Device Attributes: $\overline{\text{CS}}$ Latency	0	01	
20	SDRAM Device Attributes: $\overline{\text{WE}}$ Latency	0	01	
21	SDRAM Module Attributes	Registered/Buffered with PLL	IF	

1. In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM $\overline{\text{CAS}}$ latency).
2. Minimum application clock cycle time is 7.5ns (133MHz).
3. cc = Checksum Data byte, 00-FF (Hex).
4. ww = Binary coded decimal week code, 01-51 (Decimal) ' 01-34 (Hex).
5. yy = Binary coded decimal year code, 0-00 (Decimal) ' 00-63 (Hex).
6. ss = Serial number data byte, 00-FF (Hex).
7. These values apply to PC100 applications only, per Intel PC66/100 SPD standards.

Serial Presence Detect Data EXAMPLE Raw Card Version 'B', 16Mx72 Registered DIMM (Part 2 of 2)

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
22	SDRAM Device Attributes: General	Write-1/Read Burst, Pre-charge All, Auto-Precharge	0E	
23	Minimum Clock Cycle at CLX-1 (CL = 2)	15.0ns	F0	1, 2
24	Maximum Data Access Time (t_{AC}) from Clock at CLX-1 (CL = 2)	9.0ns	90	
25	Minimum Clock Cycle Time at CLX-2 (CL = 1)	N/A	00	
26	Maximum Data Access Time (t_{AC}) from Clock at CLX-2 (CL = 1)	N/A	00	
27	Minimum Row Precharge Time (t_{RP})	20.0ns	14	
28	Minimum Row Active to Row Active delay (t_{RRD})	15.0ns	0F	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD})	20.0ns	14	
30	Minimum $\overline{RAS}$ Pulse width (t_{RAS})	45.0ns	2D	
31	Module Bank Density	128MB	20	
32	Address and Command Setup Time Before Clock	1.5ns	15	
33	Address and Command Hold Time After Clock	0.8ns	08	
34	Data Input Setup Time Before Clock	1.5ns	15	
35	Data Input Hold Time After Clock	0.8ns	08	
36 - 61	Reserved	Undefined	00	
62	SPD Revision	JEDEC 2	02	
63	Checksum for bytes 0 - 62		cc	3
64 - 71	Manufacturers' JEDEC ID Code			
72	Assembly Manufacturing Location			
73 - 90	Assembly Part Number			
91 - 92	Assembly Revision Code			
93 - 94	Assembly Manufacturing Date			4, 5
95 - 98	Assembly Serial Number			6
99 - 125	Reserved			
126	Reserved		64	7
127	Reserved		85	7
128 - 255	Open for Customer Use	Undefined	00	

1. In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM $\overline{CAS}$ latency).
2. Minimum application clock cycle time is 7.5ns (133MHz).
3. cc = Checksum Data byte, 00-FF (Hex).
4. ww = Binary coded decimal week code, 01-51 (Decimal) ' 01-34 (Hex).
5. yy = Binary coded decimal year code, 0-00 (Decimal) ' 00-63 (Hex).
6. ss = Serial number data byte, 00-FF (Hex).
7. These values apply to PC100 applications only, per Intel PC66/100 SPD standards.

Product Label

The following label should be applied to all PC133-compatible DIMMs, to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A minimum font size of 8 points should be used, and the number can be printed in one or more rows on the label.

Format:

PC133m-abc-dde-fg

Where:

m: Module Type
- R = Registered DIMM
- U = Unbuffered DIMM (no registers on DIMM)

a: SDRAM CAS Latency

b: SDRAM minimum t_{RCD} specification (in clocks)

c: SDRAM minimum t_{RP} specification (in clocks)

dd: SDRAM t_{AC} specification (into 50pF load), with no decimal point
- 54= 5.4ns t_{AC}

e: JEDEC SPD Revision used on this DIMM
- 2 = JEDEC SPD Revision 2.0

f: Gerber file used for this design (if applicable)
- A: Reference design for R/C ‘A’ is used for this assembly
- AA: Reference design for R/C ‘AA’ is used for this assembly
- B: Reference design for R/C ‘B’ is used for this assembly
- C: Reference design for R/C ‘C’ is used for this assembly
- D: Reference design for R/C ‘D’ is used for this assembly
- E: Reference design for R/C ‘E’ is used for this assembly
- Z: None of the ‘Reference’ designs were used on this assembly

g: Revision number of the reference design used:
- 1: 1st revision (1st release)
- 2: 2nd revision (2nd release)
- 3: 3rd revision (3rd release)
- Blank: Not Applicable (used with ‘Z’ above)

Example:

PC133R-333-542-B2

is a PC133 Registered DIMM

with CL = 3, t_{RCD} = 3, t_{RP} = 3

and a t_{AC} = 5.4ns, using JEDEC SPD Revision 2

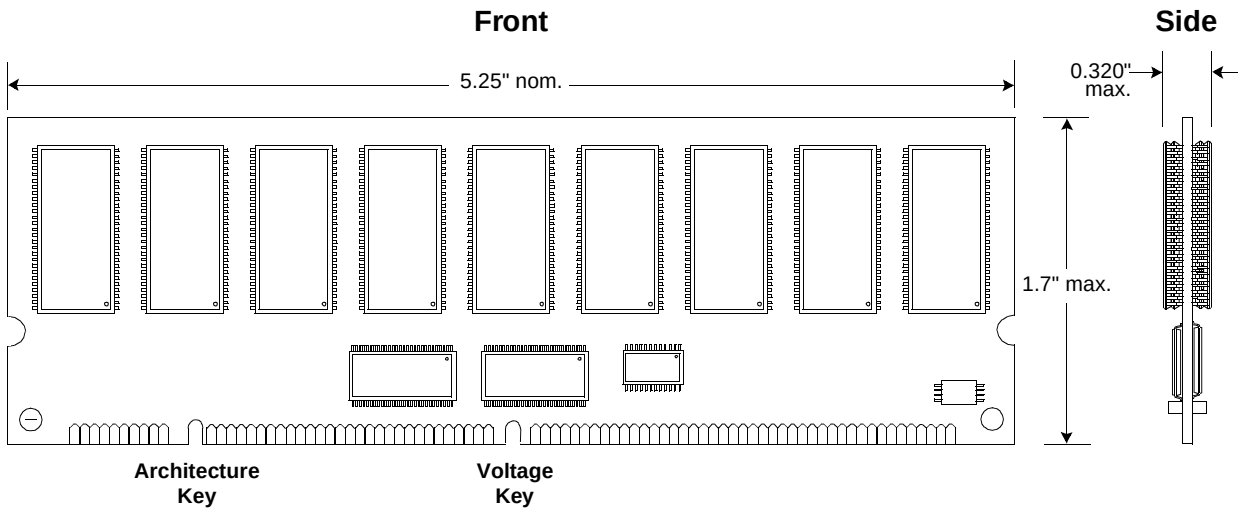
and produced based on the ‘B’ raw card Gerber, 2nd release

DIMM Mechanical Specifications

JEDEC has standardized detailed mechanical information for the 168 Pin DIMM family. This information can be accessed on the worldwide web as follows:

1. Go to http://www.jedec.org.
2. Click on ‘Free Standards and Docs.’
3. Scroll down and double click on ‘Publication 95.’
4. Under ‘Outlines/Registrations,’ click on ‘Microelectronics Outlines.’
5. Scroll down and select ‘MO-161’ to download the PDF for this product family.

Simplified Mechanical Drawing with Keying Positions



Note:
The keying defines the DIMM as a 3.3V Registered DIMM with Serial PDs.

- The center key position defines the voltage for the DIMM. For PC133, this key is in the center of the opening, defining this as a 3.3V DIMM.
- The left key position defines the architecture of the DIMM. For PC133, this key is in the right portion of the opening, defining the DIMM as a ’second generation’ 168 pin DIMM with serial PDs.

Supporting Hardware

Clock Reference Board

To facilitate the measurement of clock arrival time to the SDRAM for both Unbuffered and Registered SDRAM DIMMs, a ‘Clock Reference Board’ has been released. This board includes the following:

- A frequency synthesizer *to provide 100MHz and 133MHz clocks*
- A clock buffer *to re-drive clocks to the module socket and reference nets*
- A 168P DIMM socket, with four clock inputs wired *CS and CKE pins are tied inactive*
- A ‘Registered’ DIMM reference net *consistent with this PC133 spec and the Intel PC100 Revision 1.2 and later DIMMs*
- An ‘Unbuffered’ DIMM reference net *consistent with the Intel PC100 Unbuffered DIMM spec*
- A clock buffer ‘standard test load’ *to permit characterization of the clock buffer into its test load*

This clock reference board is generally available in the industry, and should be used by module producers, as well as system designers, to ensure modules meet the intended clock timings defined in this specification. Every effort has been taken to minimize clock variations and clock skew on these boards.

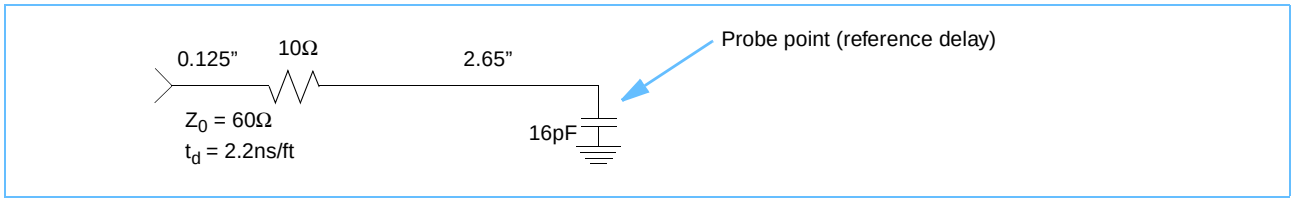
Note: On PC133 Registered DIMMs, as well as PC100 Registered DIMMs produced to the Intel Specification Revision 1.2 and higher, the clock arrival time at the SDRAM will differ by several hundred picoseconds when compared to the PC100 Unbuffered DIMMs (the clock on the Registered DIMMs will be ‘earlier’). This is due to the reduction in PLL input padding capacitance on the Registered DIMMs, from the original 24pF (on early PC100 Registered DIMMs) to the current 12pF value. This reduction results in a lower input capacitance on the Registered DIMM clock (CK0) than on the clocks used on the Unbuffered DIMMs, causing the Registered DIMM clock to arrive at the PLL earlier. This reduction in PLL input capacitance results in an improved clock rise-time on Registered DIMMs (permitting higher frequency operation), and in addition, helps to reduce jitter.

Application Notes

Clocking Timing Methodology

The clock to SDRAM delay is intended to be identical to PC100 Registered DIMMs. As with PC100 Registered DIMMs, the entire clock delay is present between the clock tab pin and the PLL input, and is accomplished via a trace length, a series resistor, and the inclusion of an input padding capacitor at the input of the PLL. This delay should be modeled by the module supplier, to ensure accuracy, if a raw card other than one of the 'reference designs' is utilized. The clock 'Reference Net' below is provided for use during module simulation to ensure an accurate clock delay, since measurement of the delay is impractical (due to the reflections at the clock tab pin).

Registered DIMM Clock Reference Net



The clock delay from the input of the PLL to the input of any SDRAM is designed to be 0ns (nominal). The clock arrival time at the PLL input should not be adjusted, although sources of timing variation include PLL input capacitance, padding capacitor and series resistor tolerances, and DIMM impedance variations (the latter items have a minor affect). Due to these variations, it is possible that there will be a difference between the input of the PLL and the input of the SDRAM --a reasonable target for this variation is +/-100ps.

The most important factor in clock measurements is to ensure consistent clock arrival times at the SDRAM. The clock reference board Registered DIMM reference net provides the standard net delay for this measurment. The DIMM suppliers must adjust the value of the feedback capacitor to place the clock arrival at the SDRAM on the DIMM within +/-100ps of the clock arrival at the Registered DIMM clock reference net (measured as a 'mean', since the PLL and source jitter makes this measurement difficult). This value is a target for DIMM suppliers and does not include worst case contributions of PLL skew, PLL phase error, feedback capacitor variations, and DIMM variations.

The clock to the register should lead the SDRAM clock by approx. 450ps (nominal), with a target range of +100ps/-150ps (adjusted). The actual delay may vary as a result of the input capacitance of the SDRAMs, the register clock input capacitance, variations of the PCB parasitics, and measurement skew (the later two having secondary effects).The register clock to SDRAM clock relationship may be adjusted by doing the following:

1. For register clocks arriving less than 450ps (nominal) prior to the SDRAM input clock:
   - Resistors on the clock nets to the SDRAMs may be increased in value in order to increase the propagation delay to the SDRAMs.
2. For register clocks arriving greater than 450ps (nominal) prior to the SDRAM input clock:
   - A padding capacitor location is included in the register clock net, and when populated, this capacitor will increase the propagation delay to the registers.
   - Resistors on the SDRAM clock nets, where applicable, may be reduced in value in order to reduce the propagation delay to the SDRAMs.

All changes defined above require simulation to verify the targeted results. Simulation of the clock nets will allow each DIMM manufacturer to determine the most effective method for achieving a -450ps nominal relationship between the register input clock and the SDRAM input clock. It is critical that this analysis be done in order to maintain the required rise-time characteristics as well as signal integrity at the input of both the SDRAM and the registers. In cases where the register clock cannot be placed in the ideal timing window, post-register timings will need to be adjusted, by the DIMM producer, to ensure robust module operation.

Revision Log (Part 1 of 5)

Revision Info	Page of Revision	Description of Change
Revision 0.8 12/4/98	p 2	Updated the footnote in the SDRAM Module Configurations Table. Update typo on addressing for the 256MB SDRAM Module Configuration.
	p 11	Updated address information to include maximum addressing.
	p 13	Updated block diagram to reflect the design- each chip select sees nine SDRAM loads each.
	p 14	Updated block diagram to reflect the design- each chip select sees nine SDRAM loads each.
	p 15	Inserted a new block diagram which reflects the Raw Card Version C and D designs, whereby Chip selects alternate between upper and lower SDRAMs in order to enhance thermal character-istics.
	p 16	Updated the register wiring for the Raw Card Version B,C and D to clarify the use of CKE0 and 1. Removed the note on this table indicating that this info was preliminary.
	pp 17-20	Inserted a note clarifying which Raw Card utilizes the defined pin assignment.
	p 18	Removed the note indicating that one raw card would support both Version 1 and 2 SDRAM pin assignments.
	p 19	Fixed typo in header.
	p 21	Changed the input capacitor value for a terminated clock net to 12pF to match rev 1.2 of the Intel PC100 RDIMM specification. Removed Note 2 under the clock net wiring section.
	p 30	Updated note on topology info to indicate that info pertaining to R/C B accurately depicts the cur-rent design, while A, C and D are not verified to date.
	pp 31-41	Updated all topology information to accurately reflect the Raw Card Version ‘B’ design.
	p 31	Moved the Register Clock input topology to the next page to clarify that it is a PLL output. Changed the input capacitor value for a terminated clock net to 12pF to match rev 1.2 of the Intel PC100 RDIMM specification.
	p 32	Renamed wire lengths for the PLL output to the SDRAM. Added a resistor to the PLL output to the SDRAM net. Changed table for clarification. Updated clock loading for SDRAMs to show differences between R/C A and R/C B, C & D.
	pp 34 & 35	Removed L4 from topology as L3 = L4.
	p 39	Added note to clarify use of CKE0 and 1 on the different Raw Card Versions.
	p 42	Updated Max I/O capacitance to 6.5pF.
	p 43	Changed definition of T_{RP},T_{RAS},T_{RCD},T_{RRD} and T_{RC} into ns.
	p 44	Changed definition of T_{DPL} into ns. Added specification for T_{RFC}.
	pp 45 & 46	Added an example SPD table for Raw Card Version B, 16Mx72.
	p 47	Changed V_{DD} to 3.3 V +-0.3V. Updated Critical Register Specifications. Created a new note listing early register suppliers.

Revision Log (Part 2 of 5)

Revision Info	Page of Revision	Description of Change
Revision 0.8 12/4/98	p 48	Changed V_{DD} to 3.3V +-0.3V. Added Operating frequency. Created a note listing early PLL suppliers.
Revision 0.9 2/5/99	p 2	Added JEDEC SPD document as additional reference document.
	p 3	Updated the overall module height, so that it was specified consistently with JEDEC's mechanical definitions.
	p 4	Added a new definition for Dimension 'T' to the mechanical DIMM dimensions and changed current 'T' to 'T1'.
	p 10	Corrected pin assignment to be consistent with JEDEC defined 168 pin Registered DIMMs (previously columns were placed in the incorrect order).
	pp 12-15	Changed An to A12 in all of the references to addresses in the block diagram.
	p 14	Removed note in reference to CS alternating decks.
	p 16	Removed note referring to preliminary wiring for Raw Card Version A. Added A12 to the register wiring for use with 256Mb SDRAMs. Clarified use of CKE1 on Raw Card Version D.
	p 17	Removed x16 SDRAM pinout, as it does not apply to the specified DIMMs.
	p 19	Added a new page to reflect the 256Mbit SDRAM stacked Staktek™ pin assignment.
	p 20	Removed A12 and A13 labels from the bank select pins. Corrected organization label below pin assignment.
	p 22	Updated clock net wiring drawing for CK0 to clarify the PLL to register structure, and to indicate the design goal for the relationship between the PLL clk input and the SDRAM clk input.
	pp 23-24	Added a description of the clocking methodology, as well as the clock reference board.
	p 25	Updated post-register timing example. Added a description of the post-register timing methodology.
	p 28	Changed board impedance tolerance to ±10% to be consistent with the latest Intel PC100 specification. Removed dielectric constant specification, as without test methodology this number has little meaning.
	p 33	Updated Note which indicates the contents of the topology pages.
	pp 34 & 45	Updated all topology information to accurately reflect Raw Card Version A and C.
	p 34	Updated Note 3 in the table to indicate that SDRAM capacitance also impacts the feedback capacitor value utilized.
	pp 37 & 38	Corrected R1 value to be consistent with the Gerber release.
	p 39	Updated topology diagram to clarify wiring for chip selects on Raw Card Version A.
	p 40	Corrected R1 value to be consistent with the Gerber release.
	p 41	Updated topology diagram to clarify wiring for CKE on Raw Card Version A.
	p 42	Updated and added notes to clarify the use of CKE1 on Raw Card Version D only.

Revision Log (Part 3 of 5)

Revision Info	Page of Revision	Description of Change
Revision 0.9 2/5/99	p 43	Removed Raw Card Version A description from this topology in order to clarify wiring. Changed labels for signals to be consistent with the rest of the documentation. Added a note to the topology.
	p 44	Added a page to describe the Address and Control topology for Raw Card Version A (removed table for resistance values, which is now incorporated into the table on this new page).
	p 46	Added a page to describe the input loading characteristics of the DIMMs.
	p 47	Removed Iccslfrf and Iccac from the SDRAM specifications, as it is an unnecessary value for the purposes of this spec.
	p 49	Changed t_{RFC} from 80ns to 75ns to match the JEDEC PC133 ballot.
	p 51	Indicated that Byte 126 and 127 in the SPDs are 'Reserved'.
	p 52	Indicated that equivalent part numbers may also be used in the register component specification table. Added a specification for register clock input capacitance. Added a note to the critical register specifications table.
	p 53	Updated text to indicate that the133MHz specifications are required. Deleted reference to 'B' in PLL P/N.
	p 54	Added a page to describe the Gerber releases (dates and applicable specifications).
	p 55	Added a page to describe the labeling requirements for PC133 RDIMMs.
Revision 0.91 4/1/99	all	Reorganized sections and added section numbers to facilitate the use of this document as the basis of future module design specifications. Adjusted terminology to match industry standards. Made no changes in technical content. Replaced DIMM Dimensions and Tolerances table and detailed mechanical drawings with instructions to locate JEDEC's worldwide web site where up-to-date information and drawings for these DIMMs can be found.
Revision 1.0 5/25/99	p 4	Clarified standard for JEDEC SDRAM DIMM info and added website address info
	p 12	Added 'max' to number of SDRAM loads per clock output Updated wording in the notes section of the 'Clock Net Wiring for CK0' for clarification
	p 13	Removed CKE1 from register pins (as well as note 2 in the table which referenced these pins) for Raw Card D
	p 15	Removed the incorrect reference to an 8Mx8 SDRAM on this pin assignment
	p 16	Added x8 pinout for 256Mbit planar
	p 19	Remove reference to IBIS section for VOH and VOL
	p 20	Updated tRP and tRCD to 20.0ns to be PC100 backwards compatible
	pp 20 & 21	Added 100MHz to the SDRAM operating frequency for the PC133 SDRAMs in the header column

Revision Log (Part 4 of 5)

Revision Info	Page of Revision	Description of Change
Revision 1.0 5/25/99	p 22	Added Raw Card E to DIMM Register Use table Clarified that any register type (ALVC or AVC or equivalent) can be used on any of the DIMM configurations in the DIMM Register Use table Added T_A to critical register specifications Updated register clock input capacitance Removed early potential register source list Added information on register sourcing
	p 23	Added DIMM PLL Use Table which includes a note describing R/C 'AA' Clarified PLL skew Added typical PLL clock input capacitance specification Removed early potential PLL source list Added information on PLL sourcing
	p 24	Added R/C E to Reference Designs Table, as well as a note describing its purpose Removed CKE1 capability from R/C D in Input Loading Matrix Added R/C E to Input Loading Matrix
	p 25	Added R/C AA and E (in development) for Gerber releases Updated specification revision which is applicable to the reference designs Added release of R/C D
	p 27	Added R/C E to Component Placement Label
	p 30	Added R/C D to list of reference designs represented in the net structures document, and added reference to future additionof R/C E
	pp 30-43	Added Raw Card D net structure info
	pp 35 & 36	Removed total net length from net structure length table to avoid confusion
	p 44	Updated 4mil stackup example to result in better centered board impedance around the specifed impedance
	p 45	Updated Post Register TImings to reflect accurate numbers for skew and other timing factors, and added a table to explain the contributions to t_{Skew}
	pp 46 & 47	Updated text which describes the use of the SPD data (removed direct reference to Intel SPDs) Updated Bytes 18,23,24,27,& 29 to be consistent with the finalized SPD data
	p 48	Added Raw Card Versions AA and E to the label list
	p 50	Updated description of clock reference board to indicate that boards are now readily available
	p 51	Updated explanation of clock tuning methodology and incorporated the use of the clock reference board into the explanation of this tuning process.

Revision Log (Part 5 of 5)

Revision Info	Page of Revision	Description of Change
Revision 1.1 7/12/99	pp 4-57	Changed all references to V_{CC} to V_{DD}
	p 5	Changed "Absolute Max Rating" header to "Environmental Parameters"
	p 7	Added CKE1 to the Registered SDRAM DIMM pinout
	p 11	Added Block Diagram for Raw Card Version E
	p 13	Added Registered Functional Assignments for Raw Card E
	pp 14-21	Changed all references to clock from "CLK" to CK"
	pp 14 & 15	Added 128Mbit density to label under the 54 pin SDRAM pin assignments
	p 19	Added a note referencing JEDEC documentation for the latest SDRAM specification
	p 20	Changed t_{SI} and t_{HI} to t_{IS} and t_{IH}
	p 24	Added Raw Card Version "AA" to the SDRAM Module Configurations Table. Removed the note indicating that R/C Version E was new
	p 25	Updated spec revision to 1.1 Added original release dates for R/C Version "AA" and "E"
	p 26	Inserted note describing component placement which had previously been incorrectly placed
	pp 30-44	Added new Raw Card Version E Net Structure Descriptions and Lengths
	p 45	Added a note indicating that the layer stack ups were only examples of the possible stack up options.
	p 46	Update t_{SETUP} and t_{HOLD} naming convention to t_{IS} and t_{IH} in order to be consistent with the SDRAM specifications
	p 52	Updated register to SDRAM clock relationship to 450 +100/-150ps target in order to allow for SDRAM, register, and DIMM inherent characteristics. Added wording to indicate that when altering clock relationships, it is critical to focus on signal integrity after any changes.