# 65816 Microprocessor Quick Reference

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### **Registers:**

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7		6	5	4	3	2	1	0
							Accumulator (B) <sup>1</sup> Accumulator (A) <sup>1</sup>																	
Data Bank Register (DBR)								X Index Register (X) <sup>2</sup>																
									Y Index Register (Y) <sup>2</sup>															
0	0	0	0	0	0	0	0	Direct Page Register (D)																
0	0	0	0	0	0	0	0	Stack Pointer (S)																
Program Bank Register (PBR)								Program Counter (PC)																
								Processor Status Register (P) E																
															ľ	1	V	Μ	Х	D	Ι	Z	C	

#### Notes:

1. Accumulator is 16-bit (C) when M=0, 8-bit (A and B) when M=1.

2. Index registers are 16-bit when X=0, 8-bit when X=1.

#### **Processor Status Register:**

N - Negative (1=negative)

- M Memory/Accumulator Select (1=8-bit, 0=16-bit)
- D Decimal Mode (1=decimal, 0=binary) Z - Zero (1=zero result)
- E Emulation (0=native mode)

#### Switching Modes:

V - Overflow (1=overflow)
X - Index Register Select (1=8-bit, 0=16-bit)
I - IRQ Disable (1=disabled)
C - Carry (1=carry)

Go to native mode:	Go to emulation mode:
CLC	SEC
XCE	XCE
Select 16-bit memory and 16-bit index registers: REP #%00110000	Select 8-bit memory and 8-bit index registers: SEP #%00110000
Select 16-bit memory and 8-bit index registers:	Select 8-bit memory and 16-bit registers:
REP #%00100000	SEP #%00100000
SEP #%00010000	REP #%00010000

#### **Emulation Mode Features:**

- 1. Emulation mode is default on power up/reset.
- 2. Separate 8-bit accumulators (A and B).
- 3. 8-bit index registers (X and Y).
- 4. Stack is limited to page 1.
- 5. Direct page indexing wraps.
- 6. B flag in P reflects BRK status (instead of X).
- 7. Uses 6502 interrupt vectors.

## **New Addressing Modes:**

Addressing Mode	Example
Program Counter Relative Long	BRL JMPLABEL
Stack Relative	LDA 3,S
Stack Relative Indirect Indexed with Y	LDA (5,S),Y
Block Move	MVP 0,0
Absolute Long	LDA \$02F000
Absolute Long Indexed with X	LDA \$12D080,X
Absolute Indirect Long	JMP [\$2000]
Direct Page Indirect Long	LDA [\$55]
Direct Page Indirect Long Indexed with Y	LDA [\$55],Y

#### **New Instructions:**

BRL	Branch always long	REP	Reset status bits
COP	Co-processor empowerment	RTL	Return from subroutine long
JML	Jump long	SEP	Set status bits
JSL	Jump to subroutine long	$\operatorname{STP}^*$	Stop the processor
MVN	Block move negative	TCD	Transfer 16-bit accumulator to direct page register
MVP	Block move positive	TCS	Transfer accumulator to stack pointer
PEA	Push effective absolute address onto stack	TDC	Transfer direct page register to 16-bit accumulator
PEI	Push effective indirect address onto stack	TSC	Transfer stack pointer to 16-bit accumulator
PER	Push effective PC relative address onto stack	TXY	Transfer index registers X to Y
PHB	Push data bank register onto stack	TYX	Transfer index registers Y to X
PHD	Push direct page register onto stack	$WAI^*$	Wait for interrupt
PHK	Push program bank register onto stack	WDM	Reserved for future two-byte opcodes
PLB	Pull data bank register from stack	XBA	Exchange the B and A accumulators
PLD	Pull direct page register from stack	XCE	Exchange carry and emulation bits

Note: STP and WAI are available in the WDC 65C02. The 65816 also supports all 65C02 instructions except for the Rockwell-specific RMB, SMB, BBR, and BBS instructions..

#### **Interrupt Vector Locations:**

Vector	Emulation Mode	Native Mode
IRQ	\$FFFE, \$FFFF	\$FFEE, \$FFEF
RESET	\$FFFC, \$FFFD	-
NMI	\$FFFA, \$FFFB	\$FFEA, \$FFEB
ABORT	\$FFF8, \$FFF9	\$FFE8, \$FFE9
BRK	-	\$FFE6, \$FFE7
СОР	\$FFF4, \$FFF5	\$FFE4, \$FFE5

Note: All locations are in bank zero.