65C02 Microprocessor Quick Reference

Jeff Tranter <tranter@pobox.com>

Updated: 10-Jul-2012

This sheet summarizes the software extensions and differences for the 65C02 processor over the NMOS 6502.

New Addressing Modes:

Indirect Zero Page	e.g. LDA ($12)
Absolute Indexed Indirect	e.g. JMP ($1234,X)

New Instructions:

BRA *nn*	Branch Always
PHX	Push X
PHY	Push Y
PLX	Pull X
PLY	Pull Y
STZ *nn*	Store Zero
STZ *nn*,X	Store Zero
STZ *nnnn*	Store Zero
STZ *nnnn*,X	Store Zero
TRB *nn*	Test and Reset Bit
TRB *nnnn*	Test and Reset Bit
TSB *nn*	Test and Set Bit
TSB *nnnn*	Test and Set Bit

Instructions With New Addressing Modes:

ADC (*nn*)	EOR (*nn*)
AND (*nn*)	INC A
BIT #*nn*	JMP (*nnnn*,X)
BIT *nn*,X	LDA (*nn*)
BIT *nnnn*,X	ORA (*nn*)
CMP (*nn*)	SBC (*nn*)
DEC A	STA (*nn*)

Enhancements:

Invalid op codes are executed as NOPs.
JMP (*nn*FF) correctly increments page address.
Decimal flag is cleared on reset and interrupt.
N, V, and Z flags are valid in decimal mode.

Rockwell and Western Design Center 65C02-Specific Instructions:

BBR	-	Branch on Bit Reset
BBS	-	Branch on Bit Set
RMB	-	Reset Memory Bit
SMB	-	Set Memory Bit

Western Design Center 65C02-Specific Instructions:

STP	-	Stop Processor
WAI	-	Wait For Interrupt