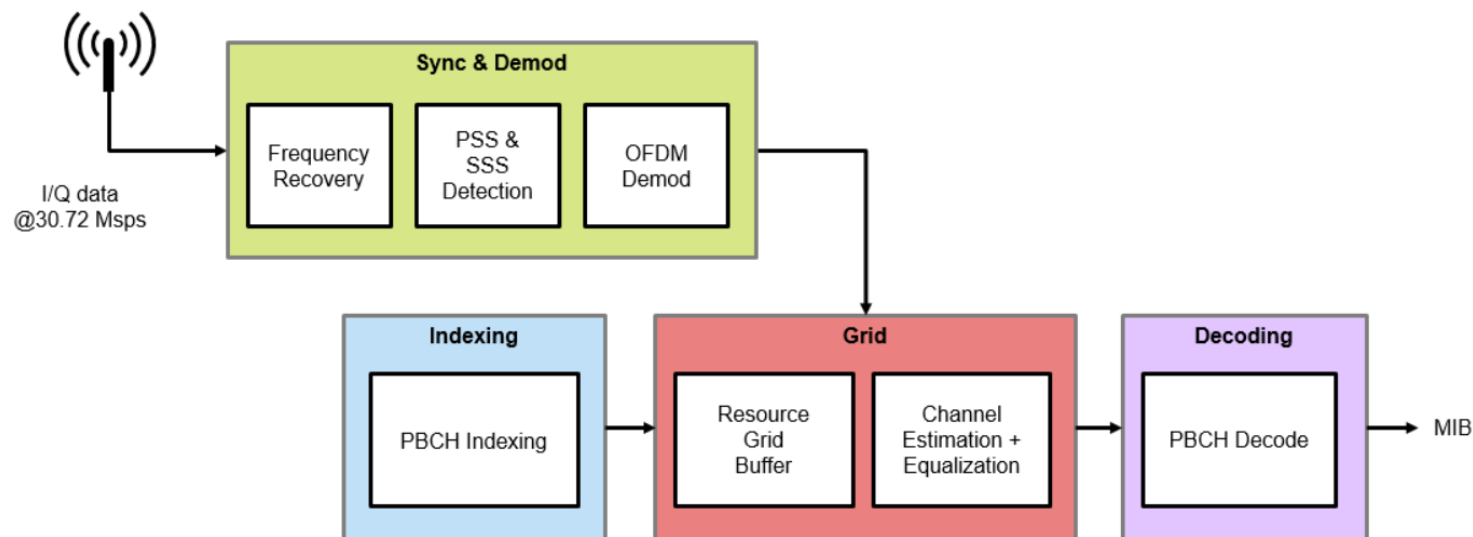


LTE

Project: LTE Cell Search Cohort 9



Team: The Correlators

Jeffrey High

Mahesh Valavala

Satish Nichanametla

Shubhadip Paul



What is LTE Cell search about?



LTE stands for **Long Term Evolution** and referred as 4G LTE. It's a standard for wireless data transmission.



A Physical **Cell ID** (PCI) is an important parameter to establish connection with LTE network



Establish time and frequency synchronization with **LTE signals** and extract cell ID.



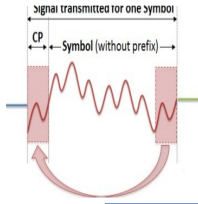
To decode LTE cell ID, Primary Synchronization Signal (**PSS**) and Secondary Synchronization Signal (**SSS**) signals should be decoded.



Xilinx Zynq® UltraScale+™ **RFSoc** with giga sample RF data converters is used.

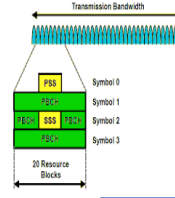
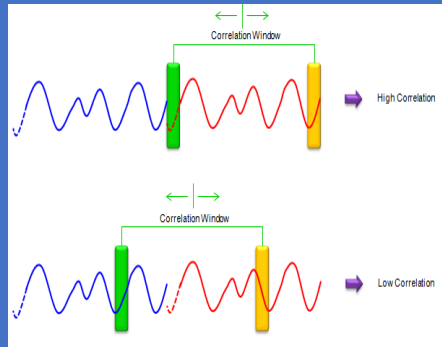


Main LTE Blocks - For Cell Search



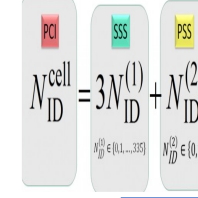
CP Correlation

- Cyclic Prefix is an exact copy of the last part of OFDM symbol



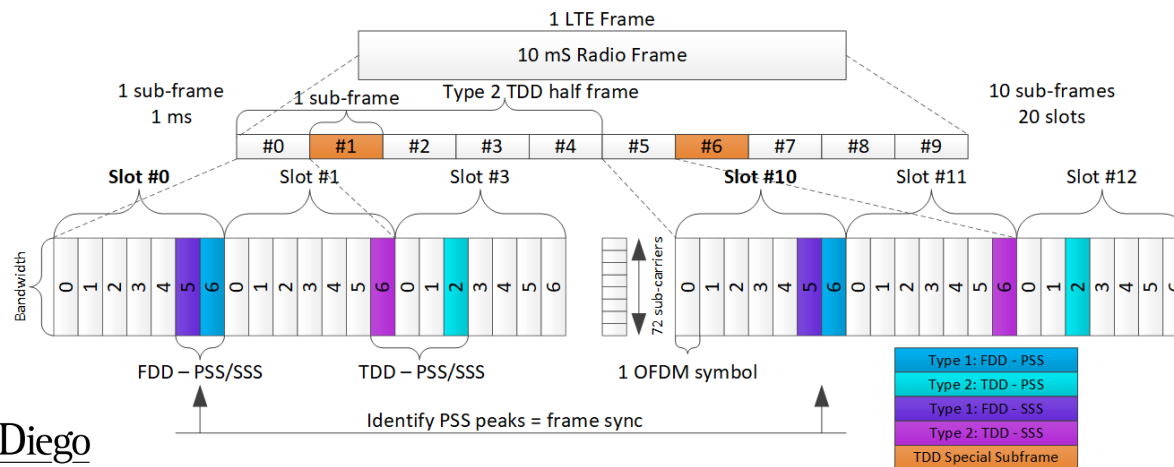
PSS

- 3 Zadoff-Chu root sequences defined in Frequency domain.
- IFFT to get time domain sequences which reduces HW complexity.
- Correlate Rx signal with 3 known time domain PSS sequences.



SSS

- 1 of 168 known sequences.
- Polynomial based 3 binary sequences on Galois field.
- Correlation in frequency domain by taking 128-point FFT on Rx Symbol.

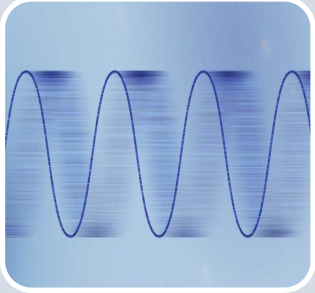


The physical cell identity, N_{ID}^{cell} , is defined by the equation:

$$N_{ID}^{CELL} = 3N_{ID}^{(1)} + N_{ID}^{(2)}$$

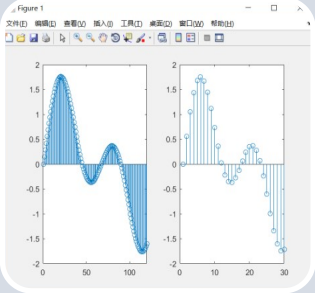
- $N_{ID}^{(1)}$ is the physical layer cell identity group (0 to 167).
- $N_{ID}^{(2)}$ is the identity within the group (0 to 2).

System Requirements and Configurations



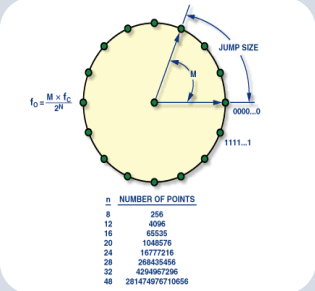
ADC Configuration

- RF SoC supports F_s in range of 1024 MHz - 4096 MHz.
- Our LTE Cell search IP needs F_s of 1.92MHz.
- ADC F_s is configured to 3932.16MHz as it is a multiple of 30.72MHz (LTE Rate). Reference ADC clock needed 491.52MHz.



Decimation

- Our System needs decimation of 2048.
- 8x decimation in RF Soc. From 3932.16MHz to 491.52MHz.
- 256x decimation in our custom IP to achieve F_s of 1.92MHz at LTE Cell search IP.

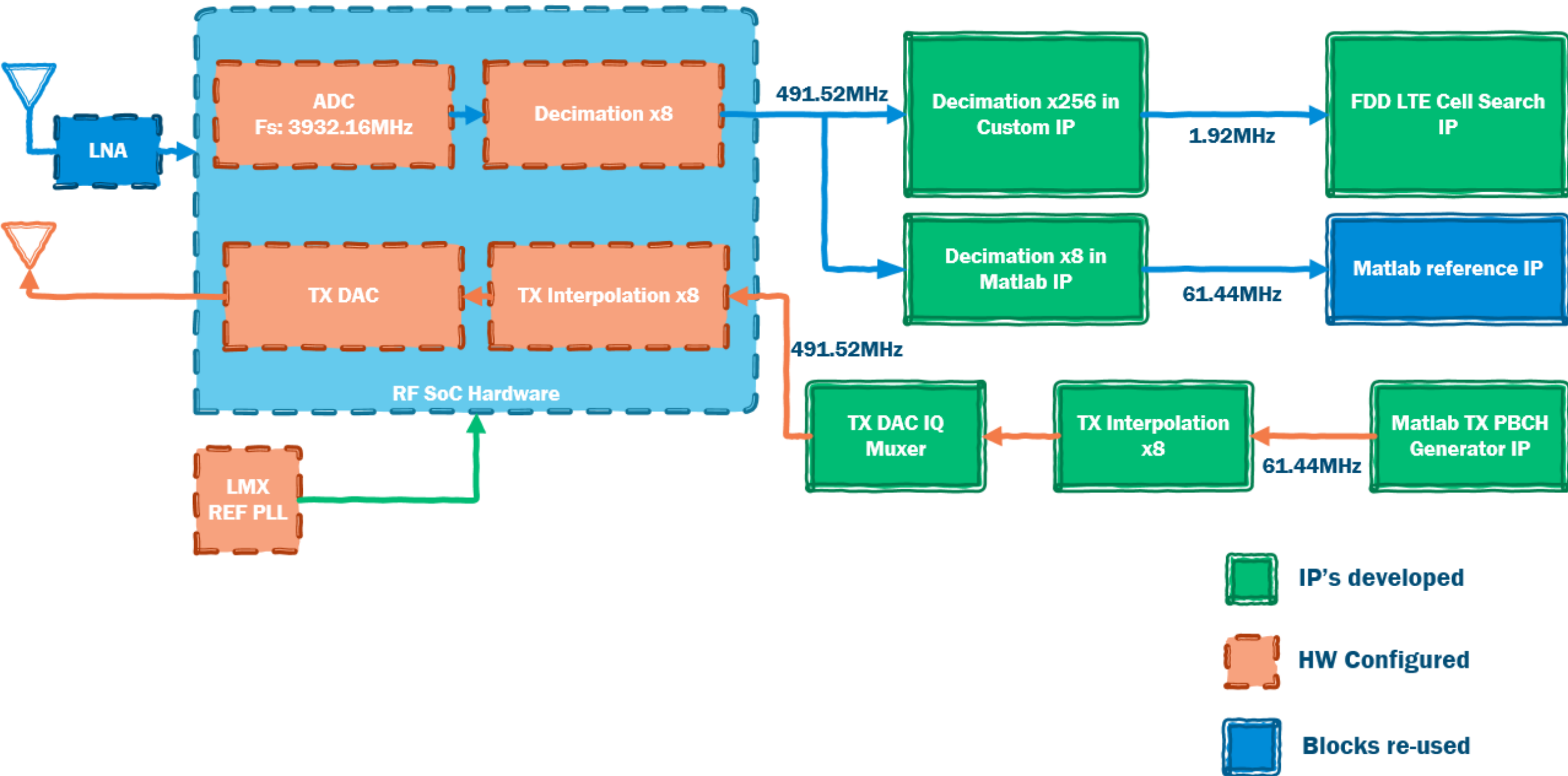


NCO (Numerically Controlled Oscillator)

- NCO configured to down convert carrier frequency to DC.
- 48-bit NCO per RF-ADC.
- Mixer is programmed to fine mode.



LTE Cell Search - System Block Diagram

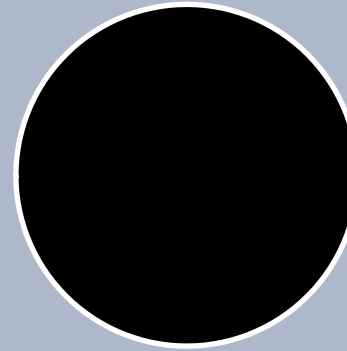


LTE Cell Search Test Bench



Loop Back Mode

LTE waveform from DAC loop back



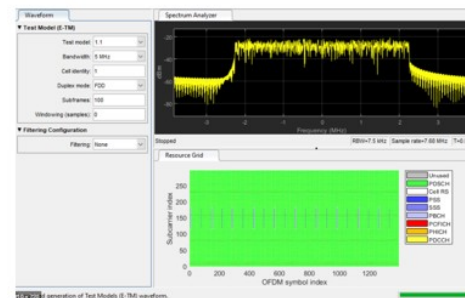
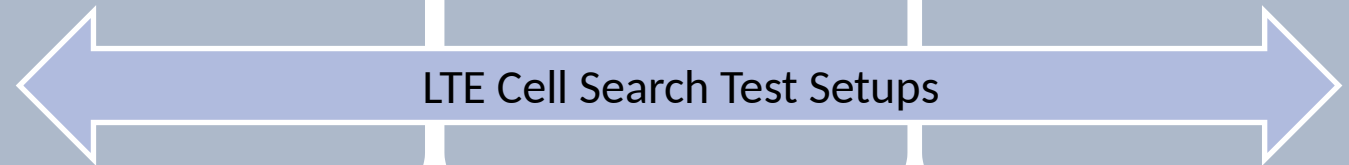
External Signal Generator

Single Tone/CW and LTE waveform testing at various carrier frequencies.

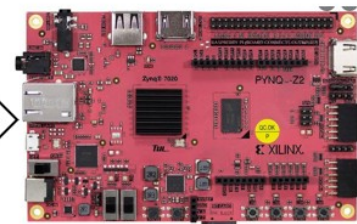


Pluto SDR

Wireless testing with LTE waveform

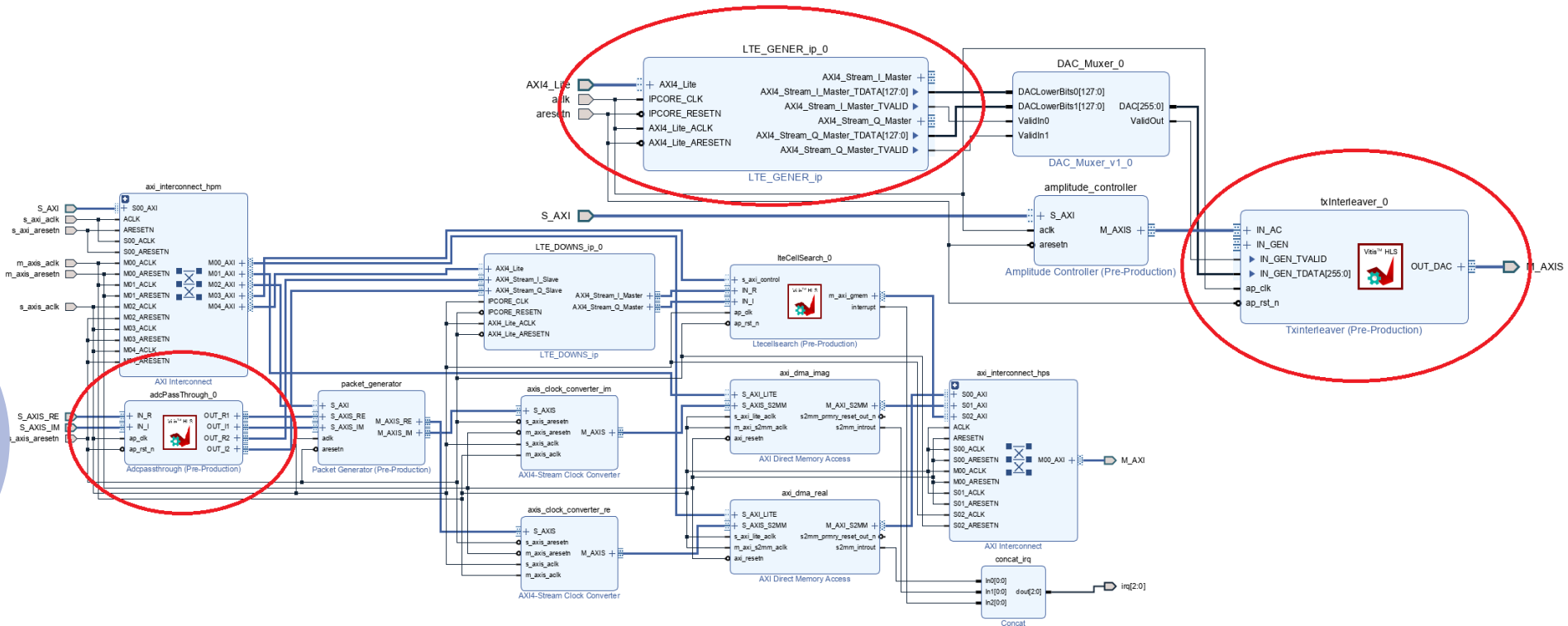
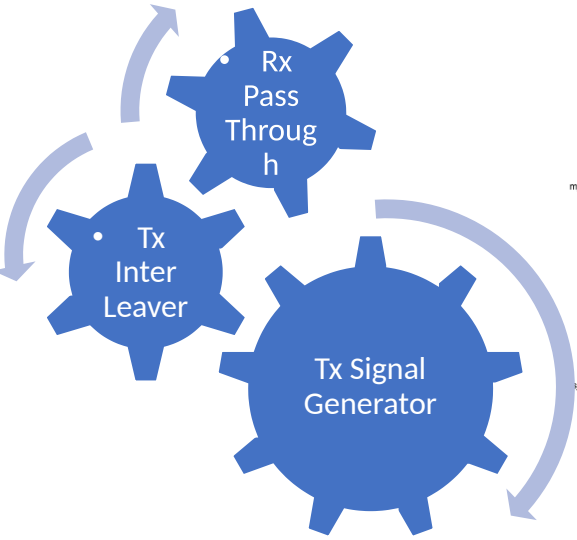


RTL
Digitizer



FPGA IP Research

Enablement Modules :



VITIS HLS

XILINX
VITIS™

- Blocks - Rx Pass Through, Tx Inter Leaver

Matlab Simulink

MATLAB®
& SIMULINK®

- Blocks - TX Signal Generator

IPs to be developed on FPGA and their development platforms, reference models

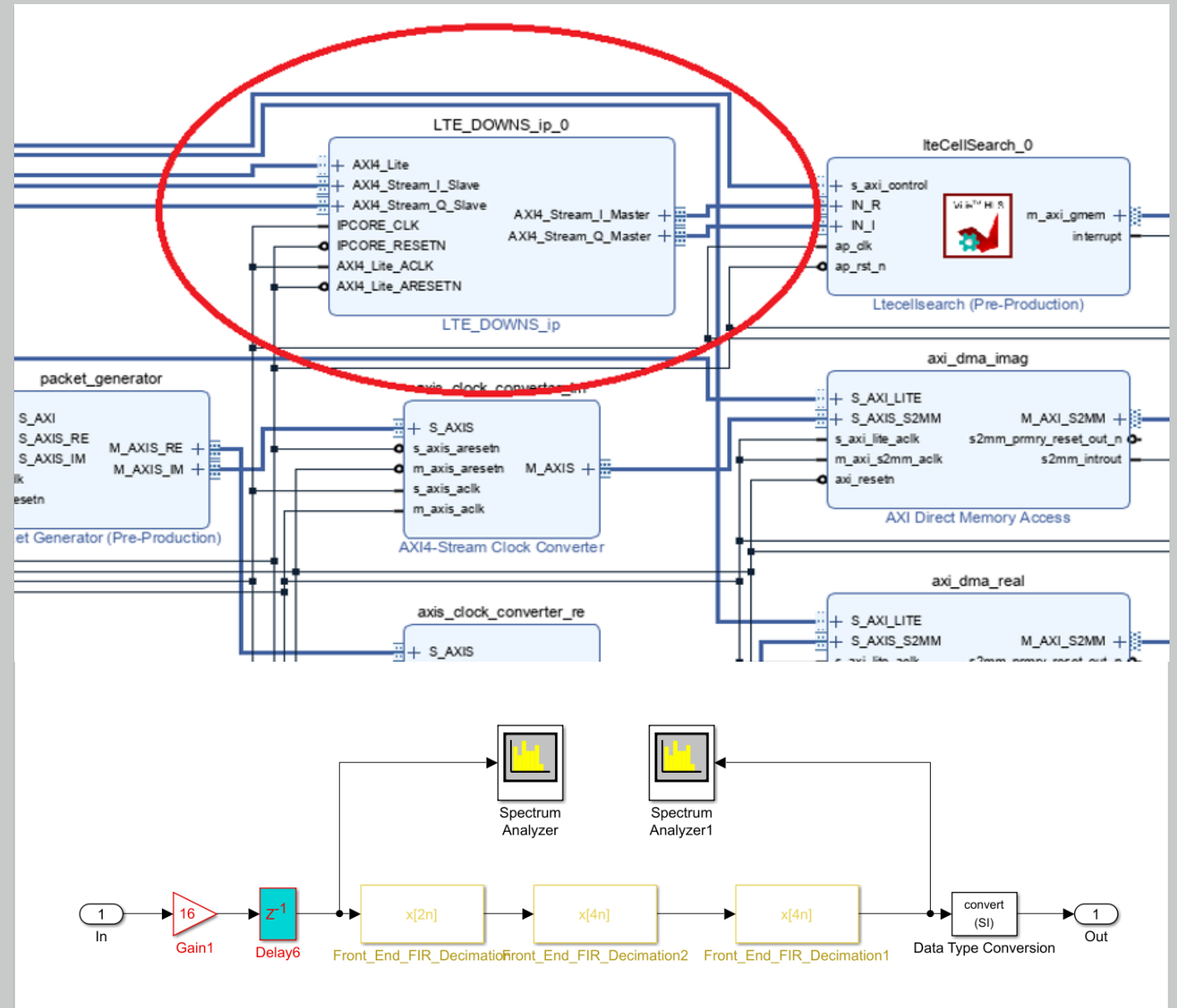
FPGA IP Research (cont'd..)

Front End Module

- $F_s = 491.52\text{MHz}$.
- Packed ADC samples.
- 8 I/Q samples
- Outputs 1.92MHz I/Q samples

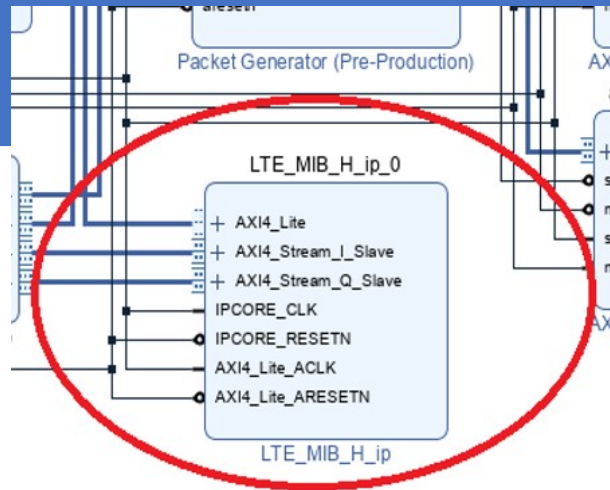
Simulink Design

- Developed using Simulink Cascade Filters
- Designed with MATLAB filter designer

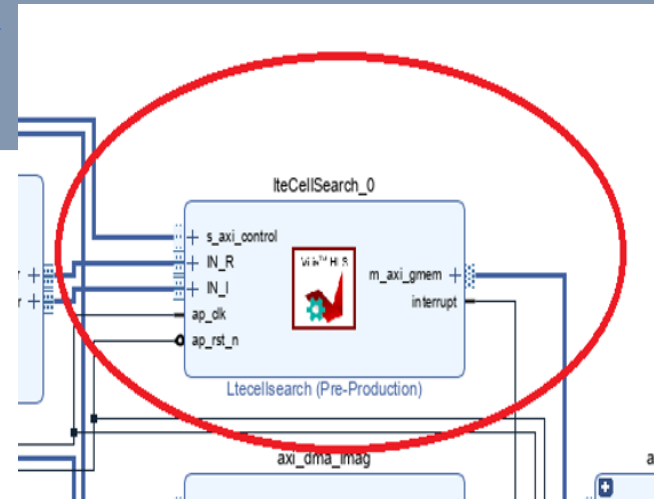


FPGA IP Research (cont'd..)

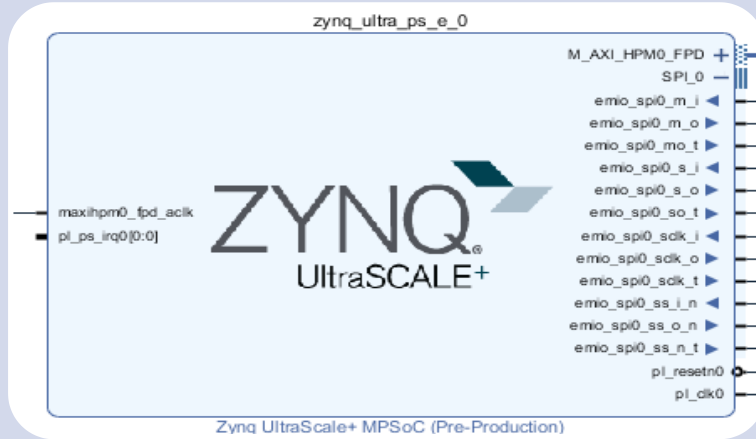
- ✓ 1. Benchmark IP on CH #1
- ✓ 2. Used for validating the setup
- ✓ 3. Decided to use Simulink LTE MIB detector design



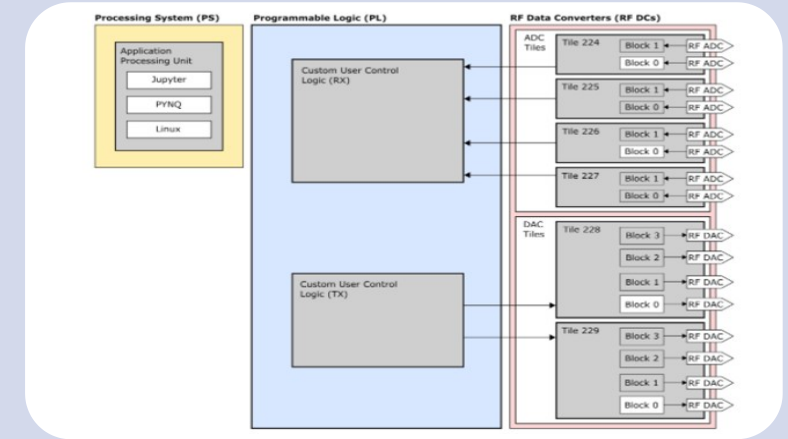
- 1. Own custom cell search algorithm on CH #2.
- 2. Used MATLAB to develop algorithms
- 3. Used Vitis HLS to implement algorithms.



Overlay Research



Console Messages Log Reports Design Rules																	
Item	Constants	Status	WNS	TNS	WHS	THS	TPHS	Total Power	Failed Routes	L	FF	BRAM	URAM	DSP	Start	Elapsed	
✓ synth_1 (active)	constants_1	synth_design Complete										0	0	0	0	52022.514 AM	00:00
✓ impl_1	constants_1	write_bitstream Complete	0.014	0.000	0.010	0.000	0.000	0.414	0	109916	140817	347.0	0	1696	52022.551 AM	01:15	
Out-Of-Context Module Runs																	
✓ base		Submodule Run Complete															
✓ base_LTE_MIB_H_0_0_synth_1	base_LTE_MIB_H_0_0	synth_design Complete								26784	38074	73.0	0	255	52022.514 PM	18:24	
✓ base_McCellSearch_0_0_synth_1	base_McCellSearch_0_0	synth_design Complete								17205	11650	6.5	0	30	52022.544 AM	00:10	
✓ base_sdr_0_0_synth_1	base_sdr_0_0	synth_design Complete								17112	21926	25.5	0	3	52022.542 PM	00:10	
✓ base_LTE_DOWNING_0_0_synth_1	base_LTE_DOWNING_0_0	synth_design Complete								11037	9489	23.0	0	572	52022.522 PM	00:10	
✓ base_drc_1_synth_1	base_drc_1	synth_design Complete								2766	1568	0.0	0	0	52022.510 PM	00:10	
✓ base_drc_vhdl_1_synth_1	base_drc_vhdl_1	synth_design Complete								1738	274	6.5	0	0	52022.510 PM	00:10	
✓ base_LTE_GENERATOR_0_0_synth_1	base_LTE_GENERATOR_0_0	synth_design Complete								1700	2871	19.0	0	418	52022.514 PM	00:10	
✓ base_rdr_0_synth_1	base_rdr_0	synth_design Complete								1607	2102	0.0	0	0	52022.537 PM	00:10	
✓ base_rdr_1_synth_1	base_rdr_1	synth_design Complete								1186	967	0.0	0	0	52022.530 PM	00:10	
✓ base_shutdown_int_0_synth_1	base_shutdown_int_0	synth_design Complete								898	1960	0.0	0	0	52022.516 PM	00:10	
✓ base_rdr_7_synth_1	base_rdr_7	synth_design Complete								774	731	0.0	0	0	52022.508 PM	00:10	
✓ base_rdr_11_synth_1	base_rdr_11	synth_design Complete								751	624	0.0	0	0	52022.508 PM	00:10	
✓ base_adpPassThrough_0_0_synth_1	base_adpPassThrough_0_0	synth_design Complete								612	2033	0.0	0	0	52022.235 AM	00:10	
✓ base_adp_1_synth_1	base_adp_1	synth_design Complete								439	634	0.0	0	0	52022.519 PM	00:10	
✓ base_ic_1_synth_1	base_ic_1	synth_design Complete								401	374	0.0	0	0	52022.513 PM	00:10	
✓ base_interrupter_0_0_synth_1	base_interrupter_0_0	synth_design Complete								369	1323	0.0	0	0	52022.754 PM	00:10	
✓ base_rdr_rdr_rdr_0_0_synth_1	base_rdr_rdr_rdr_0_0	synth_design Complete								359	0	0.0	0	0	52022.520 PM	00:10	



Base Overlay:

1. RF SoC PYNQ image has default Base overlay.
2. The base design allows generation of bitstream with IPs to use RF ADC's and DAC's.

VIVADO IP Integration:

1. Added our HW IPs to base overlay and rebuild the base overlay.
2. Used 'base.tcl' script to generate VIVADO project with IP Integrator for the base overlay

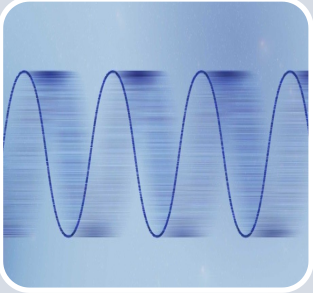
RF Data Converters:

- PYNQ Base image has notebooks to interact with Radio IP subsystem in the base overlay which allowed us to control RF Data Converters.

01_rf_dataconverter_intro.ipynb
02_rf_spectrum_analysis.ipynb

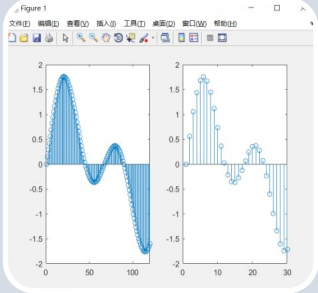
Choosing a reference overlay for RFSoc2x2 and application for implementing Cell Search

Challenges



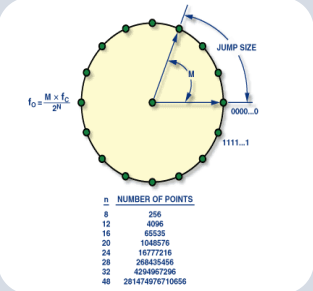
ADC Clock

- F_s of 3932.16MHz needed a reference clock of 491.52MHz.
- Register settings for this reference clock are not available
- Used TIC Pro TI software to generate the register settings for reference clock



IP Restart Algorithms

- In order scan over frequency, algorithms should have the ability to restart after tuning to a new frequency.
- Need to ensure the IP restart would not stall design



NCO Configurations

- Bug in PYNQ base overlay wrapper NCO settings.
- Found base reference host SW not supporting mixer in fine mode.



Thanks!

**Prof. Ryan
Kastner
Prof. Fred
Harris
Prof. John
Eldon
Patrick Ling**

UC San Diego

JACOBS SCHOOL OF ENGINEERING



References

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5. https://www.sharetechnote.com/html/FrameStructure_DL.html#Overview