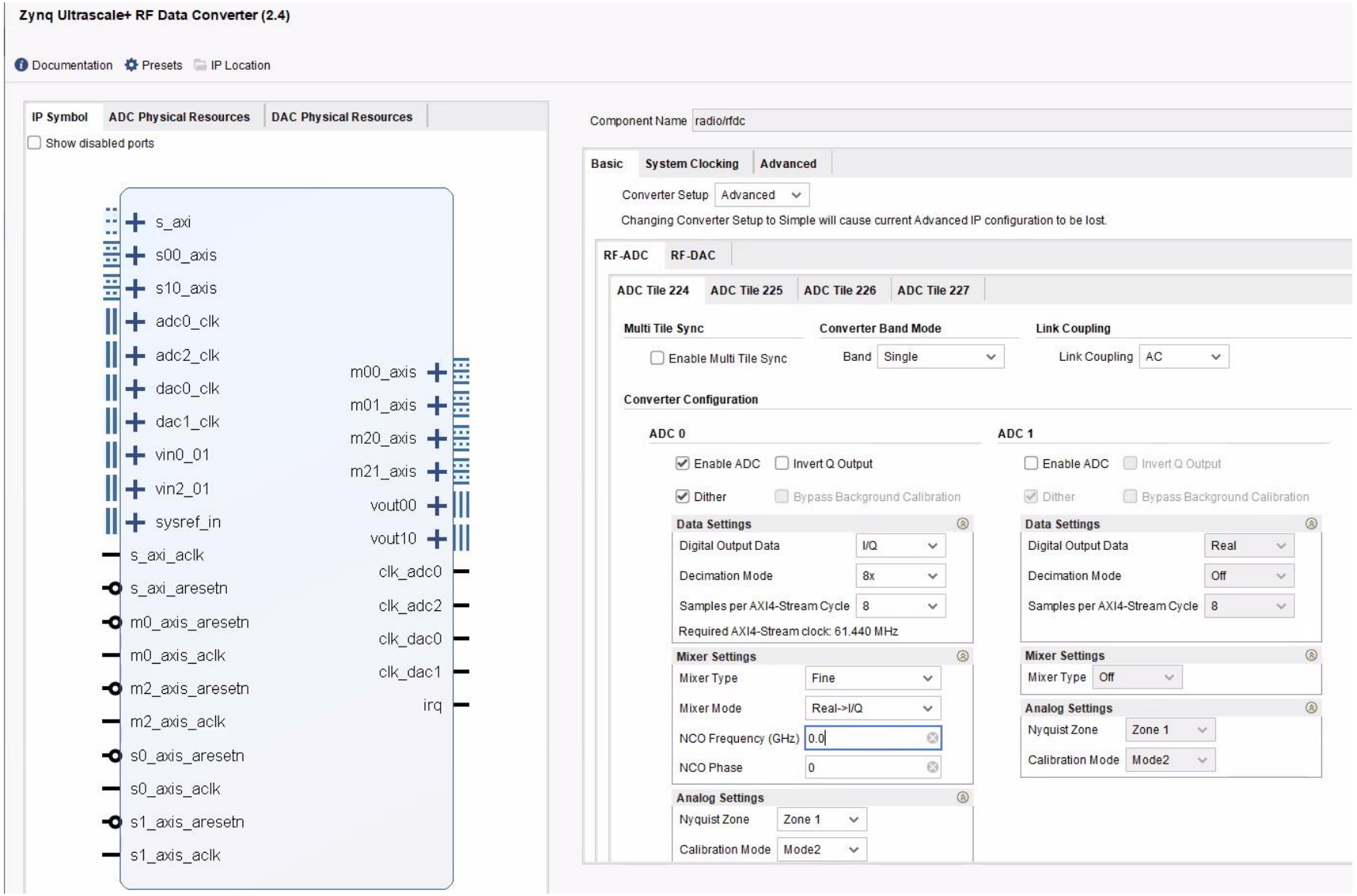
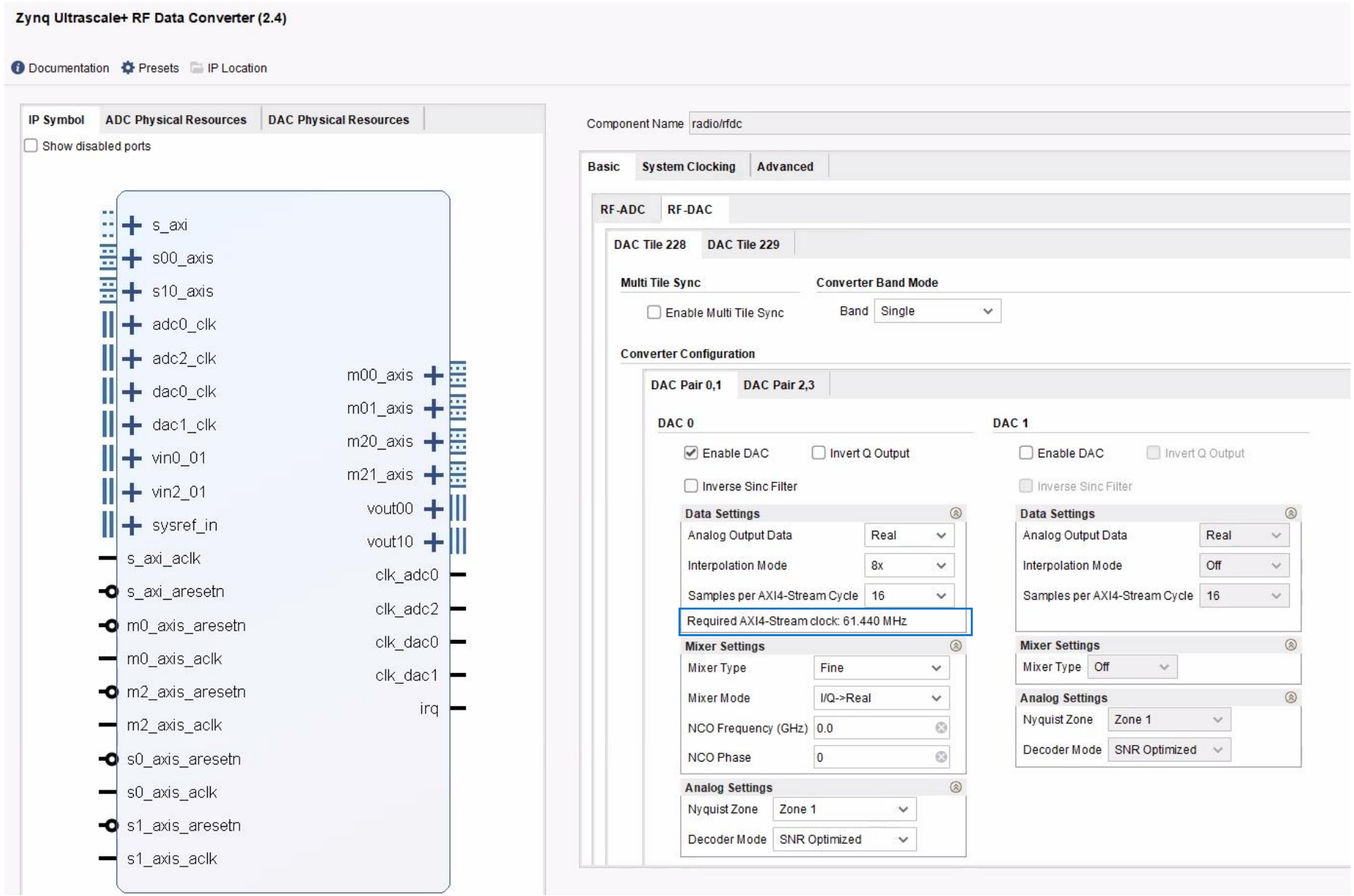
LTE Cell Search:

RF Soc - RF Data converter ADC Configurations:



LTE Cell Search:

RF Soc - RF Data converter DAC configurations:



LTE Cell Search:

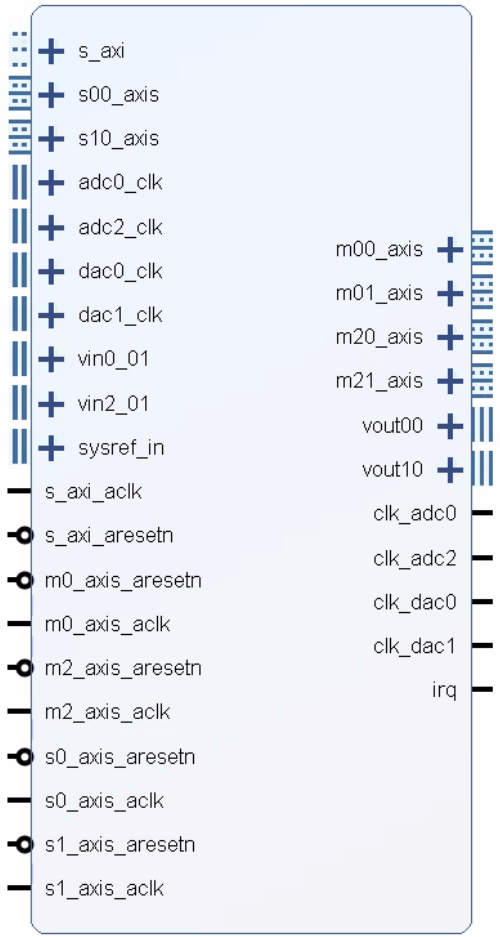
RF Soc - RF Data converter ADC/DAC Clock Configurations:

Zynq Ultrascale+ RF Data Converter (2.4)

Documentation | Presets | IP Location

IP Symbol | ADC Physical Resources | DAC Physical Resources

Show disabled ports



Component Name: radio/rfdc

Basic | System Clocking | Advanced

AXI4-Lite Interface Configuration

AXI4-Lite Clock (MHz): 100.0

Tile Clocking Settings

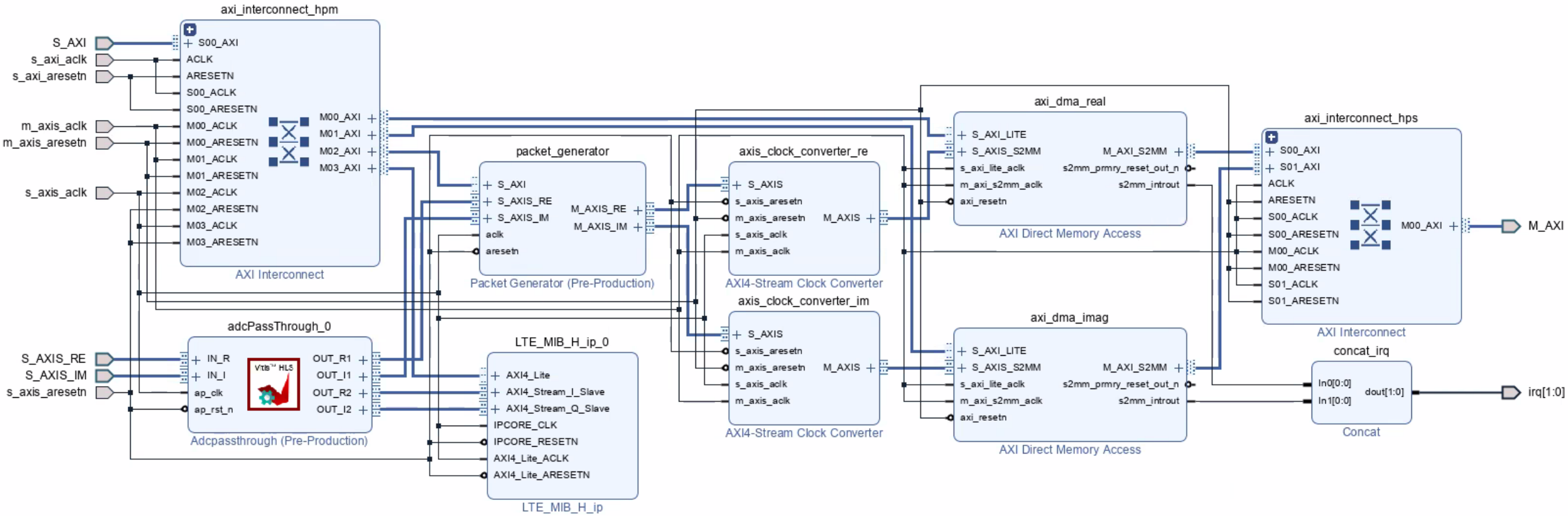
Tile	Sampling Rate (GSPS)	Max Fs (GSPS)	PLL	Reference Clock (MHz)	PLL Ref Clock (MHz)	Ref Clock Divider	Fabric Clock (MHz)	Clock Out (MHz)
ADC 224	3.93216	4.096	☑	491.520	491.52	1	61.440	61.440
ADC 225	2.0	4.096	☐	2000.000	-	1	0.0	15.625
ADC 226	3.93216	4.096	☑	491.520	491.52	1	61.440	61.440
ADC 227	2.0	4.096	☐	2000.000	-	1	0.0	15.625
DAC 228	3.93216	6.554	☑	491.520	491.52	1	61.440	61.440
DAC 229	3.93216	6.554	☑	491.520	491.52	1	61.440	61.440

PLL Summary Settings

Tile	Vco (MHz)	Fb Div	M	R
ADC 224	11796.480000000001	24	3	1
ADC 225	-	-	-	-
ADC 226	11796.480000000001	24	3	1
ADC 227	-	-	-	-
DAC 228	11796.480000000001	24	3	1
DAC 229	11796.480000000001	24	3	1

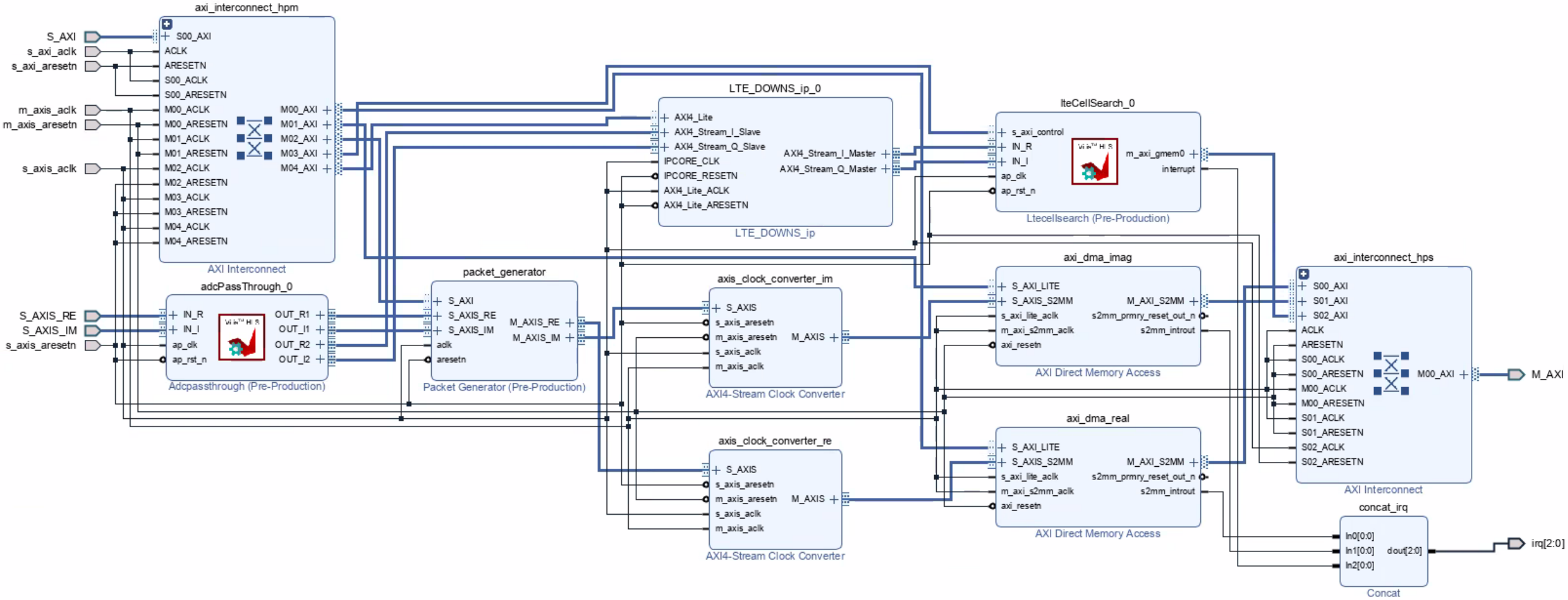
LTE Cell Search:

Vivado Block Diagram for Vitis Receiver: **Reference Simulink Implementation**



LTE Cell Search:

Vivado Block Diagram for Vitis Receiver: **Custom implementation**



LTE Cell Search:

Vivado Block Diagram for Transmitter: **Loopback Mode**