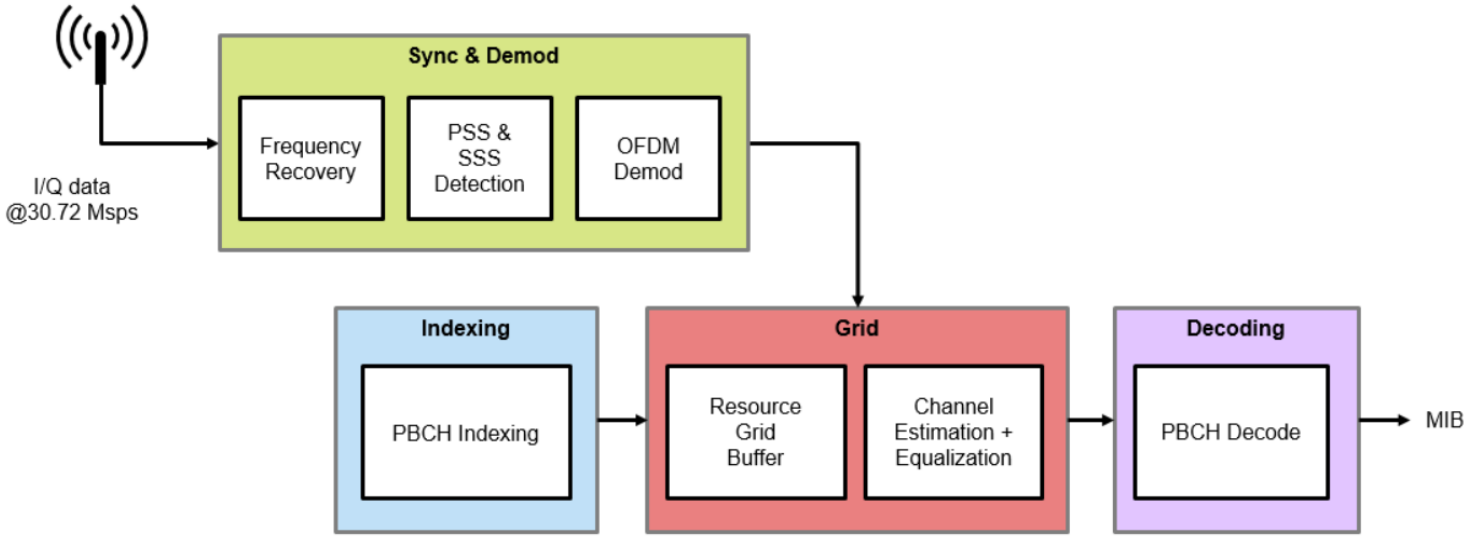
LTE

Project: LTE Cell Search
Cohort 9



Team: The Correlators

Jeffrey High
Mahesh Valavala
Satish Nichanametla
Shubhadip Paul

What is LTE Cell search about?

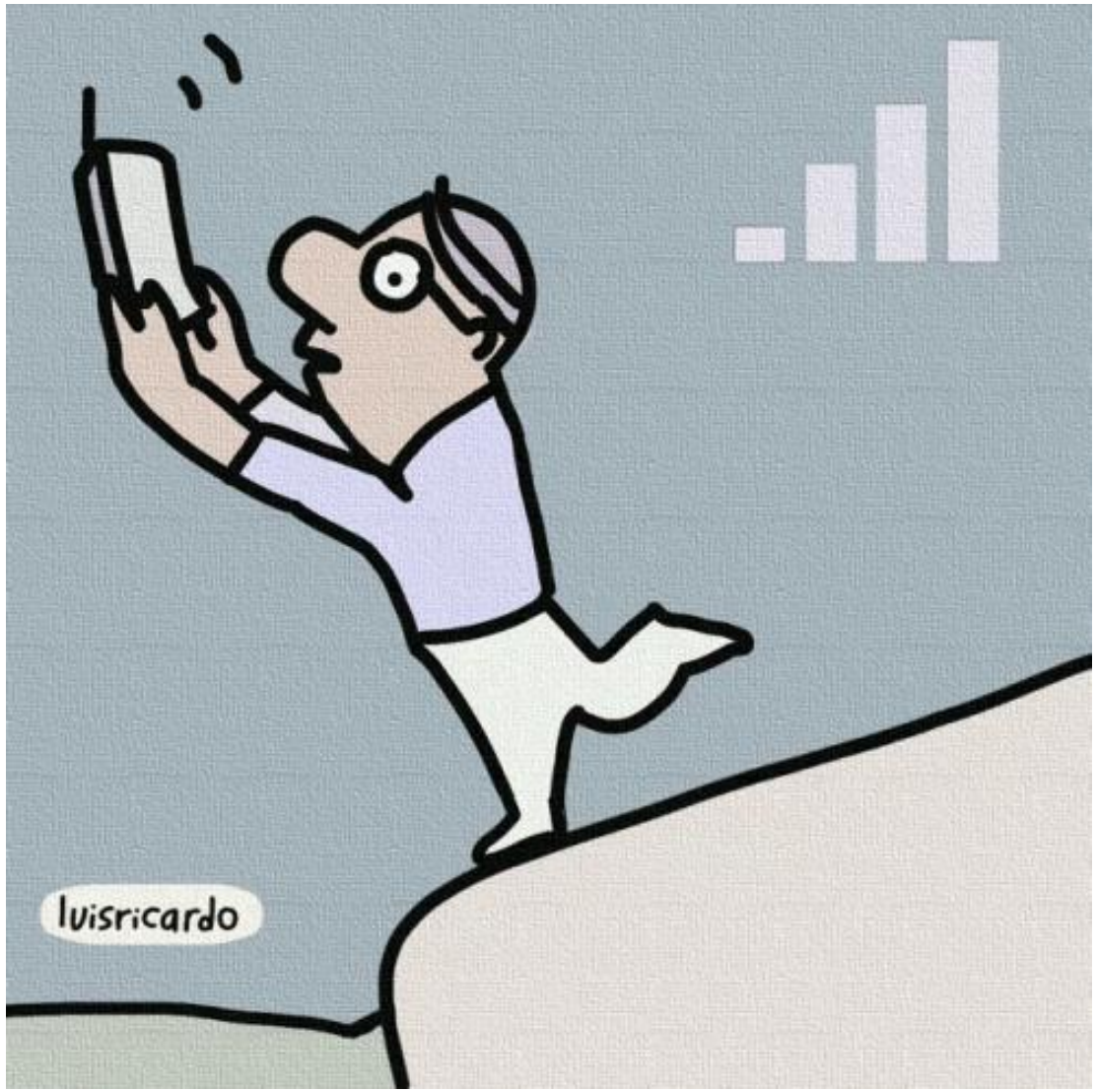
LTE stands for **Long Term Evolution** and referred as 4G LTE. It's a standard for wireless data transmission.

A Physical **Cell ID** (PCI) is an important parameter to establish connection with LTE network

Establish time and frequency synchronization with **LTE signals** and extract cell ID.

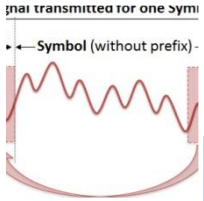
To decode LTE cell ID, Primary Synchronization Signal (**PSS**) and Secondary Synchronization Signal (**SSS**) signals should be decoded.

Xilinx Zynq® UltraScale+™ **RFSoC** with giga sample RF data converters is used.

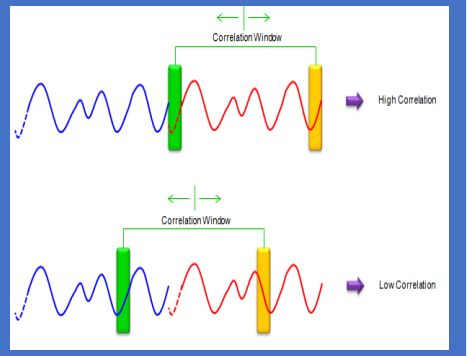


Main LTE Blocks – For Cell Search

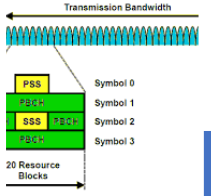
CP Correlation



- Cyclic Prefix is an exact copy of the last part of OFDM symbol



PSS

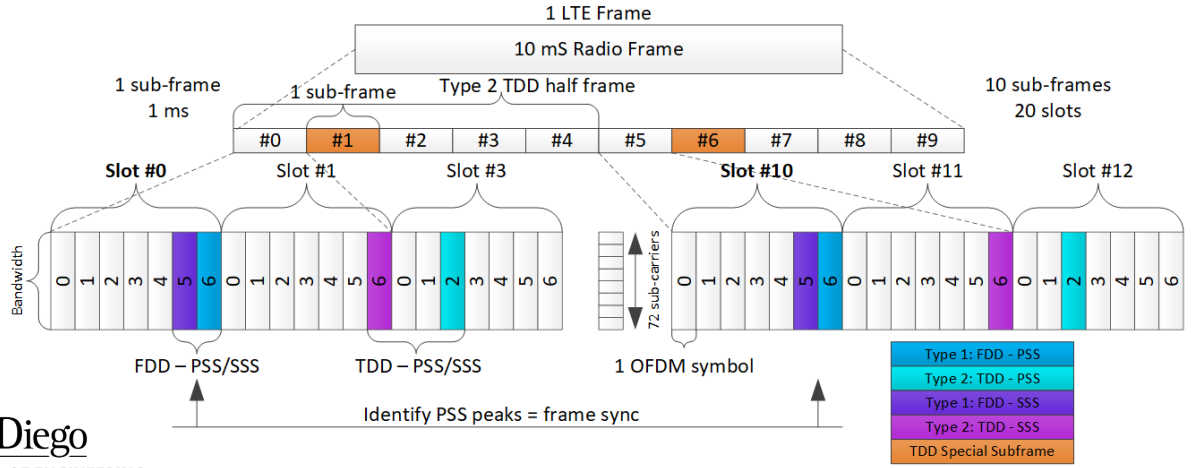


- 3 Zadoff-Chu root sequences defined in Frequency domain.
- IFFT to get time domain sequences which reduces HW complexity.
- Correlate Rx signal with 3 known time domain PSS sequences.

SSS

$$= 3N_{\mathrm{ID}}^{(1)} + \underset{N_{ID}^{(1)} \in \{0,1,\ldots,335\}}{\mathrm{SSS}}$$

- 1 of 168 known sequences.
- Polynomial based 3 binary sequences on Galois field.
- Correlation in frequency domain by taking 128-point FFT on Rx Symbol.

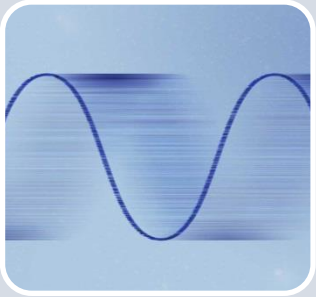


The physical cell identity, N_{ID}^{cell}, is defined by the equation:

$$N_{ID}^{CELL} = 3N_{ID}^{(1)} + N_{ID}^{(2)}$$

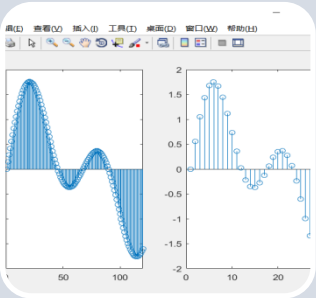
- $N_{ID}^{(1)}$ is the physical layer cell identity group (0 to 167).
- $N_{ID}^{(2)}$ is the identity within the group (0 to 2).

System Requirements and Configurations



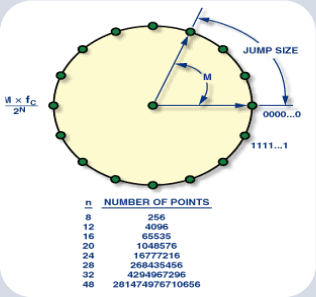
ADC Configuration

- RF SoC supports Fs in range of 1024 MHz - 4096 MHz.
- Our LTE Cell search IP needs Fs of 1.92MHz.
- ADC Fs is configured to 3932.16MHz as it is a multiple of 30.72MHz (LTE Rate). Reference ADC clock needed 491.52MHz.



Decimation

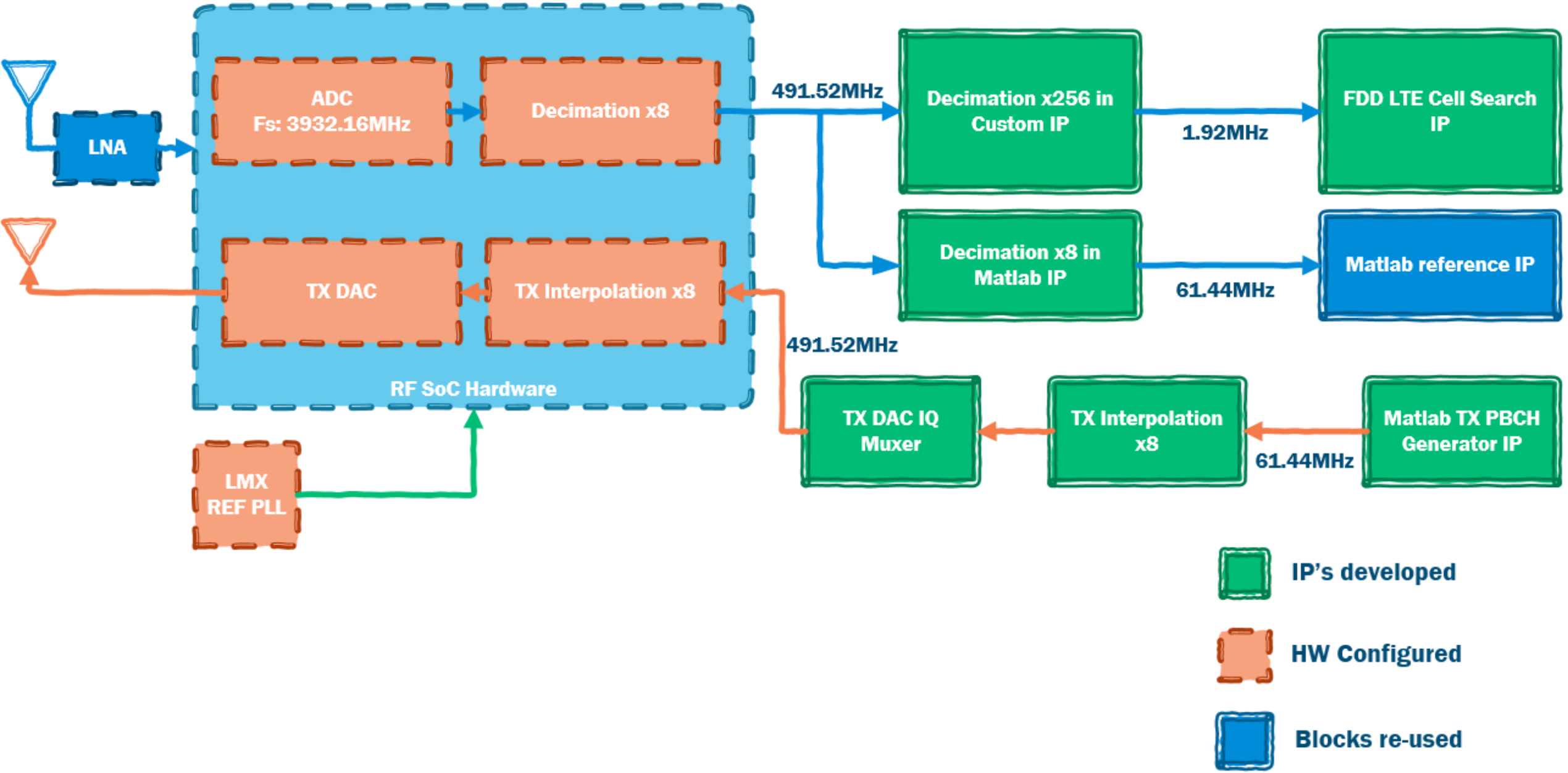
- Our System needs decimation of 2048.
- 8x decimation in RF Soc. From 3932.16MHz to 491.52MHz.
- 256x decimation in our custom IP to achieve Fs of 1.92MHz at LTE Cell search IP.



NCO (Numerically Controlled Oscillator)

- NCO configured to down convert carrier frequency to DC.
- 48-bit NCO per RF-ADC.
- Mixer is programmed to fine mode.

LTE Cell Search - System Block Diagram



LTE Cell Search Test Bench

Loop Back Mode

LTE waveform from DAC loop back

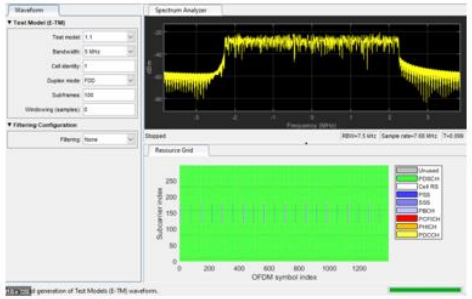
External Signal Generator

Single Tone/CW and LTE waveform testing at various carrier frequencies.

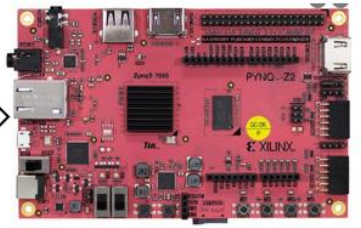
Pluto SDR

Wireless testing with LTE waveform

LTE Cell Search Test Setups



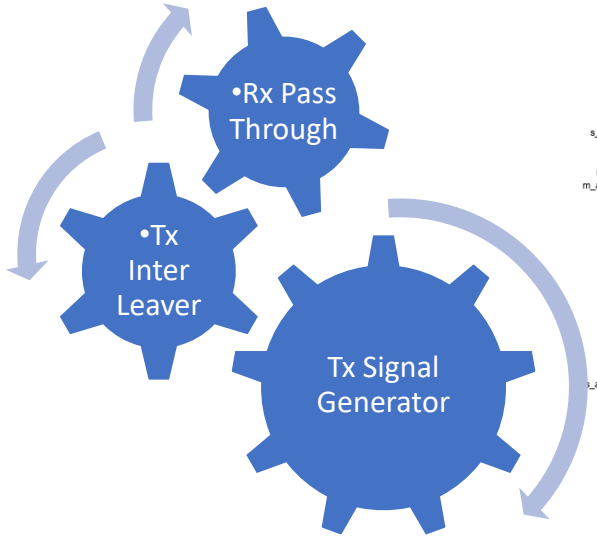
RTL Digitizer

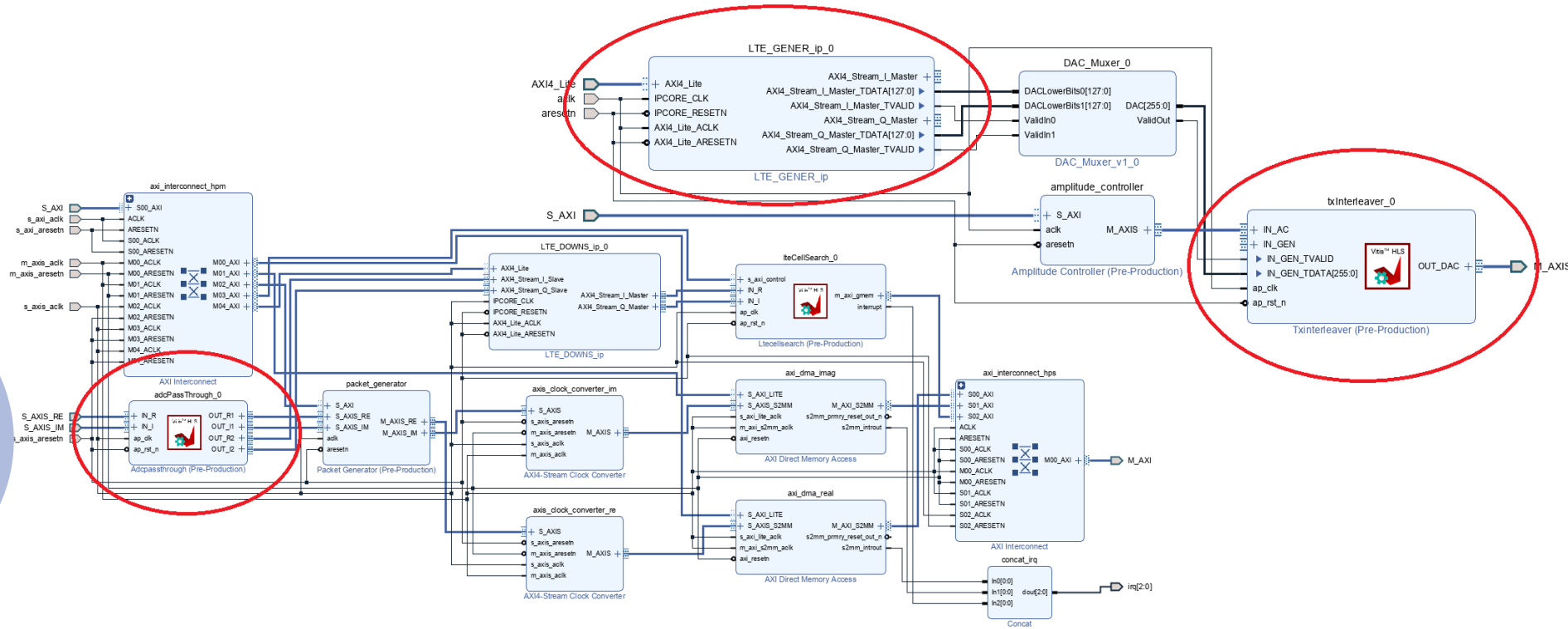


UC San Diego
JACOBS SCHOOL OF ENGINEERING

FPGA IP Research

Enablement Modules :





VITIS HLS

- Blocks - Rx Pass Through, Tx Inter Leaver

Matlab Simulink

- Blocks - TX Signal Generator

IPs to be developed on FPGA and their development platforms, reference models

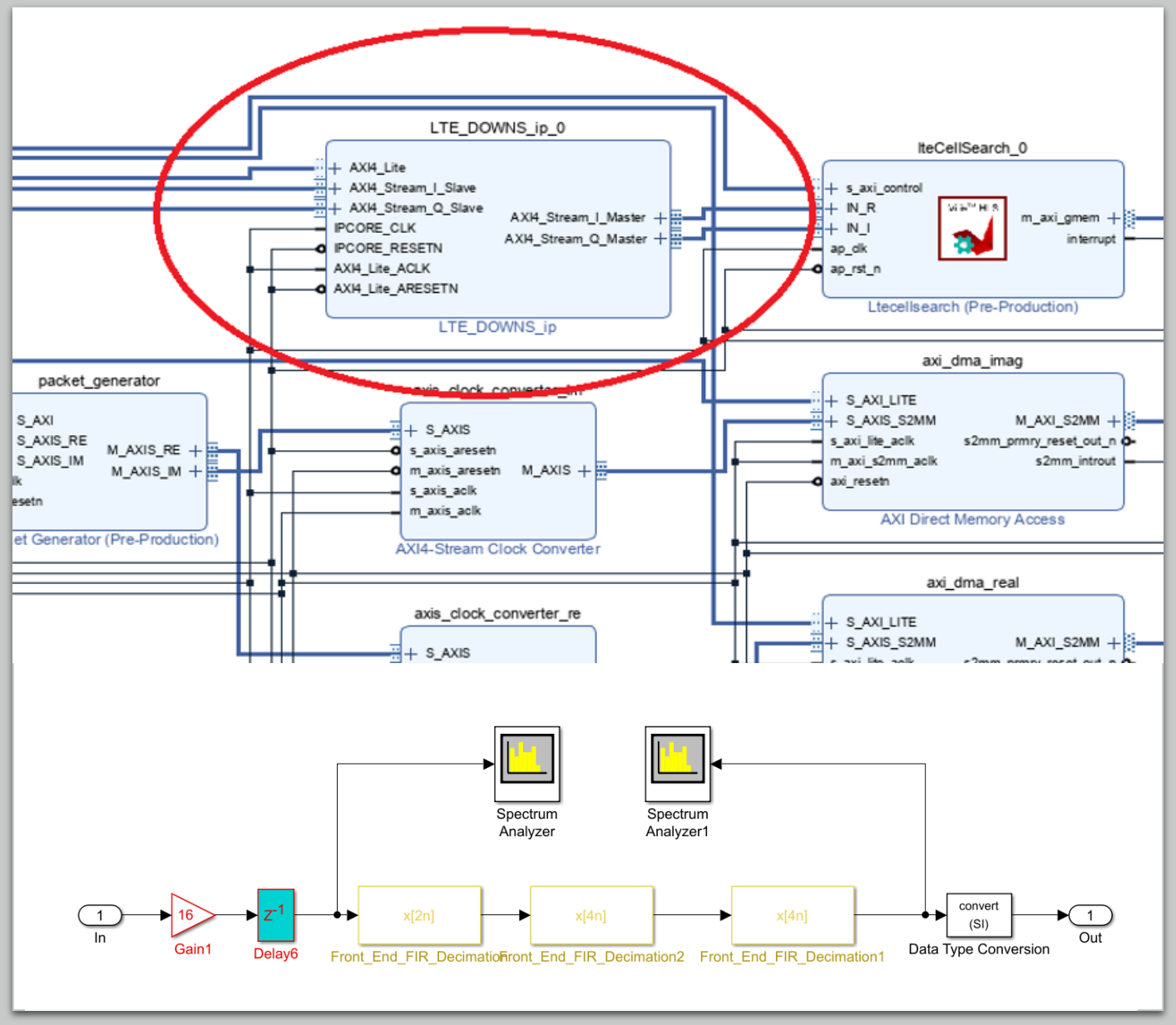
FPGA IP Research (cont'd..)

Front End Module

- Fs = 491.52MHz.
- Packed ADC samples.
- 8 I/Q samples
- Outputs 1.92MHz I/Q samples

Simulink Design

- Developed using Simulink Cascade Filters
- Designed with MATLAB filter designer



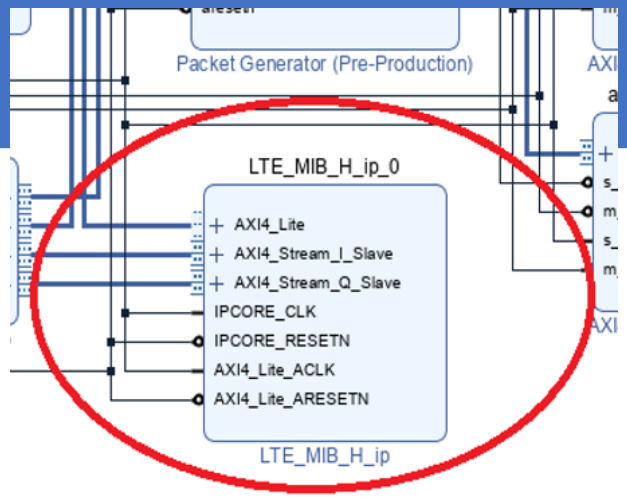
FPGA IP Research (cont'd..)

Reference Module

✓1. Benchmark IP on CH #1

✓2. Used for validating the setup

✓3. Decided to use Simulink LTE MIB detector design

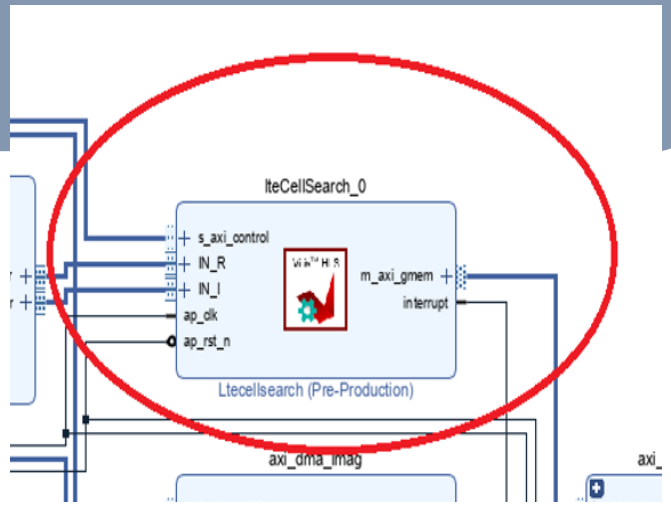


Custom Module

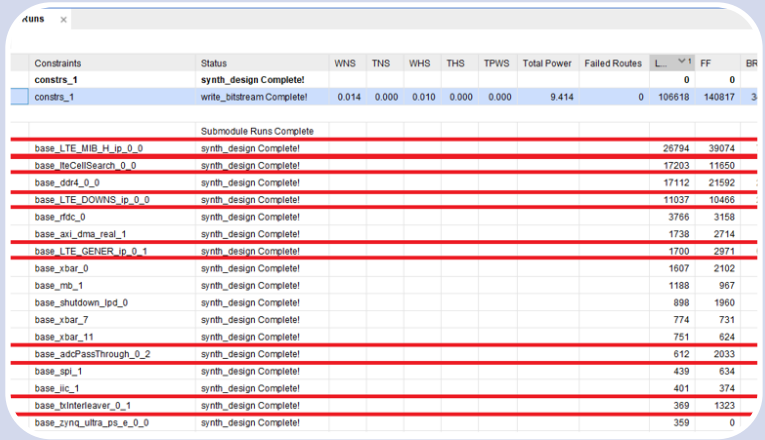
1. Own custom cell search algorithm on CH #2.

2. Used MATLAB to develop algorithms

3. Used VITIS HLS to implement algorithms.

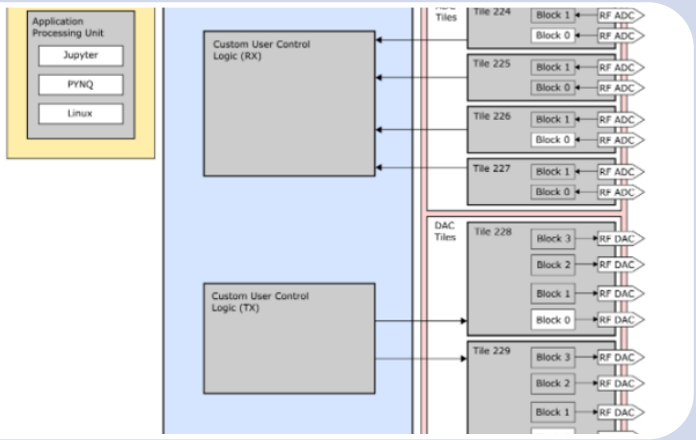


Overlay Research



Runs

Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	L...	FF	BR
constrs_1	synth_design Complete!								0	0	
constrs_1	write_bitstream Complete!	0.014	0.000	0.010	0.000	0.000	9.414	0	106618	140817	3
	Submodule Runs Complete										
base_LTE_MIB_H_ip_0_0	synth_design Complete!								26794	39074	
base_lteCellSearch_0_0	synth_design Complete!								17203	11650	
base_ddr4_0_0	synth_design Complete!								17112	21592	
base_LTE_DOWNS_ip_0_0	synth_design Complete!								11037	10466	
base_rfdc_0	synth_design Complete!								3766	3158	
base_axi_dma_real_1	synth_design Complete!								1738	2714	
base_LTE_GENER_ip_0_1	synth_design Complete!								1700	2971	
base_xbar_0	synth_design Complete!								1607	2102	
base_rnb_1	synth_design Complete!								1188	967	
base_shutdown_lpd_0	synth_design Complete!								898	1960	
base_xbar_7	synth_design Complete!								774	731	
base_xbar_11	synth_design Complete!								751	624	
base_adcPassThrough_0_2	synth_design Complete!								612	2033	
base_spi_1	synth_design Complete!								439	634	
base_iic_1	synth_design Complete!								401	374	
base_txInterleaver_0_1	synth_design Complete!								369	1323	
base_zynq_ultra_ps_e_0_0	synth_design Complete!								359	0	



Base Overlay:

1. RF SoC PYNQ image has default Base overlay.

2. The base design allows generation of bitstream with IPs to use RF ADC's and DAC's.

VIVADO IP Integration:

1. Added our HW IPs to base overlay and rebuild the base overlay.

2. Used 'base.tcl' script to generate VIVADO project with IP Integrator for the base overlay

RF Data Converters:

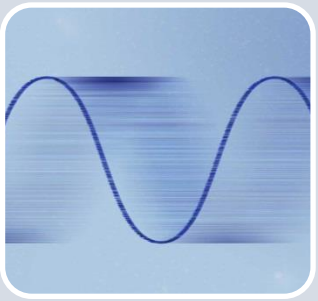
PYNQ Base image has notebooks to interact with Radio IP subsystem in the base overlay which allowed us to control RF Data Converters.

01_rf_dataconverter_intro.ipynb

02_rf_spectrum_analysis.ipynb

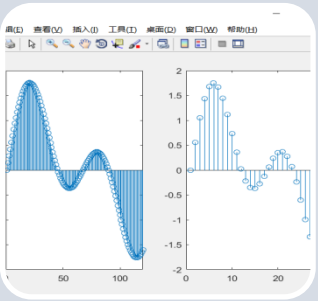
Choosing a reference overlay for RFSoC2x2 and application for implementing Cell Search

Challenges



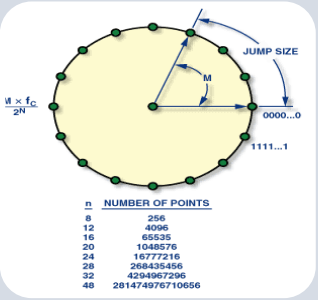
ADC Clock

- Fs of 3932.16MHz needed a reference clock of 491.52MHz.
- Register settings for this reference clock are not available
- Used TIC Pro TI software to generate the register settings for reference clock



IP Restart Algorithms

- In order scan over frequency, algorithms should have the ability to restart after tuning to a new frequency.
- Need to ensure the IP restart would not stall design



NCO Configurations

- Bug in PYNQ base overlay wrapper NCO settings.
- Found base reference host SW not supporting mixer in fine mode.

Thanks!

Prof. Ryan Kastner
Prof. Fred Harris
Prof. John Eldon
Patrick Ling

UC San Diego
JACOBS SCHOOL OF ENGINEERING

References
[1] https://www.rfsoc-pynq.io/overlays.html
[2] https://www.rfsoc-pynq.io/base_overlay.html
[3] https://github.com/Xilinx/RFSoC2x2-PYNQ.git
[4] https://github.com/strath-sdr/rfsoc_sam
[5] https://github.com/strath-sdr/rfsoc_ofdm
[6] https://www.mathworks.com/help/wireless-hdl/ug/lte-hdl-cell-search.html
[7] https://www.mathworks.com/help/lte/ug/synchronization-signals-pss-and-sss.html
[8] https://ieeexplore.ieee.org/document/599949
[9] https://www.mathworks.com/help/lte/ug/cell-search-mib-and-sib1-recovery.html
[10] https://www.sharetechnote.com/html/FrameStructure_DL.html#Overview