

LTE Cell Search:

Initial Project Setup and Configuration

Board File – Parts selection (Vivado Project Setup)

1. Board File Installation Instructions: https://www.rfsoc-pynq.io/board_files.html
2. Steps used in this project (instructions/script out of date based on Vivado version)
 - a. Download: <https://github.com/Xilinx/XilinxBoardStore/tree/2020.1/boards/Xilinx/rfsoc2x2/>
 - b. Linux path to place files prior to starting/running Vivado:
/tools/Xilinx/Vivado/2020.2/data/boards/board_files/rfsoc2x2/1.1
3. New Project: Browse Board tab menu (not Parts) to locate the board file configuration.

Follow Installation Instructions:

1. Linux steps may vary to generate similar results
2. https://github.com/jehigh-sd/LTE_Cell_Search/tree/main/HARDWARE

LTE Cell Search:

RF Soc - RF Data converter ADC Configurations:

Zynq Ultrascale+ RF Data Converter (2.4)

Documentation
Presets
IP Location

IP Symbol

ADC Physical Resources

DAC Physical Resources

☐ Show disabled ports

+

 s_axi

+

 s00_axi

+

 s10_axi

+

 adc0_clk

+

 adc2_clk

+

 dac0_clk

+

 dac1_clk

+

 vin0_01

+

 vin2_01

+

 sysref_in

+

 s_axi_aclk

+

 s_axi_aresetn

+

 m0_axis_aresetn

+

 m0_axis_aclk

+

 m2_axis_aresetn

+

 m2_axis_aclk

+

 s0_axis_aresetn

+

 s0_axis_aclk

+

 s1_axis_aresetn

+

 s1_axis_aclk

+

 m00_axis

+

 m01_axis

+

 m20_axis

+

 m21_axis

+

 vout0

+

 vout10

+

 clk_adc0

+

 clk_adc2

+

 clk_dac0

+

 clk_dac1

+

 irq

Component Name radio/rfdc

Basic

System Clocking

Advanced

Converter Setup

Advanced

Changing Converter Setup to Simple will cause current Advanced IP configuration to be lost.

RF-ADC

RF-DAC

ADC Tile 224

ADC Tile 225

ADC Tile 226

ADC Tile 227

Multi Tile Sync

Converter Band Mode

Link Coupling

☐ Enable Multi Tile Sync

Band

Single

Link Coupling

AC

Converter Configuration

ADC 0

ADC 1

☒ Enable ADC
☐ Invert Q Output
☒ Dither
☐ Bypass Background Calibration

Data Settings

Digital Output Data

I/Q

Decimation Mode

8x

Samples per AXI4-Stream Cycle

8

Required AXI4-Stream clock: 61.440 MHz

Mixer Settings

Mixer Type

Fine

Mixer Mode

Real->I/Q

NCO Frequency (GHz)

0.0

NCO Phase

0

Analog Settings

Nyquist Zone

Zone 1

Calibration Mode

Mode2

☐ Enable ADC
☐ Invert Q Output
☒ Dither
☐ Bypass Background Calibration

Data Settings

Digital Output Data

Real

Decimation Mode

Off

Samples per AXI4-Stream Cycle

8

Mixer Settings

Mixer Type

Off

Analog Settings

Nyquist Zone

Zone 1

Calibration Mode

Mode2

RF Soc - RF Data converter DAC configurations:

RF Soc - RF Data converter ADC/DAC Clock Configurations:

Component Name	radio/rfdc
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☐ Show disabled ports

Basic	System Clocking	Advanced
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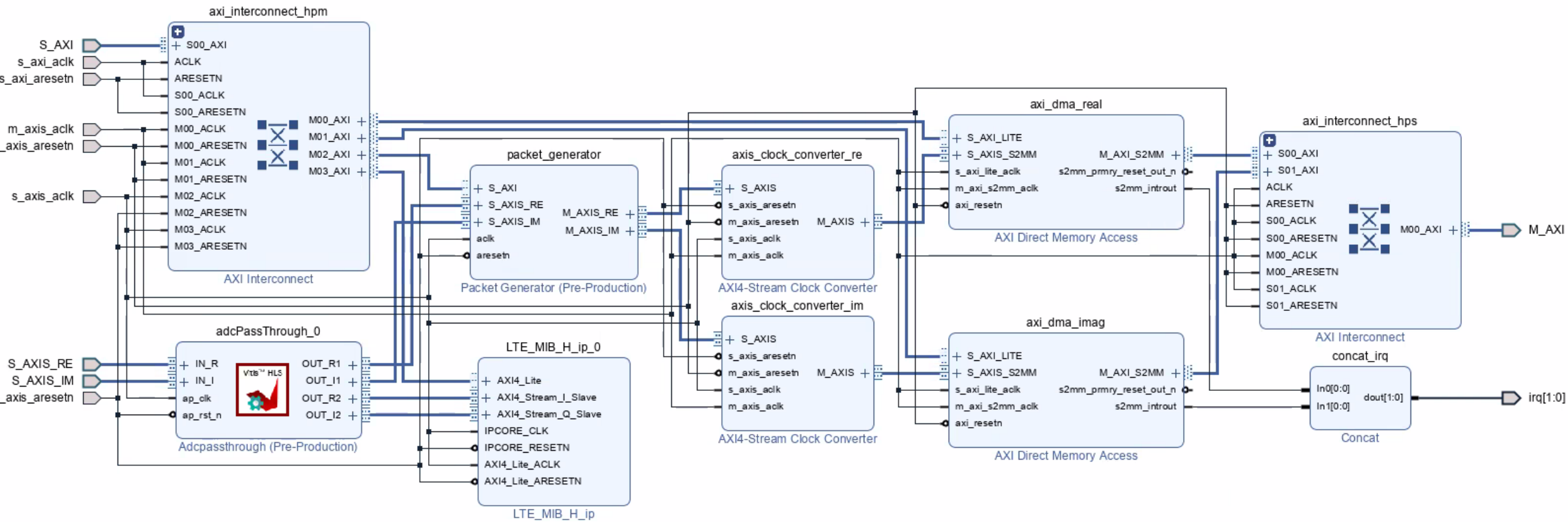
AXI4-Lite Clock (MHz) 100.0

Title	Sampling Rate (GSPS)	Max Fs (GSPS)	PLL	Reference Clock (MHz)	PLL Ref Clock (MHz)	Ref Clock Divider	Fabric Clock (MHz)	Clock Out (MHz)
ADC 224	3.93216	4.096		491.520	491.52	1	61.440	61.440
ADC 225	2.0	4.096		2000.000	-	1	0.0	15.625
ADC 226	3.93216	4.096		491.520	491.52	1	61.440	61.440
ADC 227	2.0	4.096		2000.000	-	1	0.0	15.625
DAC 228	3.93216	6.554		491.520	491.52	1	61.440	61.440
DAC 229	3.93216	6.554		491.520	491.52	1	61.440	61.440

Title	Vco (MHz)	Fb Div	M	R
ADC 224	11796.480000000001	24	3	1
ADC 225	-	-	-	-
ADC 226	11796.480000000001	24	3	1
ADC 227	-	-	-	-
DAC 228	11796.480000000001	24	3	1
DAC 229	11796.480000000001	24	3	1

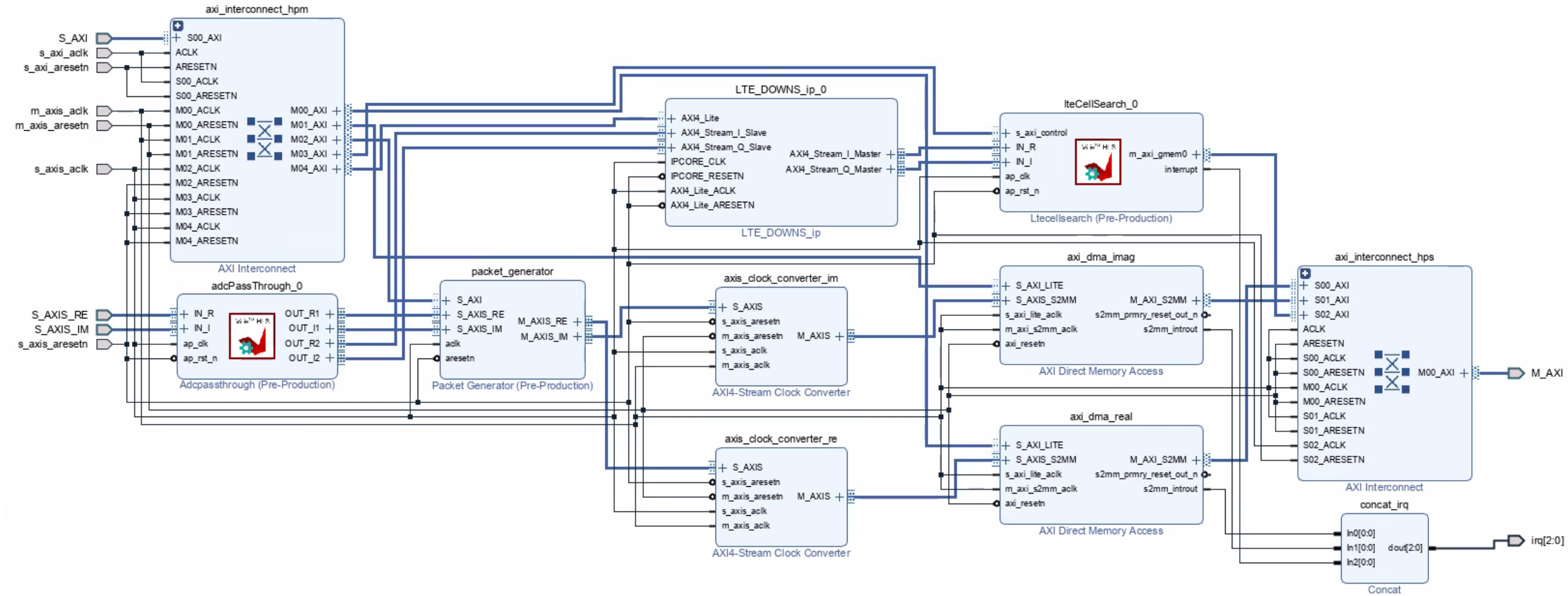
LTE Cell Search:

Vivado Block Diagram for Vitis Receiver: Reference Simulink Implementation



LTE Cell Search:

Vivado Block Diagram for Vitis Receiver: Custom implementation



LTE Cell Search:

Vivado Block Diagram for Transmitter: Loopback Mode

