

LTE CELL SEARCH HARDWARE DETAILS

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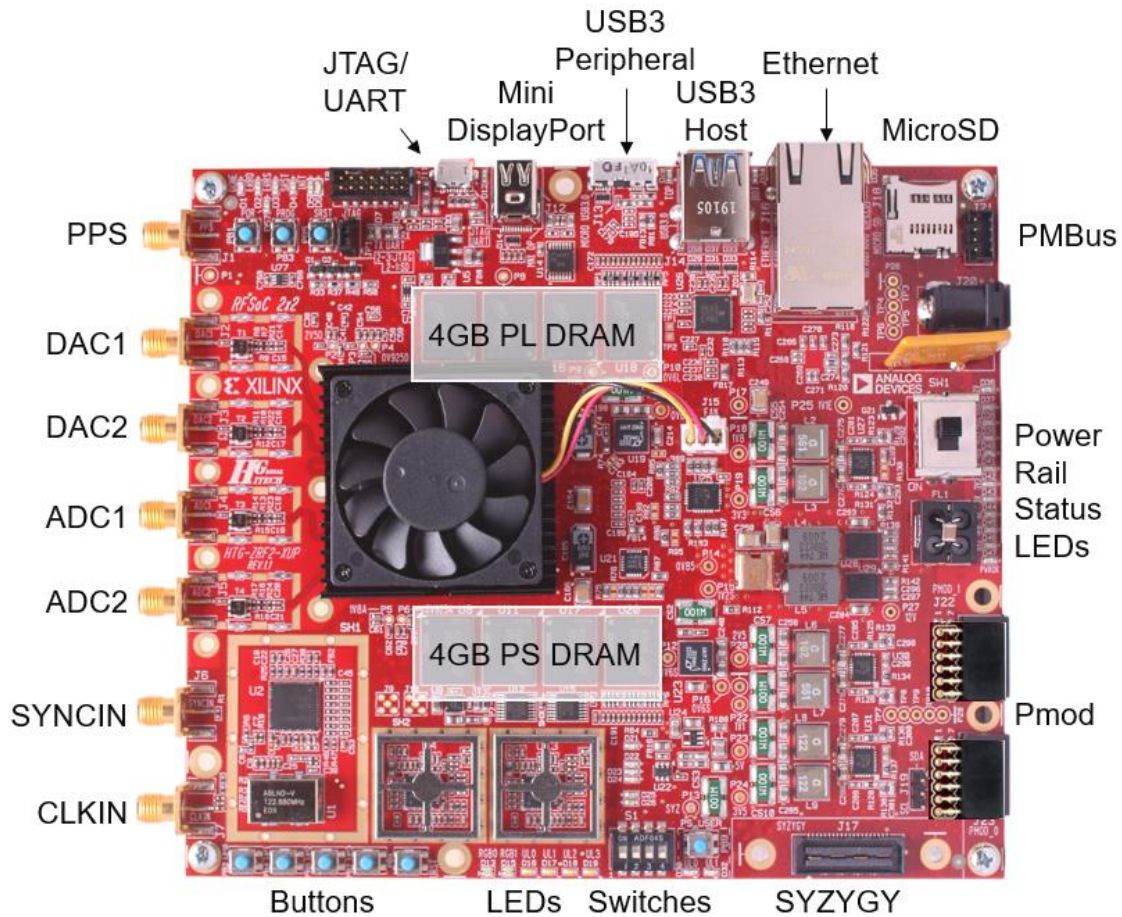
RFSoc:

[\[https://www.rfsoc-pynq.io/overview.html\]](https://www.rfsoc-pynq.io/overview.html)

Xilinx's Radio Frequency System-on-Chip (RFSoc) device combine high-accuracy ADCs and DACs operating at Giga samples per second (Gsps), with programmable heterogeneous compute engines. RFSoc 2x2 board with 2 RF DAC and 2 RF ADC channels. The RFSoc 2x2 has a Zynq Ultrascale+ XCZU28DR-FFVG1517-2-E with a Quad-core ARM Cortex A53 Processing System (PS) and Xilinx Ultrascale+ Programmable Logic (PL). There are BALUNs between the SMA connectors and the Zynq RFSoc on the board, which means that antenna and external signal sources can be connected directly to the board.

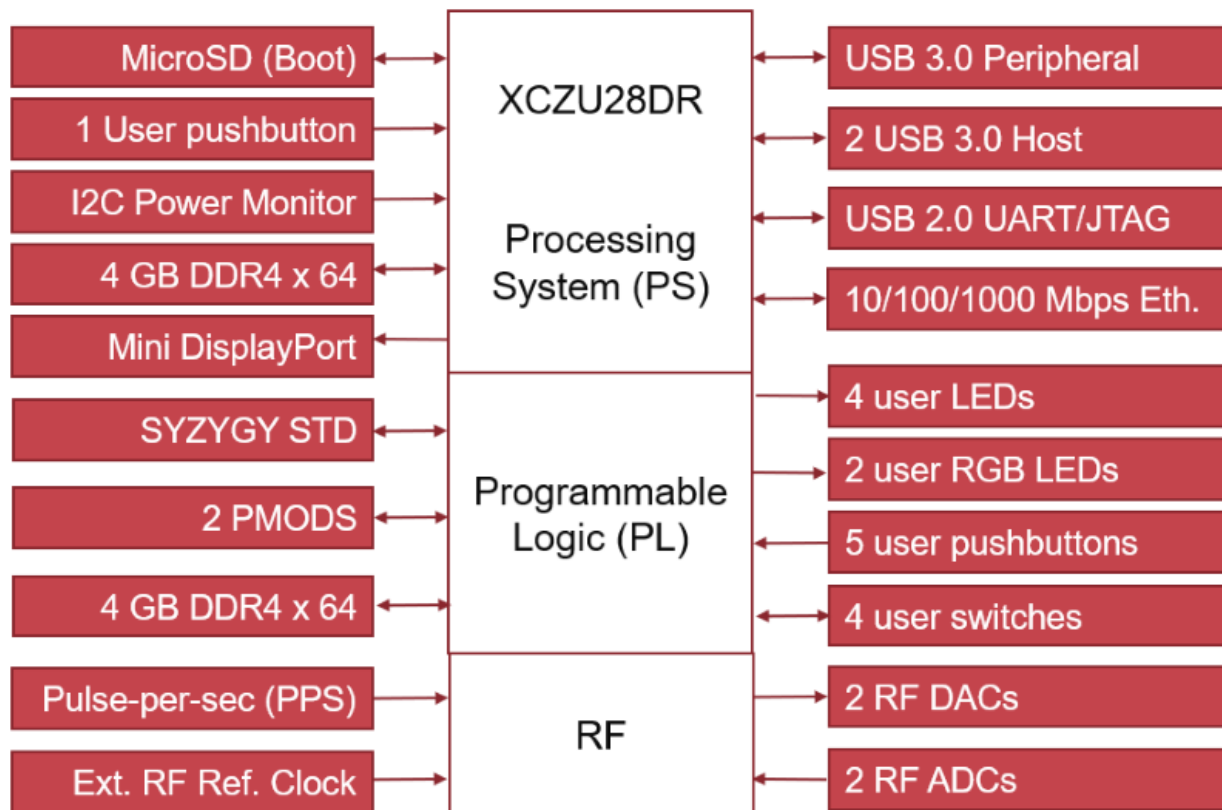
RFSoc Board:

[\[https://www.rfsoc-pynq.io/overview.html\]](https://www.rfsoc-pynq.io/overview.html)



RFSoc Block Diagram:

[\[https://www.rfsoc-pynq.io/overview.html\]](https://www.rfsoc-pynq.io/overview.html)



RFSoc LMX Configuration:

- [LMX2596 Configuration files](#)
- Configured ADC Clock for LTE OTA RF input
- Live Signal Target = 30.72 MHz
- ADC Sample Rate = 3932.16MHz
- IP Decimates from 3932.16MHz to 1.92MHz. 2048 decimation. RF SoC supports F_s in range of 1024 MHz - 4096 MHz.
- Our LTE Cell search IP needs F_s of 1.92MHz.
- ADC F_s is configured to 3932.16MHz as it is a multiple of 30.72MHz (LTE Rate).
- Reference ADC clock needed 491.52MHz.
- Our System needs decimation of 2048.
- 8x decimation in RF Soc. From 3932.16MHz to 491.52MHz.
- 256x decimation in our custom IP to achieve F_s of 1.92MHz at LTE Cell search IP.
- NCO configured to down convert carrier frequency to DC.
- 48-bit NCO per RF-ADC.
- Mixer is programmed to fine mode

There are three main components of the platform configuration.

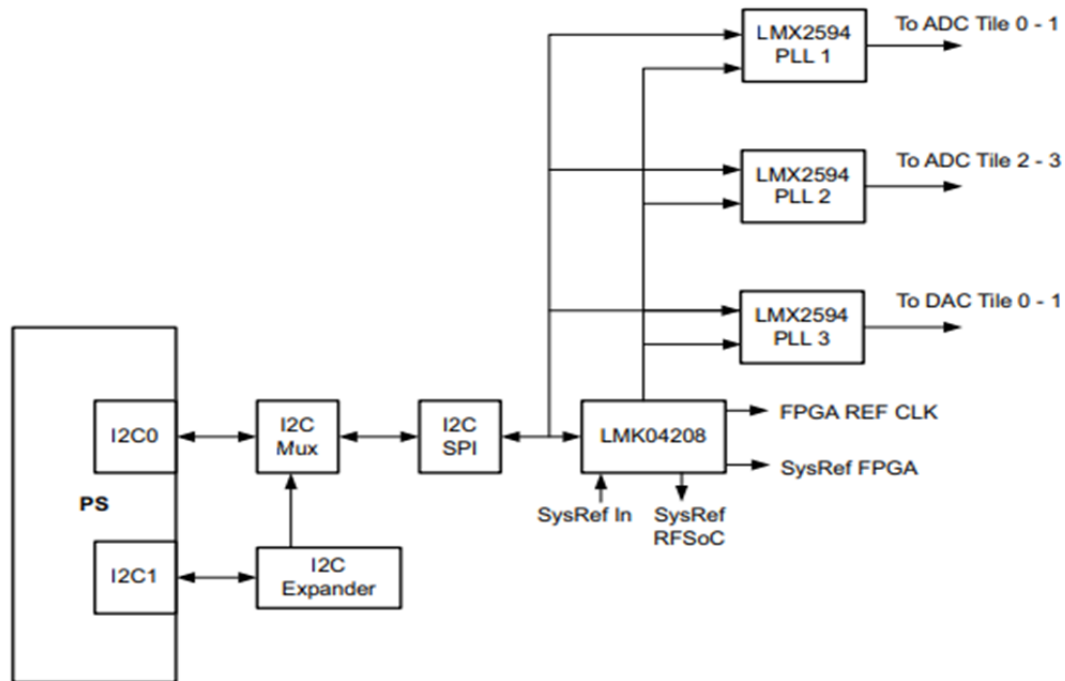
1. ADC Sampling: The sampling rate of the on-board ADC is configured to 3932.16MHz because it is multiple of LTE standard sampling rate.
2. Decimation: The hardware IP requires a sampling frequency of 1.92MHz. As a result, the system requires several stages of decimation.
3. Numerically Controlled Oscillator: The NCO is runtime configured to down convert the carrier frequency to DC.

RFSoc PLL configuration path using LMX:

[RFSoc Data Converter Evaluation Tool User Guide UG1287 (v2021.2)
October 28, 2021

Chapter 4: Clocking, Figure 4-1 ZCU111 AMS Clocking Structure:

https://www.xilinx.com/content/dam/xilinx/support/documents/boards_and_kits/zcu111/2021_2/ug1287-zcu111-rfsoc-eval-tool.pdf



LMX Configuration to configure to 245.76MHz

TICS Pro - LMX2594

File USB communications Select Device Options Tools Default configuration Help

LMX2594
User Controls
Raw Registers
PLL
RAMP
Burst Mode

General Context

Field Name: OSC_2X
Register Name: R9
Start Bit: 12
Stop Bit: 12
Length: 1
Description: Reference Path Doubler
0: Disabled
1: Enable

VCO Calibration

FCAL_LPFD_ADJ Fpd>=10
FCAL_HPFD_ADJ 100<Fpd<=150
CAL_CLK_DIV Div1, Fosc<=200
ACAL_CMP_DLY 10

VCO Assist

QUICK_RECEN_EN Estimate Settings
Start Amplitude 300
Start VCO VCO4
Start Capcode 1

MASH and Phase Synchronization

PFD_DLY_SEL 3
MASH_ORDER 3rd Order Modulator
MASH_RESET_N
MASH_SEED_EN
MASH_SEED 0
VCO_PHASE_SYNC
Toggle Sync Pin

SYSREF

SYSREF_EN
SYSREF_REPEAT
SYSREF_PULSE
SYSREF Delay Control
63 0 0 0
Toggle SysRefReq Pin

Approximate Current (mA) = 437

Effective Charge Pump Gain 15 mA

Approximate VCO Gain (MHz/V) = 69

Fvco 7864.32 MHz

FCAL_EN Toggle FCAL_EN to lock VCO after changing frequency

Channel Divider 32

2 x 2 x 8 x 2

SEG1_EN

Output MUX

RFoutA 245.76 MHz

OUTA_PD

OUTB_PD

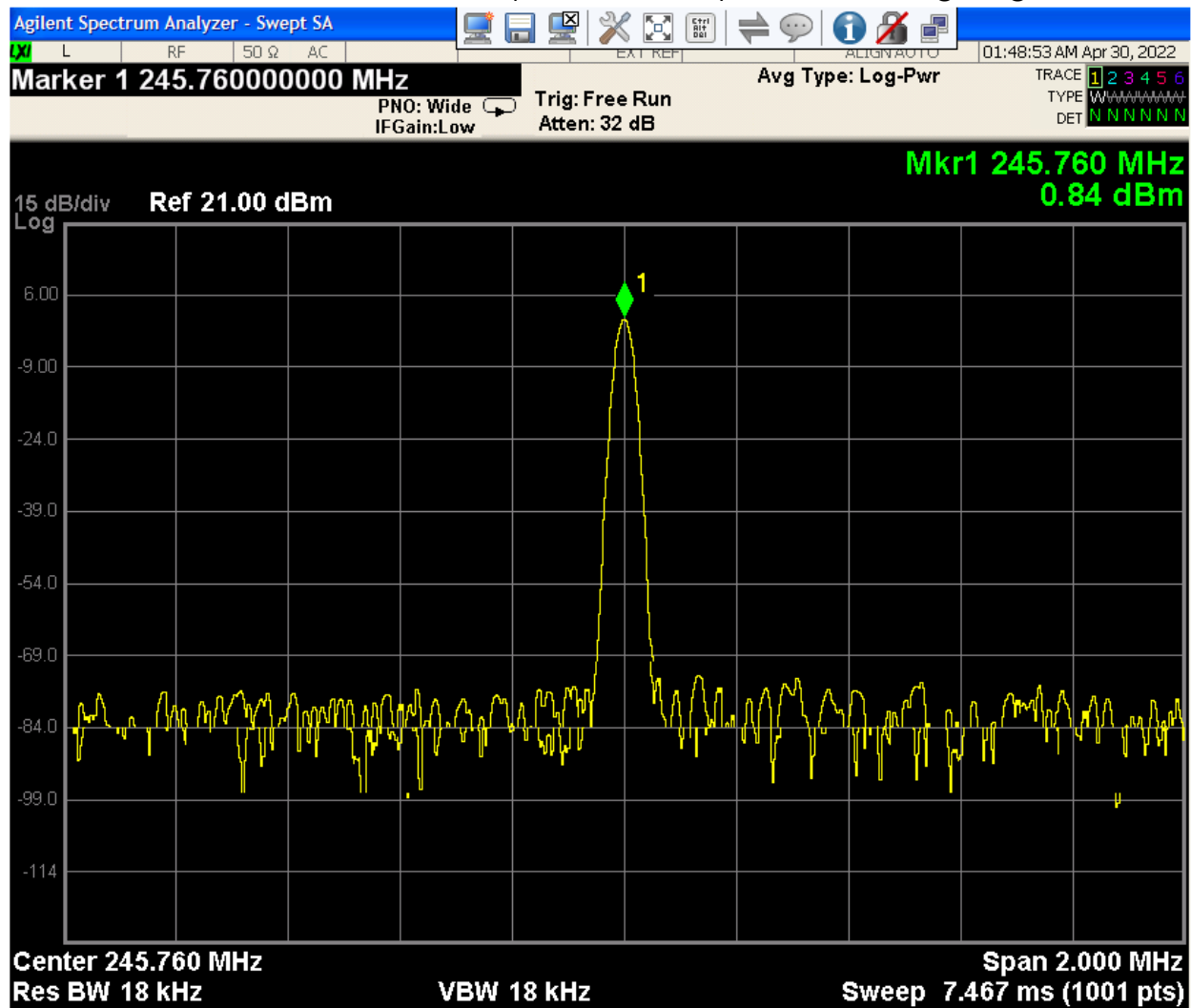
RFoutB 245.76 MHz

Write Register R0x2 as 0x02 0500
Write Register R0x1 as 0x01 0808
Write Register R0x0 as 0x00 249C

Protocol: SPI
Connection Mode: USB24576

TEXAS INSTRUMENTS

245.76MHz Tone measured in the Spectrum Analyzer after configuring LMX 2596



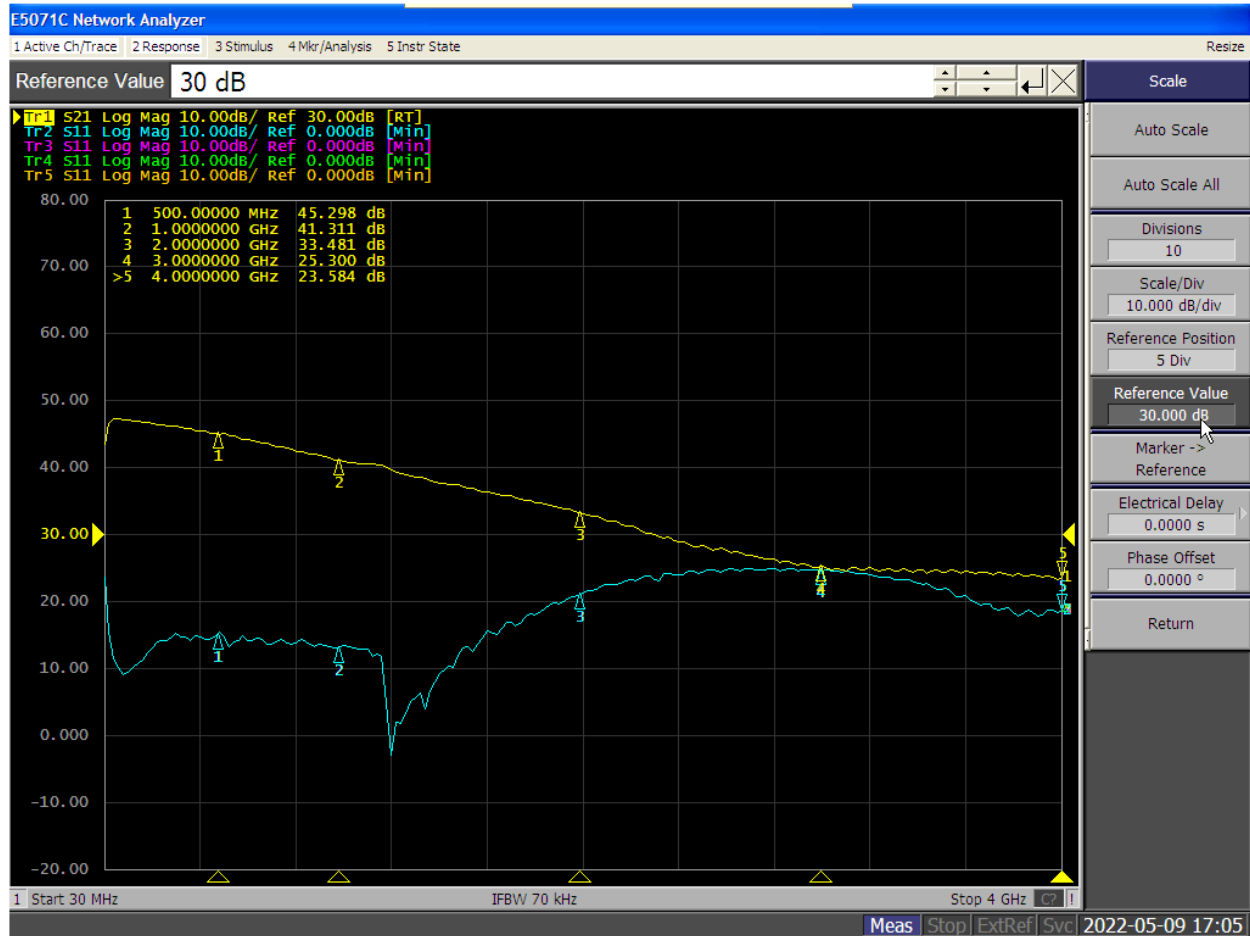
Low Noise Amplifier

- Used Vega Barebones - Ultra Low-Noise Variable Gain Amplifier (VGA) Module for RF & Software Defined Radio (SDR) from Nooelec.
- Highly Linear & Wideband 30MHz-4000MHz Frequency Capability w/Bias Tee & USB Power Options.
- Characterized Nooelec LNA for its Gain modes and return loss performance using KeySight E5071C vector network Analyzer
- Measured Gain (S21) for different Analog gain modes.
- Conclusion: ~40 dB of gain around ~1GHz and ~34 dB of gain around ~2GHz
- Return loss (S11) performance is reasonable in the entire bandwidth

Gain across frequency with 5 Gain modes



Gain (S21) and Return Loss (S11) performing at Max Gain mode



Nooelec LNA – Variable Gain Amplifier

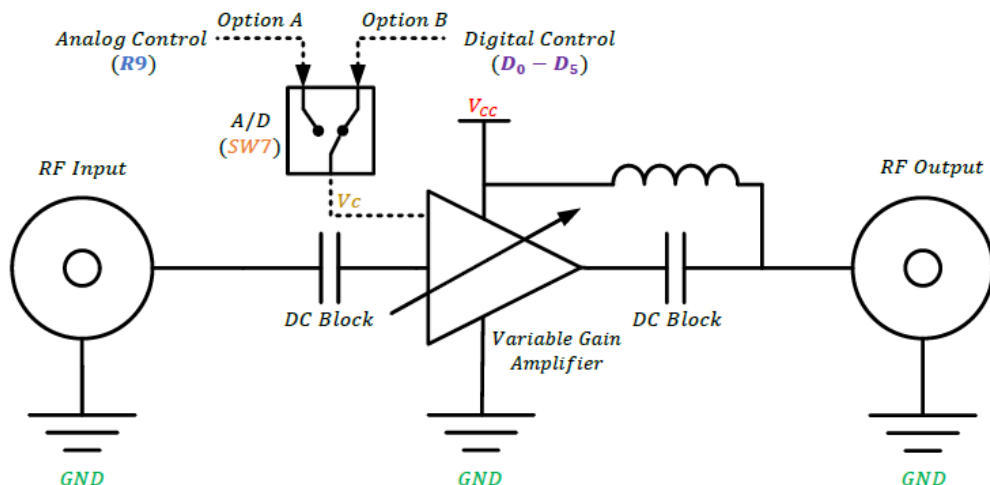
[\[https://www.noelec.com/store/vega-barebones.html\]](https://www.noelec.com/store/vega-barebones.html)



Information from Data Sheet

[https://www.nooelec.com/store/downloads/dl/file/id/103/product/334/vega_datasheet_revision_1.pdf]

Simplified Schematic



Calculating Vc Value

Option	Function	Type	Description
Option A	A/D Switch (SW7) not pressed	Analog Control By R9	$0.1 \text{ Volts} < V_c < 3.2 \text{ Volts}$
Option B	A/D Switch (SW7) pressed	Digital Control By $D_0 - D_5$	$V_c = 1.60 * D_5 + 0.80 * D_4 + 0.40 * D_3 + 0.20 * D_2 + 0.10 * D_1 + 0.05 * D_0$

Example Calculation:

If **Option 2** is enabled by pressing the A/D switch (SW7) and D_5, D_1 and D_0 pressed while D_4, D_3 and D_2 are not pressed then:

$$D_5 = D_1 = D_0 = 1$$

$$D_4 = D_3 = D_2 = 0$$

$$V_c = 1.60 * D_5 + 0.80 * D_4 + 0.40 * D_3 + 0.20 * D_2 + 0.10 * D_1 + 0.05 * D_0$$

$$V_c = 1.60 * 1 + 0.80 * 0 + 0.40 * 0 + 0.20 * 0 + 0.10 * 1 + 0.05 * 1$$

$$V_c = 1.60 + 0 + 0 + 0 + 0.10 + 0.05$$

$$V_c = 1.75 \text{ Volts}$$