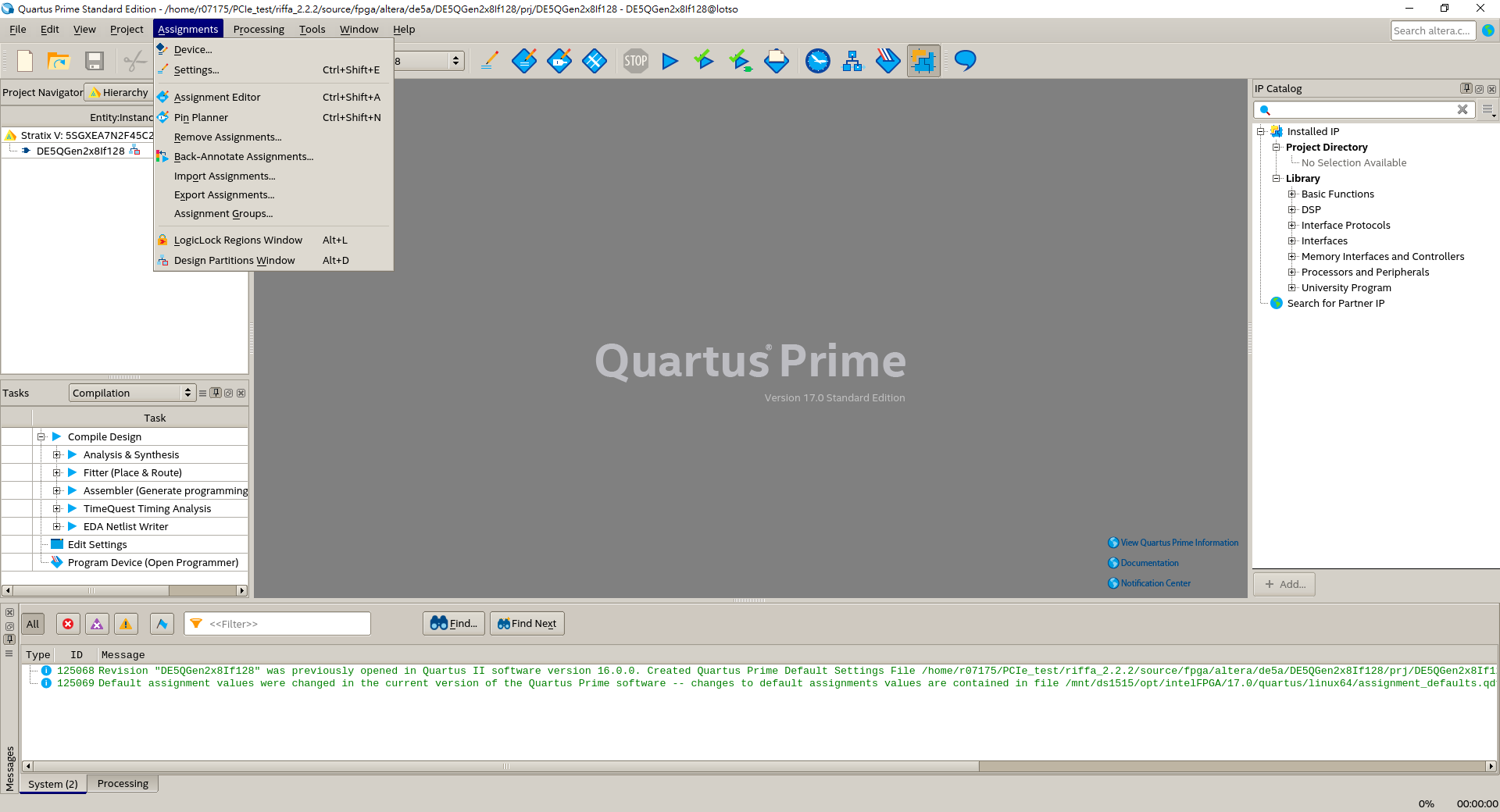
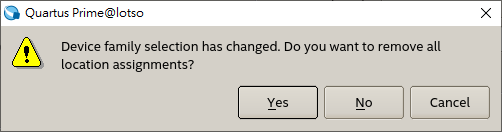
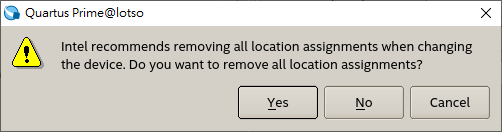
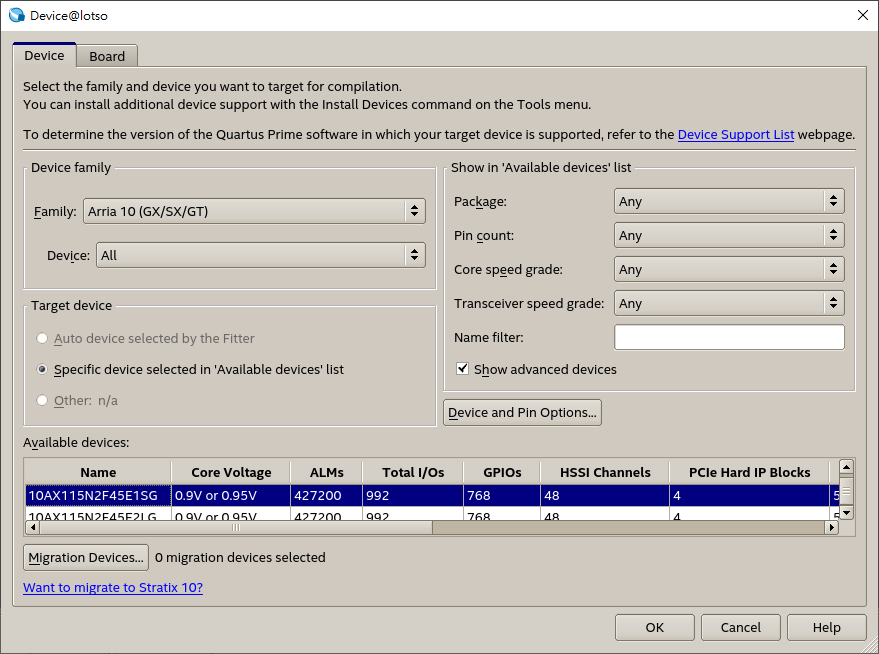
DE5a-Net RIFFA Setup Tutorial

1. **前置作業**
   1. 啟動Quartus
   2. 根據PCIe需求，開啟對應的DE5 project  
      如: ./riffa\_2.2.2/source/fpga/altera/de5/DE5QGen2x8If128/prj/ DE5QGen2x8If128.qpf
2. **修改Quartus Project的FPGA型號**
   1. 點選 Assignments -> Device…

**A**

* 1. Device Family選擇Arria 10 (GX/SX/GT)
  2. 詢問是否移除location assignments，選擇No
  3. Available devices選擇10AX115N2F45E1SG
  4. 再次詢問是否移除location assignments，選擇No
  5. 完成修改，點選OK



**F**

**D**

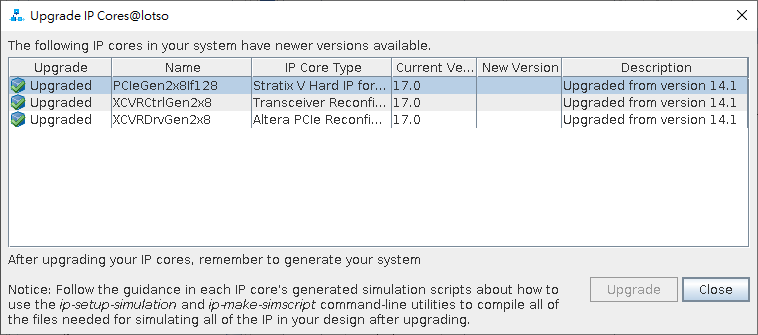
**E**

**C**

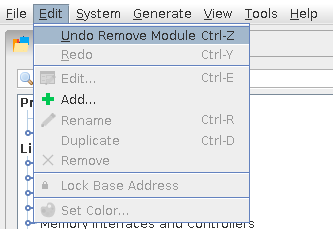
**B**

1. **更新Qsys IP**

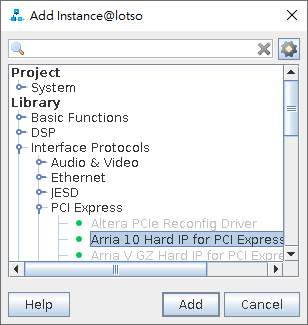
**A**

* 1. 從工具列開啟Qsys視窗
  2. 開啟對應的Qsys檔案 File -> Open  
     如: (.qpf檔的位置)/../ip/QsysDE5Gen2x8If128.qsys
  3. 關閉Upgrade IP Core視窗

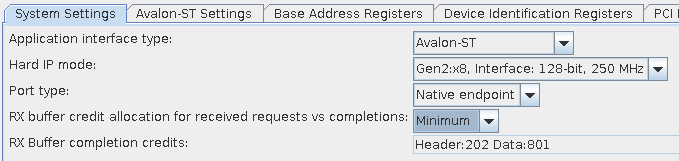
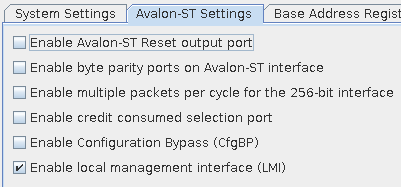
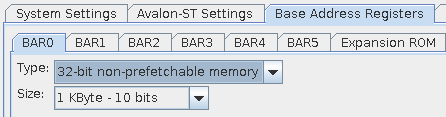
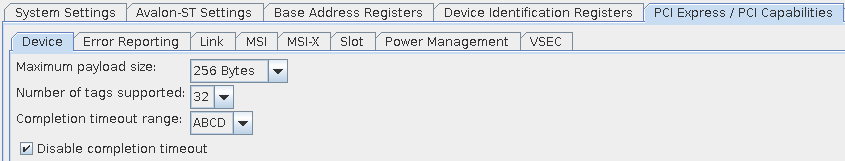
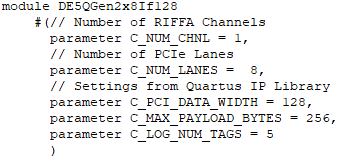
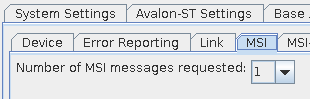
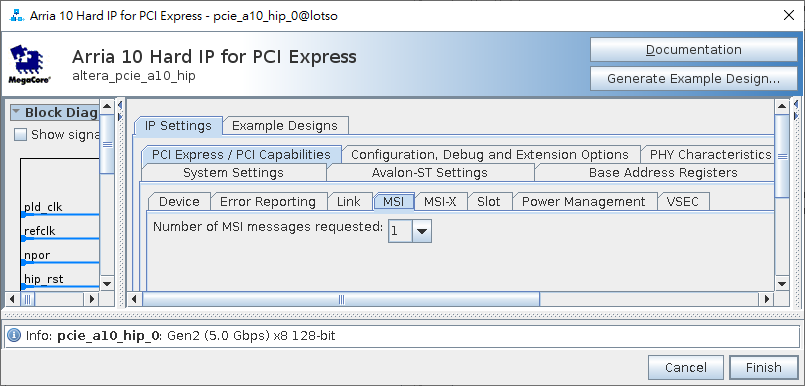
**C**

* 1. 將面板中所有IP刪除(點選IP -> 右鍵 -> Remove)
  2. 新增IP (Edit -> Add..)

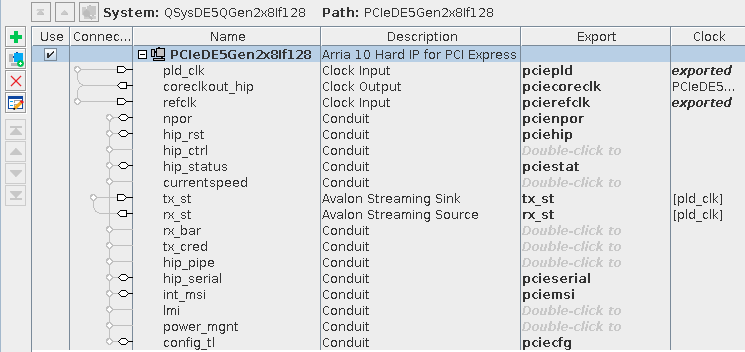
**E**

* 1. 選擇Library -> Interface Protocols -> PCI Express -> Arria 10 Hard IP for PCI Express，按Add

**F**

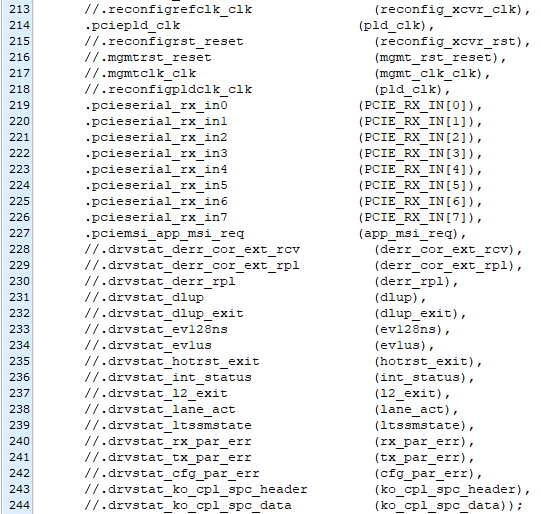
* 1. IP System設定如下。Hard IP mode選擇與原本的project對應的模式
  2. Avalon-ST Settings設定如下
  3. Base Address Registers -> BAR0設定如下
  4. PCI Express / PCI Capability -> Device設定如下。其中兩個參數需與top module中相符
  5. PCI Express / PCI Capability -> MS設定如下
  6. 點選Finish，完成IP設定

**L**

* 1. 修改Name與Export如下。Name對應PCIe模式

**M**

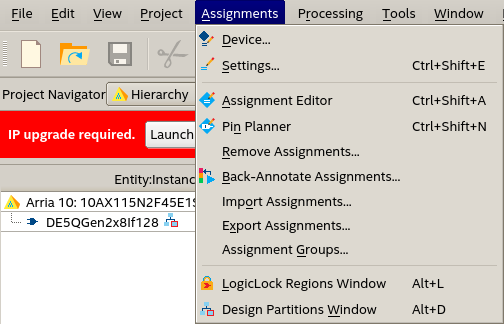
* 1. 儲存並關閉Qsys。若出現詢問是否generate，選擇是
  2. 回到Quartus，出現詢問是否將Qsys IP加入project，選擇是

1. **修改Top Module**
   1. 以文字編輯器開啟top module之verilog檔  
      (.qpf檔的位置)/../hdl/QsysDE5Gen2x8If128.v
   2. 將QSysDE5QGen2x8If128 pcie\_system\_inst module的下列input port註解或刪除(括號和分號記得保留)。

移到下一行

1. **修改Location Assignment**
   1. 關閉Quartus
   2. 以文字編輯器開啟Assignment檔  
      如: (.qpf檔的位置)/./QsysDE5Gen2x8If128.qsf
   3. 參考附件之.qsf檔與下方表格修改Assignment檔。需修改之內容包含但不限於PIN名稱(location assignment)、IO standard參數、PCIe Gen、Arria 10 PCIe新增內容、Stratix V PCIe內容…。若使用PCIe Gen2x8 128bit，可直接複製參考.qsf檔之內容。

|  |  |  |
| --- | --- | --- |
| Top Module內名稱(供參考) | DE5 Pin名稱 | DE5a Pin名稱 |
| PCIE\_REFCLK | PIN\_AK38 | PIN\_AH40 |
| PCIE\_RESET\_N | PIN\_AU33 | PIN\_AT25 |
| PCIE\_RX\_IN[0] | PIN\_BB43 | PIN\_AU42 |
| PCIE\_RX\_IN[0](n) | PIN\_BB44 | PIN\_AU41 |
| PCIE\_RX\_IN[1] | PIN\_BA41 | PIN\_AR42 |
| PCIE\_RX\_IN[1](n) | PIN\_BA42 | PIN\_AR41 |
| PCIE\_RX\_IN[2] | PIN\_AW41 | PIN\_AN42 |
| PCIE\_RX\_IN[2](n) | PIN\_AW42 | PIN\_AN41 |
| PCIE\_RX\_IN[3] | PIN\_AY43 | PIN\_AL42 |
| PCIE\_RX\_IN[3](n) | PIN\_AY44 | PIN\_AL41 |
| PCIE\_RX\_IN[4] | PIN\_AT43 | PIN\_AJ42 |
| PCIE\_RX\_IN[4](n) | PIN\_AT44 | PIN\_AJ41 |
| PCIE\_RX\_IN[5] | PIN\_AP43 | PIN\_AG42 |
| PCIE\_RX\_IN[5](n) | PIN\_AP44 | PIN\_AG41 |
| PCIE\_RX\_IN[6] | PIN\_AM43 | PIN\_AE42 |
| PCIE\_RX\_IN[6](n) | PIN\_AM44 | PIN\_AE41 |
| PCIE\_RX\_IN[7] | PIN\_AK43 | PIN\_AC42 |
| PCIE\_RX\_IN[7](n) | PIN\_AK44 | PIN\_AC41 |
| PCIE\_TX\_OUT[0] | PIN\_AY39 | PIN\_AV44 |
| PCIE\_TX\_OUT[0](n) | PIN\_AY40 | PIN\_AV43 |
| PCIE\_TX\_OUT[1] | PIN\_AV39 | PIN\_AT44 |
| PCIE\_TX\_OUT[1](n) | PIN\_AV40 | PIN\_AT43 |
| PCIE\_TX\_OUT[2] | PIN\_AT39 | PIN\_AP44 |
| PCIE\_TX\_OUT[2](n) | PIN\_AT40 | PIN\_AP43 |
| PCIE\_TX\_OUT[3] | PIN\_AU41 | PIN\_AM44 |
| PCIE\_TX\_OUT[3](n) | PIN\_AU42 | PIN\_AM43 |
| PCIE\_TX\_OUT[4] | PIN\_AN41 | PIN\_AK44 |
| PCIE\_TX\_OUT[4](n) | PIN\_AN42 | PIN\_AK43 |
| PCIE\_TX\_OUT[5] | PIN\_AL41 | PIN\_AH44 |
| PCIE\_TX\_OUT[5](n) | PIN\_AL42 | PIN\_AH43 |
| PCIE\_TX\_OUT[6] | PIN\_AJ41 | PIN\_AF44 |
| PCIE\_TX\_OUT[6](n) | PIN\_AJ42 | PIN\_AF43 |
| PCIE\_TX\_OUT[7] | PIN\_AG41 | PIN\_AD44 |
| PCIE\_TX\_OUT[7](n) | PIN\_AG42 | PIN\_AD43 |
| LED[0] | PIN\_AW37 | PIN\_AF10 |
| LED[1] | PIN\_AV37 | PIN\_AF9 |
| LED[2] | PIN\_BB36 | PIN\_Y13 |
| LED[3] | PIN\_BB39 | PIN\_W11 |
| LED[4] | PIN\_AH15 | PIN\_T11 |
| LED[5] | PIN\_AH13 | PIN\_R11 |
| LED[6] | PIN\_AJ13 | PIN\_N15 |
| LED[7] | PIN\_AJ14 | PIN\_M15 |
| OSC\_BANK3D\_50MHZ | PIN\_BC28 | PIN\_AN7 |

* 1. 存檔後關閉.qsf檔；重啟Quartus project
  2. 點選Assignment -> Assignment Editor，檢查是否有修改成功。(Transceiver Analog Setting Protocol、VCCA\_GXB Voltage顯示invalid為正常現象，可忽略)

**A**

**完成設定**

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**2021.05.05 v1.0 黃家翰**