# VLSI Signal Processing

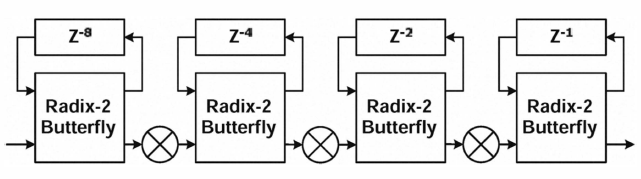
# Homework 1

***Due Tuesday, April 9, 3pm @ (EE2-144)***

**A pipelined 32-point FFT processor**

**Part 1**

In this assignment, you are asked to design and implement a 32-point single-path delay feedback (SDF) FFT processor. A 16-point radix-2 SDF FFT processor is shown below for your reference. Note that, as we mentioned in the class, the butterfly module also needs to play as a cross-switch. You are free to choose the radix format and decimation type (decimation in time (DIT) or decimation in frequency (DIF)). The test patterns will be fed into the FFT processor sequentially in the order of *x*[0], *x*[1], …, *x*[31], and the results need to be properly ordered **within** the processor in order to generate the correct output *X*[0], *X*[1], …, *X*[31].



**Specifications:**

* Input: 12 bits (signed and complex valued)
* Output: 16 bits (signed and complex valued)
* Output SNR ≥ 40 dB (test pattern provided)
* Latency ≤ 68 cycles
* Clock frequency: 100MHz
* Technology: UMC 0.18μm process

The output SNR is evaluated by

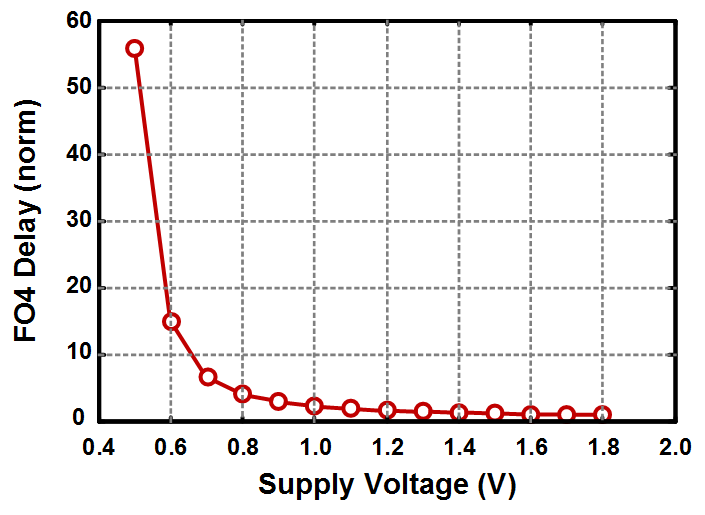
,

where *X*[*k*] is the output of your processor and *X*[*k*]’ is the output from the provided output pattern.

**Part 2**

Assume the delay of logic gates can be modeled by the relation and figure below, where, , and the nominal voltage is 1.8V for the UMC 0.18μm process.

.



Based on your design in Part 1, please explore other FFT implementations operating **at lower supply voltage to achieve the same throughput** by using architectural transformation techniques (such as pipelining and parallelism) that we discussed in class. The power dissipation associated to a new architecture can be estimated by

,

where *C* is proportional to the silicon area.

**Submission:**

* Report (hardcopy, in class):
  + Describe your design strategy. For example, what radix format you choose, how you generate required twiddle factors, and what kind of delay element you choose. If you put any features in the design, detail it. Also, report the output SNR that you achieve.
  + Describe the architectures you explore and the operating conditions (supply voltage, clock frequency) and circuit performance (latency, power, area, power-area product (PAP)).
  + Attach related block diagrams/circuit schematics.
  + Summarize the implement results of ALL your designs. An example is shown below.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | Output SNR  [dB] | VDD  [V] | *f*clk  [MHz] | Latency  [cycle] | Power  [mW] | Area  [μm2] | PAP  [mW∙μm2] |
| Baseline | 48.7 | 1.8 | 100 | 65 | 4.15 | 121544 | 504701 |
| Parallel |  |  |  |  |  |  |  |
| Pipeline |  |  |  |  |  |  |  |

* Upload your report, RTL code, and synthesis script to CEIBA.

**Grading policy:**

* Report (30%)
* Power-area product (the best number among all your designs) (70%)