6 ADCs and DACs for Software-Defined Radio

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6.1 INTRODUCTION

The analog-to-digital converter (ADC) in the receiving (RX) path and the digital-to-analog converter (DAC) in the transmitting (TX) path of a transceiver form a bridge between the analog front end and the digital signal processor (DSP) at the back end. Consequently, they are indispensable in any modern communication system. The shift to multi-mode transceivers increases their importance even further. A software-defined radio (SDR) system should be able to handle any modern communication standard. This should be achieved by reconfiguring the transceiver with software. This means that the settings and performance of the transceiver can be changed without a need for additional hardware. In an SDR system, the ADC and DAC should be fast and accurate enough for each communication standard. Moreover, due to the flexibility requirements of the multi-mode transceiver, the analog front end is often simplified, leading to tougher specifications for the ADC and DAC. As wireless systems are mostly battery operated, the power consumption of the ADC and DAC should be minimized.

Furthermore, technology scaling can result in more difficult specifications for the ADC and DAC. The drive behind technology scaling is the fact that each step makes digital signal processing cheaper and cheaper. However, this is not true for analog signals. Because of noise and mismatch limitations, the area of analog blocks doesn't scale the same as digital. Moreover, the low supply voltages make analog design even more complicated. Therefore, a general trend is to shift as much complexity as possible to the digital domain. For example, filtering in transceiver front ends is shifted as much as possible to the DSP. However, such measures tend to increase the requirements put on the ADC and DAC. For example, the bandwidth of the ADC should be higher to counteract the reduced aliasing suppression due to less

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analog filtering. As a result, optimal design of the ADC and DAC becomes of utmost importance.

In Section 6.2 the requirements for the ADC and DAC in wireless systems are summarized. In Section 6.3 we discuss and compare different options to obtain a multi-mode system. In Section 6.4 we describe briefly the requirements for reconfigurable systems. Sections 6.5 and 6.6 focus on the implementation of reconfigurable ADCs and DACs. Different architectures are evaluated, and methods to make them suitable for multi-mode reception are discussed. Section 6.7 concludes the chapter. The majority of the chapter deals with the implications of the SDR concept on data converters when more-or-less traditional transceiver concepts are used. Some interesting concepts that deviate from the traditional approach are introduced briefly.

6.2 ADC AND DAC REQUIREMENTS IN WIRELESS SYSTEMS

Each communication standard has different requirements for all parts of the transceiver: different carrier frequencies, bandwidths, TX-power and RX-sensitivity requirements, and so on. The derivation of building block specifications from a specified standard is a very complex task that involves a multitude of trade-off decisions, which is outside the scope of this chapter. Table 6.1 summarizes some numbers available in the literature [1–5], to serve as a frame of reference.

Table 6.1 allows us to derive some general specifications of a flexible multi-standard transceiver for current wireless standards. It should support:

- Carrier frequencies from 400 MHz to 5 GHz
- Channel bandwidths up to 40 MHz
- An ADC dynamic range up to 90 dB
- Transmitter power up to 2 W

TABLE 6.1 Overview of Wireless Communication Standards

Standard	Carrier Frequency	Channel Bandwidth	ADC Dynamic Range	Maximum TX Power
GSM	850–1900 MHz	200 kHz	90 dB	2 W
EDGE	850–1900 MHz	200 kHz	87 dB	2 W
GPRS	850–1900 MHz	200 kHz	84 dB	2 W
CDMA2000	450–2100 MHz	1.228 MHz	80 dB	
W-CDMA	1900/2100 MHz	3.84 MHz	60 dB	2 W
Bluetooth	2.4 GHz	1.1 MHz	66 dB	100 mW
IEEE802.11a	5 GHz	20 MHz	55 dB	800 mW
IEEE802.11b	2.4 GHz	5.5 MHz	55 dB	1 W
IEEE802.11n	2.4/5 GHz	20/40 MHz	55 dB	1 W

We use these numbers to evaluate the viability of the multi-standard transceiver architectures discussed, as they provide a sufficiently good frame of reference. If future standards are to be supported, these numbers have to be updated with appropriate estimates.

6.2.1 Evaluating ADC Feasibility

In general, the main specifications for the ADC are the channel bandwidth and dynamic range (DR) required. As indicated before, system-level choices will severely affect the specifications of the ADC: the choice of antialiasing filtering will affect the sampling frequency of the ADC; the DR required depends on many factors, such as variable-gain amplifier (VGA) gain, input sensitivity, and interferer levels.

Evaluating the feasibility of a certain set of specifications is a difficult task since it is dependent on a large number of parameters, such as ADC topology, process technology, design choices, and so on. A rough estimate can be made by using a figure of merit (FOM). For ADCs the following FOM is commonly used:

$$\text{FOM} = \frac{P}{2^{\text{ENOB}} \cdot 2\text{BW}} \qquad \text{fJ/conversion} \tag{6.1}$$

where P is the power consumption, BW the converted bandwidth, and ENOB denotes the effective number of bits achieved over this bandwidth when considering both noise and distortion [i.e., the signal-to-noise-and-distortion ratio (SNDR)]. The dimension of this FOM is energy per conversion, and hence it is a measure of the efficiency of the converter.

Typical values of this FOM for state-of-the art ADC designs are around 1 pF/conversion. The best FOM reported in 2007 was 65 fJ/conversion [6]. When assuming that this FOM value can be achieved at all points in the performance space, it can be used to estimate the ADC power consumption. For example, using (6.1), the power consumption of a converter requiring 72 dB SNDR (i.e., 12 effective bits) over a bandwidth of 5 MHz can be estimated as follows:

$$P = 65 \text{ fJ/conv.} \cdot 2^{12} \cdot 2 \cdot 5 \text{ MHz} = 2.66 \text{ mW} \tag{6.2}$$

When comparing this estimation with real-world designs (e.g., [1,7]) one can see that it is an underestimation of real-world power. Nevertheless, this method is useful to give a generic idea of the feasibility of a certain set of specifications.

6.2.2 Evaluating DAC Feasibility

A very similar story holds for the DAC in the transmitter chain. Again system-level decisions have large impact on the specifications of this building block. The number of channels transmitted and out-of-band emissions will determine the linearity and noise requirements, the type of power amplifier will influence the DAC output power required, and so on.

As for ADCs, a similar FOM-based technique can be used to evaluate the feasibility of a set of DAC specifications. The most commonly used FOM for telecommunication DACs is

$$\text{FOM} = \frac{2^N \cdot \text{BW}}{P} \qquad \text{MHz/mW} \tag{6.3}$$

where P is the power consumption, N the number of bits, and BW the maximum frequency with a spurious free dynamic range (SFDR) larger than $6N - 1$. For DACs the SFDR is used rather than the SNDR since most converters are limited by quantization noise instead of circuit noise, and hence the distortion components are dominant in the SNDR. The best FOM at present is 36,900 MHz/mW, reported in [8]. This value is used in the remainder of the chapter. For most telecommunication standards, a DAC SFDR of approximately 60 dB is sufficient.

6.3 MULTI-STANDARD TRANSCEIVER ARCHITECTURES

In this section we describe a set of tentative multi-standard transceiver architectures. The advantages and disadvantages of each implementation are discussed. A practical multi-standard transceiver can be a combination of more architectures. For example, a transceiver that should be able to cope with two low-bandwidth and one high-bandwidth communication standard can be made using two parallel transceivers, whereby the low-bandwidth transceiver is made reconfigurable.

6.3.1 Parallel Transceivers

One could design a multi-standard transceiver by implementing a separate transceiver for each standard supported, as illustrated in Fig. 6.1. The digital back end has a separate DSP for each transceiver. This is a very power-efficient solution, as only the

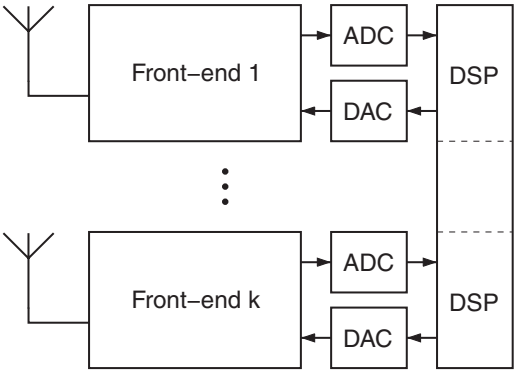


FIGURE 6.1 Parallel transceiver.

parts that are required at a certain time should be activated. Moreover, each transceiver can be optimally designed for its intended communication standard. As front ends for the various standards are readily available, feasibility is not a problem.

The main disadvantage of this approach is cost. Aside from the large engineering cost associated with implementing multiple transceivers, the extra area and external components required increase the manufacturing cost. Second, this solution is not flexible. If support for another standard is desired, a new transceiver has to be added to the system, which can only be achieved by a hardware redesign.

6.3.2 Software Radio

The other extreme is a software radio (SR), illustrated in Fig. 6.2. The ADC and DAC are connected to the antenna with only minimal analog circuitry (e.g., just the transmitting/receiving multiplexer). The idea is to shift all signal processing to the digital domain. The received signal is digitized as soon as possible, while the transmitting path has its digital-to-analog conversion as late as possible. The DSP is responsible for all signal processing, such as filtering, equalization, mixing, and (de)modulation. A first remark is that the DSP in such a system should be extremely powerful and therefore will be power hungry.

The major advantage is that this architecture offers ultimate flexibility. If another communication standard is wanted, the DSP software can be reprogrammed to perform signal processing accordingly. An SR also allows us to process all desired standards at the same time.

The downside is that the requirements for the ADC and DAC in an SR are tremendous. Due to the lack of analog mixing, the bandwidth of both the ADC and DAC is determined by the carrier frequency instead of the channel bandwidth. For the specifications outlined in Section 6.2, this results in a bandwidth requirement of at least 5 GHz. The Nyquist sampling theorem hence dictates a sample rate of at least 10 GS/s. Although this raw sample rate is achievable in modern CMOS technologies, the converter should also maintain a sufficiently high dynamic range over this range. Current state-of-the-art ADCs with bandwidths over 1 GHz are limited to 25 dB DR [9], while high-accuracy converters are limited to about 1 MHz of signal bandwidth [10]. Even if the FOM of [6] is achievable, (6.1) shows that an ADC with 5 GHz of bandwidth and a dynamic range of 100 dB would consume approximately 67 W.

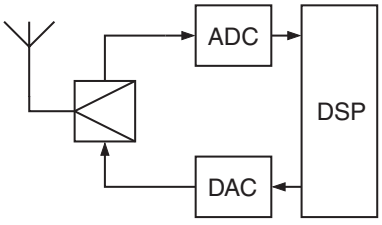


FIGURE 6.2 Software radio transceiver.

Achieving simply the DR required by the most stringent standard (90 dB in Table 6.1) does not suffice for an SR. These requirements were derived such that the system can cope gracefully with the remaining in-band interferers after automatic gain control (AGC) and channel filtering. The lack of AGC in an SR requires that additional DR must be present to cope with varying input power levels. The absence of channel filtering means that the ADC needs extra DR to handle out-of-band interferers.

As an example, consider an SR-based device that is receiving both a GSM and a wireless LAN (WLAN) signal. The device is positioned far from the GSM base station but immediately next to the WLAN base station. It might receive the GSM signal at -80 dBm while the WLAN signal received power is 20 dBm. To receive both signals linearly, another 100 dB of dynamic range is required in addition to the specifications in Table 6.1.

In an SR transmitter the DAC is placed directly at the antenna of the transmitter. Therefore, the DAC should convert the modulated signal directly with sufficient precision, linearity, and speed. This comes down to a sample frequency that is at least twice the highest carrier frequency (5 GHz) (i.e., 10 GS/s). When considering an oversampling ratio (OSR) of 10 to alleviate the reconstruction filter design (see Section 6.6.2), the sample rate required becomes 100 GS/s. The resolution and linearity at each carrier frequency should meet the requirements of the corresponding standard(s).

However, speed and accuracy specifications for the DAC are not the only limiting factors. If the DAC is placed directly at the antenna, it should also provide sufficient power to the antenna. This is a serious issue, especially in low-voltage technologies. High-speed CMOS DACs tend not to output more than 10 dBm, being insufficient to handle all wireless standards in Table 6.1. Any transmitter power control or simultaneous multi-standard conversion increases the DR specification for the DAC to unrealistic levels, very similar to the effect of ADC input power on its DR.

6.3.3 Software-Defined Radio

A single transceiver is used in an SDR. But all parts can be reconfigured by the software, as illustrated in Fig. 6.3. By doing so, multi-standard operation becomes

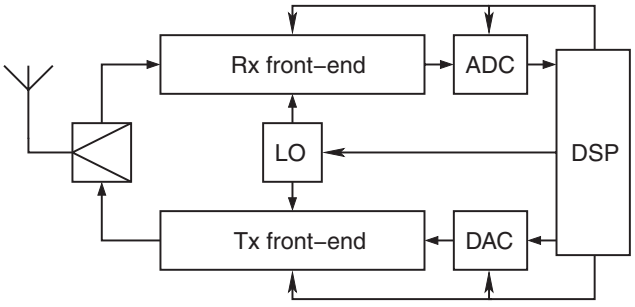


FIGURE 6.3 Software-defined radio transceiver.

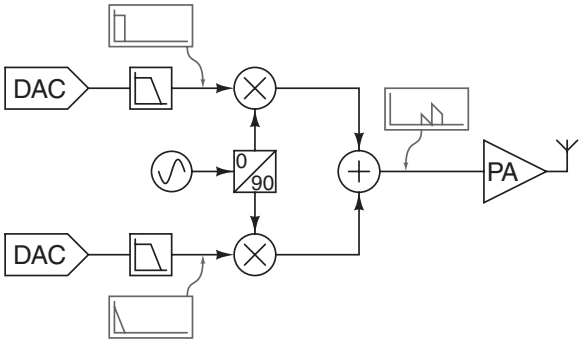


FIGURE 6.4 Direct-conversion transmitter architecture.

possible. This reconfigurability requires new circuit design techniques. A strategy to achieve this is to make the analog front end as simple as possible, shifting the design complexity to the ADC and DAC. However, good system-level design is required to find power-optimized solutions.

The ADC should be designed such that it can meet the specifications for the communication standard with the toughest accuracy requirement and the speed of the standard with the largest channel bandwidth. For each standard, the ADC should then be reconfigured to obtain the specifications required with minimal power consumption. For the transmitting path, a direct conversion (or homodyne) implementation might be preferable over the traditional heterodyne transmitter [11]. In a direct-conversion architecture, the DAC output is directly up-converted by a single mixer stage to the carrier frequency required. This topology is shown in Fig. 6.4.

The filtering requirements of a heterodyne transmitter are very problematic for reconfigurable front ends. The often-used SAW filters are impossible to reconfigure and are hence to be avoided in SDR front ends. A direct-conversion architecture requires fewer filters, making it easier to implement in a reconfigurable manner. Of course, a direct-conversion transmitter also demonstrates some drawbacks [e.g., local oscillator (LO) pulling].

A potential issue of a system such as Fig. 6.3 arises when multiple modes must be received concurrently. In such a case, the ADC should be able to convert the entire band between the two modes, leading to almost the same specifications as the SR concept of Section 6.3.2. For such systems it might be necessary to combine an SDR with a parallel transceiver architecture, leading to a system with a few reconfigurable transceivers.

6.4 EVALUATING RECONFIGURABILITY

As pointed out in Section 6.3.3, reconfigurable hardware is mandatory to obtain an SDR transceiver. However, a method is needed to evaluate the performance of a

TABLE 6.2 Power and Area Overhead for the ADC Part of a Dual-Mode GSM–WLAN Transceiver

Architecture	Power Overhead, GSM Mode	Area Overhead, GSM Mode	Power Overhead, WLAN Mode	Area Overhead, WLAN Mode
Parallel	≈ 0	A_{WLAN}	≈ 0	A_{GSM}
SR	Very large	Small	Very large	Small
SDR, fixed ADC	$\sim \frac{f_{\text{C,WLAN}}}{f_{\text{C,GSM}}}$	$< A_{\text{WLAN}}$	$\sim \frac{\text{DR}_{\text{GSM}}}{\text{DR}_{\text{WLAN}}}$	$< A_{\text{GSM}}$
SDR, reconf. ADC	(Very) small	$< A_{\text{WLAN}}$	(Very) small	$< A_{\text{GSM}}$

certain reconfiguration method. To do so, the reconfigurable building block must be compared with a dedicated solution for each of its operating modes.

Two performance metrics for a reconfiguration method are the power overhead and the area overhead. The *power overhead* is the additional power consumption above that required for a dedicated solution. The *area overhead* is the additional area needed to implement the reconfigurability.

These concepts are illustrated in Table 6.2 for the ADC of four hypothetical implementations of a dual-mode transceiver for GSM and IEEE802.11a. For a parallel architecture, there is no power overhead if the transceiver not in use can be powered off. However, the area overhead is very large: namely, the ADC of the other transceiver. For an SR transceiver, the power overhead is very large, whereas the area overhead will be small. For an SDR transceiver, two cases are considered. In the first, an ADC is made that can cope with the two standards without reconfigurability. As a result, the power overhead for GSM is determined by the required increase in bandwidth, while the power overhead for WLAN is determined by the increase in DR [12]. The total area should be smaller than the area for two separate converters. In the second case, one reconfigurable ADC is used. Now the power overhead will be small for both modes and will depend on the reconfigurability method chosen. The area will be slightly larger than in the previous case, due to the additional circuitry to implement the reconfigurability, but is expected to be less than two separate converters.

6.5 ADCs FOR SOFTWARE-DEFINED RADIO

6.5.1 ADC Topologies

There exist many different topologies to implement an ADC. For each region in the accuracy–speed plane, another topology is optimally suited. This is shown in Fig. 6.5. Very low-speed but high-accuracy ADCs are implemented as integrating types of ADCs. This type of converter requires many clock cycles to convert one sample. Low-accuracy but very fast ADCs, on the other hand, are implemented using a flash architecture. These process one sample each clock cycle.

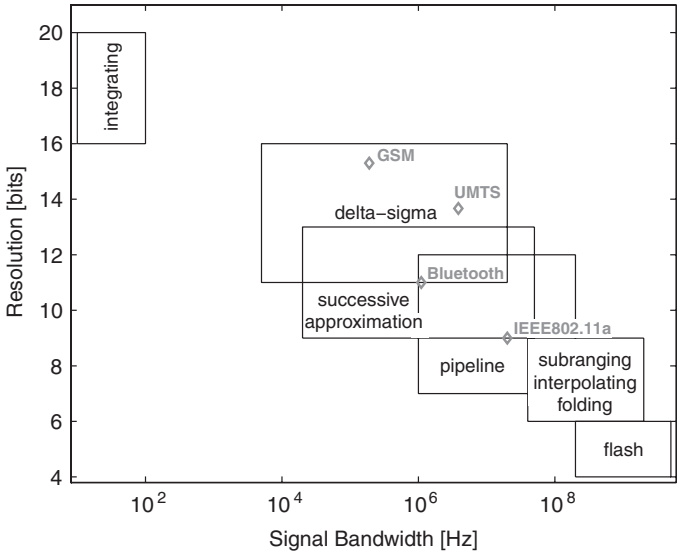


FIGURE 6.5 Operating ranges for various ADC topologies.

Also indicated in Fig. 6.5 are the ADC requirements for various wireless communication standards. An SDR ADC should be able to meet all those standards with minimal power consumption. Three architectures are prime candidates for achieving this: $\Delta\Sigma$, successive approximation, and pipelined ADCs. In the remainder of this section we explain their operating principles and focus on how they can be implemented such that they can be used in a multi-mode receiver.

6.5.2 Delta-Sigma ADCs

6.5.2.1 Operation Delta-sigma ADCs are able to obtain high accuracies while using a low-accuracy (often 1-bit) quantizer. This is achieved with two principles: oversampling and noise shaping. By using a sampling frequency much higher than the Nyquist frequency, the large quantization noise spreads out over a large bandwidth. A sharp digital decimation filter is placed at the output of the converter, to filter out all noise above the signal bandwidth. As a result, only a small portion of the quantization noise remains after the filter. Noise shaping is a process to shape the quantization noise such that most of it falls outside the signal band. As a result, the remaining quantization noise is even lower.

Figure 6.6 shows the architecture of a $\Delta\Sigma$ converter. As the quantization noise has a different path to the output, $H(z)$ can shape the quantization noise without affecting the input signal. If a lowpass function for $H(z)$ with sufficient dc gain is chosen, the quantization noise will be shaped to high frequencies while leaving the signal nearly unaffected in the signal bandwidth. Therefore, $H(z)$ is implemented mostly as a cascade of integrators.

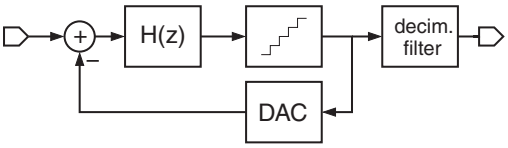


FIGURE 6.6 General delta-sigma architecture.

When assuming that the quantization noise can be modeled as a white noise source, and if the filter is composed of a cascade of n integrators, the resulting signal-to-noise ratio (SNR) can be calculated [equation (6.4)]. B is the number of bits used in the quantizer, and OSR is the oversampling ratio (defined as $f_S/2f_B$, with f_S the sampling frequency and f_B the signal bandwidth):

$$\text{SNR} = \frac{3\pi}{2}\left(2^B - 1\right)^2 (2n+1)\left(\frac{\text{OSR}}{\pi}\right)^{2n+1} \tag{6.4}$$

In reality this performance cannot be achieved. Due to the nonlinearity of the quantizer, scaling coefficients must be introduced for stability of the loop. These will degrade the filter characteristic. Therefore, for higher-order $\Delta\Sigma$ ADCs, cascading is often used. These converters consist of a cascade of low-order filters. The outputs of the quantizer of each filter are then recombined digitally. However, this requires accurate control of the analog filter coefficients to avoid quantization noise leakage, often leading to more stringent filter specifications [13].

As can be seen from (6.4), another possibility for increasing the SNR is to increase the number of bits of the quantizer. The main problem for such multi-bit converters is the fact that the quantized signal must be fed back to the input of the filter. As it is added directly to the input signal there, it doesn't undergo any shaping. As a result, the DAC in the feedback path in Fig. 6.6 needs the same accuracy as does the $\Delta\Sigma$ converter itself. To achieve this, dynamic element matching (DEM) techniques are often used [14].

Also at the system level, $\Delta\Sigma$ ADCs offer a large advantage over other topologies. The oversampling nature of $\Delta\Sigma$ ADCs is beneficial for the filtering in front of it. Because the sampling frequency is higher than the signal bandwidth, less aggressive antialiasing filtering is necessary. This allows easier reconfigurability of this filter [15]. In deep-submicron CMOS, the intrinsic speed of the technology can be used to maintain a high OSR, even for large signal bandwidths [16].

6.5.2.2 Reconfigurability Figure 6.7 shows different methods to make a $\Delta\Sigma$ ADC reconfigurable. In most implementations, some of these methods are combined to enable a broad operating range. There are two methods of changing the signal bandwidth of the converter. The first one is simply to scale the sampling frequency [1,7,17] so that for the same OSR the signal bandwidth changes. This technique is very easy to implement, as it requires no additional circuitry. However, all components of the filter and ADC must be designed to operate correctly at the maximal sampling

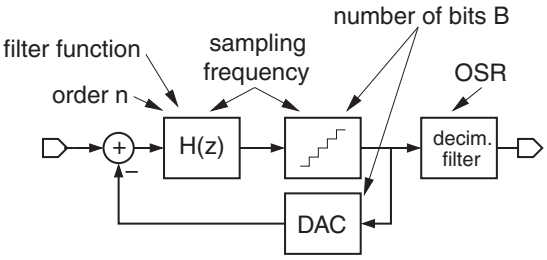


FIGURE 6.7 Reconfigurability options for $\Delta\Sigma$ ADC.

frequency. When such circuits are operating at a lower frequency, they often have a large power overhead.

Second, the OSR can be changed [7,17]. This has no consequences for an analog loop filter. For a decimation filter, this can be achieved by switching off some down-sampling stages, resulting in only a very small circuit overhead. However, as the OSR is lowered, the SNR also decreases. If a broad signal bandwidth range must be covered with the same SNR, a combination with other reconfiguration methods is mandatory.

The SNR can be changed by changing the number of quantizer bits [2]; for example, a multi-bit quantizer can be implemented in parallel with a 1-bit structure. By making sure that the multi-bit quantizer and DAC can be turned off when they are not required, there is no additional power overhead. However, the additional quantizer and more complicated DAC will increase the chip area of the ADC. It is beneficial to combine this method with a variable filter function. A multi-bit topology has fewer stability problems. Therefore, more aggressive noise-shaping functions are possible, leading to a further increase in SNR.

Changing the order of the filter function is also possible. It is easiest to implement in cascade $\Delta\Sigma$ ADCs, where the latter stages can be switched off when their noise-shaping ability is not required [2].

Finally, the transfer function of the filter can be changed [1]. Introducing zeros can lead to a higher SNR [18]. In a reconfigurable ADC, the location of these zeros should be shifted depending on the signal bandwidth wanted [7,17].

To optimize power consumption, the capacitors in the filter should be made scalable. Their ratios determine the filter characteristic and their size determines the thermal noise floor. For a differential implementation, the SNR due to thermal noise can be approximated by [13]

$$\mathrm{SNR}_{\mathrm{thermal}} = \frac{(2 \cdot \mathrm{OL} \cdot V_{\mathrm{REF}})^2}{2} \frac{\mathrm{OSR} \cdot C_S}{4kT} \tag{6.5}$$

The maximal capacitor value is determined by the standard supported, which requires the highest SNR. When converting signals from other standards, the capacitors' size and hence the OTA current required can be decreased [7].

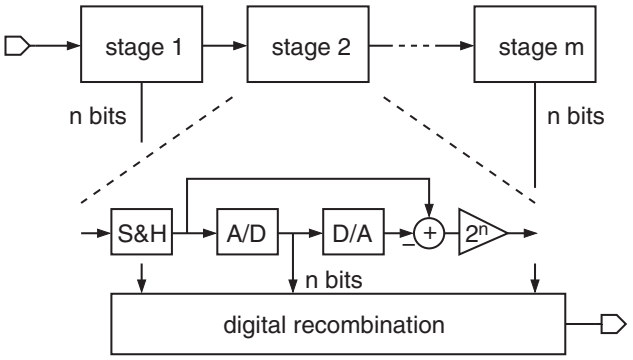


FIGURE 6.8 An m-stage n-bit per stage pipelined ADC.

6.5.3 Pipelined ADCs

6.5.3.1 Operation Figure 6.8 shows the operation of an m-stage, n-bit per stage pipelined converter. In this example, each stage quantizes n bits. It calculates the difference between the input and the quantized signal, amplifies this, and feeds it to the next stage. After m stages, the input is quantized with $m \cdot n$ bits. Quite often, 1.5 bits per stage and a gain of 2 are used. This configuration introduces some redundancy, enabling digital error correction. This reduces the accuracy requirements for the comparators of each stage. To obtain higher accuracies, some form of calibration is necessary. The calibration should compensate for effects such as finite OTA gain and capacitor mismatch, to correct the gain of each stage. As each stage incorporates gain, the input-referred thermal noise of subsequent stages is suppressed. As a consequence, stages farther down the pipe can be scaled down, saving power.

Almost all pipelined ADCs are made using switched capacitor techniques. A switched capacitor pipeline stage alternates between the sampling and amplifying phases. Moreover, each stage is always opposite in phase to the preceding one. As the OTA is used only in the amplifying phase, it can be shared between two stages. For a gain of 2 per stage and taking the stage scaling into account, this OTA sharing technique could lead to a power reduction of 33% compared to a standard pipelined ADC. In a quadrature receiver, even more power savings are possible. If separate ADCs are used for the I and Q paths, the OTA can be shared between the same stage of each of the two pipeline ADCs. As this allows perfect scaling for each stage, a 50% power saving is possible [19].

6.5.3.2 Reconfigurability The resolution of a pipeline ADC can be changed using *stage bypass*. As each stage converts a certain number of bits, switching off some stages decreases the total number of bits converted. This leads to a less accurate but lower-power ADC. As lower accuracies allow a higher thermal noise floor, it is best to bypass the first stages of the pipe, as these are the most power hungry [20].

The resolution can also be varied by using residue feedback. By resending the output of the last stage through some stages, more bits are obtained. However, this

technique will lower the sampling rate, as some stages are now used twice for each output sample. This is also not power optimal. In a standard solution each stage is scaled down, whereas here "oversized" stages are used after the residue feedback. The bandwidth can be changed by scaling the sampling frequency. For optimal power design, the OTA biasing currents should be changed as well.

Another bandwidth-improving technique is interleaving. By alternating between two pipeline ADCs, the bandwidth is doubled. Moreover, as the OTA in each stage of a pipeline ADC is used only in half a clock period, each OTA can be shared between the two converters. As a result, interleaving with two pipeline ADCs results in very little power consumption increase. The area, on the other hand, is almost doubled.

6.5.4 Successive Approximation ADCs

6.5.4.1 Operation The architecture of an n-bit successive approximation ADC is shown in Fig. 6.9. A successive approximation ADC actually implements a binary search algorithm to convert the input signal to a digital value. Starting with the most significant bit (MSB), each clock cycle an additional bit is converted, by comparing the sampled input signal with the value converted so far. As a result, the sample rate equals the clock frequency divided by n.

The advantage of a successive approximation ADC is the small area and simple architecture. Only a comparator is needed. Everything else can be implemented using switches and scaled capacitors [6]. However, because n clock cycles are required to convert to an n-bit word, its maximal signal bandwidth is rather limited.

The comparator needs to be as accurate as the entire ADC, as it must be able to correctly resolve the least significant bit (LSB). Redundancy as with the pipelined converter cannot be introduced here.

The DAC is often implemented as a capacitive DAC, composed of binary-scaled capacitors which are charged either to a reference voltage or to ground. As a result, the accuracy is determined by the capacitor ratios. Therefore, to obtain over about 12-bit accuracy in standard CMOS technologies, some form of trimming or calibration will be required.

6.5.4.2 Reconfigurability The resolution can be changed simply by converting less bits. Consequently, for the same output data rate, the clock frequency can also be lowered. Simply by scaling the clock speed, the bandwidth can be modified. In

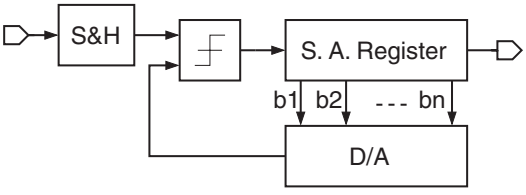
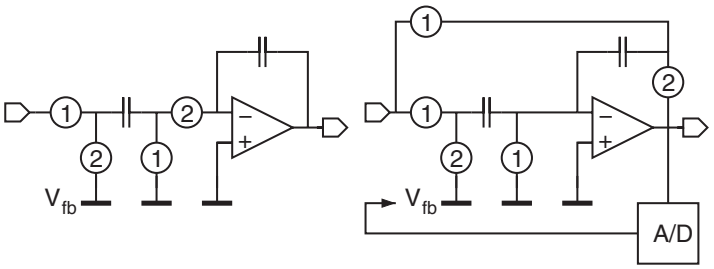


FIGURE 6.9 General n-bit successive approximation architecture.



(a) Switched capacitor integrator (b) Switched capacitor pipeline stage

FIGURE 6.10 Configuration modes for a filter element in a hybrid $\Delta\Sigma$-pipelined ADC.

[6], a SAR which has only dynamic power consumption, is described. As a result, power scales linearly with clock frequency. This is very advantageous when a large range in bandwidth must be covered, as power-efficient operation can be achieved for any frequency. This is achieved by using passive charge sharing. The input is first sampled onto a capacitor. Then a comparator determines the MSB and a precharged capacitor is used to add or remove charge from the value sampled. This is repeated for all bits, with binary-scaled precharged capacitors. This ADC achieves 8 effective bits with signal bandwidths up to 20 MHz.

6.5.5 Hybrid ADCs

It is also possible to combine different types of ADCs. For example, a switched capacitor integrator of a $\Delta\Sigma$ ADC [shown in Fig. 6.10(a)] doesn't differ much from a pipeline stage [shown in Fig. 6.10(b)]. This means that with a few additional switches a switched capacitor $\Delta\Sigma$ ADC could be changed in a pipeline ADC. In [20] this idea is used to implement a hybrid $\Delta\Sigma$-pipelined converter, with an adaptive bandwidth up to 10 MHz and between 6 and 16 effective bits. In $\Delta\Sigma$ mode, the accuracy is changed by changing the OSR and sampling frequency. In pipeline mode, capacitor sizes and pipeline length can be modified using stage bypass. A PLL is used to sense the clock frequency and adapts the bias current of the op-amps automatically.

6.6 DACs FOR SOFTWARE-DEFINED RADIO

Selection of an appropriate DAC for an SDR system is subject to a multitude of considerations. In this section we present the most important system- and implementation-level topics. As indicated in Section 6.2, the selection and design of a DAC for SDR is largely dependent on the topology chosen for the entire transmitter. The various options regarding the frequency planning and intermediate frequencies result in different specifications for the filters used in the transmitter. The specifications of these filters, especially the reconstruction filter, are very important when determining the

specifications of the DAC. Furthermore, all practical DACs introduce some sort of amplitude distortion. This can also be exploited to simplify the system-level design of an SDR.

In this section we provide an overview of the dominant topologies used to implement wide-bandwidth telecommunication DACs, along with some recent CMOS DAC implementations. Their usability in an SDR radio is discussed for standard transmitter architectures. The section ends with the introduction of some interesting ideas that deviate from the standard transmitter concept.

6.6.1 Topologies for High-Speed CMOS DACs

From the multitude of DAC topologies that exist, the current-steering DAC is the most common, if not the only, topology used for CMOS implementations targeting telecommunication applications. Due to its lack of high-impedance nodes experiencing voltage swing and the absence of a closed-loop output stage, it can achieve very high update rates and signal frequencies. This topology is also capable of achieving the required accuracy and linearity (up to 14 bits). Since they require only CMOS transistors and no resistors or capacitors, current-steering DACs can be implemented in a fully digital CMOS technology.

Current-steering DACs use a current as the reference quantity for its output signal. The output is constructed by switching weighted current sources according to the binary input word. Based on the weighting used for switching the current sources, three different implementations can be distinguished:

- Binary weighted
- Unary weighted
- Segmented

In a binary-weighted DAC the switched currents are weighted according to the binary weight of the bit that controls the switch. In a unary-weighted DAC the switched currents are all equal, and the digital input word is converted into thermometer code, which is used to drive the switches. A segmented DAC combines a binary and unary section. The LSBs of the input word are applied directly to a binary-weighted section, while the MSBs are converted to thermometer code and drive a unary-weighted section. The number of MSBs that are converted into thermometer code define the degree of segmentation of the converter.

The main advantage of a binary-weighted DAC is the design simplicity, enabling very high update rates [21]. It also features a low implementation area and a very low power consumption [22]. The disadvantage is the lower spectral purity at high signal frequencies due to MSB switching transients.

A unary-weighted DAC requires a full binary-to-thermometer-code converter. The power and area of such converters scale exponentially with the number of bits. As a result, for high-resolution DACs the power and area consumed by this block is very high. The main advantage of the unary-weighted DAC is the high linearity, even at high signal frequencies [23].

The segmented topology provides a trade-off between the properties of both the binary- and unary-weighted DACs. The less important LSBs of the input word are implemented in a binary-weighted manner. Hence, their implementation is simple and consumes little power. Due to the exponential scaling of power and area used by a thermometer-code converter, reducing its number of bits has a large impact on the performance of the complete converter. On the other hand, the binary LSBs limit the linearity of the complete converter. Hence, a trade-off between linearity and area/power consumption is established [23].

6.6.1.1 Performance Limits of Current-Steering D/A Converters

Update Rate Limits The first fundamental limit on a current-steering DACs performance is the maximal clock frequency for correct operation of the digital section in the converter. According to the Nyquist theorem, the maximal output signal bandwidth is equal to half of the update rate. Hence, the maximal update rate presents an upper bound on the output signal frequency.

Signal-to-Noise Ratio In most DACs the quantization noise is the major noise limit. The SNR of a quantized digital signal is approximately equal to

$$\mathrm{SNR}_q \approx 6.02N \tag{6.6}$$

For a quantized signal with quantization step Δ, the integrated quantization noise power is

$$P_e = \frac{\Delta^2}{12} \tag{6.7}$$

For signals that are sufficiently active (such as telecommunication signals), the quantization noise can be seen as white noise, distributed between 0 and f_s. This means that the spectral density of the noise can be calculated as

$$S_n(f) = \sqrt{\frac{\Delta^2}{12}\frac{1}{f_s}} \tag{6.8}$$

This result shows that by increasing the sampling frequency, the noise spectral density is decreased. The in-band quantization noise power, assuming a brick-wall reconstruction filter with bandwidth BW, can then be calculated as

$$P_{\mathrm{noise}} = \int_{-\mathrm{BW}}^{\mathrm{BW}} S_n^2(f) = 2\mathrm{BW}\frac{\Delta^2}{12}\frac{1}{f_s} = \frac{P_e}{\mathrm{OSR}} \tag{6.9}$$

Therefore, we can see that the in-band noise power improves:

$$\frac{P_{\mathrm{noise}}}{P_e} = \frac{1}{\mathrm{OSR}} \tag{6.10}$$

Improving the signal-to-noise ratio at (6.6) into

$$\begin{aligned} \mathrm{SNR}_{q,\text{in-band}} &= 10\log\frac{P_{\text{signal}}}{P_{\text{noise}}} = 10\log\left(\frac{P_{\text{signal}}}{P_e}\cdot \mathrm{OSR}\right) \\ &= \mathrm{SNR}_q + 10\log(\mathrm{OSR}) \end{aligned} \tag{6.11}$$

Hence, oversampling with a factor of 4 improves the SNR with the equivalent of 1 bit. This allows for systems to synthesize small-band signals with very high-speed, low-resolution DACs and still have sufficient SNR. In reality the reconstruction filter is not a brick-wall filter, resulting in a diminished effect of the OSR on the converter noise. For non-first-order filters, the error made can be neglected.

An extension of the simple oversampling presented in the preceding paragraph is the addition of noise shaping as introduced in Section 6.5.2.1. This results in a higher SNR in the signal band. However, it moves significant amounts of energy out-of-band and this has to be filtered out, placing extra constraints on the reconstruction filter.

Static Accuracy and Linearity Limits Besides the inherently limited accuracy of the digital source signal, the DAC can limit the accuracy even more due to nonlinear conversion. Mismatch-induced errors are a first cause of nonlinear conversion. Since the actual currents provided by the unit current cells deviate from the nominal unit current value, the analog output value deviates from the nominal output value, resulting in a nonlinear overall static transfer function for the DAC. This phenomenon is frequency independent and hence provides a frequency-independent upper bound on the achievable linearity of the converter. At higher frequencies, however, this is not the dominant cause of nonlinearity.

Dynamic Accuracy and Linearity Limits At high output signal frequencies, additional effects start limiting the linearity of the conversion. The most important effects, commonly recognized as the output-frequency limiting factor, are related to the limited isolation of the current cell internal nodes from the output signal. The output current is usually converted to a voltage (e.g., by a resistor) in order to perform further signal processing. Even if the output current is not explicitly converted to a voltage, there is still some implicit current-to-voltage conversion at the output of the converter, due to the nonzero input impedance of the next processing stage.

However, the output impedance of the converter is not constant. It consists of the parallel network of the impedances of all current cells that are switched on. Therefore, the output impedance itself is signal dependent. The current flowing through this signal-dependent output impedance as a result of the voltage at the output is added to the intentional signal current and introduces higher-order harmonics. The relation between the noninfinite converter output impedance, the nonzero load impedance, and the output signal linearity is well studied [8,24,25].

Since a current-steering DAC is a mixed-signal system, more effects causing unwanted signal-dependent current and distortion are present (e.g., switching of

the switch source node capacitance [26] and timing issues [27]). Most of them are proportional to the output signal frequency.

It is important to note that the majority of the dynamic nonlinearities are independent of the update rate. This means that a converter should be designed for the worst-case linearity–bandwidth requirement. It also means that increasing the update rate of a converter doesn't necessarily degrade its linearity, a property that can be exploited to simplify reconstruction filter design.

6.6.1.2 Reconfigurability of Current-Steering D/A Converters Due to their mostly digital nature, the reconfiguration of current-steering DACs is fairly straightforward. If the converter is designed for the most stringent linearity specification that the system should be able to handle, it can easily be reconfigured to operate in the most favorable point of the performance–power trade-off curve.

Signal-to-Noise Ratio and Signal Bandwidth As shown in Section 6.6.1.1, the SNR of a given DAC core can be traded for bandwidth by changing the OSR and/or the use of noise shaping. Since bandwidth is assumed to be determined by the standard, changing the oversampling rate requires a flexible clock frequency. For this, a resampling/interpolation block might be required to convert between the DSP data rate and the DAC sample rate. These operations are digital and hence well suited for the SDR concept.

Output Power To facilitate power control in the transmitter, flexible control over the output swing of the converter is desirable. In current-steering DACs, this can be achieved by modifying the reference current used to derive the cell current. Although the output current has some influence on the linearity, the control range can still be fairly large ([23] reports one octave). Another option is to incorporate an active output stage [28] with reconfigurable gain.

Power Consumption The power consumption of a current-steering DAC can be split into four parts: clock, digital, analog, and output power. A large part of the total converter power is due to clock distribution. The digital power is consumed mainly by the thermometer-code converter (if present). The clock and digital power follow the trends in digital power scaling. Hence, they are linearly dependent on the clock speed if the supply voltage is not scaled. If the supply voltage is scaled, the digital power exhibits a cubic dependency. This means that the update rate has a significant influence on the power consumption of the converter.

Since most of the analog section consists of "pseudodigital" circuits (switch drivers and resynchronization latches), it also follows the digital power-scaling rules. However, headroom requirements in the analog circuits prevent down-scaling of the supply voltage. Consequently, the analog power scales linearly with the clock frequency.

The signal frequency influences the power consumption of the digital and analog sections. Higher signal frequencies result in higher switching activity, hence higher power consumption. The output current is also a significant contributor to the total

output power, especially in converters with low segmentation [29]. It is independent of clock and signal frequency.

6.6.2 Dealing with Nyquist Images

Digital signal processing theory teaches that the spectrum of a sampled signal equals an infinite replication of the spectrum of the base signal. When a digital signal is converted into the analog domain, this property remains intact. These replicas are highly unwanted since they result in out-of-band signals, possibly violating the emission masks. Therefore, systems using a DAC have to incorporate some means of dealing with these images. This can have a significant impact on the reconfigurability of the transmitter.

The most straightforward method of suppressing images is to filter them out using an analog lowpass filter. When using a brick-wall lowpass filter with a cutoff frequency at $f_s/2$, the image is completely removed from the output spectrum. Implementing brick-wall (infinite-order) filters is not possible, however, and even high-order analog filters are far from trivial to design. Therefore, real-world applications are limited to lower-order (typically, around four) filters.

The transfer function of an Nth-order lowpass filter with cutoff frequency f_p can be approximated as

$$H(f) = \frac{1}{[1 + j(f/f_p)]^N} \tag{6.12}$$

For signals that are well above the cutoff frequency of the filter, we can thus write the amplitude transfer as

$$|H(f)| \approx \left(\frac{f_p}{f}\right)^N \tag{6.13}$$

Should the system require a bandwidth BW with an out-of-band suppression S and we use a reconstruction filter that has its cutoff frequency at $f_p = \mathrm{BW}$, we can determine the following relation between the sample frequency f_s of the converter and the filter order N:

$$S_{\mathrm{dB}} = N \cdot 20 \log\left(\frac{f_s}{\mathrm{BW}} - 1\right) \tag{6.14}$$

If we define the oversampling ratio of the DAC as the ratio between the actual sampling frequency and the minimal sampling frequency to fulfill the Nyquist criterion,

$$\mathrm{OSR} = \frac{f_s}{2f_{\mathrm{Nyquist}}} = \frac{f_s}{2\mathrm{BW}} \tag{6.15}$$

we can rewrite the Nyquist image attenuation (NIA) as

$$\mathrm{NIA}_{\mathrm{filter}} = (2\mathrm{OSR} - 1)^N \tag{6.16}$$

This equation indicates the trade-off between the required filter order and the DAC sampling frequency. In case of minimal sampling frequency (OSR $\approx$ 1), the filter order approaches infinity, corresponding to a brick-wall filter. For a system that requires a NIA larger than 60 dB we can calculate that when using an OSR equal to 10, a third-order reconstruction filter is required. As mentioned before, a filter order higher than 4 is difficult and/or expensive to implement.

Another conclusion that can be drawn from the equations above is that when changing the signal bandwidth or DAC update rate, the reconstruction filter should be changed accordingly. This means that the degree of reconfigurability of a DAC is not only a function of its own reconfigurability but also of its associated reconstruction filter.

6.6.3 Pulse-Shape-Induced Amplitude Distortion

Besides the image components introduced by sampling, a DAC also introduces amplitude distortion. This due to the fact that a DAC uses real-world pulses instead of the mathematical Dirac impulse trains used in sampling theory. The pulse shape used by the DAC determines the properties of the distortion. The resulting distortion can introduce a significant error. To compensate for this effect, the digital signal is often predistorted, especially for low oversampling rates. On the other hand, this amplitude distortion can be exploited to lower the amplitude of the Nyquist images.

6.6.3.1 Zeroth-Order-Hold DAC The zeroth-order-hold DAC is the most common type of DAC. Each output value is held for one clock period, resulting in a square pulse shape. The distortion introduced by this pulse shape is characterized by the following equation:

$$|H(f)| = \frac{\sin[\pi(f/f_s)]}{\pi(f/f_s)} = \operatorname{sinc}\frac{f}{f_s} \tag{6.17}$$

The sinc distortion can be used to implement some form of reconstruction filtering. It has an inherent lowpass characteristic, having $|H(nf_s)| = 0$ for integer values of n. If sufficient oversampling is used, the sinc shaping can provide a significant filtering of the Nyquist images: for a signal located between dc and BW, the Nyquist image is located between $f_s - \text{BW}$ and f_s. Therefore, the amplitude of the highest image component (i.e., the one at $f_s - \text{BW}$) is

$$|H(f)| = \operatorname{sinc}\frac{f_s - \text{BW}}{f_s} = \operatorname{sinc}\left(1 - \frac{1}{2\text{OSR}}\right) \tag{6.18}$$

For example, for an oversampling ratio of 10, the attenuation of the Nyquist images by the sinc response is approximately 26 dB. This effect is solely dependent on the OSR and is independent of blocks external to the DAC. Therefore, it is an interesting property for reconfigurable systems.

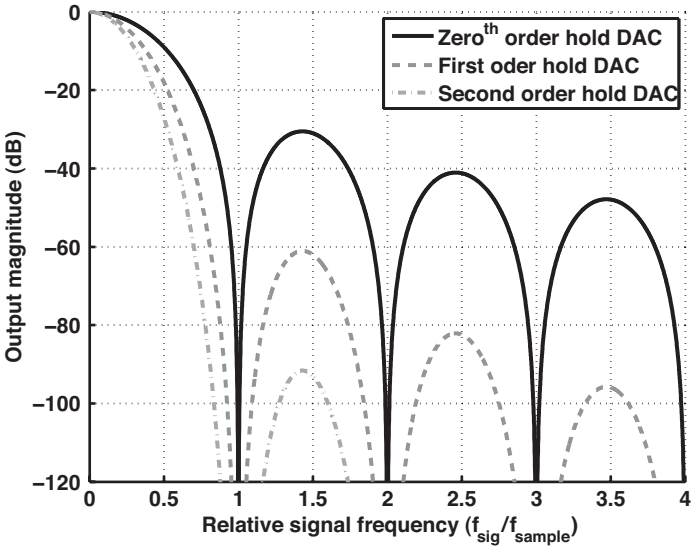


FIGURE 6.11 Amplitude distortion for higher-order-hold D/A converters.

6.6.3.2 Higher-Order-Hold Converters In a higher-order-hold converter the analog output is interpolated between two or more sampled values. The amplitude shaping of a *K*th-order hold converter can be described as

$$|H(f)| = \text{sinc}\left(\frac{f}{f_s}\right)^{K+1} \tag{6.19}$$

The main property of these higher-order-hold converters is that they have a higher Nyquist image attenuation. The amplitude distortion for first- and second-order-hold DACs is plotted in Fig. 6.11. In certain cases this effect, combined with some oversampling, can be sufficient to deal with the Nyquist images. The Nyquist image attenuation due to the *K*th-order-hold effect can be calculated as

$$\text{NIA}_K = \text{sinc}\left(1 - \frac{1}{2\text{OSR}}\right)^{K+1} \tag{6.20}$$

However, implementation of such higher-order-hold converters is not trivial, resulting in approximations such as *L*-fold linear interpolation [30].

6.6.4 CMOS DAC Implementations for Wideband Communication

Over the last decade, several high-performance CMOS DACs have been described in the open literature. In this section we highlight some of these to provide an overview of the current state-of-the-art. A first-order assessment is made whether these converters

can be used to achieve 10-bit performance (60 dB SFDR) over a 0- to 50-MHz signal bandwidth. The filter order needed to suppress the Nyquist images is also estimated.

A 10-Bit 500-MS/s DAC in 0.35-μm CMOS One of the first wideband high-resolution CMOS DACs was presented in [23]. It was implemented in a 0.35-μm CMOS technology and consumes 125 mW at 500 MS/s. The converter achieves approximately 60 dB linearity over a 50-MHz signal bandwidth when running at 400 MS/s. For higher update rates, the linearity drops below 60 dB; hence the OSR is restricted to 4. The zeroth-order-hold output waveform results in approximately 17 dB of NIA. The remaining 43-dB suppression needed to ensure that the first Nyquist image lies below the 60-dB specification mandates the use of a third-order reconstruction filter. An OSR of 4 results in an extra 6 dB of signal-to-quantization-noise ratio (SNRQ) (i.e., 1 bit).

A 10-Bit 1-GS/s DAC in 0.35-μm CMOS Another benchmark high-speed, high-resolution CMOS DAC was presented in [31]. This design was also manufactured in a 0.35-μm CMOS technology and consumes 110 mW at 1 GS/s. It achieves a 60-dB linearity over its complete first Nyquist zone (500 MHz). The oversampling ratio when using this converter would be 10, resulting in 26 dB of NIA due to pulse-shape distortion. A second-order filter would ensure sufficient aggregate NIA. The OSR of 10 lowers the in-band quantization noise with 10 dB.

A 10-Bit 250-MS/s DAC in 0.18-μm CMOS The design presented in [22] and [29] shows that binary converters are also able to convert large signal bandwidths. The converter was designed in a 0.18-μm CMOS technology and achieves 60 dB of linearity over its complete Nyquist range when running at 250 MS/s. It consumes 40 mW. To achieve the specifications derived in Section 6.2.2, a fourth-order filter would be required. As the OSR is only 2.5, the NIA due to pulse-shape distortion is 12 dB, leaving the remaining 48 dB to be achieved by means of the reconstruction filter.

A 6-Bit 4.5-GS/s DAC in 0.13-μm CMOS The converter presented in [21] demonstrates a 6-bit DAC implemented in a 130-nm CMOS technology that operates up to 4.5 GS/s. It consumes 30 mW from a 1.2-V supply. The very high update rate and low power consumption are due largely to its fully binary architecture. For signal frequencies up to 50 MHz at an update rate of 3 GS/s, it achieves a linearity of approximately 50 dB. This means that it is unable to meet the linearity specifications. However, to illustrate the concept of highly oversampled DACs, the calculations are included. Due to the very high update rate, an OSR of 30 is possible, resulting in an extra 2.5 bits of quantization noise performance. This means that the 6-bit converter achieves approximately 8-bit quantization noise performance, due to its very high OSR. A first-order filter combined with the sinc distortion suffices to suppress the Nyquist images at these oversampling rates.

A 68-dB SFDR 100-MHz Bandwidth ΔΣ-DAC in 0.13-μm CMOS The DAC introduced in [8] combines the very high update rate with noise shaping to improve baseband SNR. The converter described uses a 5-bit core combined with a third-order digital ΔΣ modulator to achieve an in-band SNDR of 68 dB over a bandwidth of 100 MHz. It consumes only 11 mW, resulting in a peak FOM of 36,900 MHz/mW. The 10-fold oversampling, combined with the third-order noise shaping, results in 12 effective bits in the 50-MHz band. The high core sample rate ensures that the Nyquist images can still be filtered using a first-order filter. The noise-shaping operation will, however, result in significant out-of-band noise power that has to be filtered. This should be accounted for when determining the order of the reconstruction filter.

A 1.5-V 13-Bit 130-300-MS/s DAC in 0.13-μm CMOS In [28] a dynamically calibrated converter with an active output stage is presented. It is designed in 0.13-μm CMOS technology and achieves 68 dB of linearity over a 50-MHz bandwidth while running at 300 MHz. This means that it exceeds the linearity specification set in Section 6.2.2. Since the OSR is only 3, the converter requires a fourth-order reconstruction filter to remove the Nyquist images.

6.6.5 Advanced Techniques and Implementations

Recently, some new architectures and techniques have been proposed to ease the implementation and integration of transmitters. A lot of them are interesting from an SDR perspective, and some are discussed in the following section.

6.6.5.1 Digital IF Multi-Step Architecture An architecture greatly simplifying the front end is the digital-IF architecture, shown in Fig. 6.12. This architecture tries to combine the advantages of a direct conversion and a multi-step architecture. The signal is first up-mixed digitally, resulting in a real signal that corresponds to the quadrature-modulated IF signal in a multi-step transmitter. Then it is converted using a high-speed DAC, followed by a single-sideband up-mixer.

The digital up-mixing causes the modulated signal to be centered around an ac carrier (as opposed to around dc for the direct-conversion transmitter). This allows the subsequent stage to be ac coupled, preventing LO leakage caused by dc offsets. The digital-IF technique hardens the requirements of the DAC, since its output signal

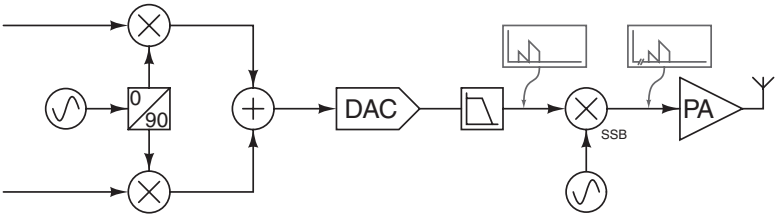


FIGURE 6.12 Digital-IF architecture.

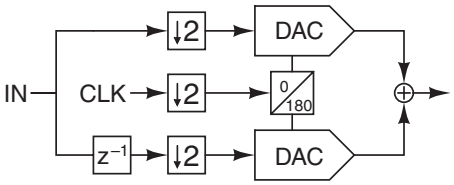


FIGURE 6.13 Two converters clocked with complementary clocks. The two output currents are summed by tying them to the same node. The inputs are constructed such that the first set of Nyquist images is suppressed.

frequency is higher. More important, it increases the demands on the reconstruction filter, since the oversampling ratio is smaller. The filter alternatives presented in Section 6.6.5.2 can be used to cope with this. Another approach is to use a higher-order hold converter and careful frequency planning to exploit the amplitude distortion [32].

6.6.5.2 Parallel-Path Converter Following Nyquist's theorem, for a bandlimited waveform with bandwidth BW, at least $2 \cdot \mathrm{BW}$ samples per second must be provided to the converter. It is possible to use multiple converters with a lower sample rate to obtain a combined sample rate $2 \cdot \mathrm{BW}$ for the system. This can be achieved by time-interleaving the output of multiple DACs [28]. However, this requires additional analog circuitry, increasing area and power consumption.

Another option is to sum the outputs of multiple DACs together, as indicated in Fig. 6.13 for two converters. This configuration was introduced in [33]. It enables the suppression of half of the Nyquist images when the appropriate inputs are applied. Although not fully equivalent to a double-speed DAC, the parallel-path DAC is functionally equivalent for practical oversampling ratios.

A remark should be made regarding the amplitude distortion of the parallel-path converters. Since their output is the linear combination of N separate DACs each running at f_s/N, the amplitude distortion exhibits the frequency response equal to that of one DAC running at f_s/N. Figure 6.14 shows the amplitude distortion of a parallel-path DAC compared to a traditional DAC running at the same update rate.

6.6.5.3 RF-DAC and Direct-to-RF Modulators A recent trend in telecommunication DAC design is to combine the D/A function together with an up-mixing function in order to obtain a converted spectrum around a RF carrier. A first method to achieve this is to exploit the high-frequency Nyquist images that are present in the converted spectrum. The most straightforward method is to filter these images out using a bandpass filter at RF, as shown in Fig. 6.15(a). The main disadvantage of this technique is the reduced output power of the image due to the sinc amplitude distortion. This can be alleviated by using current sources that are switched at the target RF frequency as shown in Fig. 6.15(b) [34]. This boosts the amplitude of the Nyquist image significantly at the current cell switching frequency.

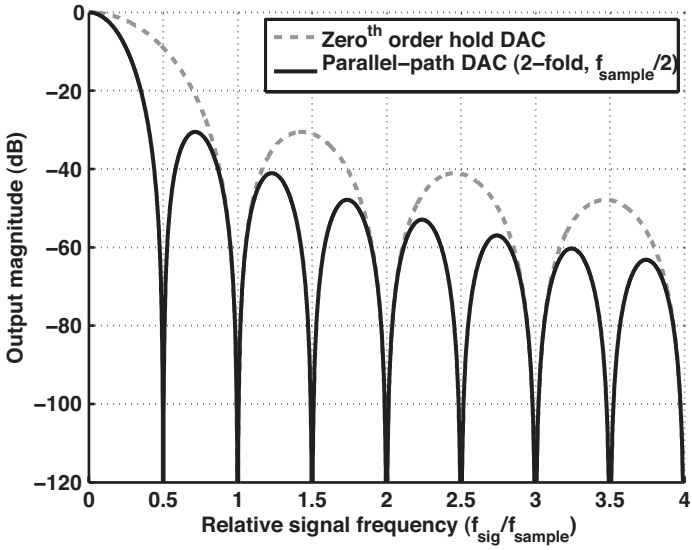
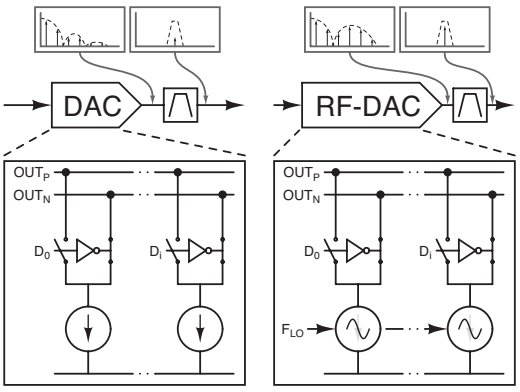


FIGURE 6.14 Amplitude distortion for parallel-path D/A converters.

A further development of this was presented in [35]. Instead of switching the current source on and off, the entire cell is replaced by a Gilbert mixer, as shown in Fig. 6.16. The carrier frequency desired is applied to the RF port, and the digital control signal to the LO port. By using a large degree of oversampling, the need for an intermediate lowpass filter or a reconstruction bandpass filter is avoided.

An interesting side effect of using a pulse shape having zero value at the digital switching time instant is that it improves the general linearity performance of the



(a) Direct use (b) RF boosting

FIGURE 6.15 Use of higher-order Nyquist images by bandpass-filtering the DAC output.

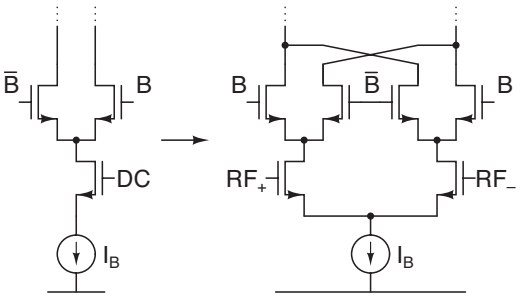


FIGURE 6.16 Transformation to a Gilbert-style mixing cell.

converter. It lowers the sensitivity to clock jitter and reduces intersymbol interference. In RF-DACs this is achieved by ensuring that the RF frequency is an integer multiple of the converter clock rate.

6.7 CONCLUSIONS

In this chapter we discussed ADC and DAC requirements for multi-standard transceivers. Three categories of multi-standard transceivers (parallel, SR, and SDR) can be distinguished, although combinations are possible. By applying widely used definitions of FOMs, it is shown that a full SR system is impossible to build and would consume an enormous amount of power. Instead, it is wiser to make the transceiver reconfigurable (or "software defined").

The basic operating principles of three different ADC architectures ($\Delta\Sigma$, pipelined, and successive approximation), which are typically used in receivers, are explained. For each architecture, numerous options to make them reconfigurable are discussed and evaluated. Recent state-of-the-art publications prove that reconfiguration in accuracy and speed is possible, without much power overhead.

Implementations for the DAC are covered, together with different methods to filter out the Nyquist images in the output spectrum. The possibility of reconfiguration of these methods is addressed. This is elaborated further with a comparison of six state-of-the-art DACs. Finally, some advanced techniques particularly suited for reconfigurable systems are discussed briefly.

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