```
1   `timescale 1ns / 1ps
2   /**********************************************************************************
3    *
4    * Author:   Jesus Luciano & Rosswell Tiongco
5    * Filename: MIPS_CPU.v
6    * Date:     3/21/2019
7    * Version:  1.0
8    *
9    * Notes:1.0 Module Instantiates Control Unit, Instruction Unit, Datapath, and
10   *           Data Memory
11
12   *       1.1 Modified for final implmentation. Removed data memory, added signal
13   *           as outputs for data memory and io memory
14   *
15   **********************************************************************************/
16  module MIPS_CPU(clk, reset, intr, inta, dm_cs, dm_wr, dm_rd, dm_address,
17                  dm_d_in, dm_out, io_rd, io_wr, io_out, io_cs);
18      //inputs
19      input      clk, reset, intr;
20
21      //IDP wires and outputs
22      wire        c, n, z, v, HILO_ld, D_En, stack;
23      wire [ 1:0] DA_Sel;
24      wire [ 2:0] Y_Sel, T_Sel;
25      wire [ 4:0] FS, S_Addr, T_Addr, D_Addr, shamt, flags_in, flags_out;
26
27      //IU wires
28      wire        im_cs, im_wr, im_rd, pc_ld, pc_inc, ir_ld;
29      wire [ 1:0] pc_sel;
30      wire [31:0] IR_out, PC_out, SE_16;
31
32      //Data Memory wires
33      output wire        dm_cs, dm_wr, dm_rd;
34      output wire [31:0] dm_d_in, dm_address;
35
36      input [31:0] dm_out;
37
38      //Control Unit outputs
39      output       inta;
40
41      //IO memory/intrrupt inputs/outputs
42      input [31:0] io_out;
43      output wire  io_rd, io_wr, io_cs;
44
45      //Module Instantiations
46      MCU Control_Unit(.sys_clk(clk), .reset(reset), .intr(intr), .c(c), .n(n),
47      .z(z), .v(v), .IR(IR_out), .int_ack(inta), .pc_sel(pc_sel), .pc_ld(pc_ld),
48      .pc_inc(pc_inc), .ir_ld(ir_ld), .im_cs(im_cs), .im_rd(im_rd), .im_wr(im_wr),
49      .D_En(D_En), .DA_sel(DA_Sel), .T_sel(T_Sel), .HILO_ld(HILO_ld),
50      .Y_sel(Y_Sel), .dm_cs(dm_cs), .dm_rd(dm_rd), .dm_wr(dm_wr), .FS(FS),
51      .S_Addr(S_Addr), .T_Addr(T_Addr), .D_Addr(D_Addr), .shamt(shamt),
52      .io_rd(io_rd), .io_wr(io_wr), .io_cs(io_cs), .stack(stack),
53      .flags_out(flags_out), .flags_in(flags_in) );
54
55      IU Instruction_Unit(.clk(clk), .reset(reset), .im_cs(im_cs),
56      .im_wr(im_wr), .im_rd(im_rd), .pc_ld(pc_ld), .pc_inc(pc_inc),
57      .ir_ld(ir_ld), .PC_in(dm_address), .PC_out(PC_out), .IR_out(IR_out),
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58        .SE_16(SE_16), .pc_sel(pc_sel) );
59
60        IDP Datapath(.clk(clk), .reset(reset), .S_Addr(S_Addr), .FS(FS),
61        .HILO_ld(HILO_ld), .D_En(D_En), .D_Addr(D_Addr), .T_Addr(T_Addr), .DT(SE_16),
62        .T_Sel(T_Sel), .C(c), .V(v), .N(n), .Z(z), .DY(dm_out), .PC_in(PC_out),
63        .Y_Sel(Y_Sel), .ALU_OUT(dm_address), .D_OUT(dm_d_in), .DA_Sel(DA_Sel),
64        .shamt(shamt), .io_rd(io_rd), .io_out(io_out), .stack(stack),
65        .flags_in(flags_out), .flags_out(flags_in) );
66
67    endmodule
68
```