```
1   `timescale 1ns / 1ps
2   /**********************************************************************************
3    *
4    * Author:   Jesus Luciano
5    * Filename: reg32.v
6    * Date:     2/14/2019
7    * Version:  1.0
8    *
9    * Notes:    Structural implementation of a 32-bit register
10   *           Output Q changes only on the rising edge of a clock and if the
11   *           load input is asserted, otherwise it stays the same
12   *
13   **********************************************************************************/
14  module reg32(clk, reset, ld, D, Q);
15      input             clk, reset, ld;
16      input      [31:0] D;
17
18      output reg [31:0] Q;
19
20      always @(posedge clk, posedge reset)
21          if(reset)
22              Q <= 32'h0;
23          else
24              //output changes only is ld is asserted
25              if(ld)
26                  Q <= D;
27              else
28                  Q <= Q;
29
30  endmodule
31
```