```
1   `timescale 1ns / 1ps
2   /**********************************************************************************
3    *
4    * Author:   Jesus Luciano & Rosswell Tiongco
5    * Filename: Memory.v
6    * Date:     2/25/2019
7    * Version:  1.0
8    *
9    * Notes:    4096x8 Byte Addressable Memory
10   *
11   **********************************************************************************/
12  module Memory(clk, cs, wr, rd, Address, D_In, D_Out);
13
14      input         clk, cs, wr, rd;
15      input  [31:0] Address, D_In;
16
17      output [31:0] D_Out;
18
19      reg     [7:0] M [4095:0]; //4096x8 Memory
20
21      wire [11:0] mem_addr;
22      //use only 12 least significant bits of input
23      assign mem_addr = Address[11:0];
24
25      //synchronous write
26      always @ (posedge clk)
27          //chip select and write must be asserted in order for memory to
28          //be written to
29          if(cs & wr)
30                      {M[mem_addr], M[mem_addr+1],
31           M[mem_addr+2], M[mem_addr+3]} <= D_In;
32
33
34      //asynchronous read
35      //chip select and read must be asserted in order to read contents of memory
36      //4 bytes are read simultaneously
37      assign D_Out = (cs & rd) ?
38                      {M[mem_addr  ], M[mem_addr+1],
39                       M[mem_addr+2], M[mem_addr+3]} : 32'hz;
40
41
42  endmodule
```