```
1   `timescale 1ns / 1ps
2   /**********************************************************************************
3    *
4    * Author:   Jesus Luciano
5    * Filename: reg32.v
6    * Date:     3/5/2019
7    * Version:  1.0
8    *
9    * Notes:    Structural implementation of a 32-bit register with an increment
10   *           and load signal. Output Q increases by 4 only when the inc signal
11   *           is asserted. Out Q changes to the input of D only when the load
12   *           signal is asserted. All other combinations of inputs results in
13   *           Q staying the same.
14   *
15   **********************************************************************************/
16  module reg32_inc(clk, reset, ld, inc, D, Q);
17      input             clk, reset, ld, inc;
18      input      [31:0] D;
19
20      output reg [31:0] Q;
21
22      always @(posedge clk, posedge reset)
23          if(reset)
24              Q <= 32'h0;
25          else
26              case({ld, inc})//output only changes based on ld and inc inputs
27                  2'b0_1 : Q <= Q + 4;//inc
28                  2'b1_0 : Q <= D;    //load
29                  default: Q <= Q;
30              endcase
31
32  endmodule
33
```