# Identifying Reliability High-Correlated Gates of Logic Circuits With Pearson Correlation Coefficient

Zhanhui Shi, Jie Xiao, *Member, IEEE*, Jianhui Jiang, Ying Zhang, *Member, IEEE*, and Yuhao Zhou

***Abstract*—Identifying reliability high-correlated gates (HRCGs) is vital for fault location and exclusion, especially for cascading faults. By executing a linear fit based on the results of the circuit's reliability evaluation and calibrating the fit function using regression residual analysis, this brief first proves the existence of HRCGs. A time-series-oriented PCC model is then introduced to quantify gates' reliability correlation (GRC) and identify all the HRCGs in the circuit. Circuit-correlated primary outputs and sequential circuit-correlated flip-flops were further identified based on this approach. Experimental results on benchmark circuits show that the average accuracy of this approach is 0.9972 with the Monte Carlo (MC) method, and it is 2591 times faster than the MC method. On larger circuits, the identification rate and stability are 6.07 times and 13.55 times greater than the reference method and rand method, respectively.**

***Index Terms*—Pearson correlation coefficient, high-correlated gates, gates' reliability correlation, correlated gates.**

## I. Introduction

NANOCIRCUIT integration is constantly developing with the use of new materials and scaling technologies, while the reliability of circuits will unavoidably decrease due to extreme oscillations in static and dynamic parameters.

Reliability analysis provides improvement measures and the effects of improvements on system reliability by investigating the internal and external reasons that result in weak segments. Circuit reliability estimation techniques can broadly be divided into simulation-based and model analytical-based methods. The most prevalent simulation-based methods is the Monte Carlo (MC) method. Although this method's high accuracy is widely acknowledged in the industry, it is not suitable for large-scale circuits due to its time overhead. There are already many tools and algorithms for the model analytical-based methods, and some researchers have tried to improve these traditional techniques. For example, examining the effect of logical susceptibility and constancy of gates on Probabilistic Transfer Matrices (PTM) calculations [1]. A uniform and normal noise distribution is added to the Probabilistic Gate Models (PGM) [2]. Utilizing various structure learning and transfer learning algorithms to determine the most appropriate Bayesian Networks (BN) model [3]. In addition, some researchers combined novel models to estimate circuit reliability, such as stochastic computation [4], hybrid estimation [5], and approximate arithmetic [6], to speed up circuit reliability evaluation.

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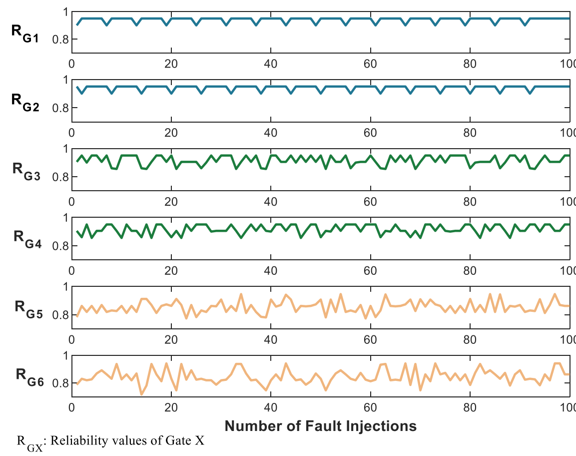


Fig. 1. Reliability of C17's six gates with 100 fault injections.

However, these methods calculate the reliability of each gate by traversing from the primary inputs to the primary outputs. The front-to-back connection relationships of the gates are considered, while the correlation between non-adjacent gates is easily ignored. As a result, the accuracy of these methods is affected, especially as the circuit size increases. For instance, the PTM method considers the effects of specific gate failures repeatedly. This results in reliability values that become smaller and smaller and eventually approach zero in very large circuits.

In fact, there is a general correlation between gates in the circuit due to the abundance of fan-out branches and re-convergence events. Some distant gates even show significant correlations. In terms of the general tendency in Fig. 1, gates closer to the primary inputs are less influenced by faults in other gates. Conversely, gates closer to the primary outputs are more vulnerable to faults caused by correlated gates passing backward. In addition, gates at similar-level locations are also influenced by the association in a similar way (refer to the colors in Fig. 1).

Identifying reliability high-correlated gates (HRCGs) not only improves reliability assessment accuracy but also provides an effective reference basis for failure locating, particularly for cascade failures. It can also be excluded in order according to the gates' reliability correlation (GRC). Furthermore, for large-scale circuits with numerous primary outputs could be precisely determined the single-output or multiple-outputs reliability by GRC. Decomposing the circuit with guaranteed accuracy to simplify reliability calculations.

Similarly, voltage correlation-based analysis [7], power correlation-based analysis [8], and time correlation-based analysis [9] at the circuit level and system level are similar in identifying HRCGs to assist in fault diagnosis. There are few studies to estimate gate correlation in terms of reliability and identify HRCGs. Therefore, we calculated the logic circuit's GRC using the Pearson correlation coefficient (PCC) and then identified all of the HRCGs in the circuit (PCC-HRCGI).

Our approach contributes to the following:

- We fitted the linear function and utilized logistic residual analysis to validate HRCGs existence based on the gates' reliability data;
- We introduced the PCC model to quantify the GRC and employed the F-significance test and correlation coefficient $\rho$ test to further examine the correctness;
- This approach was used to identify HRCGs as well as high-correlated primary outputs and sequential circuits with high-correlated flip-flops.

## II. Validate the Existence of HRCGs

### A. Acquiring Gates' Reliability

In order to avoid pseudo-randomness and high repetition rates, we initially generated $N$ uniform random input vectors based on UNBS [10]. To simulate more fault scenarios, we then randomly inject faults for all gates under each input vector. Since the SCA model [11] is an input vector-oriented reliability calculation method, the reliability values of all gates are then determined utilizing the SCA model with various input vectors. Finally, we counted the reliability value variations for each gate.

### B. Fitting Data With Distinct Linearity

To demonstrate the GRC more intuitively, we conduct further statistics and analysis on the reliability dataset generated in the previous step. By comparing the reliability values of any two gates, the two basic gates with the most comparable trends are selected. As in Fig. 2(a)'s 74148 circuit, $G_{14}$ and $G_{31}$. Fig. 2(a) shows that x=$R_{G14}$ and y=$R_{G31}$ are linear. Thus, the regression model was configured as follows:

$$\widehat{y} = \widehat{\beta}_0 + \widehat{\beta}_1 x_1 \tag{1}$$

The regression coefficients are $\widehat{\beta}_0$ and $\widehat{\beta}_1$, which are usually solved using the least squares method as in Equation (2).

$$minQ(\beta_0, \beta_1) = \sum_{i=1}^{N}\left[Y_i - \left(\widehat{\beta}_0 + \widehat{\beta}_1 x_1\right)\right]^2 \tag{2}$$

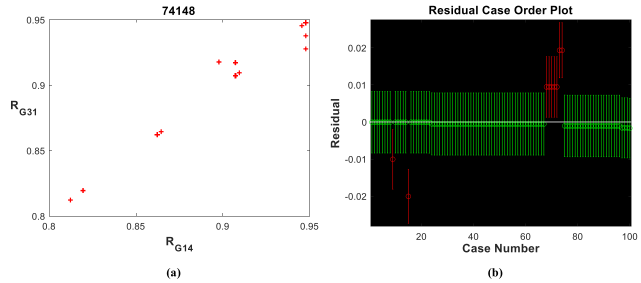


Fig. 2. Procedure for fitting and verifying the reliability correlation of 74148 circuit's $G_{14}$ and $G_{31}$.

Calculations reveal that $R_{G14}$ and $R_{G31}$ in Fig. 2 have correlation coefficients of 0.0113 and 0.9881, respectively. After the initial fit of $R_{G14}$ and $R_{G31}$, the correlation function is $R_{G31}$=0.9881×$R_{G14}$+0.0113.

### C. Validating the Reliability Fit Function

Taking into account that certain data are impacted by objective factors during the sampling process, such as fluctuations caused by the input vector with the worst reliability. Due to the regression residual analysis model could accurately identify outliers in the dataset. In this subsection, we use this model to verify and adjust the reliability fit function. Typically, outliers are assessed using standard residual values ($r$), which are calculated in Equation (3), where $s$ is the standard deviation.

$$r_{i,stand} = \frac{y_i - \widehat{y_i}}{s_{i,res}} \quad s_{i,res} = s\sqrt{1-h_i} \quad h_i = \frac{1}{N} + \frac{(x_i - \overline{x})^2}{\sum_i (x_i - \overline{x})^2} \tag{3}$$

Fig. 2(b)'s residual distribution reveals eight outliers, and their confidence intervals do not include zero. After excluding these outliers, use step 2 to obtain the most accurate relational function of $R_{G14}$ and $R_{G31}$ as: $R_{G31}$=0.9974×$R_{G14}$+0.0023. $R_{G14}$ and $R_{G31}$ are confirmed to be linearly correlated, hence G14 and G31 of 74148 are HRCGs.

## III. Identifying HRCGs

### A. Reliability Analysis for Basic Gates

The PCC-HRCGI approach creates $N$ uniform and random input vectors to prevent high repetition rates and pseudo-randomness. To reflect variances in the way faulty gates affect other gates, the PCC-HRCGI method randomly injects $N$ faults under $N$ input vectors. Contrary to the traditional overall circuit reliability analysis, GRC computation requires the probability of each gate's correct output from each fault injection. Lastly, method PCC-HRCGI computes and stores the reliability values of each gate under $N$ fault injections using the SCA model [11].

### B. PCC-Based GRC Calculation

Although logistic regression analysis (LRA) can accurately estimate the linear connection between any two gates, its temporal complexity of O($G^2$) makes it inapplicable to large-scale circuits, where $G$ is the number of basic gates in the circuit. Different from Chapter II's Part A, PCC-HRCGI employs the PCC model to quantify GRC. The PCC's superior computing

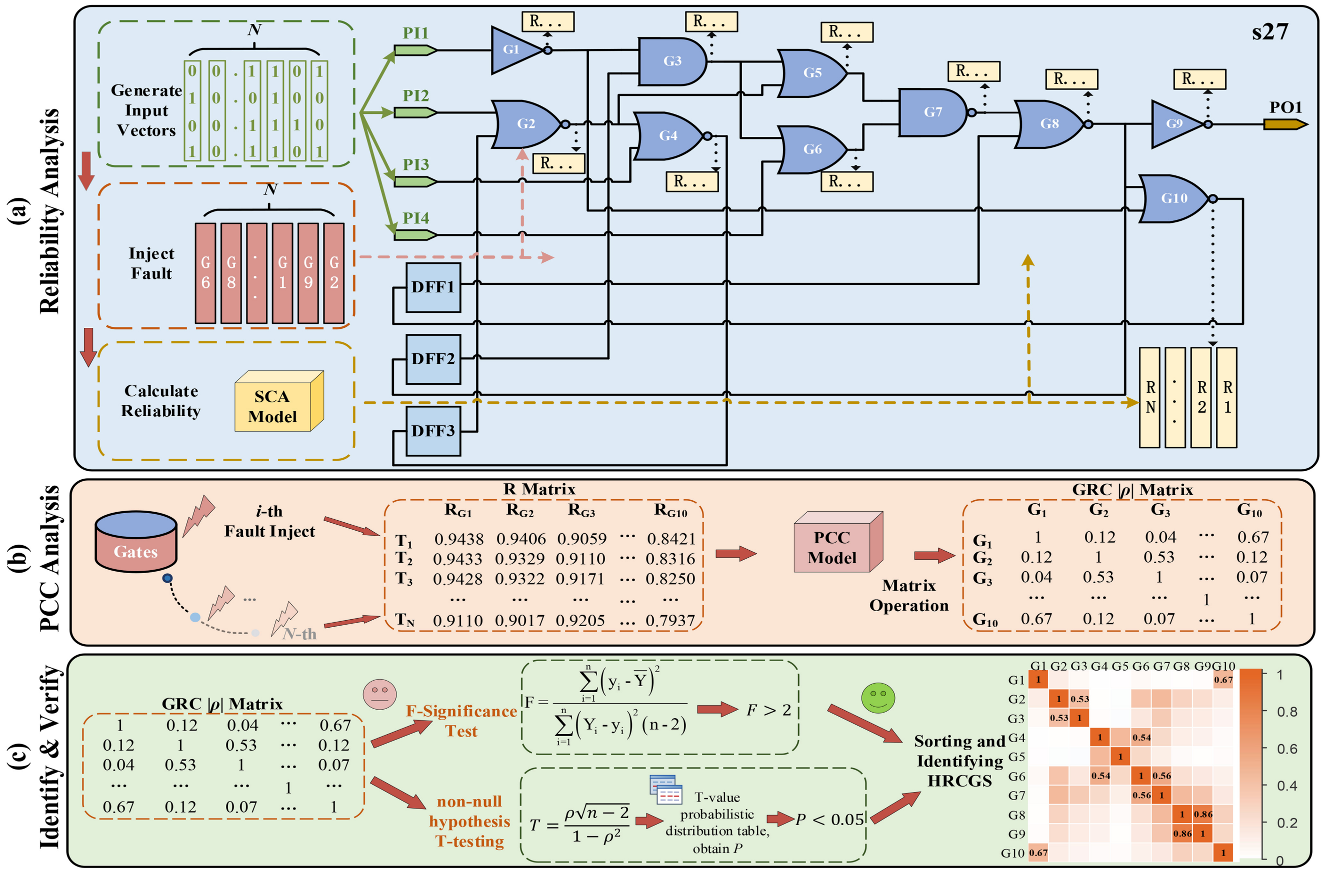

Fig. 3. An illustration of the PCC-HRCGI method on the s27 circuit.

performance and support for matrix calculation enable the PCC-HRCGI method to complete the GRC computation with the temporal complexity of O($G$).

The Pearson correlation coefficient, established by Pearson in 1895, measures the significance and direction of a correlation between variables [12]. The formula for deriving the PCC between two samples $x_i$ and $y$ is shown in Equation (4).

$$r_{x,y} = \frac{\sum_{i=1}^{N}(x_i - \overline{x})(y_i - \overline{y})}{\sqrt{\sum_{i=1}^{N}(x_i - \overline{x})^2} \times \sqrt{\sum_{i=1}^{N}(y_i - \overline{y})^2}} \tag{4}$$

The range of PCC is [−1, 1], the correlation grows stronger the larger the absolute value of $r$. While $r$=1 denotes a completely positive linear correlation, $r$=−1 means a completely negative linear correlation, and $r$=0, stands for no linear correlation.

Because the fault injection sequence has a time-series relationship with each gate reliability, the PCC-HRCGI method employs time-series PCC to accelerate GRC calculation. Thus, PCC-HRCGI creates a reliability value matrix of size $N$×$G$ (***R*** matrix, as in Fig. 3(b)). Each column in the ***R*** matrix represents the reliable value of the gate in a time series. PCC-HRCGI uses the overall correlation coefficient calculation Equation (5):

$$\rho_{R_{G_i},R_G} = \frac{\mathrm{cov}\left(R_{G_i},\ R_G\right)}{\sigma_{R_{G_i}}\sigma_{R_G}} \tag{5}$$

Similar to $r$, a value of $\rho$>0 denotes a positive correlation, $\rho$<0 denotes a negative correlation, and $\rho$=0 denotes irrelevant. A larger |$\rho$| indicates a stronger correlation. $R_{Gi}$ and $\boldsymbol{R_G}$ are the time series of reliability values of the $i$-th gate and other gates. The standard deviation is represented by $\sigma$, and the function cov($x$, $y$) is used to find covariance. The PCC-HRCGI method calculates GRC utilizing Equation (5) and generates a GRC matrix of size $G$×$G$ based on the matrix operation of ***R***. ***GRC***($i$, $j$) represents the correlation coefficient of gate $i$ and $j$.

### C. Identifying and Verifying HRCGs

Considering that not all gates are HRCGs, even though we have calculated the GRC of all gates, further identification of HRCGs from the ***GRC*** is required. It is common to check the correlation coefficient following PCC calculation by using the non-null hypothesis $T$-testing and the $F$-significance check. The former assumes that there is no significant linear relationship between the two variables (i.e., null correlation). The $T$-value in Equation (6) was used to test the correlation coefficient $\rho$ based on this hypothesis. The value of the probability $P$ that the null correlation hypothesis is correct can then be obtained by consulting the $T$-value probabilistic distribution table. A significant linear correlation between the two variables is often indicated by $P$<0.05.

$$T = \frac{\rho\sqrt{n-2}}{1-\rho^2} \tag{6}$$

In addition, the $F$-significance check is widely used as a significance test. Usually when the $F$>2 then the correlation

TABLE I
PERFORMANCE OF METHOD PCC-HRCGI ON DIFFERENT CIRCUITS

| Circuits | | Gates | PCC-HRCGI | | | | | | | | MC-based LRA [8] | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1st-HRCGs | Time(s) | *r* | *P* | *Acc* | *Ir* | *St* | F | 1st-HRCGs | $\beta_0$ | $\beta_1$ | Time(s) |
| **Combinational Logic Circuits** | | | | | | | | | | | | | | |
| **74-serial** | 74148 | 31 | G22&G26 | 0.15 | 0.9725 | 0.0004 | 1 | 1 | .001 | >2 | G22&G26 | 0.04 | 0.95 | 0.78 |
| | 74185 | 33 | G9&G21 | 0.16 | 0.8813 | 0.0015 | 1 | 1 | .001 | >2 | G9&G21 | 0.10 | 0.88 | 0.92 |
| | 74283 | 36 | G27&G36 | 0.19 | 0.9343 | 0.0009 | 1 | 1 | .001 | >2 | G27&G36 | 0.14 | 0.91 | 1.34 |
| **ISCA S85** | C432 | 160 | G86&G97 | 1.05 | 0.9997 | 0.0002 | 1 | 1 | .002 | >2 | G86&G97 | 0.05 | 0.98 | 23.12 |
| | C5315 | 2,307 | G121&G456 | 9.16 | 1 | 0 | 1 | 1 | .003 | >2 | G121&G456 | 1.49e-13 | 1.00 | 3,530.71 |
| | C7552 | 3,512 | G48&G173 | 11.47 | 1 | 0 | 1 | 1 | .003 | >2 | G48&G173 | 7.91e-14 | 1.00 | 7,090.42 |
| **EPF L** | sin_sin23 | 11,247 | G14&G1803 | 126.21 | 1 | 0 | 0.97 | 1 | .005 | >2 | G97&G127 | 0.05 | 0.90 | 440,711.53 |
| | square_70 | 24,136 | G41&G46 | 491.22 | 1 | 0 | null | 1 | .007 | >2 | null | 3.04e-11 | 0.99 | null |
| | voter_maj | 34,103 | G33945&G34090 | 484.90 | 1 | 0 | null | 0.98 | .012 | >2 | null | 6.17e-13 | 1.00 | null |
| **Sequential Logic Circuits** | | | | | | | | | | | | | | |
| **ISCA S89** | s298 | 119 | G103&G104 | 2.01 | 0.9009 | 1.01e-73 | 1 | 1 | .002 | >2 | G103&G104 | 0.0370 | 0.9176 | 109.95 |
| | s713 | 393 | G274&G284 | 5.40 | 0.9156 | 1.20e-80 | 1 | 1 | .002 | >2 | G274&G284 | 0.0288 | 0.9029 | 430.47 |
| | s1238 | 508 | G311&G318 | 6.54 | 0.8850 | 1.16e-67 | 1 | 1 | .003 | >2 | G311&G318 | 0.0342 | 0.9301 | 480.82 |
| **ITC 99** | b05 | 927 | G400&G402 | 12.66 | 0.9169 | 6.73e-81 | 1 | 1 | .002 | >2 | G400&G402 | 0.0468 | 0.9036 | 1,190.11 |
| | b20 | 19,682 | G12773&G12750 | 223.94 | 0.9829 | 1.09e-14 | null | 1 | .011 | >2 | null | 0.0155 | 0.9407 | null |
| | b21 | 20,027 | G1247&G1342 | 302.16 | 0.9756 | 2.68e-13 | null | 0.99 | .014 | >2 | null | 0.0205 | 0.9391 | null |
| **IWL S2005** | ethernet | 46,804 | G9563&G10767 | 2064.35 | 0.9093 | 7.42e-12 | null | 0.95 | .039 | >2 | null | 0.0027 | 0.9189 | null |
| | b18 | 111,241 | G29377& G44203 | 3809.22 | 0.9661 | 4.17e-10 | null | 0.93 | .054 | >2 | null | 0.0003 | 0.9420 | null |
| | vga_lcd | 124,050 | G57260&G114131 | 5688.55 | 0.8378 | 2.39e-9 | null | 0.88 | .092 | >2 | null | 0.1061 | 0.8627 | null |

is significant. The dataset of all identified HRCGs will also undergo an F-significance check by the PCC-HRCGI method. Equation (7) calculated the significance value $F$.

$$F = \frac{\sum_{i=1}^{n} \left(\widehat{y_i} - \overline{Y}\right)^2}{\sum_{i=1}^{n} \left(Y_i - \widehat{y_i}\right)^2 (n-2)} \tag{7}$$

The PCC-HRCGI method returns the final HRCGs after finishing identification and verification. In addition, to depict the strength of gate correlation, we display the gate correlation in the circuit using a heat map, as shown in Fig. 3 (c).

## IV. SIMULATING

To facilitate comparison and validation between different approaches, we employed benchmark circuits widely used in [6], [10], [11], and [12]. We contrast our approach on small- and medium-sized circuits with the MC-based Ref. [8] method. We selected the Rand-based LRA method as a reference for larger-scale circuits due to the MC method's limitations. All experiments were conducted on a personal PC with a Core i5-7550 processor (3.4 GHz) and 32GB of RAM.

### A. Evaluation Metrics

1) *Accuracy:* Equation (7) is used to calculate the accuracy of method $i$ compared to the MC method.

$$ACC_i = \frac{\overline{GRC_i}}{\overline{GRC_{MC}}} = \frac{\frac{\sum_{k=1}^{N} GRC_{i,k}}{N}}{\frac{\sum_{k=1}^{N} GRC_{MC,k}}{N}} \tag{8}$$

2) *Identification rate:* Equation (9) measures the size of the MC-supported circuits, Equation (10) measures larger-scale circuits:

$$Ir_i = \frac{\sum HRCGs_i}{\sum HRCGs_{MC}} \tag{9}$$

$$Ir_i = \frac{\sum HRCGs_i}{\sum HRCGs_i + \sum HRCGs_j} \tag{10}$$

3) *Stability:* Equation (11) measures identification of HRCGs on the same circuit with $T$ times.

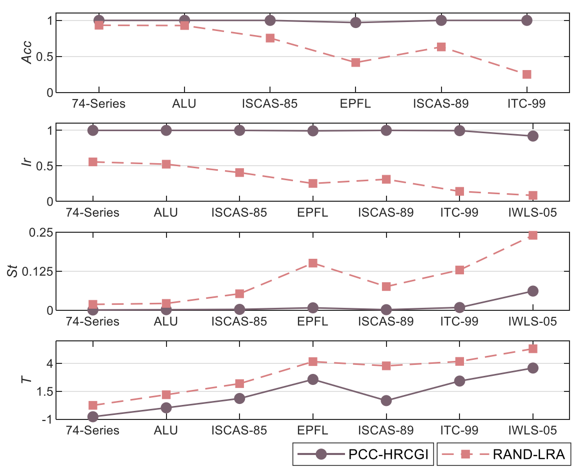


Fig. 4. Comparison of *Acc*, *Ir*, *St*, and *T* by different methods.

$$St_i = \sqrt{\frac{\sum_{t=1}^{T} \left(GRC_{i,t} - \overline{GRC_i}\right)^2}{T}} \tag{11}$$

### B. Performance Analysis

As shown in Table I, compared to the MC method, the average accuracy (*Acc*) of the PCC-HRCGI method is about 0.9972, and it is 2591 times faster than MC on average. Then we examined the identification rate (*Ir*) and stability (*St*) of the PCC-HRCGI method. The *St* and *Ir* on average are 0.0141 and 98.50%, respectively. Next, we used the LRA to precisely calculate the correlation coefficients of the identified HRCGs and further validate them using F- and T-tests due to the MC method's limitations on larger circuits.

Fig. 4 displays the evaluation metrics of the two methods for identifying HRCGs on various types of circuits. As can be observed, the PCC-HRCGI method is superior to the Rand-LRA method in terms of *Acc*, *Ir*, and *St*, especially its time overhead $T$ ($T$=$\log_{10} t$) is shorter by two orders of magnitude.

### C. Efficiency Analysis

As shown in Fig. 5, we counted the number of HRCGs identified by the method PCC-HRCGI on six distinct types

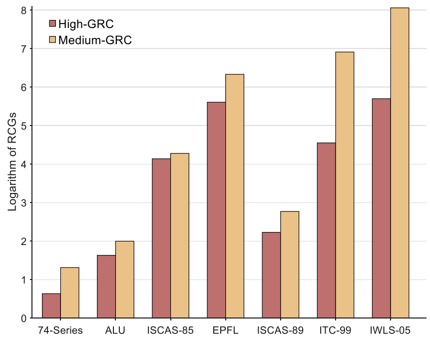


Fig. 5. Two types of RCGs number by PCC-HRCGI method.

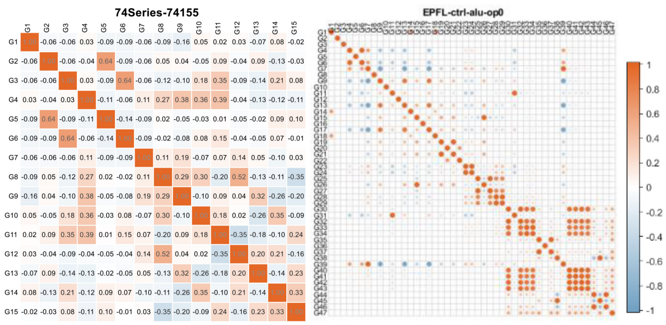


Fig. 6. GRC quantification and HRCGs identification.

of benchmark circuits to validate the method's efficiency. For moderately correlated RCGs (0.6<GRC<0.8), we use yellow bars, and for highly correlated RCGs (0.8<GRC<1), red bars.

Fig. 5 demonstrates that as circuit size increases, the method PCC-HRCGI identifies exponentially more HRCGs on combinational and sequential circuits. Especially, the IWLS-05 circuits contain more than $10^8$ identified HRCGs. It is evident that there is a regular correlation among gates.

### D. Applicability Analysis

Based on the PCC-HRCGI method, the GRC between different gates can be accurately quantified, and highly correlated HRCGs can be quickly and efficiently identified, as shown in Fig. 6. This approach could provide an effective reference basis for fault location and is especially advantageous for cascading faults.

From Fig. 7, the PCC-HRCGI method can be used to find HRCGs as well as correlations between the primary outputs or flip-flops to increase the precision of circuit reliability analysis and provide an explanation for dividing and merging multiple output circuits. Additionally, for very large-scale integration circuits, this approach can effectively calculate the correlation coefficients of any two gates, even if the identification of all HRCGs is constrained.

## V. Conclusion

In this brief, we first fit the reliability evaluation results of the circuit's gates to create the linear correlation function of HRCGs. We then used regression residual analysis to calibrate the function and demonstrate HRCGs' existence. Then, we applied a time-series-based PCC model to quantify the GRC and identified all the HRCGs in the circuit by matrix

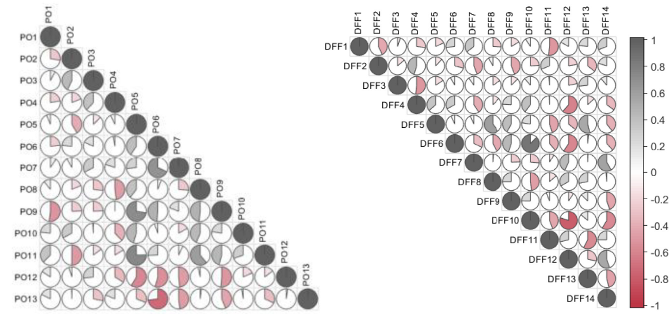

Fig. 7. Identification of correlated primary outputs (PO) and D-flip-flops with the PCC-HRCGI method on s1238 and s298.

operations, called PCC-HRCGI. Finally, we applied it to identify circuit-correlated primary outputs and sequential circuits' correlated flip-flops. Experimental results on benchmark circuits show that the average accuracy of the PCC-HRCGI method is about 0.99 with the MC-based LRA approach, and the time is roughly 2591 times faster than the MC method. On larger circuits, the identification rate and stability are 6.07 times and 13.55 times superior to the Rand-based LRA method.

## References

[1] M. F. Pontes, I. F. V. Oliveira, R. B. Schvittz, L. S. Rosa, and P. F. Butzen, "The impact of logic gates susceptibility in overall circuit reliability analysis," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Austin, TX, USA, 2022, pp. 1610–1614.

[2] M. A. K. Abuelala, A. Wassal, A. Khattab, and H. A. H. Fahmy, "A novel model for injecting error in probabilistic gates," in *Proc. 31st Int. Conf. Microelectron. (ICM)*, Cairo, Egypt, 2019, pp. 276–279.

[3] R. Pan, Z. Zhang, X. Li, K. Chakrabarty, and X. Gu, "Black-box test-cost reduction based on Bayesian network models," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 40, no. 2, pp. 386–399, Feb. 2021.

[4] J. Xiao, Q. Ji, Q. Shen, J. Jiang, Y. Huang, and J. Lou, "Accelerating stochastic-based reliability estimation for combinational circuits at RTL using GPU parallel computing," *Int. J. Intell. Syst.*, vol. 37, no. 11, pp. 8309–8326, Jun. 2022, doi: 10.1002/int.22940.

[5] C. Chen and S. Zhan, "A hybrid method for signal probability estimation with combinational circuits," in *Proc. IEEE Asia–Pacific Conf. Circuits Syst. (APCCAS)*, Shenzhen, China, 2022, pp. 472–475.

[6] Z. Wang, G. Zhang, P. Liu, J. Ye, and J. Jiang, "Accurate reliability boundary evaluation of approximate arithmetic circuit," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 30, no. 10, pp. 1507–1518, Oct. 2022, doi: 10.1109/TVLSI.2022.3193897.

[7] G. Wang, J. Yang, and J. Jiao, "Voltage correlation-based principal component analysis method for short circuit fault diagnosis of series battery pack," *IEEE Trans. Ind. Electron.*, vol. 70, no. 9, pp. 9025–9034, Sep. 2023, doi: 10.1109/TIE.2022.3210588.

[8] B. Li, X. Zhou, and P. Dong, "Power failure sensitivity analysis via grouped $L_{1/2}$ sparsity constrained logistic regression," *KSII Trans. Internet Inf. Syst.*, vol. 15, no. 8, pp. 3086–3101, Aug. 2021, doi: 10.3837/tiis.2021.08.021.

[9] M. Ni, X. Wang, F. Li, W. Rhee, and Z. Wang, "A 13-bit 2-GS/s time-interleaved ADC with improved correlation-based timing skew calibration strategy," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 2, pp. 481–494, Feb. 2022.

[10] J. Xiao, Z. Shi, X. Yang, and J. Lou, "BM-RCGL: Benchmarking approach for localization of reliability-critical gates in combinational logic blocks," *IEEE Trans. Comput.*, vol. 71, no. 5, pp. 1063–1076, May 2022, doi: 10.1109/TC.2021.3071253.

[11] Z. Shi, J. Xiao, W. Zhu, and J. Jiang, "A reliability-critical path identifying method with local and global adjacency probability matrix in combinational circuits," *IEEE Trans. Comput.*, early access, Oct. 16, 2023, doi: 10.1109/TC.2023.3323772.

[12] K. Pearson, "Contributions to the mathematical theory of evolution," *Philos. Trans. Royal Soc. London*, vol. 185, pp. 71–110, Jan. 1894. [Online]. Available: https://www.jstor.org/stable/90667