Indian Institute of Technology (IIT-Kharagpur)

AUTUMN Semester, 2022
COMPUTER SCIENCE AND ENGINEERING

(COA Laboratory)

Designing Counters and Displaying the output on the LEDs of the FPGA Board

1. **Binary Counter:** is a sequential circuit. An up-counter will count up, say from 0. Consider a 4-bit binary counter, which when reset is initialized to 0000, and then at the positive edge of the clock starts counting in the sequence: $(0000), (0001), (0010), (0011), \ldots, (1111), (0000)$. Let us consider two ways of designing the above counter.

   (a) Behavioral Design: Write a verilog code to design the up-counter. You can use verilog constructs to define the logic of the counter. The counter should have an asynchronous reset, so that the counter can be reset at any time to zero. The result of the counter should be displayed on the LEDs in your board.

   [**Note on Persistence of Human eyes:** The retina retains some of the information it has been stimulated with and takes time to process. This phenomenon, which places limits on how fast our visual system can react to changes, is known as *visual persistence*. Simply put, our visual system has a slow response to change in stimulus. We can take advantage of this to develop techniques for digital video systems.

   Although an image on the retina decays gradually, rather than lasting a specific amount of time, there is a critical period during which the stimulus changes so little that the visual system cannot take in any new information even if the eyes are open. This period, on average, is about 50 milliseconds, or one-twentieth of a second. Thus, the average human visual system can only take in about 20 different images per second before they begin to blur together. The frequency of the internal clock of the device is 100 MHz, and hence the state of the counter changes at the rate of 10 ns! So one needs to divide the clock to see the change. Strangely this weakness in humans is used for digital video systems. We shall see in a later class in context to control the LED panel of your board!!]

   (b) Structural Design: Design the architecture of the up-counter using a 4-bit adder. Note that you can design an add by one adder by optimizing the design of the RCA/CLA you have done in the last assignment. Work out the details of the optimized *add-by-one* block, and write the verilog codes. Also you need to design a D-FlipFlop as mentioned in the lab. Draw the architecture for the up-counter, with the above blocks as sub-modules. Write the verilog code, and prototype on the FPGA board. Again beware of the persistence of human eyes!