

Operational Amplifiers

10

CHAPTER OBJECTIVES

- Understand what a differential amplifier does
- Learn the basics of an operational amplifier
- Develop an understanding of what common mode operation is
- Describe double-ended input operation

01.04.19

10.1 INTRODUCTION

An operational amplifier, or op-amp, is a very high gain differential amplifier with high input impedance and low output impedance. Typical uses of the operational amplifier are to provide voltage amplitude changes (amplitude and polarity), oscillators, filter circuits, and many types of instrumentation circuits. An op-amp contains a number of differential amplifier stages to achieve a very high voltage gain.

Figure 10.1 shows a basic op-amp with two inputs and one output as would result using a differential amplifier input stage. Each input results in either the same or an opposite polarity (or phase) output, depending on whether the signal is applied to the plus (+) or the minus (-) input, respectively.

Single-Ended Input

Single-ended input operation results when the input signal is connected to one input with the other input connected to ground. Figure 10.2 shows the signals connected for this operation. In Fig. 10.2a, the input is applied to the plus input (with minus input at ground), which results in an output having the same polarity as the applied input signal. Figure 10.2b shows an input signal applied to the minus input, the output then being opposite in phase to the applied signal.

Double-Ended (Differential) Input

In addition to using only one input, it is possible to apply signals at each input—this being a double-ended operation. Figure 10.3a shows an input, V_d , applied between the two input terminals (recall that neither input is at ground), with the resulting amplified output in phase with that applied between the plus and minus inputs. Figure 10.3b shows the same action resulting when two separate signals are applied to the inputs, the difference signal being $V_{i_1} - V_{i_2}$.

of this unwanted input while providing an amplified output of the difference signal applied to the inputs. This operating feature is referred to as *common-mode rejection*.

10.2 DIFFERENTIAL AMPLIFIER CIRCUIT

The differential amplifier circuit is an extremely popular connection used in IC units. This connection can be described by considering the basic differential amplifier shown in Fig. 10.9. Notice that the circuit has two separate inputs and two separate outputs, and that the emitters are connected together. Whereas many differential amplifier circuits use two separate voltage supplies, the circuit can also operate using a single supply.

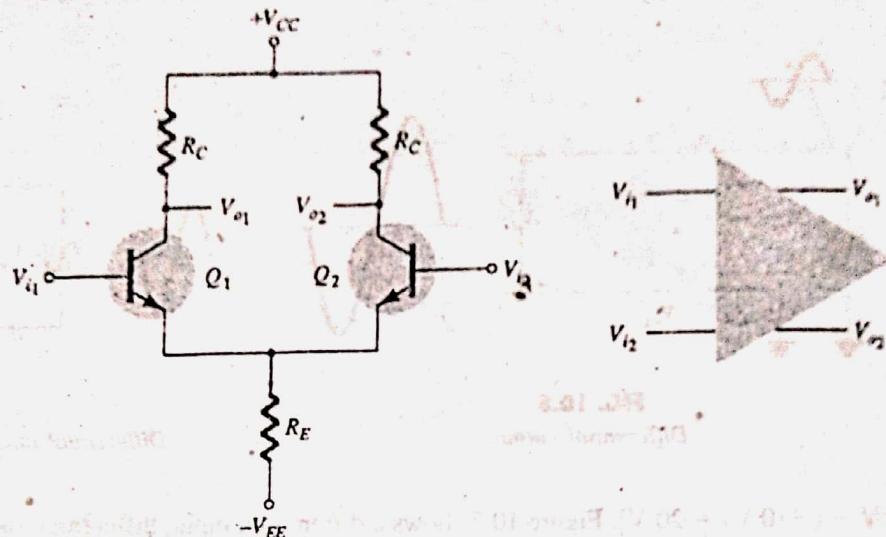


FIG. 10.9
Basic differential amplifier circuit.

A number of input signal combinations are possible:

If an input signal is applied to either input with the other input connected to ground, the operation is referred to as "single-ended."

If two opposite-polarity input signals are applied, the operation is referred to as "double-ended."

If the same input is applied to both inputs, the operation is called "common-mode."

In single-ended operation, a single input signal is applied. However, due to the common-emitter connection, the input signal operates both transistors, resulting in output from both collectors.

In double-ended operation, two input signals are applied, the difference of the inputs resulting in outputs from both collectors due to the difference of the signals applied to both inputs.

In common-mode operation, the common input signal results in opposite signals at each collector, these signals canceling, so that the resulting output signal is zero. As a practical matter, the opposite signals do not completely cancel, and a small signal results.

The main feature of the differential amplifier is the very large gain when opposite signals are applied to the inputs as compared to the very small gain resulting from common inputs. The ratio of this difference gain to the common gain is called *common-mode rejection*.

DC Bias

Let's first consider the dc bias operation of the circuit of Fig. 10.9. With ac inputs obtained from voltage sources, the dc voltage at each input is essentially connected to 0 V, as shown in Fig. 10.10. With each base voltage at 0 V, the common-emitter dc bias voltage is

$$V_E = 0 \text{ V} - V_{BE} = -0.7 \text{ V}$$

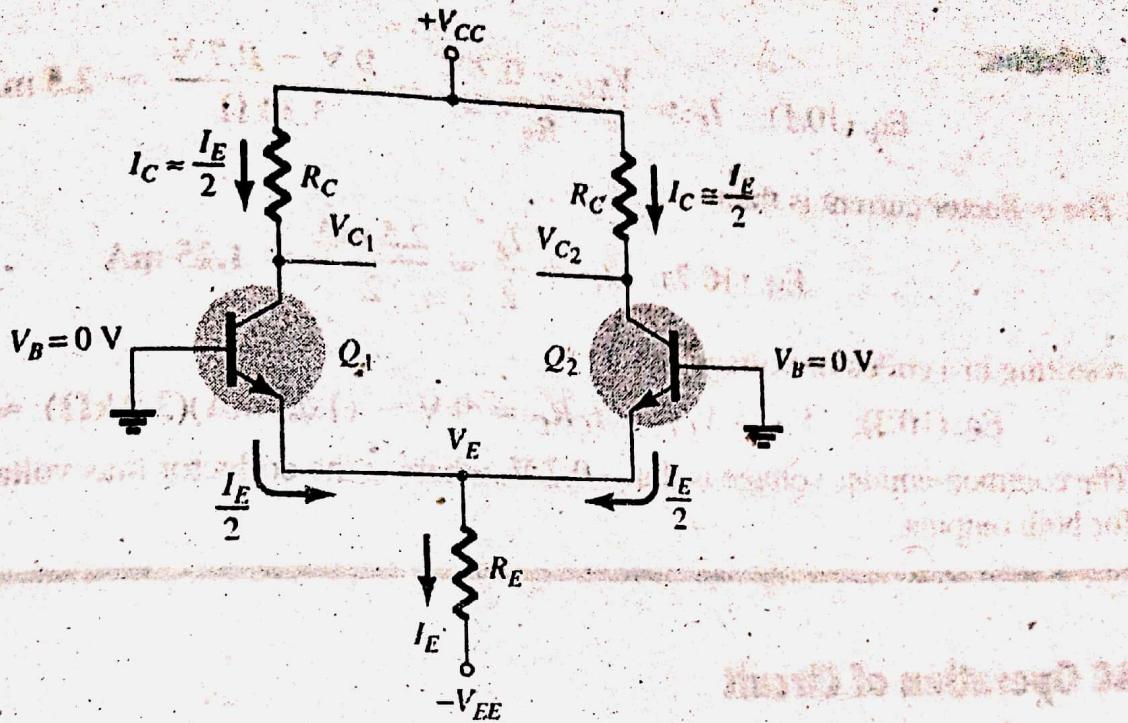


FIG. 10.10
DC bias of differential amplifier circuit.

The emitter dc bias current is then

$$I_E = \frac{V_E - (-V_{EE})}{R_E} \approx \frac{V_{EE} - 0.7 \text{ V}}{R_E} \quad (10.1)$$

Assuming that the transistors are well matched (as would occur in an IC unit), we obtain

$$I_{C_1} = I_{C_2} = \frac{I_E}{2} \quad (10.2)$$

resulting in a collector voltage of

$$V_{C_1} = V_{C_2} = V_{CC} - I_C R_C = V_{CC} - \frac{I_E}{2} R_C \quad (10.3)$$

EXAMPLE 10.1 Calculate the dc voltages and currents in the circuit of Fig. 10.11.

the common point between n MOS and p MOS transistors on one side of the circuit. This type of CMOS differential amplifier is particularly well suited for battery operation due to the low power dissipation of a CMOS circuit.

10.4 OP-AMP BASICS

An operational amplifier is a very high gain amplifier having very high input impedance (typically a few megohms) and low output impedance (less than 100Ω). The basic circuit is made using a difference amplifier having two inputs (plus and minus) and at least one output. Figure 10.29 shows a basic op-amp unit. As discussed earlier, the plus (+) input produces an output that is in phase with the signal applied, whereas an input to the minus (-) input results in an opposite-polarity output. The ac equivalent circuit of the op-amp is shown in Fig. 10.30a. As shown, the input signal applied between input terminals sees an input impedance R_i that is typically very high. The output voltage is shown to be the amplifier gain times the input signal taken through an output impedance R_o , which is typically very low. An ideal op-amp circuit, as shown in Fig. 10.30b, would have infinite input impedance, zero output impedance, and infinite voltage gain.

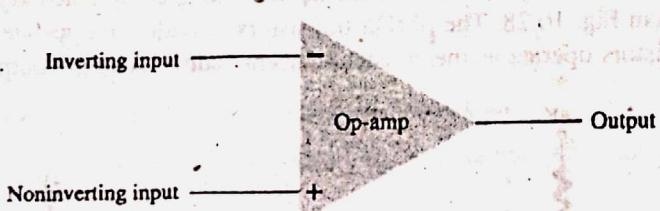


FIG. 10.29
Basic op-amp.

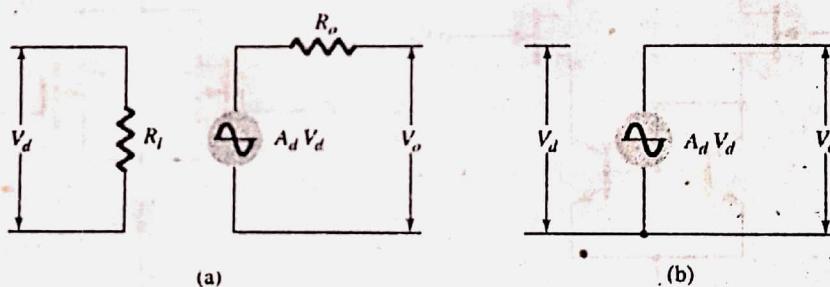


FIG. 10.30
AC equivalent of op-amp circuit: (a) practical; (b) ideal.

Basic Op-Amp

The basic circuit connection using an op-amp is shown in Fig. 10.31. The circuit shown provides operation as a constant-gain multiplier. An input signal V_1 is applied through resistor R_1 to the minus input. The output is then connected back to the same minus input through resistor R_f . The plus input is connected to ground. Since the signal V_1 is essentially applied to the minus input, the resulting output is opposite in phase to the input signal. Figure 10.32a shows the op-amp replaced by its ac equivalent circuit. If we use the ideal

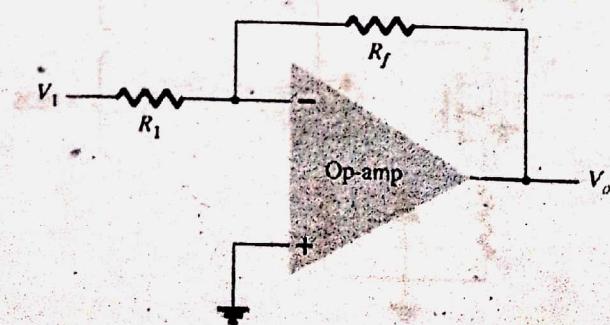


FIG. 10.31
Basic op-amp connection.

Unity Gain

If $R_f = R_1$, the gain is

$$\text{Voltage gain} = -\frac{R_f}{R_1} = -1$$

so that the circuit provides a unity voltage gain with 180° phase inversion. If R_f is exactly R_1 , the voltage gain is exactly 1.

Constant-Magnitude Gain

If R_f is some multiple of R_1 , the overall amplifier gain is a constant. For example, if $R_f = 10R_1$, then

$$\text{Voltage gain} = -\frac{R_f}{R_1} = -10$$

and the circuit provides a voltage gain of exactly 10 along with a 180° phase inversion from the input signal. If we select precise resistor values for R_f and R_1 , we can obtain a wide range of gains, the gain being as accurate as the resistors used and is only slightly affected by temperature and other circuit factors.

Virtual Ground

The output voltage is limited by the supply voltage of, typically, a few volts. As stated before, voltage gains are very high. If, for example, $V_o = -10$ V and $A_v = 20,000$, the input voltage is

$$V_i = \frac{-V_o}{A_v} = \frac{10 \text{ V}}{20,000} = 0.5 \text{ mV}$$

If the circuit has an overall gain (V_o/V_1) of, say, 1, the value of V_1 is 10 V. Compared to all other input and output voltages, the value of V_i is then small and may be considered 0 V.

Note that although $V_i \approx 0$ V, it is not exactly 0 V. (The output voltage is a few volts due to the very small input V_i times a very large gain A_v .) The fact that $V_i \approx 0$ V leads to the concept that at the amplifier input there exists a virtual short-circuit or virtual ground.

The concept of a virtual short implies that although the voltage is nearly 0 V, there is no current through the amplifier input to ground. Figure 10.33 depicts the virtual ground concept. The heavy line is used to indicate that we may consider that a short exists with $V_i \approx 0$ V but that this is a virtual short so that no current goes through the short to ground. Current goes only through resistors R_1 and R_f as shown.

Using the virtual ground concept, we can write equations for the current I as follows:

$$I = \frac{V_1}{R_1} = -\frac{V_o}{R_f}$$

which can be solved for V_o/V_1 :

$$\frac{V_o}{V_1} = -\frac{R_f}{R_1}$$

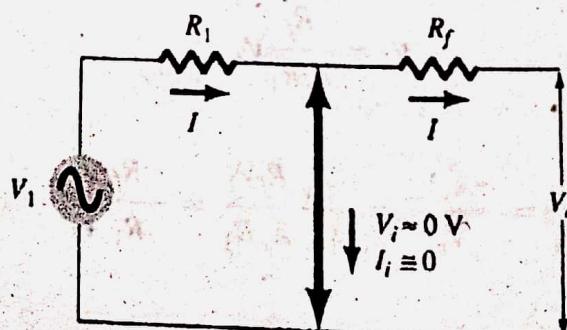


FIG. 10.33
Virtual ground in an op-amp.

The virtual ground concept, which depends on A_v being very large, allowed a simple solution to determine the overall voltage gain. It should be understood that although the circuit of Fig. 10.33 is not physically correct, it does allow an easy means for determining the overall voltage gain.

10.5 PRACTICAL OP-AMP CIRCUITS

The op-amp can be connected in a large number of circuits to provide various operating characteristics. In this section, we cover a few of the most common of these circuit connections.

Inverting Amplifier

The most widely used constant-gain amplifier circuit is the inverting amplifier, as shown in Fig. 10.34. The output is obtained by multiplying the input by a fixed or constant gain, set by the input resistor (R_1) and feedback resistor (R_f)—this output also being inverted from the input. Using Eq. (10.8), we can write

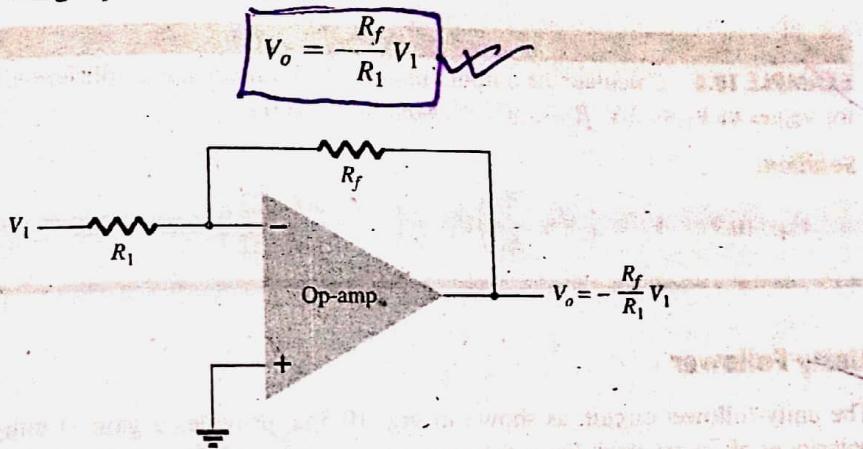


FIG. 10.34

Inverting constant-gain multiplier.

EXAMPLE 10.5 If the circuit of Fig. 10.34 has $R_1 = 100 \text{ k}\Omega$ and $R_f = 500 \text{ k}\Omega$, what output voltage results for an input of $V_1 = 2 \text{ V}$?

Solution:

$$\text{Eq. (10.8): } V_o = -\frac{R_f}{R_1} V_1 = -\frac{500 \text{ k}\Omega}{100 \text{ k}\Omega} (2 \text{ V}) = -10 \text{ V}$$

Noninverting Amplifier

The connection of Fig. 10.35a shows an op-amp circuit that works as a noninverting amplifier or constant-gain multiplier. It should be noted that the inverting amplifier connection is more widely used because it has better frequency stability (discussed later). To determine the voltage gain of the circuit, we can use the equivalent representation shown in Fig. 10.35b. Note that the voltage across R_1 is V_1 since $V_i \approx 0 \text{ V}$. This must be equal to the output voltage, through a voltage divider of R_1 and R_f , so that

$$V_1 = \frac{R_1}{R_1 + R_f} V_o$$

Voltage
divider
rule

which results in

$$\frac{V_o}{V_1} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1} \quad (10.9)$$

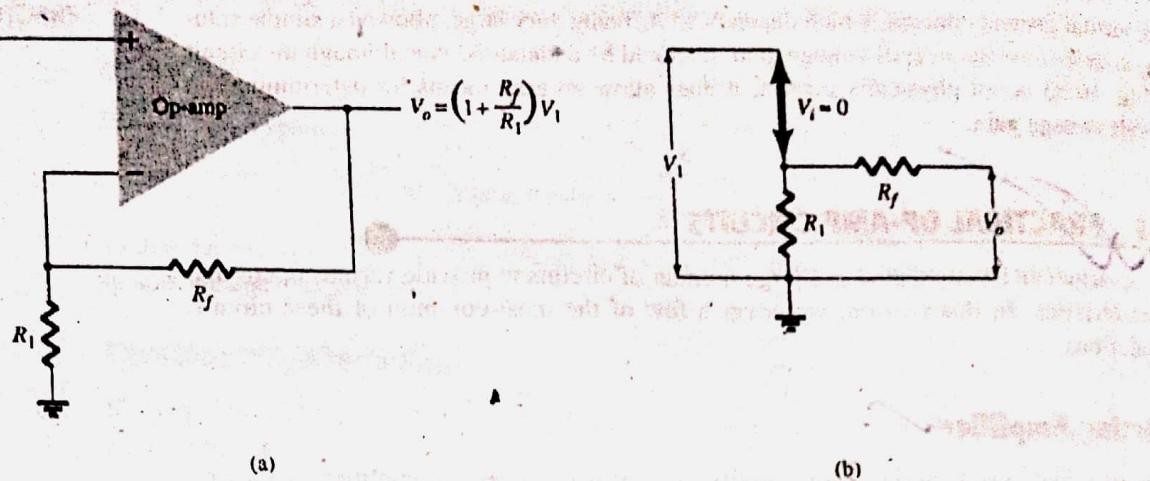


FIG. 10.35
Noninverting constant-gain multiplier.

EXAMPLE 10.6 Calculate the output voltage of a noninverting amplifier (as in Fig. 10.35) for values of $V_1 = 2 \text{ V}$, $R_f = 500 \text{ k}\Omega$, and $R_1 = 100 \text{ k}\Omega$.

Solution:

$$\text{Eq. (10.9): } V_o = \left(1 + \frac{R_f}{R_1}\right) V_1 = \left(1 + \frac{500 \text{ k}\Omega}{100 \text{ k}\Omega}\right)(2 \text{ V}) = 6(2 \text{ V}) = +12 \text{ V}$$

Unity Follower

The unity-follower circuit, as shown in Fig. 10.36a, provides a gain of unity (1) with no polarity or phase reversal. From the equivalent circuit (see Fig. 10.36b) it is clear that

$$V_g = V_1 \quad (10.10)$$

and that the output is the same polarity and magnitude as the input. The circuit operates like an emitter- or source-follower circuit except that the gain is exactly unity.

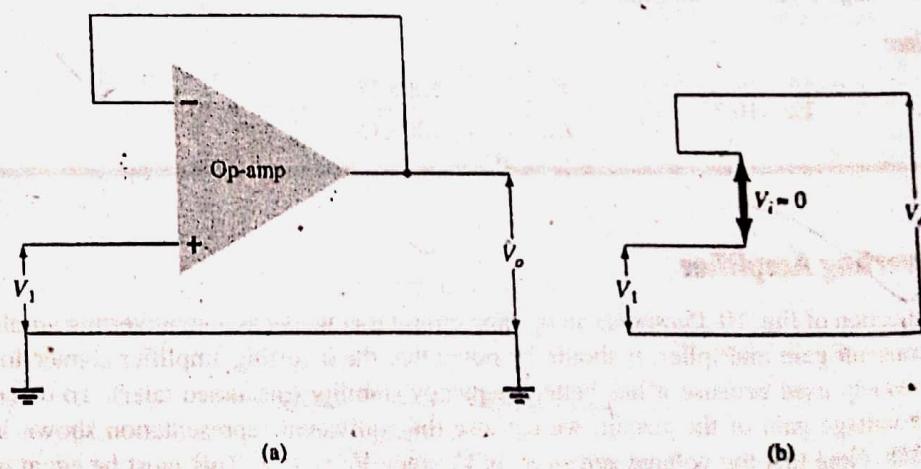


FIG. 10.36

Summing Amplifier

Probably the most used of the op-amp circuits is the summing amplifier circuit shown in Fig. 10.37a. The circuit shows a three-input summing amplifier circuit, which provides a means of algebraically summing (adding) three voltages, each multiplied by a constant-gain

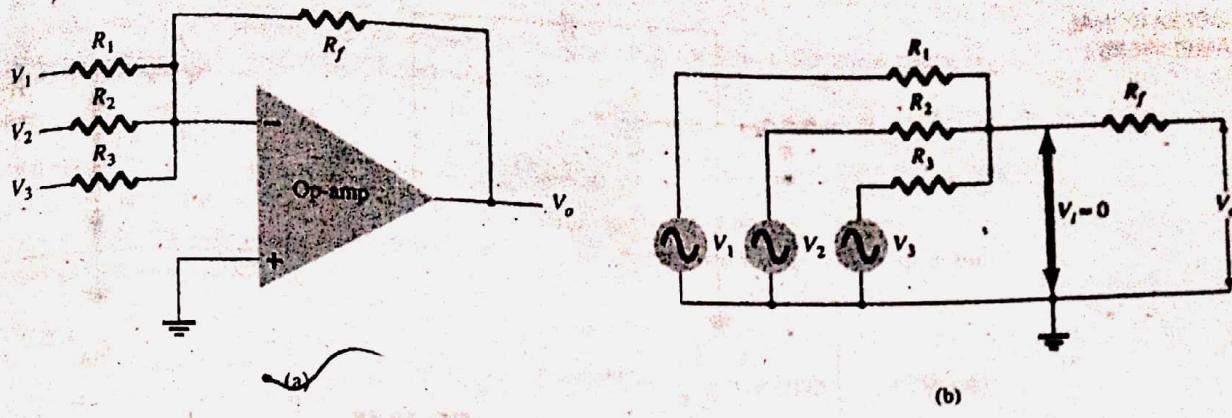


FIG. 10.37
(a) Summing amplifier; (b) virtual-ground equivalent circuit.

factor. Using the equivalent representation shown in Fig. 10.37b, we can express the output voltage in terms of the inputs as

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right) \quad (10.11)$$

In other words, each input adds a voltage to the output multiplied by its separate constant-gain multiplier. If more inputs are used, they each add an additional component to the output.

EXAMPLE 10.7 Calculate the output voltage of an op-amp summing amplifier for the following sets of voltages and resistors. Use $R_f = 1 \text{ M}\Omega$ in all cases.

- $V_1 = +1 \text{ V}, V_2 = +2 \text{ V}, V_3 = +3 \text{ V}, R_1 = 500 \text{ k}\Omega, R_2 = 1 \text{ M}\Omega, R_3 = 1 \text{ M}\Omega$.
- $V_1 = -2 \text{ V}, V_2 = +3 \text{ V}, V_3 = +1 \text{ V}, R_1 = 200 \text{ k}\Omega, R_2 = 500 \text{ k}\Omega, R_3 = 1 \text{ M}\Omega$.

Solution: Using Eq. (10.11), we obtain

$$\begin{aligned} \text{a. } V_o &= -\left[\frac{1000 \text{ k}\Omega}{500 \text{ k}\Omega}(+1 \text{ V}) + \frac{1000 \text{ k}\Omega}{1000 \text{ k}\Omega}(+2 \text{ V}) + \frac{1000 \text{ k}\Omega}{1000 \text{ k}\Omega}(+3 \text{ V})\right] \\ &= -[2(1 \text{ V}) + 1(2 \text{ V}) + 1(3 \text{ V})] = -7 \text{ V} \end{aligned}$$

$$\begin{aligned} \text{b. } V_o &= -\left[\frac{1000 \text{ k}\Omega}{200 \text{ k}\Omega}(-2 \text{ V}) + \frac{1000 \text{ k}\Omega}{500 \text{ k}\Omega}(+3 \text{ V}) + \frac{1000 \text{ k}\Omega}{1000 \text{ k}\Omega}(+1 \text{ V})\right] \\ &= -[5(-2 \text{ V}) + 2(+3 \text{ V}) + 1(+1 \text{ V})] = +3 \text{ V} \end{aligned}$$

Integrator

So far, the input and feedback components have been resistors. If the feedback component used is a capacitor, as shown in Fig. 10.38a, the resulting connection is called an *integrator*. The virtual-ground equivalent circuit (Fig. 10.38b) shows that an expression for the voltage between input and output can be derived in terms of the current I from input to output. Recall that virtual ground means that we can consider the voltage at the junction of R and X_C to be ground (since $V_i \approx 0 \text{ V}$) but that no current goes into ground at that point. The capacitive impedance can be expressed as

$$X_C = \frac{1}{j\omega C} = \frac{1}{sC}$$

where $s = j\omega$ is in the Laplace notation.* Solving for V_o/V_1 yields

$$I = \frac{V_1}{R} = -\frac{V_o}{X_C} = \frac{-V_o}{1/sC} = -sCV_o$$

*Laplace notation allows expressing differential or integral operations, which are part of calculus, in algebraic form using the operator s . Readers unfamiliar with calculus should ignore the steps leading to Eq. (10.13) and follow the physical meaning used thereafter.

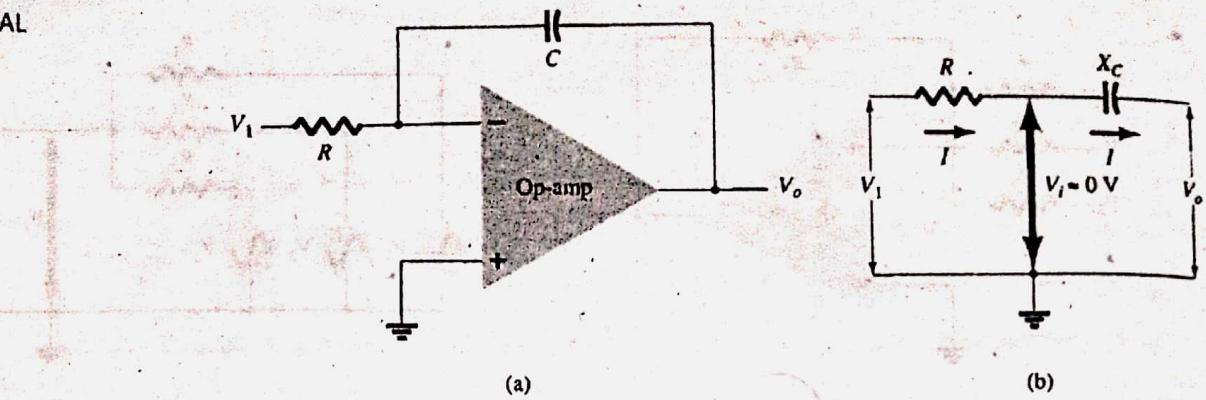


FIG. 10.38

Integrator.

$$\frac{V_o}{V_1} = \frac{-1}{sCR} \quad (10.12)$$

This expression can be rewritten in the time domain as

$$v_o(t) = -\frac{1}{RC} \int v_1(t) dt \quad (10.13)$$

Equation (10.13) shows that the output is the integral of the input, with an inversion and scale multiplier of $1/RC$. The ability to integrate a given signal provides the analog computer with the ability to solve differential equations and therefore provides the ability to electrically solve analogs of physical system operation.

The integration operation is one of summation, summing the area under a waveform or a curve over a period of time. If a fixed voltage is applied as input to an integrator circuit, Eq. (10.13) shows that the output voltage grows over a period of time, providing a ramp voltage. Equation (10.13) can thus be understood to show that the output voltage ramp (for a fixed input voltage) is opposite in polarity to the input voltage and is multiplied by the factor $1/RC$. Although the circuit of Fig. 10.38 can operate on many varied types of input signals, the following examples will use only a fixed input voltage, resulting in a ramp output voltage.

As an example, consider an input voltage $V_1 = 1$ V to the integrator circuit of Fig. 10.39a. The scale factor of $1/RC$ is

$$\frac{1}{RC} = \frac{1}{(1 \text{ M}\Omega)(1 \mu\text{F})} = -1$$

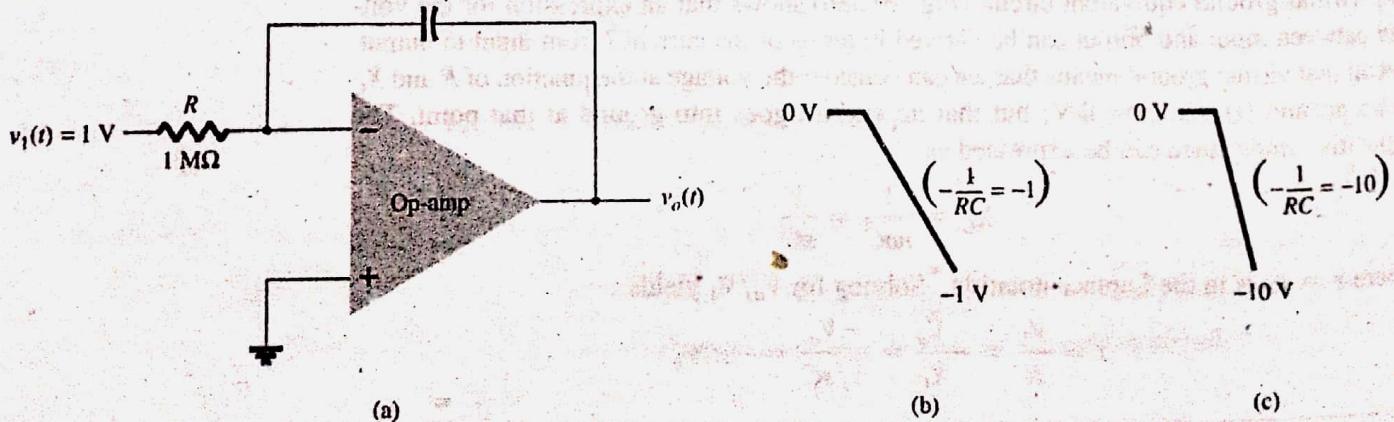


FIG. 10.39
Operation of integrator with step input.

so that the output is a negative ramp voltage as shown in Fig. 10.39b. If the scale factor is changed by making $R = 100 \text{ k}\Omega$, for example, then

$$-\frac{1}{RC} = \frac{1}{(100 \text{ k}\Omega)(1 \mu\text{F})} = -10$$

and the output is then a steeper ramp voltage, as shown in Fig. 10.39c.

More than one input may be applied to an integrator, as shown in Fig. 10.40, with the resulting operation given by

$$v_o(t) = -\left[\frac{1}{R_1C} \int v_1(t) dt + \frac{1}{R_2C} \int v_2(t) dt + \frac{1}{R_3C} \int v_3(t) dt \right] \quad (10.14)$$

An example of a summing integrator as used in an analog computer is given in Fig. 10.40. The actual circuit is shown with input resistors and feedback capacitor, whereas the analog-computer representation indicates only the scale factor for each input.

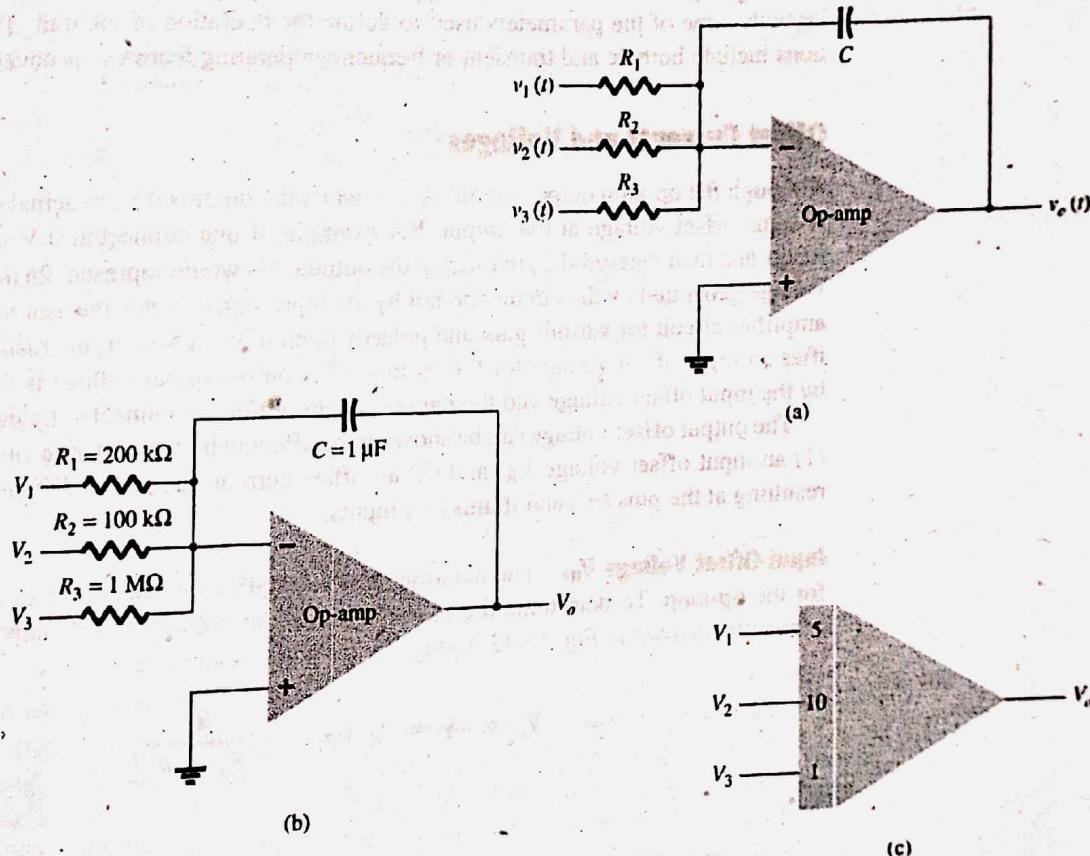


FIG. 10.40

(a) Summing-integrator circuit; (b) component values; (c) analog-computer, integrator-circuit representation.

Differentiator

A differentiator circuit is shown in Fig. 10.41. Although it is not as useful as the circuit forms covered above, the differentiator does provide a useful operation, the resulting relation for the circuit being

$$v_o(t) = -RC \frac{dv_1(t)}{dt} \quad (10.15)$$

where the scale factor is $-RC$.

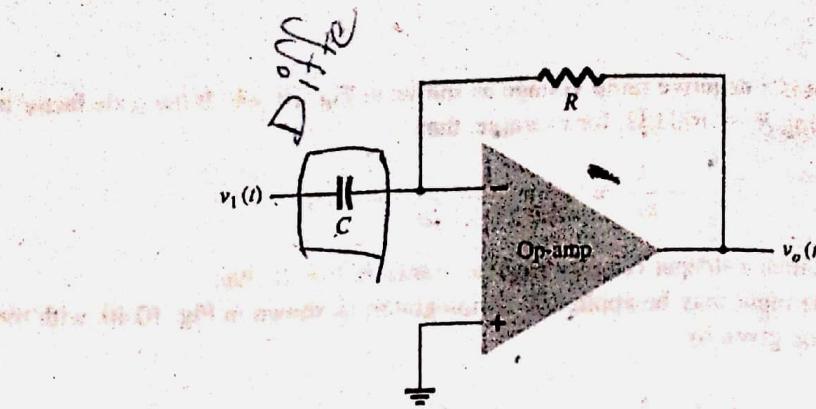


FIG. 10.41
Differentiator circuit.

10.6 OP-AMP SPECIFICATIONS—DC OFFSET PARAMETERS

Before going into various practical applications using op-amps, we should become familiar with some of the parameters used to define the operation of the unit. These specifications include both dc and transient or frequency operating features, as covered next.

Offset Currents and Voltages

Although the op-amp output should be 0 V when the input is 0 V, in actual operation there is some offset voltage at the output. For example, if one connected 0 V to both op-amp inputs and then measured 26 mV(dc) at the output, this would represent 26 mV of unwanted voltage generated by the circuit and not by the input signal. Since the user may connect the amplifier circuit for various gain and polarity operations, however, the manufacturer specifies an input offset voltage for the op-amp. The output offset voltage is then determined by the input offset voltage and the gain of the amplifier, as connected by the user.

The output offset voltage can be shown to be affected by two separate circuit conditions: (1) an input offset voltage V_{IO} and (2) an offset current due to the difference in currents resulting at the plus (+) and minus (-) inputs.

Input Offset Voltage V_{IO} The manufacturer's specification sheet provides a value of V_{IO} for the op-amp. To determine the effect of this input voltage on the output, consider the connection shown in Fig. 10.42. Using $V_o = AV_i$, we can write:

$$V_o = AV_i = A \left(V_{IO} - V_o \frac{R_1}{R_1 + R_f} \right)$$

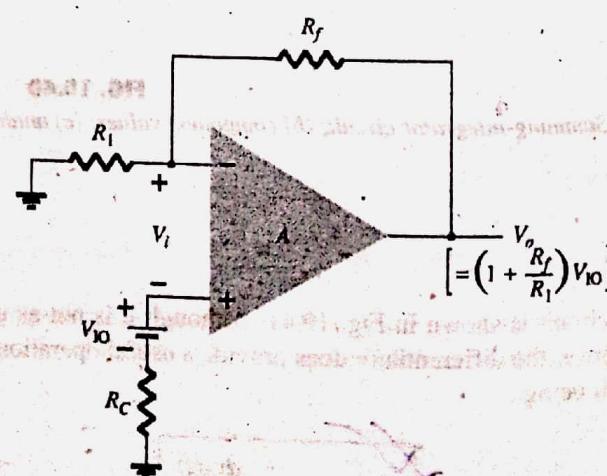


FIG. 10.42
Operation showing effect of input offset voltage V_{IO} .

Solving for V_o , we get

$$V_o = V_{IO} \frac{A}{1 + A[R_1/(R_1 + R_f)]} \approx V_{IO} \frac{A}{A[R_1/(R_1 + R_f)]}$$

from which we can write

$$V_o(\text{offset}) = V_{IO} \frac{R_1 + R_f}{R_1} \quad (10.16)$$

Equation (10.16) shows how the output offset voltage results from a specified input offset voltage for a typical amplifier connection of the op-amp.

EXAMPLE 10.8 Calculate the output offset voltage of the circuit in Fig. 10.43. The op-amp spec lists $V_{IO} = 1.2 \text{ mV}$.

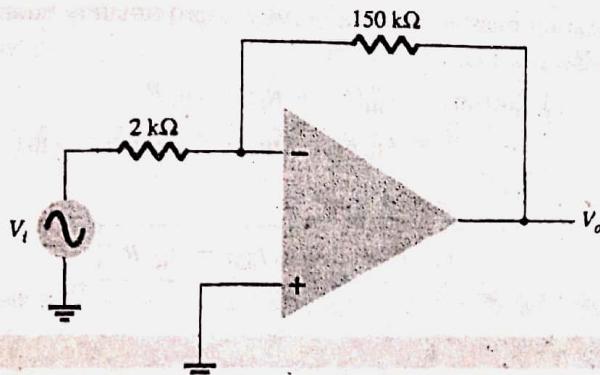


FIG. 10.43

Op-amp connection for Examples 10.8 and 10.9.

Solution:

$$\text{Eq. (10.16): } V_o(\text{offset}) = V_{IO} \frac{R_1 + R_f}{R_1} = (1.2 \text{ mV}) \left(\frac{2 \text{ k}\Omega + 150 \text{ k}\Omega}{2 \text{ k}\Omega} \right) = 91.2 \text{ mV}$$

Output Offset Voltage Due to Input Offset Current I_{IO} An output offset voltage will also result due to any difference in dc bias currents at both inputs. Since the two input transistors are never exactly matched, each will operate at a slightly different current. For a typical op-amp connection, such as that shown in Fig. 10.44, an output offset voltage can be determined as follows. Replacing the bias currents through the input resistors by the voltage drop that each develops as shown in Fig. 10.45, we can determine the expression for

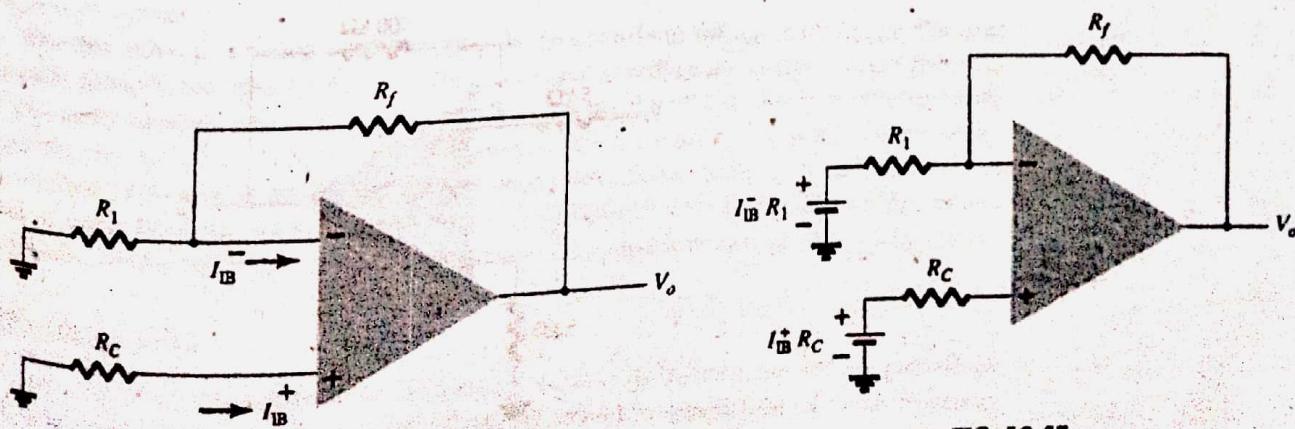


FIG. 10.44

Op-amp connection showing input bias currents.

FIG. 10.45

Redrawn circuit of Fig. 10.44.

the resulting output voltage. Using superposition, we see that the output voltage due to input bias current I_{IB}^+ , denoted by V_o^+ , is given by

$$V_o^+ = I_{IB}^+ R_C \left(1 + \frac{R_f}{R_1} \right)$$

whereas the output voltage due to only I_{IB}^- , denoted by V_o^- , is given by

$$V_o^- = I_{IB}^- R_1 \left(-\frac{R_f}{R_1} \right)$$

for a total output offset voltage of

$$V_o(\text{offset due to } I_{IB}^+ \text{ and } I_{IB}^-) = I_{IB}^+ R_C \left(1 + \frac{R_f}{R_1} \right) - I_{IB}^- R_1 \frac{R_f}{R_1} \quad (10.17)$$

Since the main consideration is the difference between the input bias currents rather than each value, we define the offset current I_{IO} by

$$I_{IO} = I_{IB}^+ - I_{IB}^-$$

Since the compensating resistance R_C is usually approximately equal to the value of R_1 , using $R_C = R_1$ in Eq. (10.17), we can write

$$\begin{aligned} V_o(\text{offset}) &= I_{IB}^+ (R_1 + R_f) - I_{IB}^- R_f \\ &= I_{IB}^+ R_f - I_{IB}^- R_f = R_f (I_{IB}^+ - I_{IB}^-) \end{aligned}$$

resulting in

$$V_o(\text{offset due to } I_{IO}) = I_{IO} R_f \quad (10.18)$$

EXAMPLE 10.9 Calculate the offset voltage for the circuit of Fig. 10.43 for op-amp specification listing $I_{IO} = 100 \text{ nA}$.

Solution: Eq. (10.18): $V_o = I_{IO} R_f = (100 \text{ nA})(150 \text{ k}\Omega) = 15 \text{ mV}$

Total Offset Due to V_{IO} and I_{IO} Since the op-amp output may have an output offset voltage due to both factors covered above, the total output offset voltage can be expressed as

$$|V_o(\text{offset})| = |V_o(\text{offset due to } V_{IO})| + |V_o(\text{offset due to } I_{IO})| \quad (10.19)$$

The absolute magnitude is used to accommodate the fact that the offset polarity may be either positive or negative.

EXAMPLE 10.10 Calculate the total offset voltage for the circuit of Fig. 10.46 for an op-amp with specified values of input offset voltage $V_{IO} = 4 \text{ mV}$ and input offset current $I_{IO} = 150 \text{ nA}$.

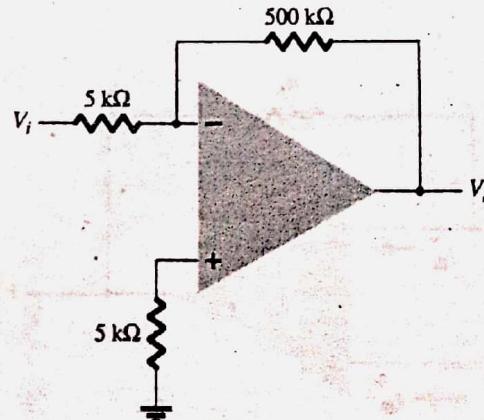


FIG. 10.46
Op-amp circuit for Example 10.10.

Solution: The offset due to V_{IO} is

$$\text{Eq. (10.16): } V_o(\text{offset due to } V_{IO}) = V_{IO} \frac{R_1 + R_f}{R_1} = (4 \text{ mV}) \left(\frac{5 \text{ k}\Omega + 500 \text{ k}\Omega}{5 \text{ k}\Omega} \right) \\ = 404 \text{ mV}$$

Eq. (10.18): $V_o(\text{offset due to } I_{IO}) = I_{IO}R_f = (150 \text{ nA})(500 \text{ k}\Omega) = 75 \text{ mV}$
resulting in a total offset

$$\text{Eq. (10.19): } V_o(\text{total offset}) = V_o(\text{offset due to } V_{IO}) + V_o(\text{offset due to } I_{IO}) \\ = 404 \text{ mV} + 75 \text{ mV} = 479 \text{ mV}$$

Input Bias Current, I_{IB} A parameter related to I_{IO} and the separate input bias currents I_{IB}^+ and I_{IB}^- is the average bias current defined as

$$I_{IB} = \frac{I_{IB}^+ + I_{IB}^-}{2} \quad (10.20)$$

One could determine the separate input bias currents using the specified values I_{IO} and I_{IB} . It can be shown that for $I_{IB}^+ > I_{IB}^-$

$$I_{IB}^+ = I_{IB} + \frac{I_{IO}}{2} \quad (10.21)$$

$$I_{IB}^- = I_{IB} - \frac{I_{IO}}{2} \quad (10.22)$$

EXAMPLE 10.11 Calculate the input bias currents at each input of an op-amp having specified values of $I_{IO} = 5 \text{ nA}$ and $I_{IB} = 30 \text{ nA}$.

Solution: Using Eq. (10.21), we obtain

$$I_{IB}^+ = I_{IB} + \frac{I_{IO}}{2} = 30 \text{ nA} + \frac{5 \text{ nA}}{2} = 32.5 \text{ nA}$$

$$I_{IB}^- = I_{IB} - \frac{I_{IO}}{2} = 30 \text{ nA} - \frac{5 \text{ nA}}{2} = 27.5 \text{ nA}$$

10.7 OP-AMP SPECIFICATIONS—

value of 1 (unity). The frequency at which the gain becomes 1 is called the unity-gain bandwidth, B_1 . Although this value is a frequency (see Fig. 10.47) at which the gain becomes 1, it can be considered a bandwidth, since the frequency band from 0 Hz to the unity-gain frequency is also a bandwidth. One could therefore refer to the point at which the gain reduces to 1 as the unity-gain frequency (f_1) or unity-gain bandwidth (B_1).

Another frequency of interest, as shown in Fig. 10.47, is that at which the gain drops by 3 dB (or to 0.707 the dc gain, A_{VD}), this being the cutoff frequency of the op-amp, f_C . In fact, the unity-gain frequency and cutoff frequency are related by

$$f_1 = A_{VD} f_C \quad (10.23)$$

Equation (10.23) shows that the unity-gain frequency may also be called the gain-bandwidth product of the op-amp.

EXAMPLE 10.12 Determine the cutoff frequency of an op-amp having specified values $B_1 = 1 \text{ MHz}$ and $A_{VD} = 200 \text{ V/mV}$.

Solution: Since $f_1 = B_1 = 1 \text{ MHz}$, we can use Eq. (10.23) to calculate

$$f_C = \frac{f_1}{A_{VD}} = \frac{1 \text{ MHz}}{200 \text{ V/mV}} = \frac{1 \times 10^6}{200 \times 10^3} = 5 \text{ Hz}$$

Slew Rate (SR)

Another parameter reflecting the op-amp's ability to handle varying signals is the slew rate, defined as

Slew rate = maximum rate at which amplifier output can change in volts per microsecond (V/ μ s)

$$SR = \frac{\Delta V_o}{\Delta t} \text{ V}/\mu\text{s} \quad \text{with } t \text{ in } \mu\text{s} \quad (10.24)$$

The slew rate provides a parameter specifying the maximum rate of change of the output voltage when driven by a large step-input signal.* If one tried to drive the output at a rate

*The closed-loop gain is that obtained with the output connected back to the input in some way.

50 mW but could go as high as 85 mW. Referring to the previous parameter, we see that the op-amp will dissipate about 50 mW when drawing about 1.7 mA using a 15-V supply. At smaller supply voltages, the current drawn will be less and the total power dissipated will also be less.

EXAMPLE 10.16 Using the specifications listed in Table 10.3, calculate the typical output offset voltage for the circuit connection of Fig. 10.50.

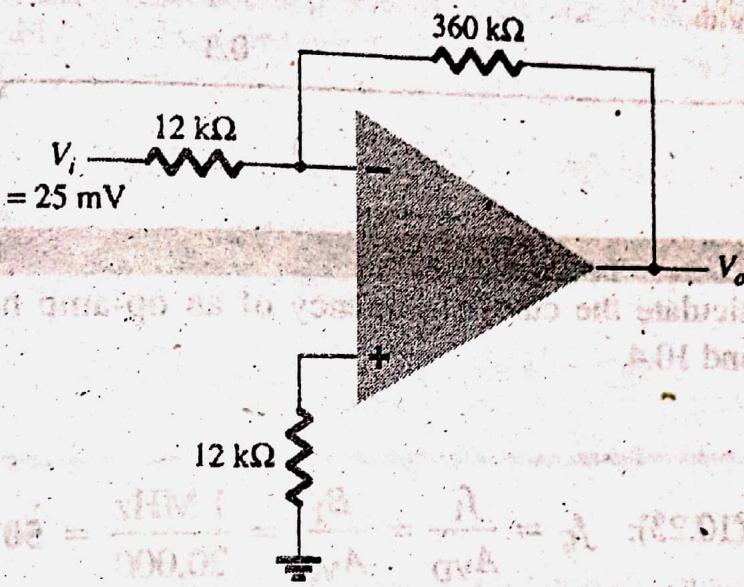


FIG. 10.50

Op-amp circuit for Examples 10.16, 10.17, and 10.19.

Solution: The output offset due to V_{IO} is calculated to be

$$\text{Eq. (10.16): } V_o(\text{offset}) = V_{IO} \frac{R_1 + R_f}{R_1} = (1 \text{ mV}) \left(\frac{12 \text{ k}\Omega + 360 \text{ k}\Omega}{12 \text{ k}\Omega} \right) = 31 \text{ mV}$$

The output voltage due to I_{IO} is calculated to be

$$\text{Eq. (10.18): } V_o(\text{offset}) = I_{IO} R_f = 20 \text{ nA} (360 \text{ k}\Omega) = 7.2 \text{ mV}$$

Assuming that these two offsets are the same polarity at the output, we obtain for the total output offset voltage

$$V_o(\text{offset}) = 31 \text{ mV} + 7.2 \text{ mV} = 38.2 \text{ mV}$$

EXAMPLE 10.17 Explain the electrical characteristics of the 741 op-amp ($r_d = 75 \Omega$, $A = 200 \text{ k}\Omega$).

Under these conditions the output voltage is $V_o = A_d V_d + A_c V_c = A_d(0\text{ V}) + A_c(1\text{ V}) = A_c$

Eq. (10.28): $V_o = A_d V_d + A_c V_c = A_d(0\text{ V}) + A_c(1\text{ V}) = A_c$
Thus, setting the input voltages $V_{i_1} = V_{i_2} = 1\text{ V}$ results in an output voltage numerically equal to the value of A_c .

Common-Mode Rejection Ratio

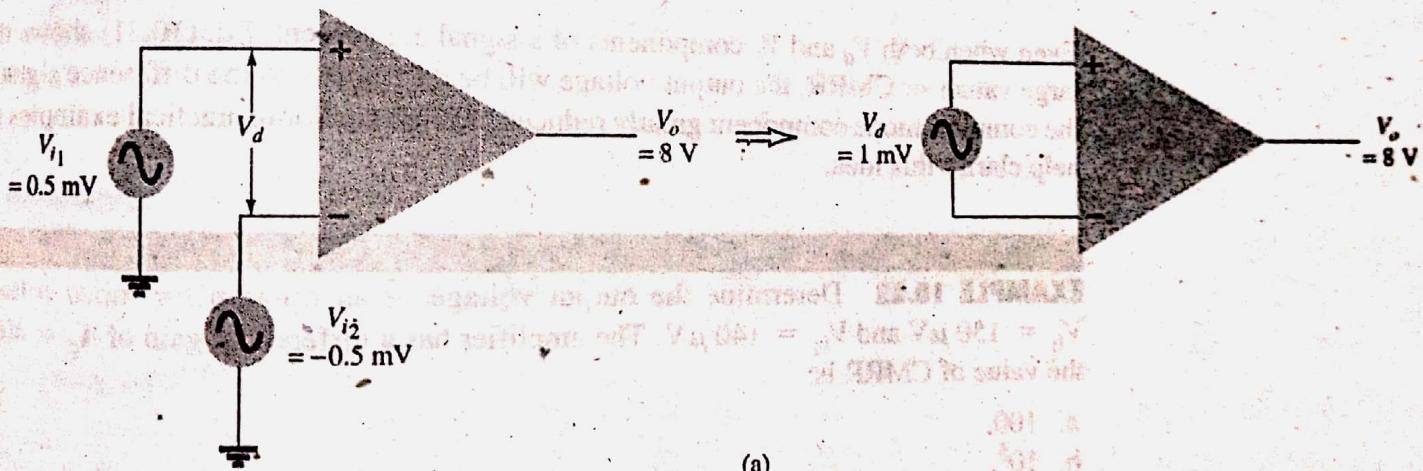
Having obtained A_d and A_c (as in the measurement procedure discussed above), we can now calculate a value for the common-mode rejection ratio (CMRR), which is defined by the following equation:

$$\text{CMRR} = \frac{A_d}{A_c} \quad (10.29)$$

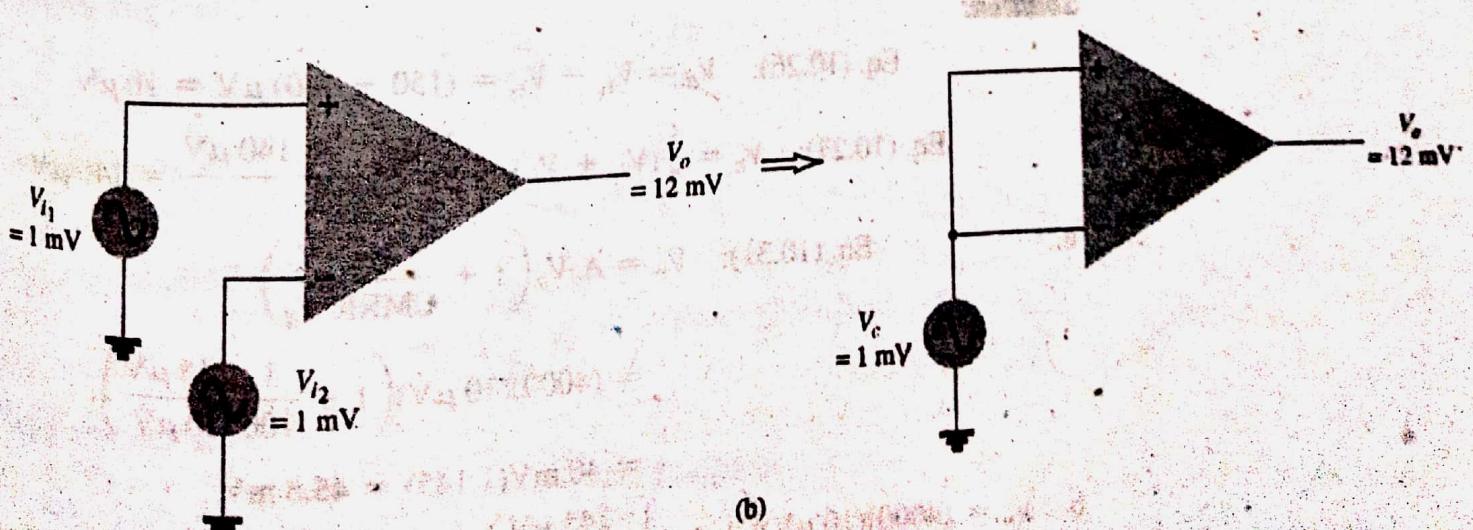
The value of CMRR can also be expressed in logarithmic terms as

$$\text{CMRR} (\log) = 20 \log_{10} \frac{A_d}{A_c} \text{ (dB)} \quad (10.30)$$

EXAMPLE 10.21 Calculate the CMRR for the circuit measurements shown in Fig. 10.52.



(a)



(b)

FIG. 10.52
(a) Differential and (b) common-mode operation.

Solution: From the measurement shown in Fig. 10.52a, using the procedure in step 1 above, we obtain

$$A_d = \frac{V_o}{V_d} = \frac{8 \text{ V}}{1 \text{ mV}} = 8000$$

The measurement shown in Fig. 10.52b, using the procedure in step 2 above, gives us

$$A_c = \frac{V_o}{V_c} = \frac{12 \text{ mV}}{1 \text{ mV}} = 12$$

Using Eq. (10.28), we obtain the value of CMRR,

$$\text{CMRR} = \frac{A_d}{A_c} = \frac{8000}{12} = 666.7$$

which can also be expressed as

$$\text{CMRR} = 20 \log_{10} \frac{A_d}{A_c} = 20 \log_{10} 666.7 = 56.48 \text{ dB}$$

It should be clear that the desired operation will have A_d very large with A_c very small. That is, the signal components of opposite polarity will appear greatly amplified at the output, whereas the signal components that are in phase will mostly cancel out so that the common-mode gain A_c is very small. Ideally, the value of the CMRR is infinite. Practically, the larger the value of CMRR, the better is the circuit operation.

We can express the output voltage in terms of the value of CMRR as follows:

$$\text{Eq. (12.22): } V_o = A_d V_d + A_c V_c = A_d V_d \left(1 + \frac{A_c V_c}{A_d V_d} \right)$$

Using Eq. (12.24), we can write the above as

$$V_o = A_d V_d \left(1 + \frac{1}{\text{CMRR}} \frac{V_c}{V_d} \right) \quad (10.31)$$

Even when both V_d and V_c components of a signal are present, Eq. (10.31) shows that for large values of CMRR, the output voltage will be due mostly to the difference signal, with the common-mode component greatly reduced or rejected. Some practical examples should help clarify this idea.

EXAMPLE 10.22 Determine the output voltage of an op-amp for input voltages of $V_{i_1} = 150 \mu\text{V}$ and $V_{i_2} = 140 \mu\text{V}$. The amplifier has a differential gain of $A_d = 4000$ and the value of CMRR is:

- a. 100.
- b. 10^5 .

Solution:

$$\text{Eq. (10.26): } V_d = V_{i_1} - V_{i_2} = (150 - 140) \mu\text{V} = 10 \mu\text{V}$$

$$\text{Eq. (10.27): } V_c = \frac{1}{2}(V_{i_1} + V_{i_2}) = \frac{150 \mu\text{V} + 140 \mu\text{V}}{2} = 145 \mu\text{V}$$

a.

$$\text{Eq. (10.31): } V_o = A_d V_d \left(1 + \frac{1}{\text{CMRR}} \frac{V_c}{V_d} \right)$$

$$= (4000)(10 \mu\text{V}) \left(1 + \frac{1}{100} \frac{145 \mu\text{V}}{10 \mu\text{V}} \right)$$

$$= 40 \text{ mV}(1.145) = 45.8 \text{ mV}$$

$$\text{b. } V_o = (4000)(10 \mu\text{V}) \left(1 + \frac{1}{10^5} \frac{145 \mu\text{V}}{10 \mu\text{V}} \right) = 40 \text{ mV}(1.000145) = 40.006 \text{ mV}$$

Example 10.22 shows that the larger the value of CMRR, the closer is the output voltage to the difference input times the difference gain with the common-mode signal being rejected.

SUMMARY

10.10 SUMMARY

Important Conclusions and Concepts

1. Differential operation involves the use of opposite-polarity inputs.
2. Common-mode operation involves the use of the same-polarity inputs.
3. Common-mode rejection compares the gain for differential inputs to that for common inputs.
4. An op-amp is an operational amplifier.
5. The basic features of an op-amp are:
 - Very high input impedance (typically megohms)
 - Very high voltage gain (typically a few hundred thousand and greater)
 - Low output impedance (typically less than $100\ \Omega$)
6. Virtual ground is a concept based on the practical fact that the differential input voltage between plus (+) and minus (-) inputs is nearly (virtually) 0 V—when calculated as the output voltage (at most, that of the voltage supply) divided by the very high voltage gain of the op-amp.
7. Basic op-amp connections include:
 - Inverting amplifier
 - Noninverting amplifier
 - Unity-gain amplifier
 - Summing amplifier
 - Integrator amplifier
8. Op-amp specs include:
 - Offset voltages and currents
 - Frequency parameters
 - Gain-bandwidth
 - Slew rate

Equations

$$\text{CMRR} = 20 \log_{10} \frac{A_d}{A_c}$$

Inverting amplifier:

$$\frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

Noninverting amplifier:

$$\frac{V_o}{V_i} = 1 + \frac{R_f}{R_1}$$

Unity follower:

$$V_o = V_i$$

Summing amplifier:

$$V_o = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right)$$

Integrator amplifier:

$$v_o(t) = -\frac{1}{RC} \int v_i(t) dt$$

$$\text{Slew rate (SR)} = \frac{\Delta V_o}{\Delta t} \quad \text{V}/\mu\text{s}$$

EXAMPLE 11.1 Determine the output voltage for the circuit of Fig. 11.2 with a sinusoidal input of 2.5 mV.

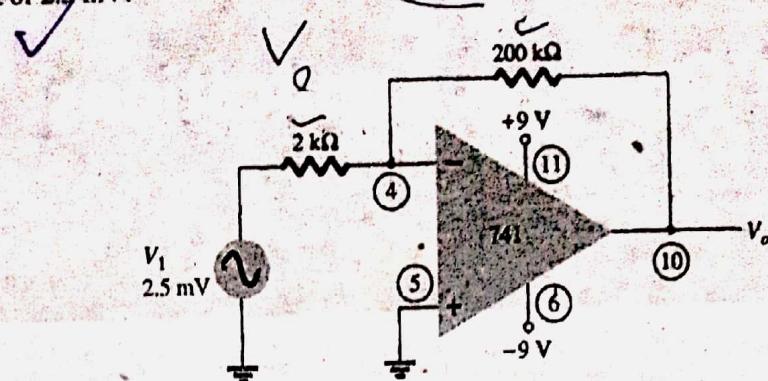


FIG. 11.2
Circuit for Example 11.1.

Solution: The circuit of Fig. 11.2 uses a 741 op-amp to provide a constant or fixed gain, calculated from Eq. (11.1) to be

$$A = -\frac{R_f}{R_1} = -\frac{200 \text{ k}\Omega}{2 \text{ k}\Omega} = -100$$

The output voltage is then

$$V_o = AV_i = -100(2.5 \text{ mV}) = -250 \text{ mV} = -0.25 \text{ V}$$

A noninverting constant-gain multiplier is provided by the circuit of Fig. 11.3, with the gain given by

$$A = 1 + \frac{R_f}{R_1} \quad (11.2)$$

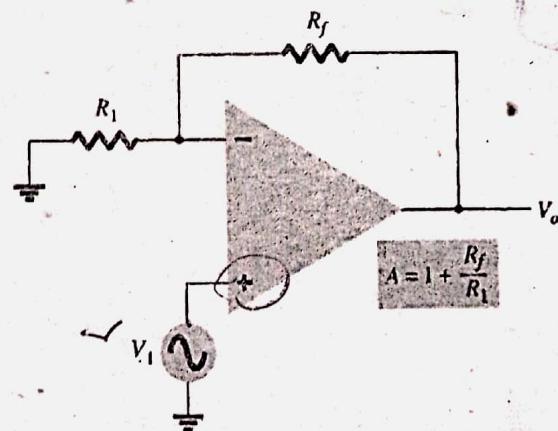


FIG. 11.3
Noninverting fixed-gain amplifier.

EXAMPLE 11.2 Calculate the output voltage from the circuit of Fig. 11.4 for an input of 120 μV.

Solution: The gain of the op-amp circuit is calculated using Eq. (11.2) to be

$$A = 1 + \frac{R_f}{R_1} = 1 + \frac{240 \text{ k}\Omega}{2.4 \text{ k}\Omega} = 1 + 100 = 101$$

The output voltage is then

$$V_o = AV_i = 101(120 \mu\text{V}) = 12.12 \text{ mV}$$

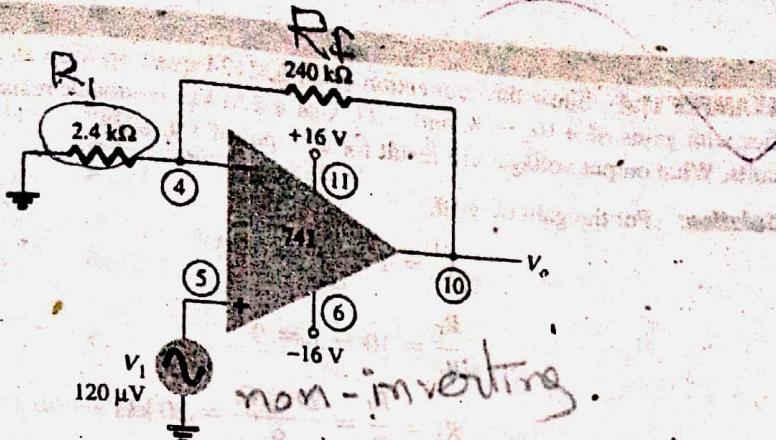


FIG. 11.4
Circuit for Example 11.2.

Multiple-Stage Gains

When a number of stages are connected in series, the overall gain is the product of the individual stage gains. Figure 11.5 shows a connection of three stages. The first stage is connected to provide noninverting gain as given by Eq. (11.1). The next two stages provide an inverting gain given by Eq. (11.1). The overall circuit gain is then noninverting and is calculated by

$$A = A_1 A_2 A_3$$

where $A_1 = 1 + R_f/R_1$, $A_2 = -R_f/R_2$, and $A_3 = -R_f/R_3$.

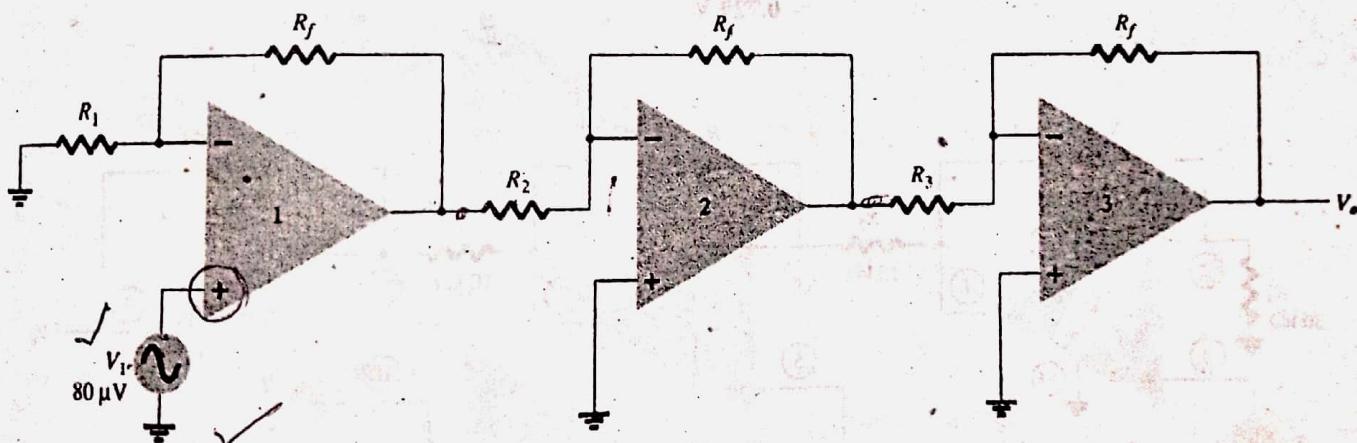


FIG. 11.5
Constant-gain connection with multiple stages.

EXAMPLE 11.3 Calculate the output voltage using the circuit of Fig. 11.5 for resistor components of value $R_f = 470 \text{ k}\Omega$, $R_1 = 4.3 \text{ k}\Omega$, $R_2 = 33 \text{ k}\Omega$, and $R_3 = 33 \text{ k}\Omega$ for an input of $80 \mu\text{V}$.

Solution: The amplifier gain is calculated to be

$$\begin{aligned} A &= A_1 A_2 A_3 = \left(1 + \frac{R_f}{R_1}\right) \left(-\frac{R_f}{R_2}\right) \left(-\frac{R_f}{R_3}\right) \\ &= \left(1 + \frac{470 \text{ k}\Omega}{4.3 \text{ k}\Omega}\right) \left(\frac{470 \text{ k}\Omega}{33 \text{ k}\Omega}\right) \left(\frac{470 \text{ k}\Omega}{33 \text{ k}\Omega}\right) \\ &= (110.3)(-14.2)(-14.2) = 22.2 \times 10^3 \end{aligned}$$

$$V_o = AV_i = 22.2 \times 10^3 (80 \mu\text{V}) = 1.78 \text{ V}$$

EXAMPLE 11.4 Show the connection of an LM124 quad op-amp as a three-stage amplifier with gains of +10, -18, and -27. Use a 270-k Ω feedback resistor for all three circuits. What output voltage will result for an input of 150 μ V?

Solution: For the gain of +10,

$$A_1 = 1 + \frac{R_f}{R_1} = +10$$

$$\frac{R_f}{R_1} = 10 - 1 = 9$$

$$R_1 = \frac{R_f}{9} = \frac{270 \text{ k}\Omega}{9} = 30 \text{ k}\Omega$$

For the gain of -18,

$$A_2 = -\frac{R_f}{R_2} = -18$$

$$R_2 = \frac{R_f}{18} = \frac{270 \text{ k}\Omega}{18} = 15 \text{ k}\Omega$$

For the gain of -27,

$$A_3 = -\frac{R_f}{R_3} = -27$$

$$R_3 = \frac{R_f}{27} = \frac{270 \text{ k}\Omega}{27} = 10 \text{ k}\Omega$$

The circuit showing the pin connections and all components used is given in Fig. 11.6. For an input of $V_1 = 150 \mu\text{V}$, the output voltage is

$$V_o = A_1 A_2 A_3 V_1 = (10)(-18)(-27)(150 \mu\text{V}) = 4860(150 \mu\text{V}) \\ = 0.729 \text{ V}$$

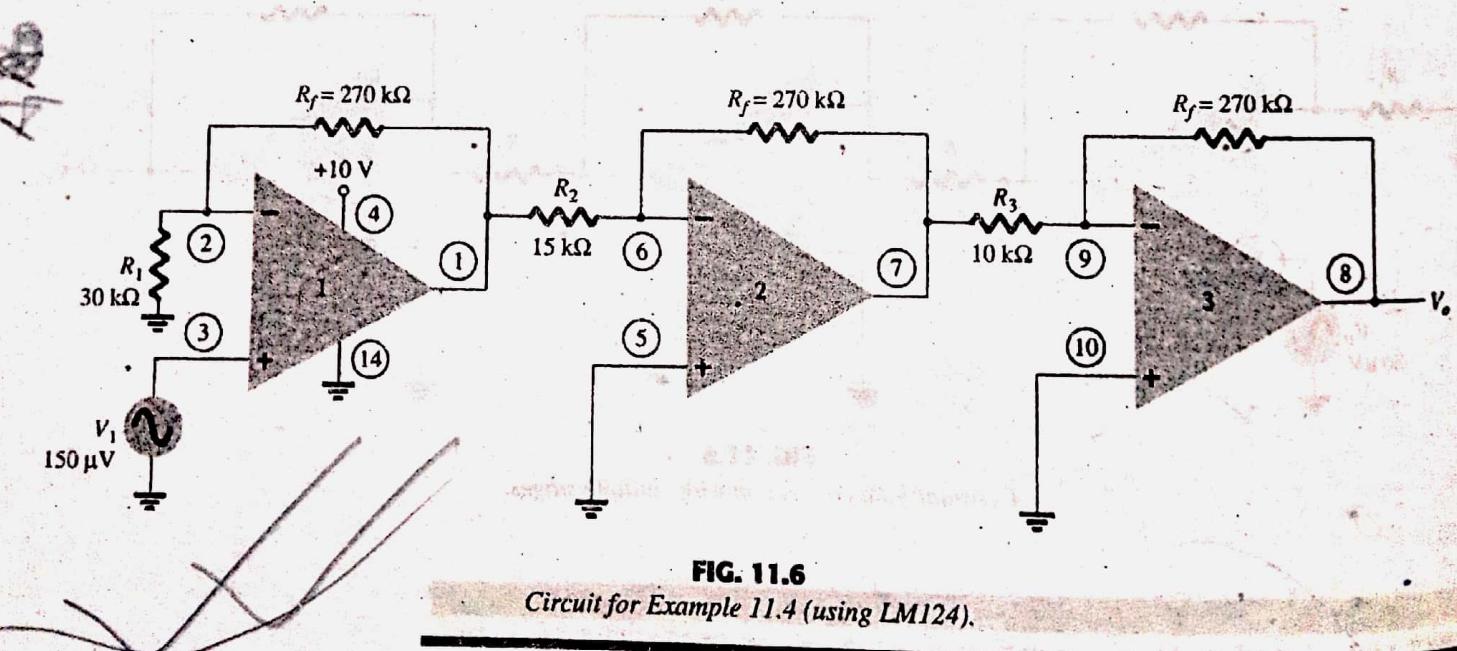


FIG. 11.6
Circuit for Example 11.4 (using LM124).

A number of op-amp stages could also be used to provide separate gains, as demonstrated in the next example.

EXAMPLE 11.5 Show the connection of three op-amp stages using an LM348 IC to provide outputs that are 10, 20, and 50 times larger than the input. Use a feedback resistor of $R_f = 500 \text{ k}\Omega$ in all stages.

Solution: The resistor component for each stage is calculated to be

$$R_1 = -\frac{R_f}{A_1} = -\frac{500 \text{ k}\Omega}{-10} = 50 \text{ k}\Omega$$

$$R_2 = -\frac{R_f}{A_2} = -\frac{500 \text{ k}\Omega}{-20} = 25 \text{ k}\Omega$$

$$R_3 = -\frac{R_f}{A_3} = -\frac{500 \text{ k}\Omega}{-50} = 10 \text{ k}\Omega$$

The resulting circuit is drawn in Fig. 11.7.

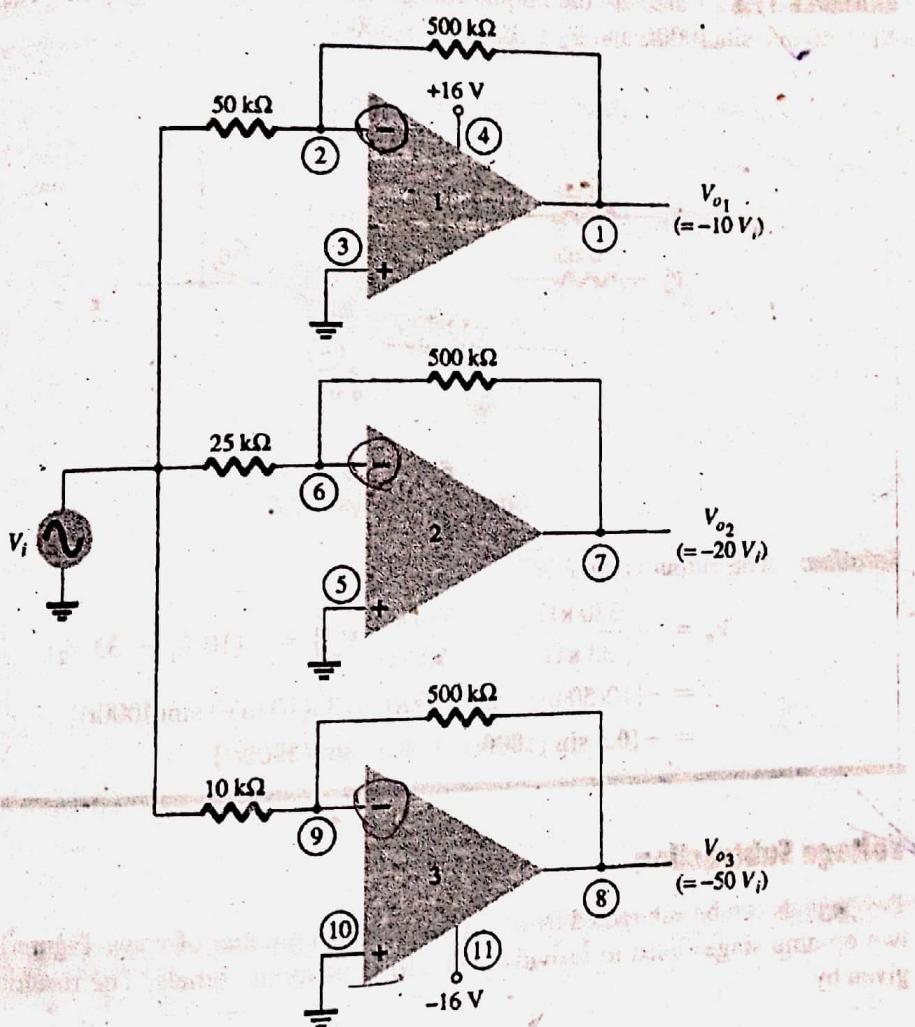


FIG. 11.7
Circuit for Example 11.5 (using LM348).

11.2 VOLTAGE SUMMING

Another popular use of an op-amp is as a summing amplifier. Figure 11.8 shows the connection, with the output being the sum of the three inputs, each multiplied by a different gain. The output voltage is

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right) \quad (11.3)$$

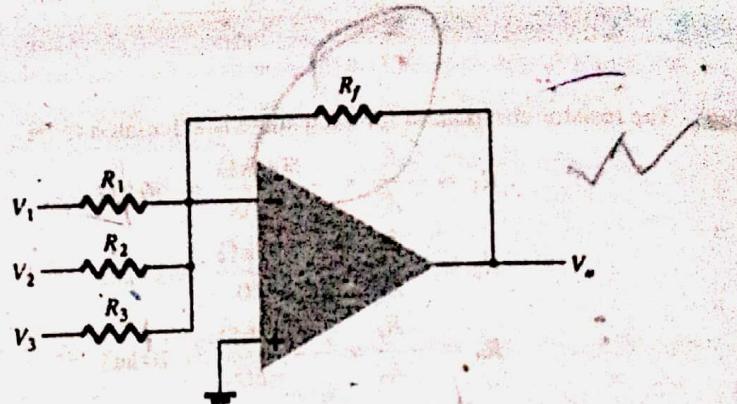


FIG. 11.8

Summing amplifier.

EXAMPLE 11.6 Calculate the output voltage for the circuit of Fig. 11.9. The inputs are $V_1 = 50 \text{ mV} \sin(1000t)$ and $V_2 = 10 \text{ mV} \sin(3000t)$.

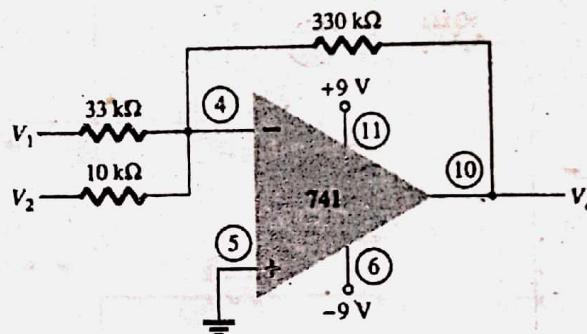


FIG. 11.9

Circuit for Example 11.6.

Solution: The output voltage is

$$\begin{aligned} V_o &= -\left(\frac{330 \text{ k}\Omega}{33 \text{ k}\Omega} V_1 + \frac{330 \text{ k}\Omega}{10 \text{ k}\Omega} V_2\right) = -(10 V_1 + 33 V_2) \\ &= -[10(50 \text{ mV} \sin(1000t)) + 33(10 \text{ mV} \sin(3000t))] \\ &= -[0.5 \sin(1000t) + 0.33 \sin(3000t)] \end{aligned}$$

Voltage Subtraction

Two signals can be subtracted from one another in a number of ways. Figure 11.10 shows two op-amp stages used to provide subtraction of input signals. The resulting output is given by

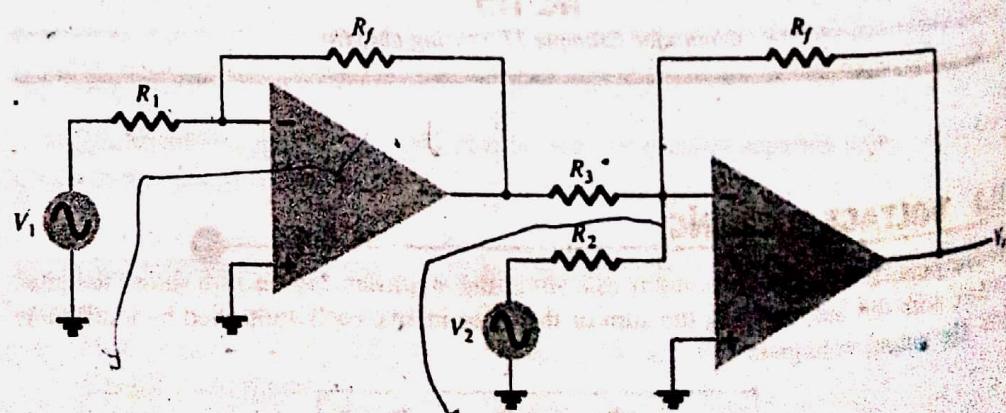


FIG. 11.10
Circuit for subtracting two signals.

$$V_o = -\left[\frac{R_f}{R_3} \left(\frac{R_f}{R_1} V_1 \right) + \frac{R_f}{R_2} V_2 \right]$$

$$V_o = -\left(\frac{R_f}{R_2} V_2 - \frac{R_f}{R_3} \frac{R_f}{R_1} V_1 \right)$$

(11.4)

EXAMPLE 11.7 Determine the output for the circuit of Fig. 11.10 with components $R_f = 1 \text{ M}\Omega$, $R_1 = 100 \text{ k}\Omega$, $R_2 = 50 \text{ k}\Omega$, and $R_3 = 500 \text{ k}\Omega$.

Solution: The output voltage is calculated to be

$$V_o = -\left(\frac{1 \text{ M}\Omega}{50 \text{ k}\Omega} V_2 - \frac{1 \text{ M}\Omega}{500 \text{ k}\Omega} \frac{1 \text{ M}\Omega}{100 \text{ k}\Omega} V_1 \right) = -(20 V_2 - 20 V_1) = -20(V_2 - V_1)$$

The output is seen to be the difference of V_2 and V_1 multiplied by a gain factor of -20 .

Another connection to provide subtraction of two signals is shown in Fig. 11.11. This connection uses only one op-amp stage to provide subtracting two input signals. Using superposition, we can show the output to be

$$V_o = \frac{R_3}{R_1 + R_3} \frac{R_2 + R_4}{R_2} V_1 - \frac{R_4}{R_2} V_2 \quad (11.5)$$

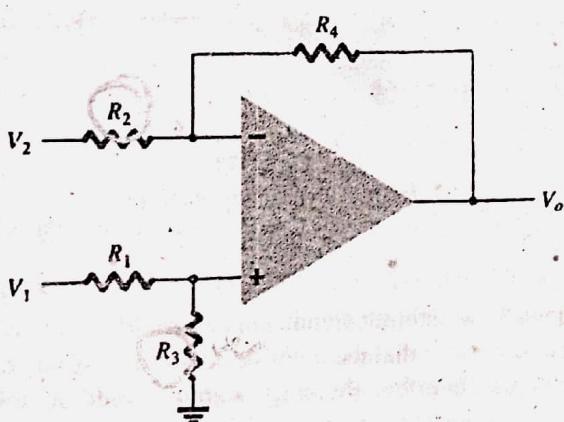


FIG. 11.11
Subtraction circuit.

EXAMPLE 11.8 Determine the output voltage for the circuit of Fig. 11.12.

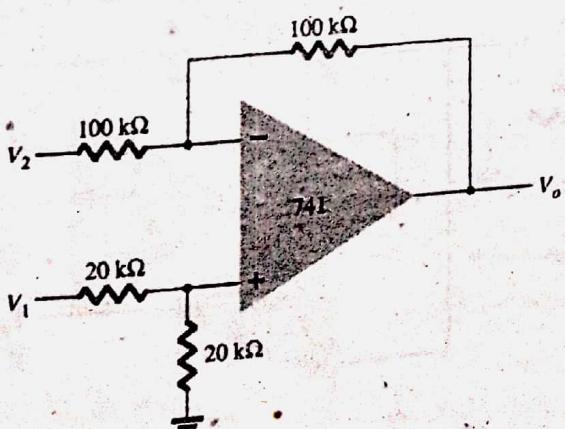


FIG. 11.12
Circuit for Example 11.8.

Solution: The resulting output voltage can be expressed as

$$\begin{aligned} V_o &= \left(\frac{20 \text{ k}\Omega}{20 \text{ k}\Omega + 20 \text{ k}\Omega} \right) \left(\frac{100 \text{ k}\Omega + 100 \text{ k}\Omega}{100 \text{ k}\Omega} \right) V_1 - \frac{100 \text{ k}\Omega}{100 \text{ k}\Omega} V_2 \\ &= V_1 - V_2 \end{aligned}$$

The resulting output voltage is seen to be the difference of the two input voltages.

11.3 VOLTAGE BUFFER

A voltage buffer circuit provides a means of isolating an input signal from a load by using a stage having unity voltage gain, with no phase or polarity inversion, and acting as an ideal circuit with very high input impedance and low output impedance. Figure 11.13 shows an op-amp connected to provide this buffer amplifier operation. The output voltage is determined by

$$V_o = V_1 \quad (11.6)$$

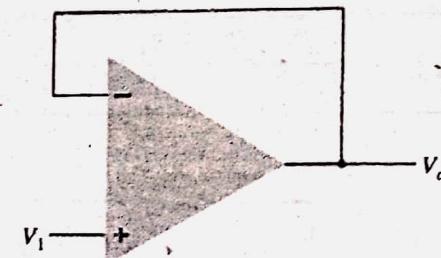


FIG. 11.13
Unity-gain (buffer) amplifier.

Figure 11.14 shows how an input signal can be provided to two separate outputs. The advantage of this connection is that the load connected across one output has no (or little) effect on the other output. In effect, the outputs are buffered or isolated from each other.

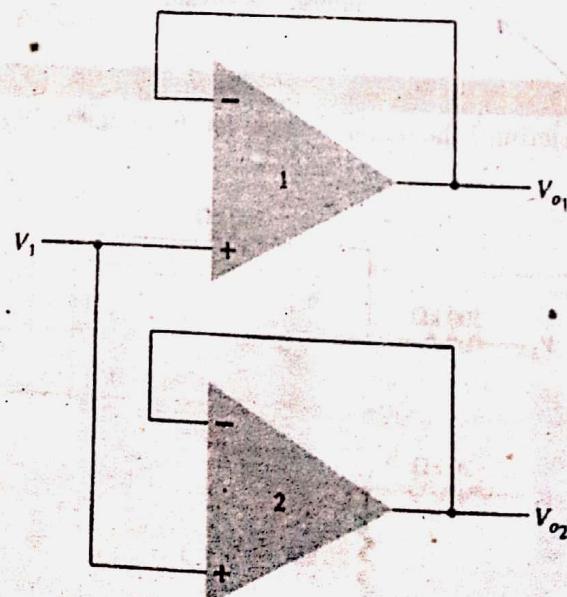


FIG. 11.14
Use of buffer amplifier to provide output signals.