# University of Rajshahi

**Department of Computer Science and Engineering**

B. Sc. (Engg) Part-II Odd Semester Examination 2020

Course: CSE-2111 (Digital System Design)

Full Marks: 52.5 Duration: 3 (Three) Hours

**Answer 06 (Six) questions taking any 03 (Three) questions from each part**

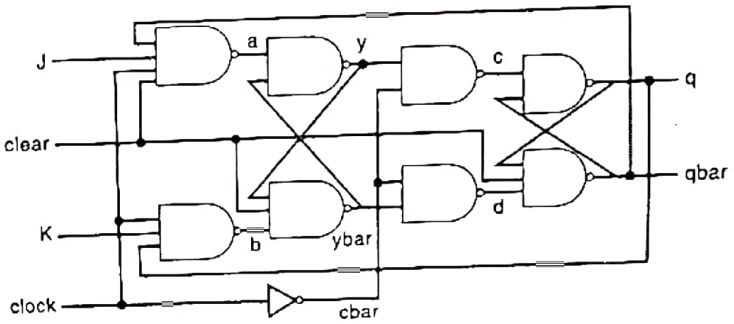
## Part-A

1. a) Why do we use binary number system instead of decimal number system in the digital devices? 1
   b) Represent $(93)_{10}$ and $(-93)_{10}$ as 8-bit i) Sign-Magnitude, ii) 1's complement, and iii) 2's Complement binary number. 2.75
   c) State the purpose of Hamming code for digital communication devices. Compute the data word with hamming code for the original binary data word $(10110010110)_2$. 5

2. a) Why NAND gate and NOR gate are called universal gate? Explain with necessary diagram. 3
   b) Prove i) $xy + \bar{x}z + yz = xy + \bar{x}z$ and ii) $\bar{x}\bar{y}\bar{z} + \bar{x}y\bar{z} + xy\bar{z} = \bar{x}\bar{z} + y\bar{z}$ using Boolean algebra properties. 3
   c) Simplify the Boolean function $F(A,B,C,D) = \sum(1,3,7,8,11,15)$ which has the don't care conditions: $d(A,B,C,D) = (0,2,5,9)$. 2.75

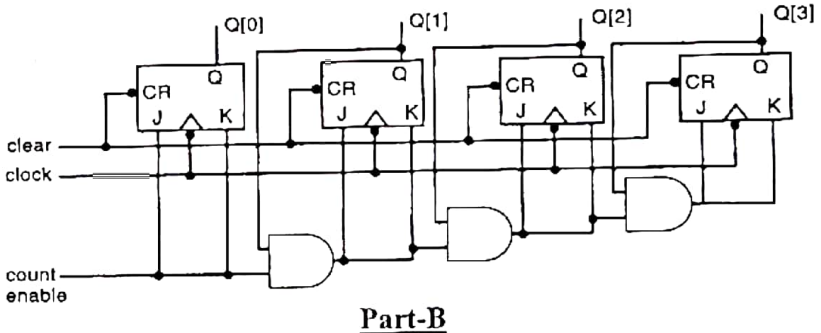
3. a) Write HDL codes for 2x2-bit combinational array multiplier. 3.75
   b) How to invoke a Verilog module from a VHDL module? Explain with an example of a mixed language description or a full adder using 2 half adders. 5

4.




The circuit diagram for the JK flip-flop is given above.

a) Implement the above circuit diagram of JK flip-flop as a Verilog HDL module. 4.75
b) Use the above JK flip-flop module to implement the following 4-bit synchronous counter. 4




## Part-B

5. a) Implement a full adder circuit using a 3-to-8 decoder. 2.5
   b) How decoder can be used as de-multiplexer? 2
   c) How could we implement an 8-to-1 multiplexer using 2-to-1 multiplexer. 2
   d) Distinguish between combinational and sequential logic circuit. 2.25

6. a) Compare between D latch and D flip-flop with timing diagram. 2.25
   b) Show the implementation of T flip-flop from D flip-flop. 2
   c) Show the circuit and timing diagram of a 4-bit bidirectional shift register. 4.5

7. a) What are advantages of synchronous counter over asynchronous counter? 2
   b) Design a 4 bit synchronous counter for counting the following binary sequence: 6.75
   $0000 \rightarrow 0101 \rightarrow 1010 \rightarrow 0110 \rightarrow 1001 \rightarrow 0011 \rightarrow 1100 \rightarrow 1111 \rightarrow 0000$

8. a) How does the binary counter work as a frequency divider? 2
   b) What is the frequency of the output of 8th FF when the input clock frequency is 512 KHz? 1.75
   c) What is full adder? Design a full adder circuit. 5

**University of Rajshahi**
**Department of Computer Science and Engineering**
**B.Sc. (Engg.) Part-2 (Odd Semester) Examination-2018**
**Course: CSE2111 (Digital System Design)**
**Marks: 52.50 Time: 3:00 Hours**

[N.B. Answer any **Six** questions taking **Three** from each section.]

## Section-A

1. a) Convert 01010010 (BCD) to Binary. You have a BCD number of two digit decimal values. Now, design a BCD-to-binary converter with 4-bit parallel adder. Draw the logic circuit and explain its operation. 5

   b) Design a BCD to Excess-3 code converter and draw its logic diagram. 3.75

2. a) Why carry-look-ahead adder is faster than regular adder – explain with diagram. 3

   b) Distinguish between 1's complement and 2's complement system. Why this circuits are necessary? 2.75

   c) Design a logic circuit that has four inputs, A B, C and D and whose output will be high only when a majority of inputs are high. 3

3. a) Define decoder and demultiplexer. How decoder can be used as a demultiplexer? 2.25

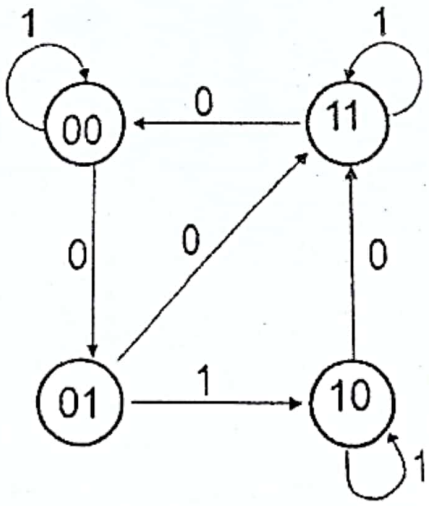
   b) Define Multiplexer. Implement the logic function $F(A,B,C,D) = \sum m(1,3,4,7,11,13,15)$ using 8x1 MUX. 4

   c) Implement the logic function $F(A,B,C) = \sum m(1,3,4,7)$ using a 3-to-8 line decoder with active low output. 2.5

4. a) What is parity bit? Implement a 4-bit even parity generator circuit and discuss the operation of the circuit with example. 2.75

   b) Define state table and state diagram with example. 2

   c) From the following state diagram, design the sequential circuit using JK flip-flops. 4



## Section -B

5. a) Define asynchronous and synchronous counter. Write the advantages of synchronous counter over asynchronous counter. 2.25
   b) Construct a binary counter that will convert a 64-kHz pulse signal into a 8-kHz square wave. 2
   c) Draw the logic diagram of a Mod-8 synchronous up/down counter. Explain its operation with timing diagram. 4.5

6. a) Define Excitation table. Write the excitation table of SR, JK, D and T flip flop. 3
   b) Design a counter with JK flip flop that will count the sequence 0,1,5,4, 3, 2, 0. 5.75

7. a) Discuss FPGA architecture in brief. Distinguish between PLA and PAL in terms of design architecture. 3
   b) Implement the Boolean function using PAL 3

$$Y_1 = \sum m(1,2,4,7)$$

$$Y_2 = \sum m(3,6)$$

   c) Determine the size of the PROM required to implement a dual 8-to-1 multiplexer with common selection inputs 2.75

8. a) What is VHDL? Briefly describe the salient features of VHDL and Verilog. 2.75
   b) Explain an 8-to-1 line Multiplexer module in Verilog HDL. 3

   c) Write a VHDL code to implement XOR operation. 3

**University of Rajshahi**
**Department of Computer Science and Engineering**
**B.Sc. Engg.(CSE) Part 2 Odd Semester Examination-2017**
**Course: CSE2111 (Digital System Design)**
**Full Marks: 52.5 Time: 3 Hours**

**[N.B. Answer SIX questions taking THREE from each Section.]**

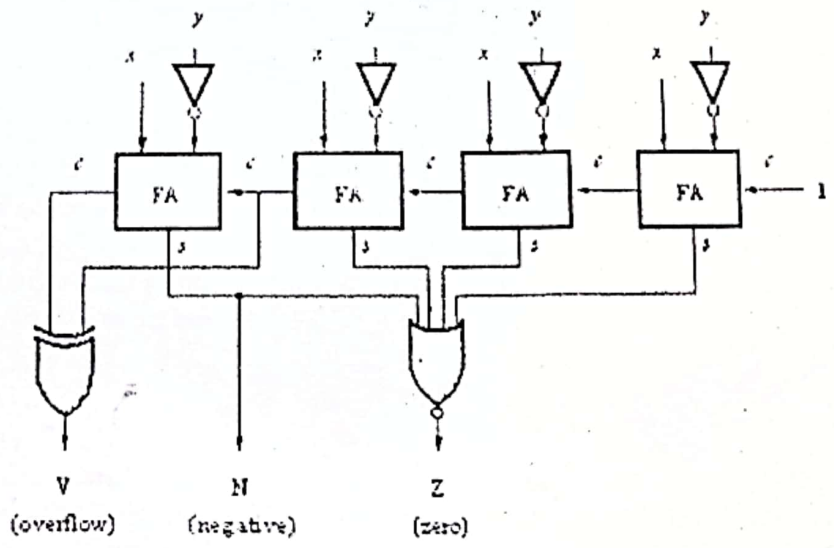
## Part A

1. (a) Represent $(-200)_{10}$ and $(200)_{10}$ using sign-magnitude, 1's complement and 2's complement binary form. 2
   (b) Represent $(275)_{10}$ and $(641)_{10}$ in BCD and then perform BCD addition. Check your result by converting back to decimal. 2
   (c) Construct a BCD adder to add two 4-bit BCD code groups using 4-bit parallel adders and discuss its operation with suitable examples. 4.75

2. (a) Design a combinational logic circuit to compare two 4-bit binary numbers A and B and to generate the outputs A<B, A=B and A>B. 3
   (b) Design a combinational circuit to convert BCD code to 7-segment code. 3.75
   (c) Design a combinational logic using suitable multiplexer to realize the following boolean expression: $Y= AD'+B'C+BC'D'$. 2

3. (a) What is priority encoder? Design a 4-line to 2-line priority encoder with active HIGH inputs and outputs with priority assigned to the higher order data input lines. 4.75
   (b) Implement a full-adder circuit using a 3-to-8 decoder. 4

4. (a) What is code converter? Draw the combinational logic circuit for binary to gray code conversion. 1.75
   (b) Design and explain a 2-bit binary multiplier combinational logic circuit. 4
   (c) In computer computations it is often necessary to compare numbers. Two four-bit signed numbers, $X = x_3x_2x_1x_0$ and $Y = y_3y_2y_1y_0$, can be compared by using the subtractor circuit in Figure, which performs the operation $X - Y$. The three outputs denote the following: $Z = 1$ if the result is 0, otherwise $Z = 0$; $N = 1$ if the result is negative, otherwise $N = 0$; $V = 1$ if arithmetic overflow occurs, otherwise $V = 0$. Show how Z, N, and V can be used to determine the cases $X = Y$, $X<Y$, $X<=Y$, $X>Y$ and $X>=Y$. 3



## Part B

5.(a) What is shift register? Design a 4-bit right shift register with parallel load of data. 3

(b) What is counter? Differentate between asynchronous and synchronous counter. List the applications of counter. 1.75

(c) Draw the truth table and design a logic diagram of a MOD-10 ripple counter. Explain its operation with timing diagram. 4

6.(a) Design a synchronous counter with JK flip-flop that will count the sequence as 0, 2, 4, 6, and repeat. 4

(b) Design a MOD-8 synchronous up/down counter and explain its operation with timing diagram. 4

(c) What is presettable counters? 0.75

7.(a) Design a magnetic core RAM using 2x4 decoder (consider 2-bits input and 2-bits output). Discuss the read/write operation. 4

(b) Distinguish between PLA and PAL in terms of design architecture. 1.75

(c) Define the different hardware of FPGA. Draw the basic FPGA architecture. Give an example. 3

8.(a) What is a hardware description language? What are the requirements of a good HDL? 3

(b) Briefly describe the salient features of VHDL and Verilog. 4

(c) What are the advantages of using JAVA HDL over Verilog? 1.75

# University of Rajshahi

**Department of Computer Science and Engineering**

B. Sc. (Engg.) Part-2 Odd Semester Examination-2016

Course: CSE2111 (Digital System Design)

Full Marks: 52.5 Duration: 3(Three) Hours

**Answer 06(Six) questions taking any 03(Three) questions from each part.**

## Part-A

1.(a) Design a 4-bit binary adder circuit with necessary figures. 2

(b) What do you mean by the terms 'carry generate' and 'carry propagate'? Define those terms with a full adder circuit and necessary equations. 2.75

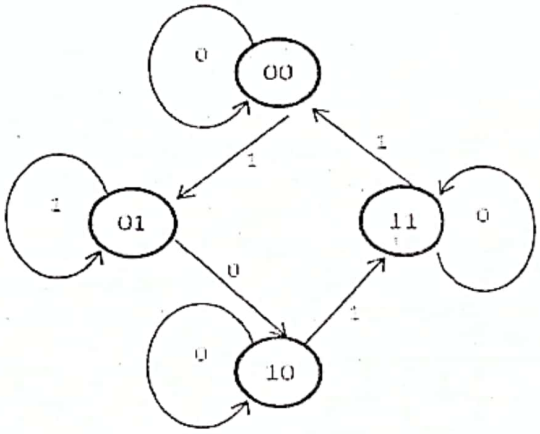
(c) Define lookahead carry-generator. Design a 4-bit carry-lookahead adder. 4

2.(a) Draw a 2-input AND gate and a 2-input OR gate using Transistor-Transistor logic 2.75

(b) There are **Four** switches to control a water pump. The water pump is turned on for the following conditions (i) if switch 1 is turned OFF but both switch 2 and 3 are turned ON, or, (ii) if switch-4 is turned ON but both switch 2 and 3 are turned OFF. Draw the truth table, derive the switching functions, minimize the switching functions by using K-map and draw the logic-gate diagram (circuit). 4

(c) What are the differences between '7400' and '74LS00'? 2

3.(a) Design a clocked sequential circuit that counts from 00 to 11 with JK flip-flops whose state diagram is given below: 4




(b) Define latch and flip-flop. Design a clocked master-slave JK flip-flop. 3

(c) Define state reduction problem. What is the benefit by considering **don't care** terms in designing a sequential circuit? 1.75

4.(a) Design the sequential circuit using register and ROM whose next state and outputs are defined by the following equations: 4

$A_1(t+1)=\Sigma(4,6)$

$A_2(t+1)=\Sigma(1,3,5,7)$

$y(A_1, A_2, x)=\Sigma(3,7)$

(b) Design a 2-input serial adder using a sequential logic procedure. 3

(c) Discuss the difference between serial and parallel modes of operation in a register. 1.75

## Part-B

5.(a) Draw the logic diagram of a 4-bit Ripple counter and explain its operation. 3

(b) What do you mean by negative-edge triggered FF, positive edge triggered FF and level triggered FF. Explain with diagrams. 2

(c) Draw the logic diagram of a 4-bit **Johnson** counter and explain its operation. 3.75

6.(a) Design an integrated circuit memory using 2×4 decoder (consider 2-bit input and 2-bit output). 4

(b) A combinational circuits is defined by the following functions 4.75

$F_1(A,B,C)=\Sigma(3,4,6,7)$

$F_2(A,B,C)=\Sigma(0,2,5,8)$

Implement the circuit with a PLA having 3 inputs, 4 product terms and 2 outputs.

7.(a) Describe the abstraction levels of Verilog HDL. 3

(b) Write the input-output connection rules of Verilog HDL with example. 2.75

(c) What is the difference between the following two lines of Verilog code? 3

i. #5 a=5;

ii. a=#5 b;

8.(a) Write Verilog HDL programs including the design and stimulus blocks for 4.75

(i) 4-1 multiplexer, +4

(ii) 4-bit full adder.

# University of Rajshahi

## Department of Computer Science & Engineering

B.Sc. (Engg.) Part-II Odd Semester Examination 2015

Course: CSE-2111 (Digital System Design)

Full Marks: 52.5 Duration: 3(Three) Hours

**Answer 6(Six) questions taking any 3(Three) from each part**

### Part-A

1. a) Why combinational logic circuit is needed? Design a BCD to Excess-4 code converter and draw its logic diagram. 4

   b) Why carry-lookahead adder is faster then carry propagation adder. Draw the logic diagram of a 4-bit lookahead carry generator. Construct a 4-bit carry-lookahead adder with a lookahead carry generator. 4.75

2. a) What is the difference between a decoder and a de-multiplexer? Implement a full adder circuit with a decoder and two OR gate. 4

   b) Define multiplexer. Implement $F(A,B,C,D) = \Sigma(1,2,4,8,9,15)$ with a 8x1 MUX. 4.75

3. Consider a synchronous sequential binary logic circuit with one input $A$ and one output $Z$. Suppose $A$ denotes single bit binary number and the input sequence is divided per every three clock cycle. Here, each division is called an *interval*. We would like to design a sequential circuit which outputs 1 at the last clock period of the interval if and only if the interval contains one or more '1's. Table-1 illustrates an example of the action.

| Clock | $C$ | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|---|
| Input | $A$ | 0 | 0 | 0 | 1 | 0 | 1 |
| Output | $Z$ | 0 | 0 | 0 | 0 | 0 | 1 |

Table- 1

   a) Draw the state transition diagram for the circuit. 2

   b) Draw the state transition table for the circuit. 2

   c) Draw the Karnaugh map for the circuit. 2

   d) Design the synchronous sequential circuit and draw it. You can only use the symbols for AND, OR, NOT, D flip-flop and JK flip-flop. 2.75

4. a) Distinguish between flip-flop and latch. Explain clocked SR flip-flop with logic diagram, function table and characteristics equation. 4

   b) Complete the diagram of the sequential circuit whose sequence is given below: 4.75

| State | a | a | b | c | d | e | f | f | g | f | g |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Input | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| Output | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |

Draw the logic diagram using SR flipflops.

## Part-B

5. a) What is shift register? Design a 4-bit bidirectional shift register with parallel load. 4.25
   b) Whet is ripple counter? Draw the logic diagram of a BCD ripple counter with timing diagram. 4.5

6. A circuit C1 shown in Fig-1 accepts n-bit unsigned binary numbers A and B as input and produce G and S as output, where G is the greater and S is the smaller between A and B respectively. When A=B, we have G=S=A=B. Fig-2 shows a circuit C2 processes numbers of one binary digit. Suppose that cascading n units of circuit C2 implement a circuit C1. The inputs *c* and *d* of circuit C2 represent that A<B and A>B respectively for more significant digits than processed by the circuit. The outputs *e* and *f* represent that A<B and A>B hold respectively including the digits being processed. $G_i$ and $S_i$ respectively represent $i^{th}$ bit of greater and smaller number.

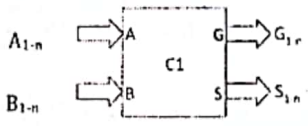



Fig-1

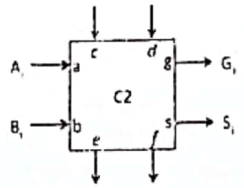



Fig-2

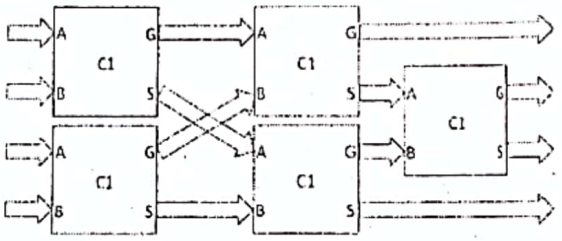



Fig-3

   a) Construct a truth table for circuit C2. Note that '1' represents *true* and '0' represents *false*. 2.5
   b) Draw a circuit diagram of C2 by using only AND, OR and NOT gate. 2.5
   c) Draw a block diagram of circuit C1 for comparing two 4-bit binary numbers by using four C2 circuit blocks. 1
   d) As shown in Fig-3, four input numbers are sorted by connecting several units of circuit C1. Following Fig-3, show an example circuit for sorting three inputs. 2.75

7. a) Distinguish between SRAM and DRAM. Briefly explain the internal organization of a 64x4 RAM. 4.25
   b) What are the major differences between CPLDs and FPGAs? Discuss FPGA architecture in brief. 4.5

8. a) State port connection rules in Verilog HDL. 2.75
   b) Explain min, max and typ delays in the gate-level design with respect to Verilog HDL. 3
   c) Describe a 8-to-1 line Multiplexer module in Verilog HDL. 3

**Department of Computer Science & Engineering**
**B.Sc. Engineering Part-2, odd Semester Examination 2014**

**Course: CSE2111 (Digital System Design)**
**Time: 3 hours** **Marks: 52.5**

(Answer **SIX** questions taking **THREE** from each part)

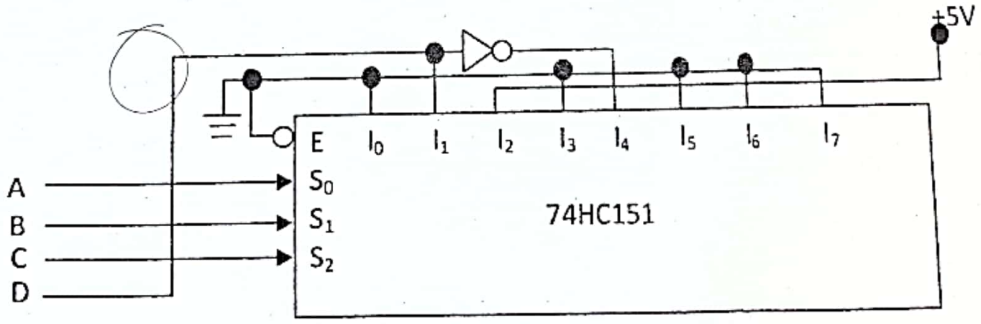
## PART-A

1. a) Define code converter? Design 3 bit Gray Code to binary converter and explain the operation. 4.25
   b) Design an 8-bit magnitude comparator using 74HC85 4-bit magnitude comparator and hence describe the operation of the following eight-bit comparison A7....A0=10101111 and B7.....B0=10101001. 4.5

2. a) Design a 4-bit binary parallel adder/subtractor circuit and explain the operation with an example. 5.5
   b) There are two types of adder, one is ripple carry and other is carry look-ahead. What will be the good design of 32-bit adder? Explain your answer. 3.25

3. a) Design a binary multiplier of two numbers A and B (two bit each), C=AxB. Explain its operation. 4.5
   b) Explain an application of magnitude comparator with a digital circuit. 4.25

4. a) Design a 1–line–to-8 line demultiplexer and discuss the operation of the circuit. 4.25
   b) From the following figure 4.5
   Set up a truth table showing the output Z for the 16 possible combinations of input variables.
   Write the sum of product expression for Z and simplify it to verify
   $Z = \overline{C}B\overline{A} + D\overline{C}BA + \overline{D}C\overline{B}A$



## PART-B

5. a) Define asynchronous and synchronous counter. Discuss the problems of asynchronous counter? 3
   b) What is MOD number of a counter? Show how to wire the 74LS293 asynchronous counter IC as a MOD-10 counter and explain its operation. 5.75

6. a) Define excitation table. Write the excitation table of JK flip flop and D flip flop. 3
   b) Design a counter with JK flip flop that will count the sequence 0,1,3,7,5,2,0 5.75

7. a) A certain memory stores 8 k x 16 bit words. How many data input lines, data output lines and address lines does it have? What is its capacity in bytes? 3
   b) Define PAL and PLA. Implement the Boolean function using PAL. 5.75
   $Y_1 = \Sigma m\ (1, 3, 5, 7)$
   $Y_2 = \Sigma m\ (2, 4)$.

8. a) What is VHDL? What are the three levels of architecture description in VHDL? Briefly discuss. 4.75
   b) Write a VHDL code for the circuit diagram given below: 4