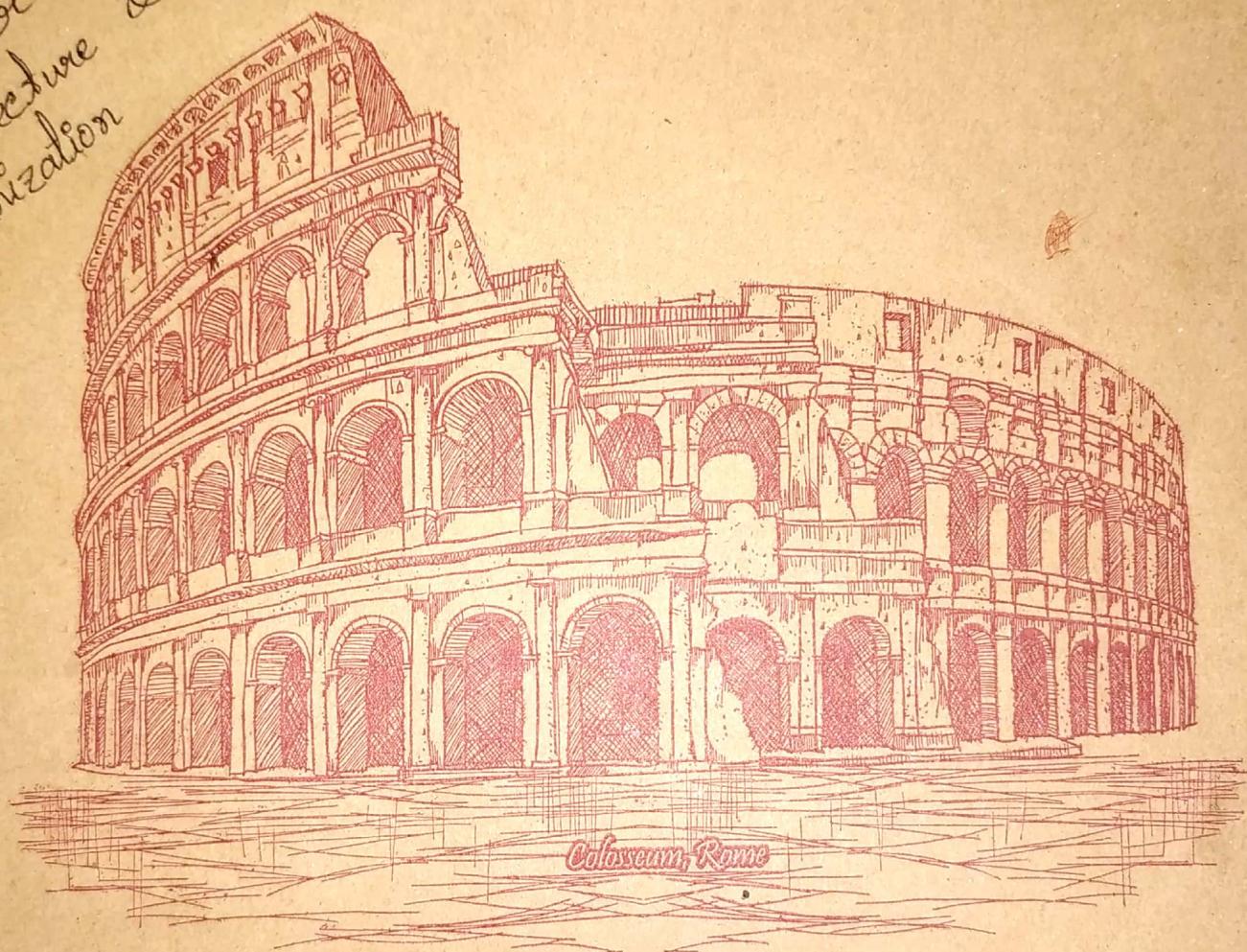


CLASSMATE

Computer
Architecture &
Organization



Colosseum, Rome

**EXERCISE
BOOK**

Mursalin

24.09.19

Computer Architecture and Organization

- programmes point of view — visible components (attribute)
- operational unit and their interconnection (organization)

Structure:

The way in which the components are inter-related.

Function:

Functional unit:

diagram (functional view) of computer

Fig - 1.1

Fig - 1.2 probable computer operation.

Fig - 1.3. The computer.

Fig - 1.4 Computer Top-level structure.

Fig - 1.5 CPU (processor) diagram

Fig - 1.6 Control unit.

* Peripheral (short distance)
* I/O communication (long distance)

Reference Book:

i) Computer Architecture & Organization

- John P. Hayes (Tata), Third Edition.

ii) Computer Organization & Architecture

- William Stallings (first chapter)

History of computer

1st generation : ENIAC

EDVAC Fig - 2.1
(First modern computer)

Fig - 2.2.

Fig - 2.3.

Question

* Program start → P.C. (memory location)

Program counter

↓
MAR (Memory Address Register)

↓
Memory

↓
MBR (Memory Buffer register)

AC (Accumulator) → temporary value will hold
Result will be held.

* table

* MAR ← PC

* Read : IBR ← MBR ← M(MAR), fetch

* Place left instruction (store) in IR and operand.
(Address) 102 in MAR, decode.

* MBR ← AC, execute.

2nd Generation: IBM 7094

Fig - 2.5.

Diagram [Question]

(different b/w, b/w
of 1st and 2nd
generation) → [Ques.]

3rd Generation: System 360. (business class PC)

Fig - 1.17 (33 page.)

↓
super computer 90
↓
parallel processing
↓
pipeline execution
(overlapping of instruction)

multi processor

4th → 5th → 6th continues. Fig - 1.19.

Processor architecture: (Page - 40) DA

Fig - 2.6 → page → 36

Performance configuration:

Fig - J. 22.

- * RISCs } Question → RAM → cache → RAM (time delay & costly)
 - * CISCs } disadvantage of 1985 (time delay & costly)
- Intel pentium → RAM (costly)

IBM 80

Performance measure:

→ speed of works operation.

units → Instruction per second (IPS) $T = \frac{N}{IPS}$

→ Cycle per instruction $CPI = \frac{(f \times 10^6)}{IPS}$ clock freq.
in Mega Hz

$$T = \frac{N \times CPI}{f \times 10^6} \text{ s.}$$

Speed up technique:

- cache
- pipe lining.
- Super scaling

Fig - J. 29

03.10.19

Fig - 3.1 (Stallings)

3.2

Instruction fetch & Execute.

Fig - 3.3.

Fig - 3.4

Fig - 3.5

Fig - 3.6.

Table - 3.1.

Fig - 3.7

3.3

Fig - 3.15.

(Stallings) chapter - 3

Fig - 3.16

Fig - 3.18

Processor Basics

(Hayes - 3.)

Fig - 3.1

{ Memory mapped I/O
I/O mapped I/O

Fig - 3.2

Fig - 3.3

Fig. 3.3 → instructions

3.2 Accumulator-based CPU.

3.3 → 142 Page.

12.11.10

A CISC machine:

coprocessors:
clk/ structure → 3.14

Number system →
Error detection & correction.

03.11.9

Additional features:

- Multipurpose register
 - 32 register (3-gen - IBM-360) → register file
 - previous - 3 (DR, AR, AC)
- Additional data
- Register for computational status.
- program control stack.

Fig - 3. 7

Pipelining:

Fig - 3.8

Ex - 3.2

ARM6 microprocessor.

- RISC
- SISC (processor - 680X0) → 68000
68060
(personal - 68020)
diagram → 68020
- Co-processor (helps main processor in arithmetic)
68871 → study Fig - 3.14

12.11.9

MMV

→ Data Representation / Number system

→ error detection fig - 3.20.

1st generation → SISC/RISC → development

→ feature → C.T.

4.1 Fixed point Arithmetic

4.2.1 Addition, subtraction

Fig - 4.1, 4.2, 4.3, 4.4

17.11.19

अंगठी के किन दृष्टिकोण से वर्तन करते होंगे?

High speed adder:

- carry-look-ahead adder
- carry generator

overflow-bit

$$V = C_{n+1} \oplus C_{n+2}$$

Fig - 4.5

Fig - 4.6

Fig - 4.7

Fig - 4.8

Fig - 4.9

Fig - 4.10

Fig - 4.11

Fig - 4.12

Multiplication

chapter - 2 (Example - 2.7)

$$P_0 = x_0 \oplus y_0$$

Fig - ab multiplier (chapter - 2)

2's complement multiplier;

Fig - 4.12

Multiplication → process / Fig - 4.12

03.12.19

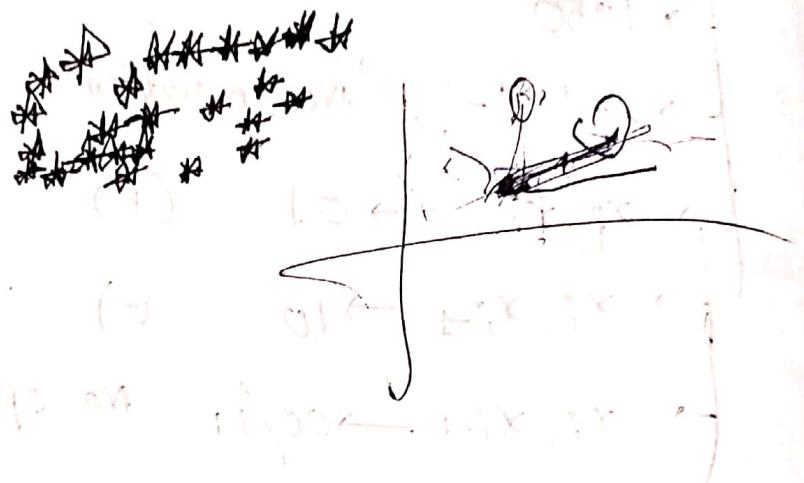
Fig. 4. 20

Division

divisor ✓

dividant D.

Quotient Q



$$\frac{D}{V} \rightarrow D \left(\frac{VQ}{R} \right)$$

Fig. 9.21

Fig. 4.2B

Fig - 4. 22

Fig. 4.26

~~ACC Stat math. CSC 211~~

14

21 18

2124

2131 2442

05.12.19

~~fucking~~ → ~~THAODR~~

Arithmetic Logic Unit:

Fig - 4. 28, 4. 29

Fig - 4. 30

Fig - 4. 31, 4. 32.

Need - Fig - 4. 6.

08.12.19

chapter - 9 (259 pages)

Fig → 4. 33, 4. 34, 4. 35, 4. 36, 4. 37, 4. 38, 4. 39

chapter - 6

Memory organization

Fig - 6. 2

Access mode

destructive readout

non " "

405 page

Fig - 6. 5

dynamic RAM
Static RAM

10.12.19

RAM:

Fig - 6.7 Fig - 6.8

Semiconductor - RAM's

Fig - 6.9

RAM design:

Fig - 6.10

Fig - 6.11

Fig - 6.12

Fig - 6.13 (MT4LC8M(8E1))

Study - ROM

Frost RAM Interface

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Fig - 6.14

serial. Access Memory

6.15, 6.16, 6.17,

(Rambus - operation)

Fig - 6.21

cost performance

* Address Translation

(6.2.2) memory mapping

Base addressing

Fig - 6.24, 6.25

Translation look-side buffer (TLB)

Fig. 6.26.

Segments

Page

Fig - 6.29

Fig - 6.30

17.12.19

Memory Allocation:

Fig: 6.33

Flooding

Fig: 6.34, 6.35.

Replacement policy

First-fit } allocation
Best-fit }

→ FIFO
→ LRU
→ OPT

Fig - 8.21

Flooding

Fig - 6.36,
Ex: 6.6.

Primitive
non primitive }

control unit:

Fig - 5.1, 5.2, 5.4

Hardware control:

Design methods (1, 2)

state table.

Melby Mealy machine type
Moore machine type

19.12.19

GCD Processor:

Ex - 5.1

$20, 12 \rightarrow \text{GCD} = 4$

Fig $\rightarrow 5.5, 5.6, 5.7, 5.8$
5.9

Imp.

One-hot method:

Test \rightarrow memory & processor today

One-hot Method / classical / side derive

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Fig - 5.10, 5.12, 5.14

Example - 5.1

Multiplexer Controller

for same org'd

System Organization:

Ex - 5.1

5.11

5.12

5.13

5.14

5.15

5.16

5.17

~~Fig - 7.23, 7.24, 7.25, 7.26, 7.27, 7.31, 7.33~~
~~7.34, 7.35,~~

~~26.12.10~~

7.1 Communication methods.

7.1.1 Base concept

fig - 7.1 communication within a computer
via a single-shared bus.
(482 → page)

power PC

7.1 - figure

The small computer system.

National standards Ins (ANSI)

VV7 BUS control

- * synchronous bus → definition
- * " " " → problem:
- * asynchronous " " → advantage & disadvantage.

Bus-interfacing → page - 499

Fig - 7.13.

Fig - 7.19 use of tri-state for bus interfacing

VV7
Bus arbitration

Fig - 7.19

Fig - 7.20, 7.21

Bus arbitration using busy claiming

(page - 59) → DMA.

7.2 I/O and system control.

VV7
I/O control methods

- I/O → CPU involvement
- programmed I/O
- DMA

29.12.19

Fig \rightarrow 7.2 1, 7.26,
7.3 \rightarrow example

Fig \rightarrow 7.3 5.

Comparator processor

This is a processor that takes two number as input and output the smallest number. The control unit is designed using the classical method.

For example : Let, $X = 20$, $Y = -10$, the output is 10.

For this, the HDL description is given below-

small Number (in: X, Y , out Z):

register $XR, YR, TEMR$;

$XR := X$;

$YR := Y$;

if (~~$XR < YR$~~)

$TEMR := XR$

else

$TEMR := YR$

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Interruption

key - 7.36, 7.37, 7.38, 7.39

lacing chain

I/O device / pipeline processor

31.12.19

Interrup:

fig - 7.36, 7.37, 7.38, 7.39

| busy char

I/O device / pipeline parameter

