University of Rajshahi

Department of Computer Science and Engineering

B. Sc. (Engg) Part-II Even Semester Examination 2020

Course: CSE 2231 (Computer Architecture and Organization)

Full Marks: 52.5 Duration: 3 (Three) Hours

Answer 06 (Six) questions taking any 03 (Three) from each section

Section-A

1.	a)	What is meant by 16-bit computer? Explain how operating system bridges the gap between software and hardware.	3.00
	b)	Define latency and throughput. Explain the factors influencing computer speed.	3.00
	c)	Suppose you have two processors A and B with clock period 5ns and 10ns respectively. On average 5.4 and 4.5 clock cycles are required to execute one instruction for A and B respectively. Compare the performance of the two processors.	2.75
2.	a)	Compare hardwired and microprogrammed controls. How PC works for branching instructions.	3.00
	b)	Explain instruction cycle with example.	3.00
	c)	Define addressing mode? Describe the instructions R1←M[B]+R3; R2←M[M[ADR]] + M[PC+H] with respect to addressing mode.	2.75
3.	a)	What is interrupt service routine? Compare vectored and non-vectored interrupts.	2.75
	b)	Discuss about different types of data manipulation instructions.	3.00
	c)	Explain I/O configuration with its proper block diagram.	3.00
4.	a)	Briefly describe the structure of a fixed point ALU with diagram.	3.00
	b)	Shortly discuss how a 16-bit bit-sliced ALU is designed by four 4-bit ALU slices.	3.00
	c)	Distinguish between Ripple-carry adder and Carry-lookahead adder with diagram.	2.75

Section-B

5.	a)	Discuss about program control instructions.	2.00
	b)	Suppose you have a CPU with only 3 registers connected as input through two multiplexers MUX A and MUX B. They are also connected as output through a multiplexer MUX D. The CPU supports only 4 instructions (ADD, SUB, MUL, DIV). Draw the register organization of the mentioned CPU and write the codewords of the instructions: R3←R2+R1; R1←R3-R2; R2←R1*R3.	3.75
	c)	Explain how pipelining improves the performance. Suppose you have a processor with 2.5GHz clock and 4 blocks for pipelining. You have a program with 3×10^5 instructions in which only 45% instructions can be executed through pipelining. Calculate speedup factor for pipelining.	3.00
6.	a)	Define peripherals with examples. Mention the requirements for I/O interface.	2.75
	b)	Compare synchronous and asynchronous data transfer scheme. Explain asynchronous data transfer system and mention its advantages.	3.00
	c)	Discuss about strobe-controlled data transfer system with necessary diagram.	3.00
7.	a)	Mention the advantages of DMA. Illustrate the steps of DMA transfer from I/O to memory.	3.00
	b)	Illustrate the function of virtual memory. Suppose your computer system needs 512B RAM and 512B ROM. Only the memory chips (RAM and ROM) of size 256B are available. Draw the diagram to illustrate the memory connection.	3.00
	c)	Explain the function of cache memory to speedup computer system? Consider that 420 of memory references are available in the cache out of 600. Calculate the cache performance.	2.75
8.	a)	Design a micro-programmed control unit based on Wilkes design.	4.00
	b)	Explain the concepts of interleaved memories.	2.75
	c)	Distinguish between CISC and RISC processors.	2.00

University of Rajshahi

Department of Computer Science and Engineering

B.Sc. (Engg.) Part-2 Even Semester Examination-2018

Course: CSE2231 (Computer Architecture and Organization)

Marks: 52.50 Time: 3 Hours

[N.B. Answer SIX questions taking THREE from each section.]

Section-A

1.	(a)	Distinguish between computer architecture and computer organization.	2.75
	(b)	Define IAS computer. Discuss the organization of the CPU and main memory of the IAS computer.	4
	(c)	Mention some important features of third generation computers.	2
2.	(a)	What do you mean by memory-mapped I/O and I/O mapped I/O. Give example.	2
	(b)	Discuss the architectural extension of recent CPUs compared with a small accumulator-based CPU with necessary figures.	4.75
	(c)	Define instruction pipelining.	2
3.	(a)	Design a multiplier that can multiply two fixed-point signed binary numbers. Give the algorithm and flowchart for the multiplication process.	5.75
	(b)	Describe the data processing part of a simple floating-point arithmetic unit with diagram.	3
4.	(a)	Define overflow. How overflow detection logic is implemented.	2
	(b)	Draw the overall structure of a high speed adder.	2.75
	(c)	Discuss the register-level view of the 74181 4-bit ALU.	4

Section-B

5.	(a)	What are the functions of control unit in a computer system? Discuss the possible control signal generated to implement a subtraction instruction of the form SUB A,B with DP unit figure.	3.75
	(b)	Design DMA controller: draw state transition graph, state table and also logic diagram using One-hot design method	5
6.	(a)	Define destructive read out (DRO). Give example.	2
	(b)	Define address mapping. Discuss the structure of a dynamic address-translation system.	4
	(c)	Define preemptive allocation with necessary figure.	2.75
7.	(a)	Distinguish between synchronous and asynchronous buses. Give example.	2.75
	(b)	Discuss bus interfacing using tri-state logic with necessary figure.	3
	(c)	Discuss bus arbitration using daisy chaining. Mention some problems with this scheme.	3
8.	(a)	Discuss how cache memory helps to speed up the operation of a computer system.	3
	(b)	Explain the concept of virtual memory and interleaved memory.	3
	(c)	What do you mean by addressing mode? Shortly discuss indirect addressing mode.	2.75

University of Rajshahi
Department of Computer Science and Engineering
B.Sc. (Engg.) Part-2 Even Semester Examination-2017
Course: CSE2231 (Computer Architecture and Organization)
Full Marks: 52.5 Time: 3:00 Hours

Section A
Answer any THREE questions.

1. (a) Mention some important features of second generation computers. 02
   (b) Discuss the organizational differences between EDVAC and IAS computers with necessary diagrams. 04
   (c) Explain some important speedup features of modern computers – in brief. 2.75

2. (a) How do you design overflow detection logic for 2's complement addition or subtraction? Design an 8-bit adder-subtractor using necessary diagram. 04
   (b) Define Booth's algorithm. Design a combinational array multiplier using full-adder array of 4x4 bit unsigned numbers. 03
   (c) Define fetch and execution cycle. 1.75

3. (a) Discuss how cache memory speeds up the operation of a computer system. 03
   (b) Explain the concepts of interleaved memories. 2.75
   (c) What do you mean by addressing mode? Discuss indirect and indexed addressing modes. 03

4. (a) Define the features of spatial and temporal expansion of ALU. 03
   (b) Discuss the organization of the 2901 4 bit ALU slice. 1.75
   (c) Write down some features of sequential ALU. Discuss in brief about the main internal features of a combinational ALU. 04

Section B
Answer any THREE questions.

5. (a) Explain the general condition of pipelining. 02
   (b) Design a control unit that computes the gcd of two positive integers. Draw the hardwired inter-connectivity, state diagram, state table and also logic diagram using one hot design methodology. 05
   (c) List the control signal needed to execute the following instruction A:=A+B. 1.75

6. (a) Distinguish the organizational differences between SRAM and DRAM. Discuss the organization of Rambus DRAM interface. 03
   (b) Define translation look-aside buffer. Discuss the two-stage address translation with segments and pages with necessary diagram. 04
   (c) Mention some reasons for using virtual memory. 1.75

7. (a) Draw and briefly discuss the structure of an I/O processor. 2.75
   (b) Discuss the operation of a typical DMA controller with block diagram. 3.5
   (c) Write the advantages and disadvantages of Programmed I/O over DMA controller with respect to program design complexity, I/O bandwidth and interface hardware cost. 2.5

8. (a) What is meant by bus arbitration? Shortly discuss different bus arbitration schemes. 04
   (b) What is interrupt? Write the steps taken by a CPU during an interrupt service handling. 03
   (c) What do you mean by CISC and RISC processors? Mention some features of RISC processors. 1.75

University of Rajshahi
Department of Computer Science and Engineering
B.Sc. (Engg.) Part-2 Even Semester Examination-2016
Course: CSE2231 (Computer Architecture and Organization)
Full Marks: 52.5 Time: 3 Hours

[N.B. Answer any **Six** questions taking **Three** from each section. Figures in the margin indicate marks.]

PART-A

1. (a) What do you mean by computer architecture and organization? 2
   (b) What are the architectural limitations of first generation computers? Which of the limitations are solved by the second generation computers? 2.75
   (c) Let A and B be two vectors comprising 325 numbers each that must be added in pairs to compute vector C, such that C(I):= A(I) +B(I), where I=1,2,....,325. Write a program using IAS instructions that will execute the program. Given that, data A, B, and C are stored sequentially, beginning in locations 1101, 2001, and 3001 respectively. 4

2. (a) What is HDL? What are the advantages and disadvantages of HDL? 3
   (b) Give a VHDL description of a half adder. 2.75
   (c) Draw and explain the internal architecture of IBM 7094 Computer. 3

3. (a) Draw and discuss the block-diagram of a simple accumulator based CPU. 2
   (b) Explain the concepts of Bit Sliced ALU. 3
   (c) What are the differences between Ripple carry adder and Carry-lookahead adder? Explain with diagrams. 3.75

4. (a) Explain IEEE 754 standard floating point number format. 3
   (b) Why do we need overflow-underflow indicator? How does it work? 2.75
   (c) What are the advantages of Excess-three code over BCD code? What are the advantages and disadvantages of decimal code? 3

PART-B

5. (a) Illustrate the Booth's multiplication algorithm. 4
   (b) Define I/O processor. 1.75
   (c) Discuss the operation of a DMA controller. 3

6. (a) Discuss the "delay element method" for designing control unit. 4.25
   (b) Describe the Wlike's model of control memory. 4.5

7. (a) Write some names of semi-random memories. Why these memories are called semi-random? 2.75
   (b) How can we implement fast RAM interfaces? 3
   (c) Define seek time, latency and data-transfer rate of a memory. 3

8. (a) What do you mean by bus arbitration? Shortly discuss different bus arbitration schemes. 5
   (b) What are CISC and RISC processors? Mention some features of RISC processors. 3.75

University of Rajshahi
Department of Computer Science and Engineering
B.Sc. (Engg.) Part-2 (Even Semester) Examination-2015
Course: CSE2231 (Computer Architecture and Organization)
Full Marks: 52.5 Time: 3 Hours

[N.B. Figures in the margin indicate full marks. Answer any **Six** questions taking **Three** from each section]

Part-A

1.	(a)	Define computer architecture and computer organization.	1.5
	(b)	What are the shortcomings of IAS computer?	2.5
	(c)	A vector of 20 non-negative numbers is stored in consecutive locations beginning in location 200 with memory of IAS computer. Write a program using IAS computer instruction set to compute the address of the largest number in this array. If several locations contain the largest number then specify the smallest address.	4.75
2.	(a)	What is meant by 64-bit processor?	1
	(b)	Discuss the S/360-370 data formats and instruction formats.	4.75
	(c)	Draw and briefly discuss the structure of an I/O processor.	3
3.	(a)	Discuss the overview of CPU behavior with flowchart.	2.75
	(b)	Discuss the register-level design of a typical CPU.	3
	(c)	What do you mean by normalization and bias exponents?	2
	(d)	What is tag?	1
4.	(a)	Draw the block diagram of an 8-bit fixed point binary multiplier and discuss its operations.	5
	(b)	Discuss the operation of 4-bit carry look ahead adder with diagram.	3.75

Part-B

5.	(a)	How do active control signals generate during an add operation A: = A+B ?	4
	(b)	Write down an algorithm to calculate greatest common divisor (GCD) of two numbers. Draw and discuss the hardware needed to generate control signals to implement GCD procedure.	4.75
6.	(a)	What is cache memory? Why is it used in computer?	3
	(b)	What do you mean by cost/performance trade-offs for choosing memory devices.	2
	(c)	Draw and discuss a typical RAM design along with its major external connections.	3.75
7.	(a)	Describe the structure of a fixed-point ALU.	3.75
	(b)	What is meant by bit-sliced ALU? Discuss how a 16-bit bit-sliced ALU is designed by four 4-bit ALU slices.	5
8.	(a)	Define different types of bus.	3
	(b)	Why do we use tri-state buffer for bus interfacing?	2
	(c)	What do you mean by DMA? Draw and discuss the circuitry required for DMA operation.	3.75

5

University of Rajshahi

Department of Computer Science & Engineering

B. Sc. (Engg.) Part-II Even Semester Examination 2014

Course: CSE-2231 (Computer Architecture and Organization)

Full Marks: 52.5 Duration: 3(Three) Hours

Answer 06(Six) questions taking any 03(Three) questions from each part

Part-A

1. a) Define the terms latency, throughput and CPU execution time. 2
   b) Why do you need to study computer architecture? What is meant by 32-bit Processor. 2
   c) Define single and multiple bus structure with block diagram. Give comparison between two bus structures. 4.75

2. a) What is meant by computer performance? Mention the factors influencing computer speed. 3
   b) Why do you need to study about performance? Define latency and throughput 3
   c) Suppose you have a processor which has 6ns of clock period. Each floating point instruction requires 7 clock cycles and for others it is 3 clock cycles. Calculate the total time to execute a program with 40 Billion instructions, which has 30% floating point instruction. 2.75

3. a) Define interrupt and its service routine. Explain the steps of interrupt service with diagram. 3.75
   b) Mention the functions of different program control status bits. 2
   c) Define program control instructions with examples. Classify the data manipulation instructions INC, CLR, AND, ROR. 3

4. a) What are addressing modes? Explain the various addressing modes with examples. 5.75
   b) The binary word W = 10001011101001 is stored in a 14 bit register. What is the decimal number represented by W if it is interpreted as an integer in each of the following codes: (i) unsigned binary, (ii) sign-magnitude and (iii) 2's complement? 3

Part-B

5. a) Explain the general condition of pipelining. 2.75
   b) Suppose you have a CPU with only 5 registers connected as input through two MUX A, B and as output through a MUX D. The CPU supports only 4 instructions (ADD, SUB, MUL, DIV). Draw the register organization of the mentioned CPU and write the codewords of the following instructions: R1←R2-R3; R2←R3/R5; R3←R1*R4. 3
   c) Draw the block diagram to execute the instruction A_i-B_i+C_i using pipelining. Suppose you have a processor with 3GHz clock and 4 blocks for pipelining. You have a program with 2×10^6 instructions in which only 45% instructions can be executed through pipelining. Calculate speedup of pipeline. 3

6. a) Illustrate the steps of asynchronous data transmission system with example. 2
   b) Explain different types of handshake controlled data transfer with necessary diagram. 3.75
   c) Illustrate and explain the functional steps of Intel 8089 IOP. 3

7. a) Does CPU work with another task during DMA? Explain. 2
   b) Mention the function of virtual memory. Suppose your computer system needs 256B RAM and 256B ROM. You have only 128B memory chips. Draw the diagram to illustrate the memory connection. 4
   c) What do you mean by Level1 and Level2 cache? Consider that 560 of memory references are available in the cache out of 1200. Calculate the cache performance. 2.75

8. a) Define memory access time, memory cycle time and data transfer rate. 1.75
   b) Explain the representation of floating point number in details. 3.5
   c) How CPU performs floating point addition/subtraction? Explain with necessary diagram. 3.5

University of Rajshahi
Department of Computer Science and Engineering
B. Sc. (Engg.) Part-II Even Semester Examination 2013
Course: CSE 2221 (Computer Architecture and Organization)
Full Marks: 52.5 **Time:** 3 Hours
[Answer any six questions taking 3 from each Group]

Group A

1. a) Discuss the advantages and disadvantages of storing programs and data in the same memory. 2.75
   b) Describe the basic functions performed by each of the following components of a computer system: CPU, main memory, IO processor, secondary memory, operating system and compiler. 6

2. a) Draw and explain the internal architecture of IBM 7094 Computer. 5.75
   b) Why are buffers used with computer input devices and latches are used with output devices? 3

3. A circuit C1 shown in Fig-1 accepts n-bit unsigned binary numbers A and B as input and produce G and S as output, where G is the greater and S is the smaller between A and B respectively. When A=B, we have G=S=A=B. Fig-2 shows a circuit C2 processes numbers of one binary digit. Suppose that cascading n units of circuit C2 implement a circuit C1. The inputs *c* and *d* of circuit C2 represent that A<B and A>B respectively for more significant digits than processed by the circuit. The outputs*e* and *f* represent that A<B and A>B hold respectively including the digits being processed. G_i and $S_i$respectively represent i^{th}bit of greater and smaller number.

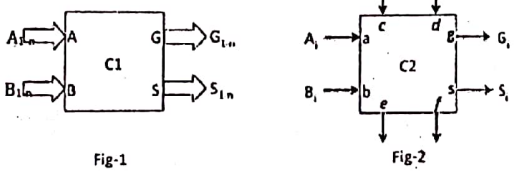

Fig-1

Fig-2

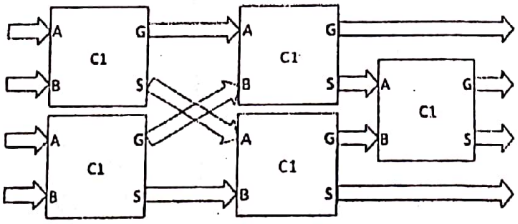

Fig-3

   a) Construct a truth table for circuit C2.Note that '1' represents *true* and '0' represents *false*. 2.5
   b) Draw a circuit diagram of C2 by using only AND, OR and NOT gate. 2
   c) Draw a block diagram of circuit C1 for comparing two 4-bit binary numbers by using four C2 circuit blocks. 1.5
   d) As shown in Fig-3, four input numbers are sorted by connecting several units of circuit C1. Following Fig-3, show an example circuit for sorting three inputs. 2.75

4. a) Define fetch cycle and execution cycle. 2
   b) Describe the formulas to perform floating point arithmetic operations. 3.75
   c) Draw the block diagram of a simple accumulator based CPU. 3

Group B

5. a) Describe the structure of a fixed point ALU. 4.75
   b) Is it possible to construct a 16-bit, bit sliced ALU using four 4-bit ALU slices? If it is possible, then justify your answer. 4

6. a) Draw and explain the internal organization of a 256x8 RAM. 4.75
   b) What is a DRAM? Write down its advantages and disadvantages over SRAM. 4

7. a) Define different types of bus. 3
   b) Compare between daisy-chaining and polling method for bus arbitration. 4
   c) What is DMA controller? 1.75

8. a) Distinguish between CISC and RISC processor with example. 3.75
   b) What does pipelining in computer science mean? How could we increase the efficiency of computer instruction execution by using pipelining? Explain with necessary diagram. 1+4

University of Rajshahi

Department of Computer Science and Engineering

B.Sc. Engineering Part-II Semester Final Examination 2012

Course: CSE2221 (Computer Architecture and Organization)

Time: 04 Hours **Full Marks:** 52.5

(Answer any Six(06) questions. Choose at least three (03) questions from each part.)

Part A

1. (a) Differentiate among computer architecture, design and organization. 2
   (b) Why do you need to study computer architecture? What is meant by 64-bit Processor? 2
   (c) Define single and multiple bus structure with block diagram. Give comparison between two bus structures. $4\frac{3}{4}$

2. (a) What is meant by computer performance? Mention the factors influencing computer speed. 3
   (b) Why do you need to study about performance? Define latency and throughput. 3
   (c) Suppose you have a processor which has 5ns of clock period. Each floating point instruction requires 10 clock cycles and for others it is 5 clock cycles. Calculate the total time to execute a program with 40 Billion instructions which has 20% floating point instruction. $2\frac{3}{4}$

3. (a) Define instruction and OpCode with examples. State the function of two registers PC and AR. 3
   (b) Define control signal. Differentiate between hardwired control and micro programmed controlled signals. 3
   (c) What is addressing mode? Describe the instructions $2\frac{3}{4}$
   R1←M[A]+F1; R2←M[M[Adr]]-M[R3] with respect to addressing mode.

4. (a) What do you mean by addressing mode? Discuss different types of addressing mode with example. 6
   (b) Describe I/O instructions with example. $2\frac{3}{4}$

Part B

5. (a) Mention the functions of different parts of CPU. 2
   (b) Suppose you have a CPU with only 3 registers connected as input through two MUX A, B and as output through a MUX D. The CPU supports only 4 instructions (ADD, SUB, MUL, DIV). Draw the register organization of the mentioned CPU and write the codewords of the instructions: R1←R2+R3; R2←R3*R1; R3←R1/R2. 3
   (c) Draw the block diagram to execute the instruction Ai*Bi+Ci using pipelining. Suppose you have a processor with 2GHz clock and 4 blocks for pipelining. You have a program with 200 instructions in which only 60% instructions can be executed through pipelining. Calculate speedup of pipeline. $3\frac{3}{4}$

6. (a) What are the basic requirements for I/O interface? What are the different interface modules? 3
   (b) Describe synchronous and asynchronous data transfer mode.
   (c) What do you mean by Direct Memory Access (DMA)? $2\frac{3}{4}$

7. (a) Show the memory hierarchy of a computer system 3
   (b) What are the difference between DRAM and SRAM? $3\frac{3}{4}$
   (c) What do you mean by virtual memory? 3

8. (a) Define multiprocessor with its possible applications. Differentiate between RISC and CISC processors. 2
   (b) Explain how parallel processing can be implemented in uniprocessor. 3
   (c) Compare SIMD and MIMD architectures with diagrams. $2\frac{3}{4}$