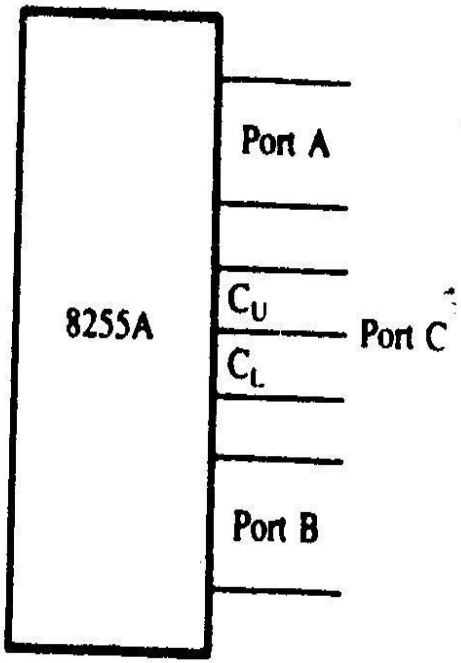
Chapter-15

General Purpose Programmable Peripheral Devices

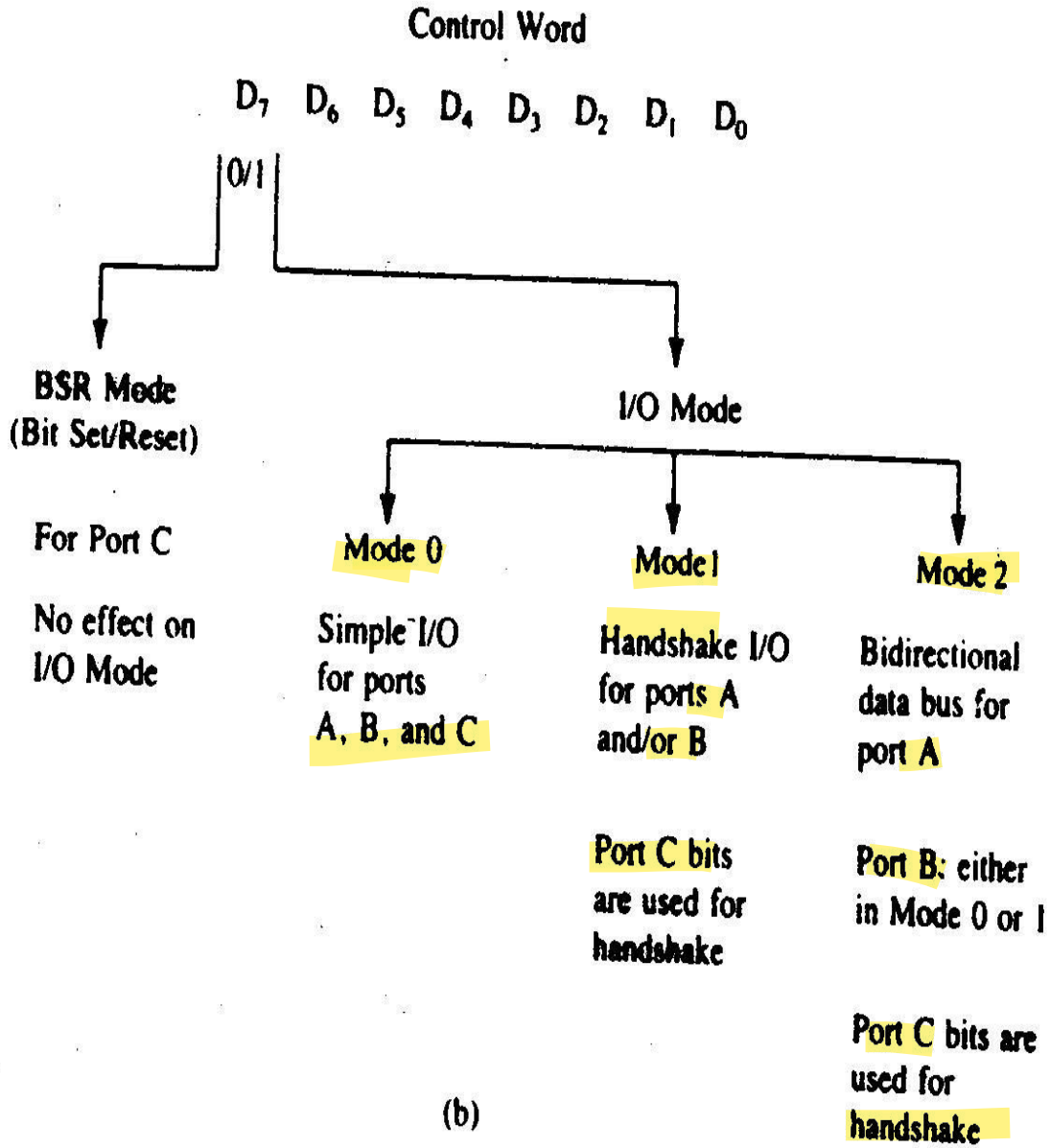
15.1 THE 8255A PROGRAMMABLE PERIHERAL INTERFACE

The 8255A is a widely used, programmable, parallel I/O device. It can be programmed to transfer data under various conditions, from simple I/O to interrupt I/O. It is flexible, versatile, and economical (when multiple I/O ports are required), but somewhat complex. It is an important general-purpose I/O device that can be used with almost any microprocessor.

The 8255A has 24 I/O pins that can be grouped primarily in two 8-bit parallel ports: A and B, with the remaining 8-bits as port C. The eight bits of port C can be used as individual bits or grouped in two 4-bit ports: C_{UPPER} (C_U) and C_{LOWER} (C_L), as in Figure 15.1(a). The functions of these ports are defined by writing control word in the control register.



(a)



(b)

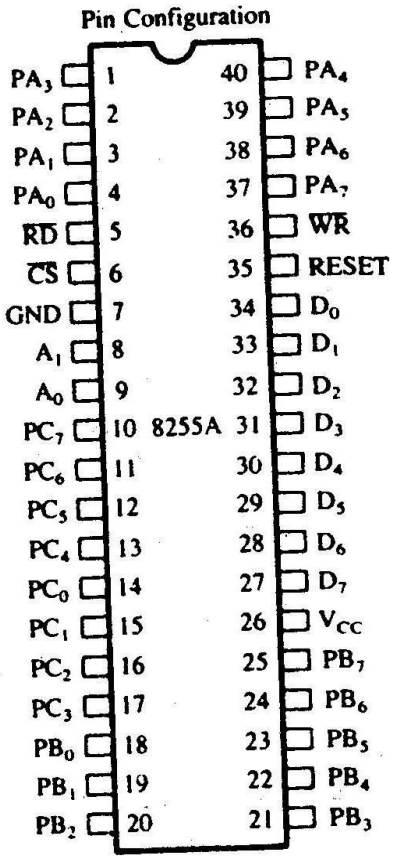
FIGURE 15.1
8255A I/O Ports (a) and Their Modes (b)

Figure 15.1(b) shows all the functions of the 8255A, classified according to two modes: the Bit Set/Reset (BSR) mode and the I/O mode. The BSR mode is used to set or reset the bits in port C. The I/O mode is further divided into three modes: Mode 0, Mode 1, and Mode 2.

- **Mode 0:** all ports function as simple I/O ports.
- **Mode 1:** handshake mode; ports A and/or B use bits from port C as handshake signals.
- **Mode 2:** port A for bidirectional data transfer using handshake signals from port C, and port B can be either Mode 0 or Mode 1.

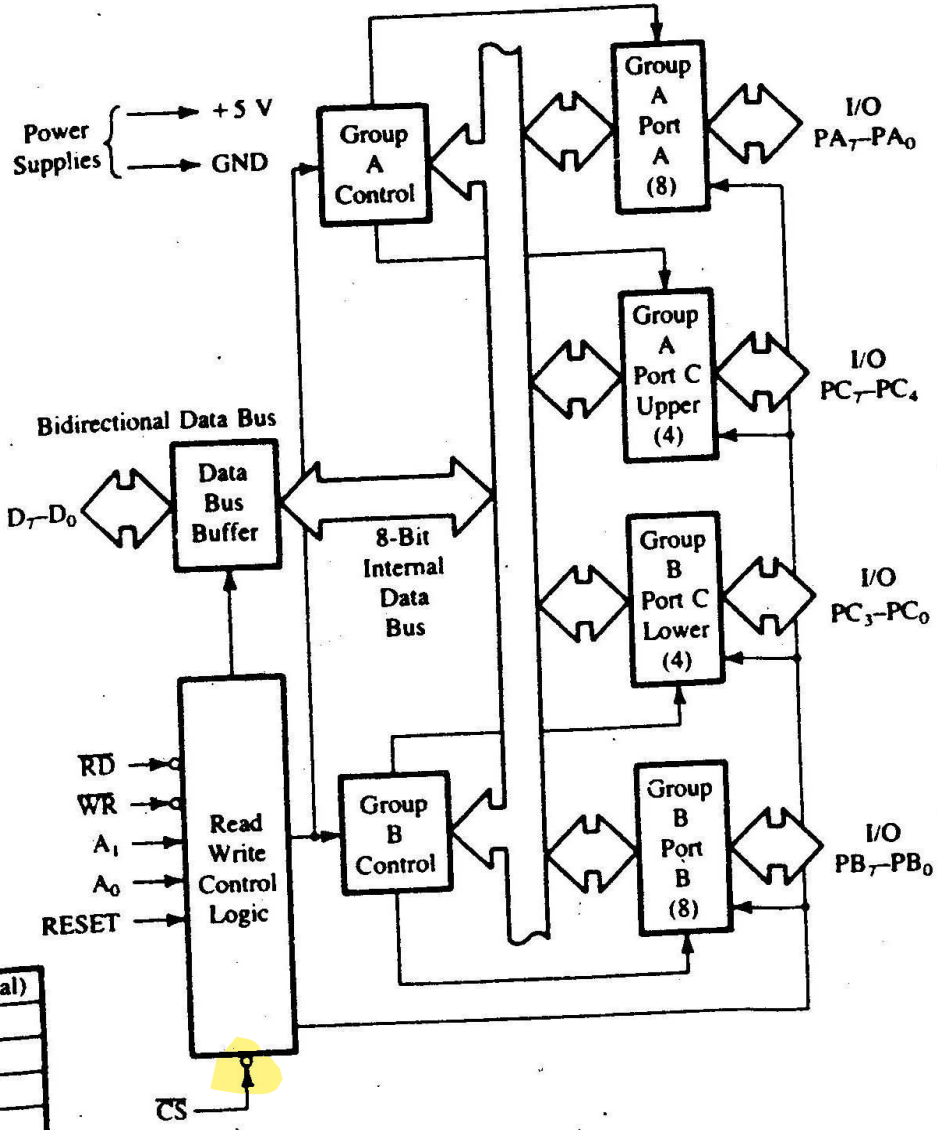
15.1.1 Block Diagram of the 8255A

The block diagram in Figure 15.2(a) shows two 8-bit ports (A and B), two 4-bit ports (C_U and C_L).

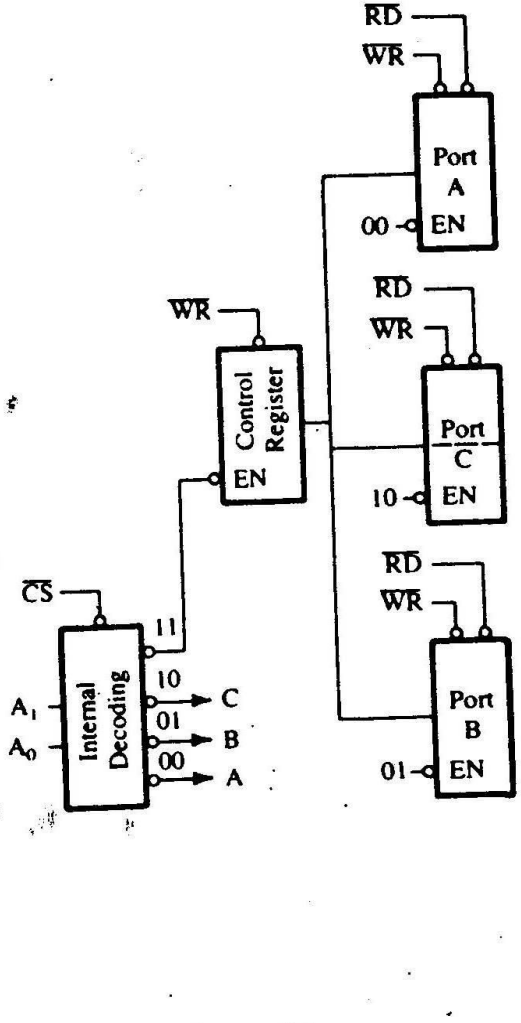


Pin Names

D_7–D_0	Data Bus (Bidirectional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7–PA_0	Port A (Bit)
PB_7–PB_0	Port B (Bit)
PC_7–PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

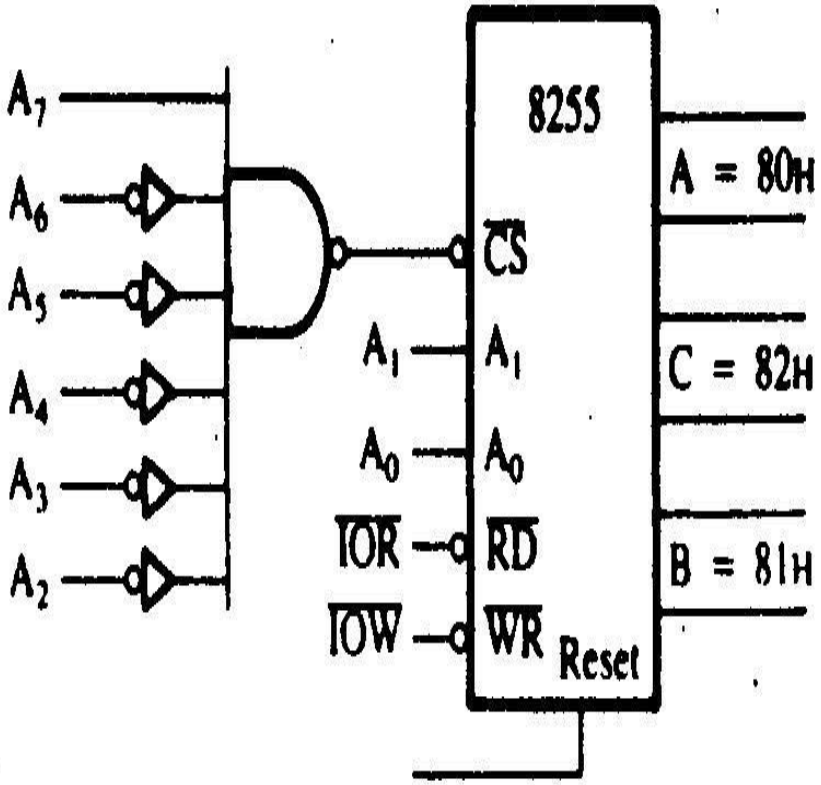


(a)



(b)

FIGURE 15.2 ... Functional Version of the Control Logic and I/O Ports (b)



(a)

$\overline{CS}$		Hex Address	Port
A_7 A_6 A_5 A_4 A_3 A_2	A_1 A_0		
1 0 0 0 0 0	0 0	= 80H	A
	0 1	= 81H	B
	1 0	= 82H	C
	1 1	= 83H	Control Register

(b)

FIGURE 15.3

8255A Chip Select Logic (a) and I/O Port Addresses (b)

CONTROL WORD

The bit D_7 specifies either the I/O function or the Bit Set/Reset function as classified in Figure 15.1(b). Figure 15.4 shows the control word format for I/O Mode.

To communicate with the peripherals through the 8255A, three step are necessary through the 8255A, three steps are necessary:

1. Determine the addresses of ports A, B, and C and of the control register according to the Chip Select logic and A_0 and A_1.
2. Write a control word in the control register.
3. Write I/O instructions to communicate through ports A, B, and C.

15.1.2 Mode 0: Simple Input or Output

In this mode, ports A and B are used as two simple 8-bit I/O ports and port C as two 4-bit ports. Each port (or half-port, in case of C) can be programmed to function as simply an input port or an output port. The input/output features in Mode 0 are as follows:

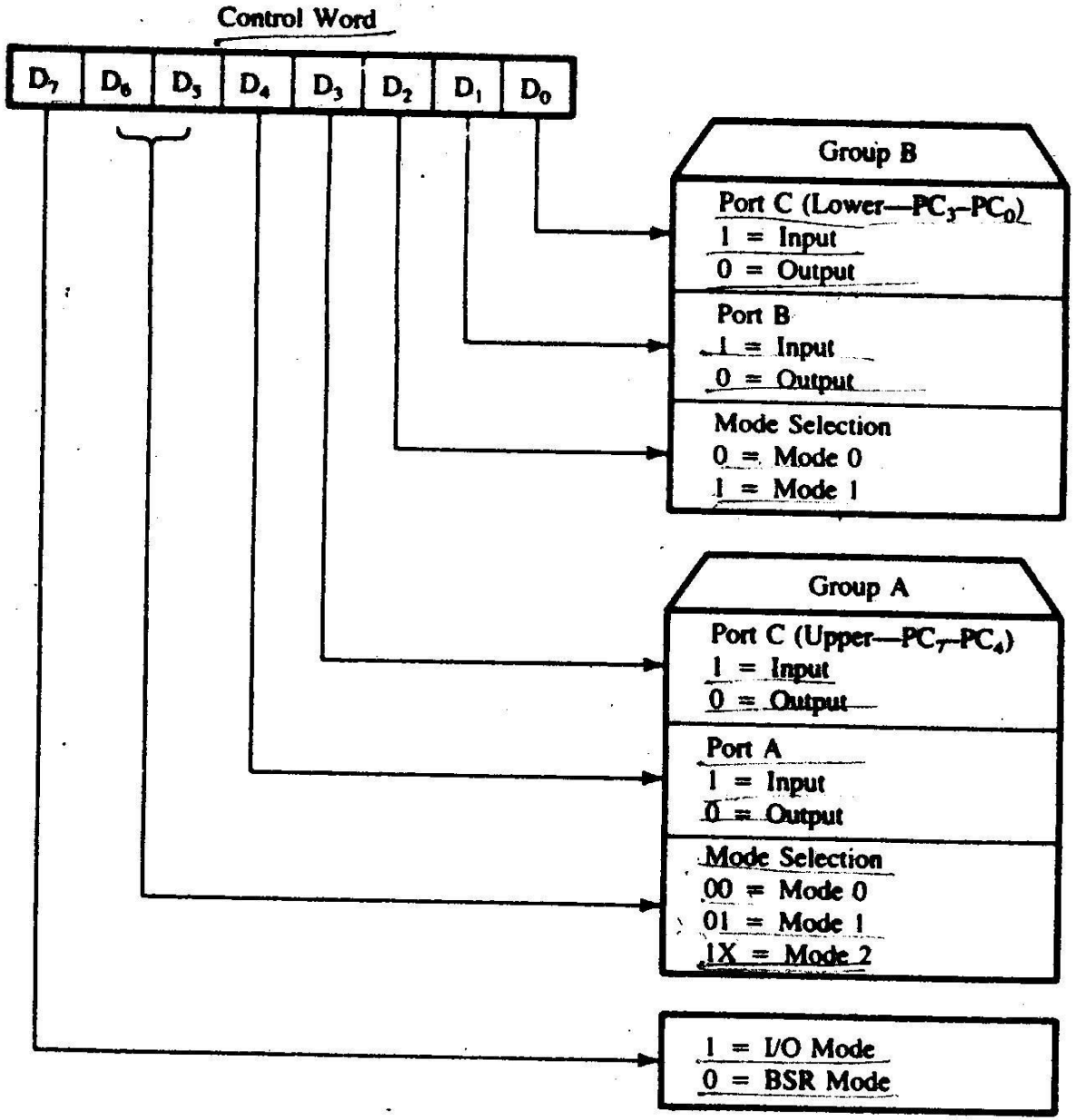


FIGURE 15.4
8255A Control Word Format for I/O Mode

SOURCE: Adapted from Intel Corporation, *Peripheral Components* (Santa Clara, Calif.: Author, 1993), p. 3–104.

1. Outputs are latched.
2. Inputs are not latched.
3. Ports do not have handshake or interrupt capability.

Example 15.1:

1. Identify the port addresses in Figure 15.5.
2. Identify the Mode 0 control word to configure port A and port C_U as output ports and port B and port C_L as input ports.
3. Write a program to read the DIP switches and display the reading from port B port A and from port C_L at port C_U.

Solution:

1. Port Addresses

Port A = 8000H (A_1=0, A_0=0)
Port B = 8001H (A_1=0, A_0=1)
Port C = 8002H (A_1=1, A_0=0)
Control Register = 8003H (A_1=1, A_0=1)

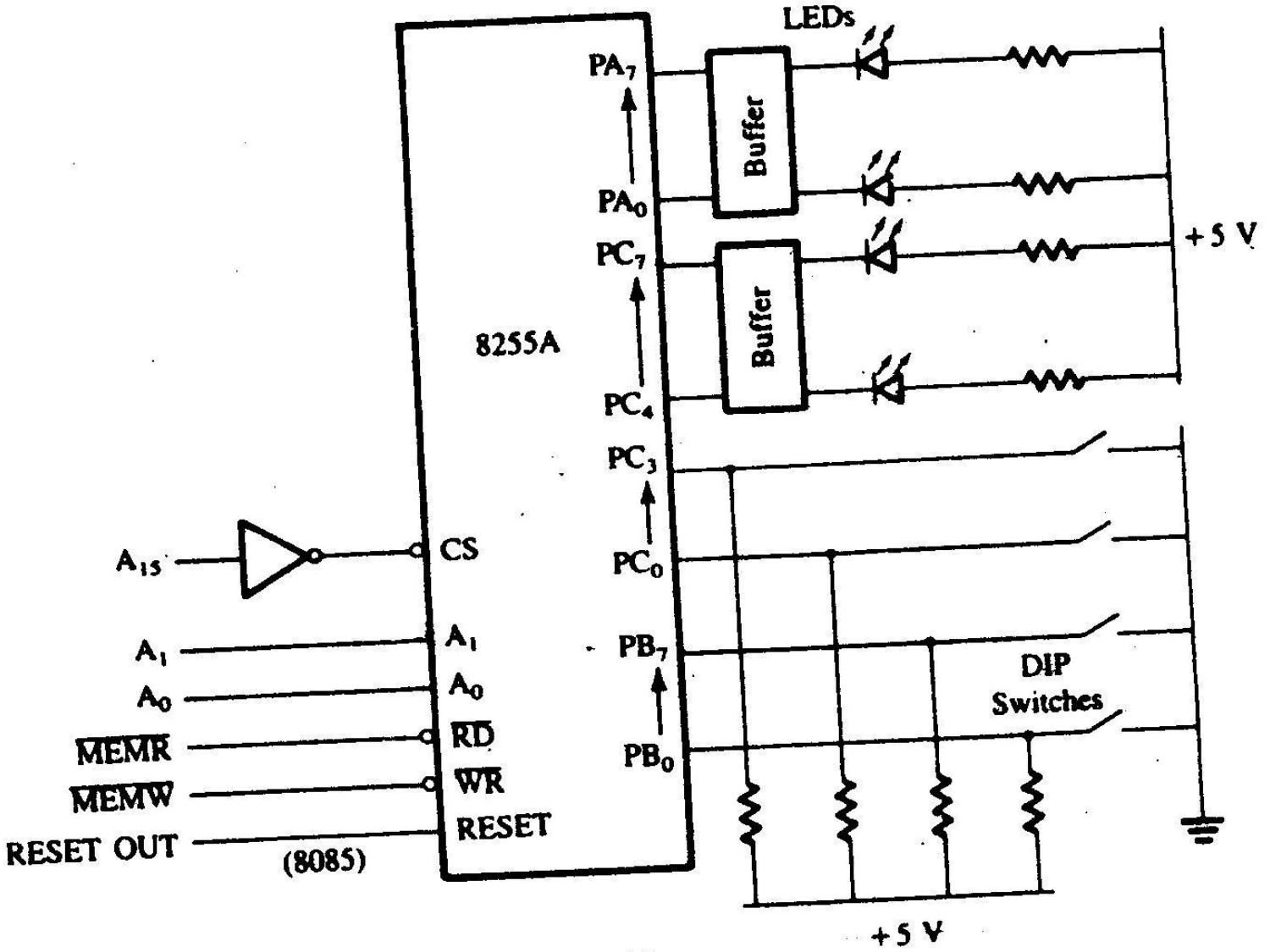


FIGURE 15.5
Interfacing 8255A I/O Ports in Mode 0

2. Control Word

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1	0	0	0	0	0	1	1	= 83H

3. Program

```
MVI A,83H
STA 8003H
LDA 8001H
STA 8000H
LDA 8002H
ANI 0FH
RLC
RLC
RLC
RLC
STA 8002H
HLT
```

B -> A
CL -> CU

A = 8000h
B= 8001H
C=8002H
Control Register=8003H

15.1.3 BSR (Bit Set/Reset) Mode

The BSR mode is concerned only with the eight bits of port C, which can be set or reset by writing an appropriate control word in the control register. A control word with bit D_7=0 is recognize as a BSR control word, and it does not alter any previously transmitted control word with bit D_7=1; thus the I/O operations of ports A and B are not affected by a BSR control word. In the BSR mode, individual bits of port C can be used for applications such as an on/off switch.

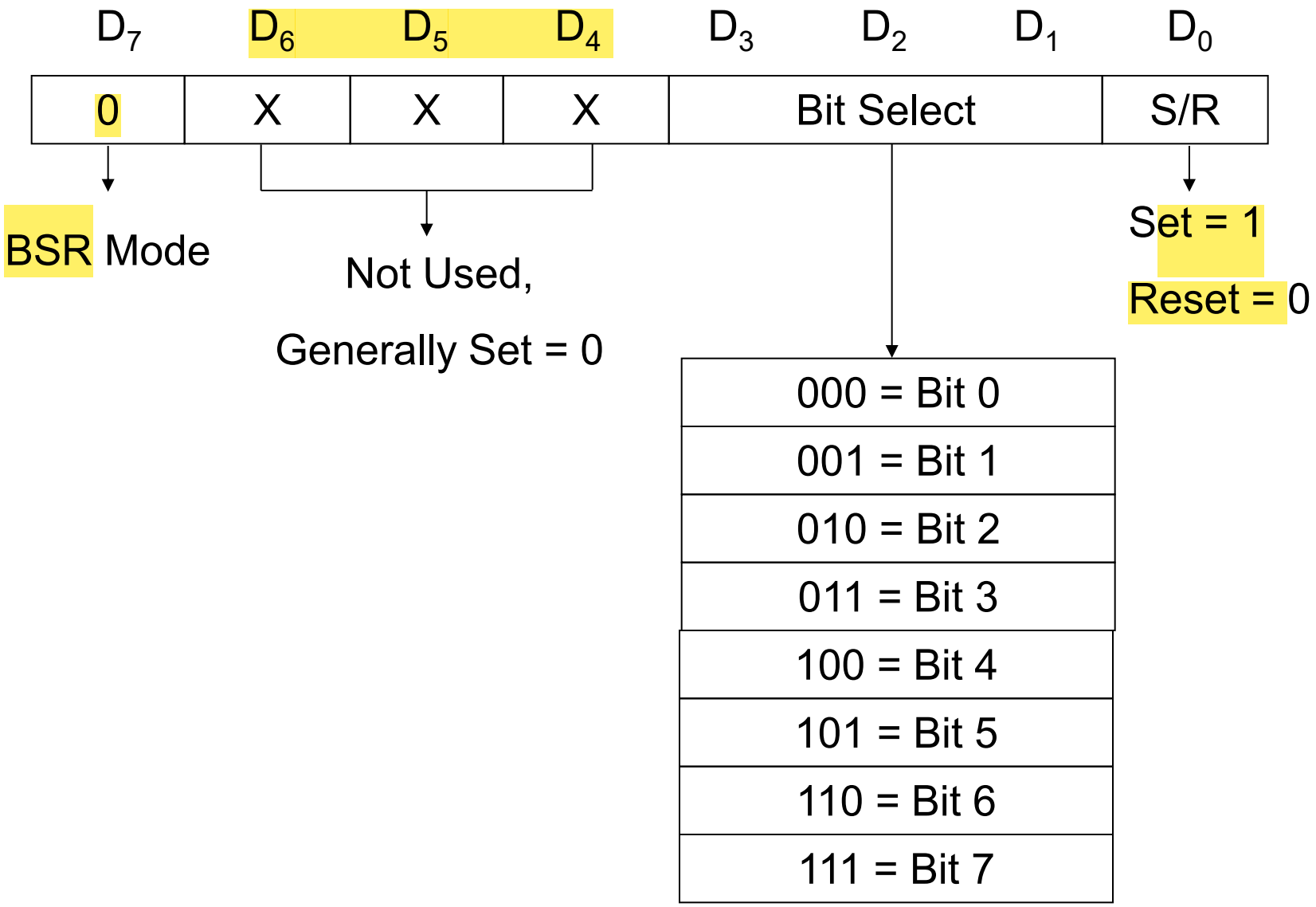
BSR CONTROL WORD

This control word, when written in the control register, sets or resets one bit at a time, as specified in Figure 15.6.

Example 15.2 :

Write BSR control word subroutine to set bits PC_7 and PC_3 and reset them after 10 ms. Use the schematic in Figure 15.3 and assume that a delay subroutine is available.

Figure 15.6 : 8255A Control Word Format in the BSR Mode



BSR Control Words

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
To set bit PC_7 =	0	0	0	0	1	1	1	1	= 0FH
To reset bit PC_7 =	0	0	0	0	1	1	1	0	= 0EH
To set bit PC_3 =	0	0	0	0	0	1	1	1	= 07H
To reset bit PC_3 =	0	0	0	0	0	1	1	0	= 06H

PORT ADDRESS

Control register address = 83H; refer to Figure 15.3(b).

SUBROUTINE

```
BSR:    MVI A, 0FH
        OUT 83H
        MVI A,07H
        OUT 83H
        CALL DELAY
        MVI A,06H
        OUT 83H
        MVI A,0EH
        OUT 83H
        RET
```

15.4 THE 8254 (8253) PROGRAMMABLE INTERVAL TIMER

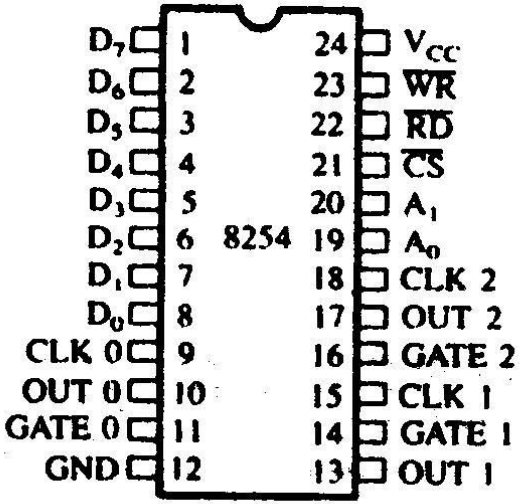
The 8254 programmable interval timer/counter is functionally similar to the software designed counters and timers described in chapter 8. It generates accurate time delay and can be used for applications such as a real-time clock, an event counter, a square-wave generator, and a complex waveform generator.

The 8254 includes three identical 16-bit counters that can operate independently in any one of the six modes. It is packaged in a 24-pin DIP and requires a single +5v power supply. To operate a counter, a 16-bit count is loaded in its register and, on command, begins to decrement the count until it reaches 0. At the end of the count, it generates a pulse that can be used to interrupt the MPU. The counter can count in binary or BCD. In addition, count can be read by the MPU while counter is decrementing.

15.4.1 Block Diagram of the 8254

Figure 15.23 is the block diagram of the 8254; it includes three counters (0, 1, 1 and 2), a data bus buffer, Read/Write control logic, and a control register. Each counter has two input signals-Clock (CLK) and GATE-and output signal-OUT.

Pin Configuration



Pin Names

D_7–D_0	Data Bus (8 Bit)
CLK N	Counter Clock Inputs
GATE N	Counter Gate Inputs
OUT N	Counter Outputs
$\overline{RD}$	Read Counter
$\overline{WR}$	Write Command or Data
$\overline{CS}$	Chip Select
A_0–A_1	Counter Select
V_{CC}	+5 Volts
GND	Ground

Block Diagram

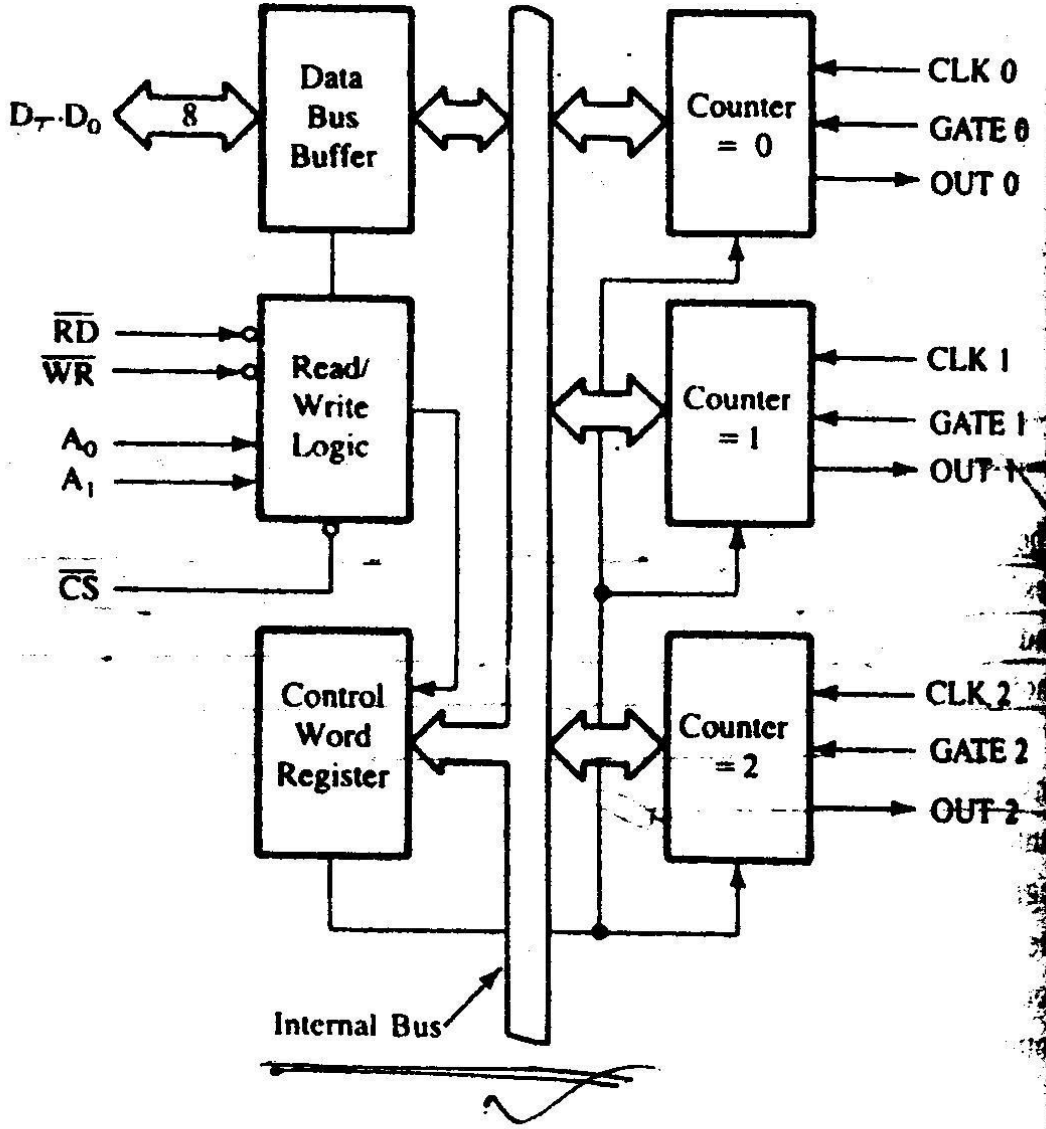


FIGURE 15.23
8254 Block Diagram

SOURCE: Intel Corporation, *Peripheral Components* (Santa Clara, Calif.: Author, 1993), p. 3–62.

CONTROL LOGIC

A_0	A_1	Selection
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Register

CONTROL WORD REGISTER

The control word format is shown in Figure 15.24. book- 508

MODE