



SECTION A
[ANSWER ANY THREE OF THE FOLLOWINGS]

- ✓(a) 'Parallel computing is the simultaneous use of multiple computing resources to solve a computational problem'. Give some real-life examples. Write the main challenges for parallel computing. 1 [3.50]
- (b) What are the levels of parallel processing? Explain each of the levels with at least one example. 2 [4.00]
- (c) Does parallel processing differ with multiprocessing? Explain your answer. 3 and qs [1.25]
- ✓(a) What do you mean by 'Flynn's Taxonomy'? Explain how SIMD and MIMD computers work with instructions and data. 4-6,7,10,11 [4.50]
- (b) 'Parallelism can be achieved in uniprocessor system using some hardware and software technologies' - what are they? 3 - 6 to 14 [2.00]
- (c) Explain how parallelism can be achieved using multiprogramming and time-sharing methods. 3 - 14 and qs [2.25]
- ✓(a) 'Data dependency is a situation in which a program statements refer to the data of a preceding statement'. What are the types of it? Explain with examples. 17 - 5 to 12 [4.00]
- (b) Consider the following code fragment of a program— 17- 11 [2.75]
*S1: Load R1,A
S2: Add R2,R1
S3: Move R1,R3
S4: Store B,R1*
Find the dependencies between the statements in the code fragment.
- (c) Explain how I2 is resource dependent on I1 in the fragment given below— [2.00]
*I1: A=B+C
I2: D=G+H*
Hence, draw the dependency graph. 17 - 15
- ✓(a) Define the following terms: (i) Speedup, (ii) Efficiency, (iii) Throughput. 24 - 14 to 16 [3.00]
- (b) A five-stage linear pipeline has clock period of $\tau=100\text{ns}$, and $n=50$ tasks. What is its throughput, efficiency and speedup? qs [3.25]
- (c) A CPU of modern computer is a good example of linear pipeline. Explain. qs [2.50]



SECTION B
[ANSWER ANY THREE OF THE FOLLOWINGS]

- 5.(a) What are the abstract parallel programming models over the hardware and memory architectures? Compare the relative advantages and disadvantages of *shared memory model* with *message passing model*. [4.75]
- (b) What do you mean by MPI? Discuss the purposes and uses of the followings— [4.00]
 i) MPI_Init, ii) MPI_Finalize, iii) MPI_Send and iv) MPI_Recv
- ✓ 6.(a) What is cache coherency? With a suitable example, explain how cache becomes incoherent due to the *write-access* of shared variables from multiple number of processors. 14 - 2 to 12 [4.00]
- (b) When two processors P_1 and P_2 have same data element X in their local caches and one processor modifies the value of X to Y , then the processor's cache becomes inconsistent with the other's processor's cache and the shared memory. Explain this inconsistency problem for the situations of both *data Sharing* and *process Migration*, in terms of *write-through* and *write-back* policies. Use suitable examples and figures. 14- 13 to 16 [4.75]
- 7.(a) Suppose you have an array {12, 14, 6, 8, 10, 16, 2, 4}, show all the phases of sorting the array using odd-even transposition sort algorithm. [4.50]
- (b) Write a program using OpenMP to implement the odd-even transposition sort algorithm. [4.25]
- ✓ 8.(a) Define linear and non-linear pipelines. Discuss their differences. 282930 - 6 [3.75]
 (b) Consider the following reservation table of a three-stage non-linear pipeline to execute a function X. [5.00]

		Time-->							
		1	2	3	4	5	6	7	8
Stage	S1	X					X		X
	S2		X		X				
	S3			X		X		X	
Reservation Table for function X									

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- i) What are the forbidden and permissible latencies?
- ii) Calculate the collision vector.
- iii) Draw the state transition diagram.

$$s_1 = \{(6-1), (8-1) | (8-1)\} = 5, 2, 7.$$

$s_2 :$

$c_7 \ c_6 \ c_5 \ c_4 \quad j$

University of Rajshahi
Department of Computer Science & Engineering
B.Sc. Engineering Part IV Odd Semester Examination 2020
Course Code: CSE 4111
Course Title: Parallel Processing and Distributed System

Full Marks: 52.5

Time: 3 Hours

[Answer any SIX (06) questions taking THREE (03) from each section]

Section A

1.
 - a) Why are we developing parallel systems instead of sequential systems? **1-3 to 8** 3
 - b) Why do we need to write parallel programs? **1-6** 2.75
 - c) How can we exploit instruction level parallelism and loop level parallelism? **2-4,5** 3

2.
 - a) If we fetch a cache line from main memory, where in the cache should it be placed? **3.25** 1
 - b) What is the bottleneck of Von Neumann architecture? **../lec-2 - 2** 1
 - c) Explain which function is **thread safe** and which is not. 2
 - d) What are the limitations of MPI_Scatter and MPI_Gather functions? **2.50** 2.50

3.
 - a) What are the key characteristics of a vector processor? 2.75
 - b) Does false sharing generate incorrect result? Explain the effects of false sharing. 3
 - c) What is cache coherence problem? Write a program to illustrate the cache coherence problem. **2021 6a (solved)** 3

4.
 - a) How can the receiver find out the following values in MPI? 3.75
 - 1. The amount of data in the message.
 - 2. The sender of the message.
 - 3. The tag of the message.
 - b) Why do we need MPI_Reduce and MPI_Allreduce function? Show the communication pattern of MPI_Allreduce. 3
 - c) Write short notes on GPU. 2

Section B

5.
 - a) Why do we use MPI_Ssend instead of MPI_Send? 2
 - b) A set of numbers (15, 11, 9, 16, 3, 14, 8, 7, 4, 6, 12, 10, 5, 2, 13, 1) and four processes are given. Show how the processes can sort the numbers using parallel odd-even transposition sort. 3.25
 - c) Write a program in MPI to sort a set of numbers using parallel odd-even transposition sort algorithm. 3.50

6.
 - a) Define grain size and latency. 2
 - b) Define different types of data dependence. **2021 3a -solved** 3.25
 - c) What are the steps of grain packing? Explain with an example. 3.50

7.
 - a) Can multiple threads simultaneously insert new nodes into a linked list without any problem? If not, explain how to insert the nodes and write a code segment to insert the nodes by multiple threads. 3.25
 - b) How can we synchronize threads? 3
 - c) What is mutex? Write a program using mutex. 2.50

8. a) What are the problems of busy-waiting? **qs** 2.50
b) Define critical section and race condition. **qs** 2.50
c) fibo[0] = fibo[1] = 1; 3.75
pragma omp parallel for num_threads(thread_count)
for (i = 2; i < n; i++)
fibo[i] = fibo[i-1] + fibo[i-2];
What will be the results if we try running the above code with more than one
thread?

Section A

Answer any THREE questions.

1. **(a)** What do you mean by parallel processing? 1 - 3 to 5
(b) Discuss different types of data dependence. 2021 3a -solved 2
(c) Two 3x3 matrices A and B are given to compute the sum of the nine elements in the resulting product matrix C=AxB. On the other hand, 150 cycles for inter-processor communication latency, 80 cycles for the nodes performing multiplication, 15 cycles for the nodes performing addition are given. Draw a fine-grain program graph. Perform grain packing and parallel scheduling. 3.5
(d) What is data-flow computer? Write a simple C program and draw its dataflow graph. 2.25
2. **(a)** How can you define speedup factor, efficiency and throughput of a k-stage pipeline processor over an equivalent non pipelined processor? 24 - 13 to 16 2.75
(b)

	1	2	3	4	5	6
S1	X					X
S2		X			X	
S3			X			
S4				X		
S5		X				X

 Considering the above reservation table
 (a) List the set of forbidden latencies and the collision vector
 (b) Draw the state transition diagram 3132333435 - 10
 (c) Determine the minimum average latency of this pipeline
(c) Write some applications of vector processor? 1
3. **(a)** Define instruction set. Briefly discuss complex instruction set and reduced instruction set. 4.75
(b) Differentiate among scalar, superscalar, and vector processor. 2
(c) Which type of memory interleaving can tolerate memory fault and which cannot? Explain. 2
4. **(a)** What is CUDA kernel function? 1.5
(b) What are the effects of launching CUDA kernel functions? 2.25
(c) Two vectors are given. Write a CUDA kernel to perform addition of two vectors. 3
(d) How can you set grid and thread block dimensions in CUDA programming? 2

Section B
Answer any THREE questions.

5. (a) Define bisection width and bisection bandwidth. 2
(b) Discuss snooping cache coherence and directory-based cache coherence method. pdf - 15,16 4
(c) Write down the Amdahl's law. 6 - 1 to 7 2.75
6. (a) Write a program to read a vector and distribute it among processes using MPI provided function. 3.25
(b) Sort the numbers 15, 11, 9, 16, 3, 14, 8, 7, 4, 6, 12, 10, 5, 2, 13, 1 using parallel odd-even transposition sort algorithm. 3.5
(c) What is the purpose of using Allgather() function in MPI? 2
7. (a) What is false sharing? Explain with an example. 2.25
(b) What are the differences among mutex, busy-waiting and semaphore? 3
(c) Can multiple threads simultaneously delete nodes of a linked list without any problem? If not, explain how to delete the nodes and write a code segment to delete the nodes by multiple threads. 3.5
8. (a) Mention the desired features of a parallel language. 2
(b) Convert the following sequential code to vector code:
DO 20 I=1, N
 A(I)=B(I-1)
20 20 B(I)=2*B(I) 2
(c) Describe the following optimization of vector functions:
 (i) Redundant express elimination.
 (ii) Constant folding at compile time 2.75+2

University of Rajshahi
 Department of Computer Science and Engineering
 B.Sc. (Engg.) Part-4, Odd Semester, Examination-2018
 Course: CSE4111 (Parallel Processing and Distributed System)
 Marks: 52.5 Time: 3:00 Hours

[N.B. Answer any Six questions taking Three from each section]

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Section-A

1. (a) Why are we developing parallel systems instead of sequential systems? 3
- (b) If a fraction r of our serial program remains unparallelized, then Amdahl's law says we can't get a speedup better than $1/r$. Illustrate with an example.
- (c) Suppose S is a shared variable that is initialized to 3. A_0, B_0 and C_0 are private and owned by core 0, on the other hand A_1, B_1, C_1 and A_2 are private and owned by core 1. What will be the value of A_2 after executing the following statements? 3.75
 How to solve the problem (if you find any)?

Time	Core 0	Core 1
0	$A_0=S;$	$A_1=3*S;$
1	$S=5;$	$B_1=C_1+1;$
2	$B_0=C_0+2;$	$A_2=4*S;$

2. (a) What happens when multiple processes first call MPI_Send simultaneously and then call MPI_Recv? How can you make your program safe if it is unsafe due to the use of MPI_Send and MPI_Recv? 3
- (b) Explain why we use MPI_Allgather. 2
- (c) Write an MPI program that implements multiplication of a vector by a scalar and dot product. The user should enter two vectors and a scalar, all of which are taken by process 0 and distributed among the processes. The results are calculated and collected from process 0, which prints them. You can assume that n , the order of the vectors, is evenly divisible by comm_sz. 3.75
3. (a) Suppose you have an array {12, 14, 6, 8, 10, 16, 2, 4}, show all the phases of sorting the array using odd-even transposition sort algorithm. 4.75
- (b) Write an OpenMP program to implement the odd-even transposition sort algorithm. 4
4. (a) Discuss the efficiency of pipelined processor over non pipelined processor for a single instruction? qs 3
- (b) What is pipelining? To perform pipelining in a processor what steps must be followed. qs 2
- (c) Draw and explain the structure of a linear pipeline for floating-point multiplication. 3.75

Section-B

1.75

5. (a) Define software parallelism and hardware parallelism. *3 - 6 to 14* 3
 (b) Is there any relation between software parallelism and hardware parallelism? Explain. *qs and google -pdf* 3
 (c) Perform a data dependence analysis on each of the following two program segments. Show the dependence graphs among the statements with justification. 4
 (i) S1: $A=B+D$ (i) S1: $X=\sin(Y)$ 1819 - 2 to 5
 (ii) S2: $C=Ax3$ (ii) S2: $Z=X+W$
 (iii) S3: $A=A+C$ (iii) S3: $Y=-25xW$
 (iv) S4: $E=A/2$ (iv) S4: $X=\cos(Z)$

6. (a) How to eliminate communication delays between processors through node duplication? Illustrate with an example. 3
 (b) Suppose two 2×2 matrices A and B are multiplied to compute the sum of the four elements in the resulting product matrix $C=AxB$. Draw a fine-grain program graph assuming each node requires 101 CPU cycles for multiplication, 8 CPU cycles for addition and 212 CPU cycles for inter-processor communication latency. Perform grain packing and show sequential schedule (before grain packing) and parallel schedule for 4 and 6 processors (after grain packing). 5.75

7. (a) Consider the following reservation table

5

	1	2	3	4	5	6	7	8
S1	X					X		
S2		X		X				X
S3			X		X		X	

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- (i) List the set of forbidden latencies and the collision vector
 (ii) Draw a state transition diagram showing all possible initial sequences (cycles) without causing a collision in the pipeline
 (iii) List all the simple cycles from the state diagram
 (b) What is the function of scoreboard in dynamic instruction scheduling? 2.75
 (c) How to calculate throughput of a pipeline? *24 - 16* 1

8. (a) Define distributed system? Why distributed systems to be needed? *8 - 9 to 11* 3
 (b) Differentiate between parallel and distributed systems. *qs* 2
 (c) What kind of naming services do you know? Why do distributed systems need this function? 2
 (d) What is distributed deadlock and why are they hard to detect? *qs* 1.75

Answer any three questions from each part.

Part-A

1. (a) What is meant by the term 'Parallel Processing'? Can you discuss the general trends in parallel processing? **1 - 8** 4
- (b) What is 'Vector Processor'? Why do we need such processors? 2.75
- (c) Can you give us a comparative study between vector and scalar processors? 2
2. (a) Discuss different types of data dependence. **2021 3a -solved** 2.5
- (b) What are the steps of grain packing? Discuss with an example. 3.75
- (c) What is data-flow computer? Write a program and draw its dataflow graph. 2.5
3. (a) Define Whetstone results. TPS and KLIPS ratings. 3
- (b) Explain harmonic mean speedup performance for a multiprocessor operating in n execution modes with respect to probability distributions. 4
- (c) Define average parallelism. 1.75
4. (a) What are the reasons behind the development of reduced instruction sets. 2
- (b) Draw the architecture of MC68040 microprocessor and discuss its major units. 3.5
- (c) Explain the concept of using overlapped register windows introduced by the Berkeley RISC architecture. 3.25

Part-B

5. (a) What do you know about the distributed database? **lec-4** 1
- (b) Describe the horizontal and vertical fragmentation of distributed database. **lec-4 6** 3.75
- (c) Describe the failures handling techniques in two-phase commit protocol. 4
6. (a) Define reservation table. 1
- (b) 4.75

	1	2	3	4	5	6
S1	X					X
S2		X			X	
S3			X			
S4				X		
S5		X				X

Considering the above reservation table:

- (a) List the set of forbidden latencies and the collision vector.
- (b) Draw the state transition diagram.
- (c) Determine the minimum average latency of this pipeline.
- (c) Explain how to reduce minimal average latency. 3

7. (a) What are the challenges in the development of future general-purpose supercomputers? 3
 (b) Discuss different types of vector instructions. 3.75
 (c) Draw the architecture of Fujitsu VP2000 series supercomputer and discuss its major units. 3

8. (a) Consider the following pure scalar loop:

```
Do K = 1, 2048
  A(K) = A(K) + S
Enddo
```

Explain how to reduce the execution time by vector, scalar-concurrent, vector-concurrent and concurrent outer/vector inner (COVI) modes.

- (b) Consider the following loop: 2

```
Do I = 1, N
  A(I) = B(I)
  C(I) = A(I) + B(I)
  E(I) = C(I+1)
Enddo
```

Show how to vectorize the code.

- (c) Consider a basic block of bubble sort program.

3.75

t8	=	j - 1	}	temp := A[j]
t9	=	4 * t8		
temp	=	A[t9]		
t10	=	j + 1	A[j+1]	
t11	=	t10 - 1		
t12	=	4 * t11		
t13	=	A[t12]		
t14	=	j - 1	A[j] := A[j+1]	
t15	=	4 * t14		
A[t15]	=	t13		
t16	=	j + 1	A[j+1] := temp	
t17	=	t16 - 1		
t18	=	4 * t17		
A[t18]	=	temp		

Show its corresponding DAG representation.