Chapter-3

8085 Microprocessor Architecture and Memory Interfacing

3.1 THE 8085 MPU

Microprocessor Unit (MPU)

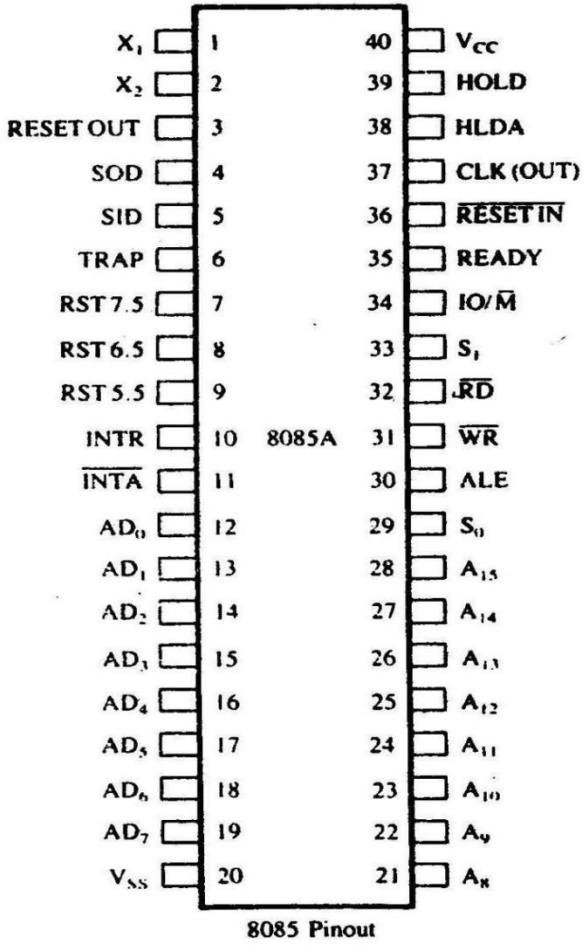
- The term microprocessor unit (MPU) define as a group of devices (as a unit) that can communicate with peripherals, provide timing signals, direct data flow, and perform computing tasks as specified by the instructions in memory.

Using above description, the 8085 microprocessor can almost qualify as an MPU, but with the following two limitations:

1. The low-order address bus of the 8085 microprocessor is multiplexed (time-shared) with the data bus. The buses need to be demultiplexed.
2. Appropriate control signals need to be generated to interface memory and I/O with the 8085.

3.11 The 8085 Microprocessor

- The 8085A commonly known as the 8085
- It is an 8-bit general-purpose microprocessor
- It is capable of addressing 64K of memory.
- It has 40 pins and requires +5V power supply.
- It can operate with a 3-MHz clock frequency.
- It is an enhanced version of its predecessor 8080A.



8085 Pinout

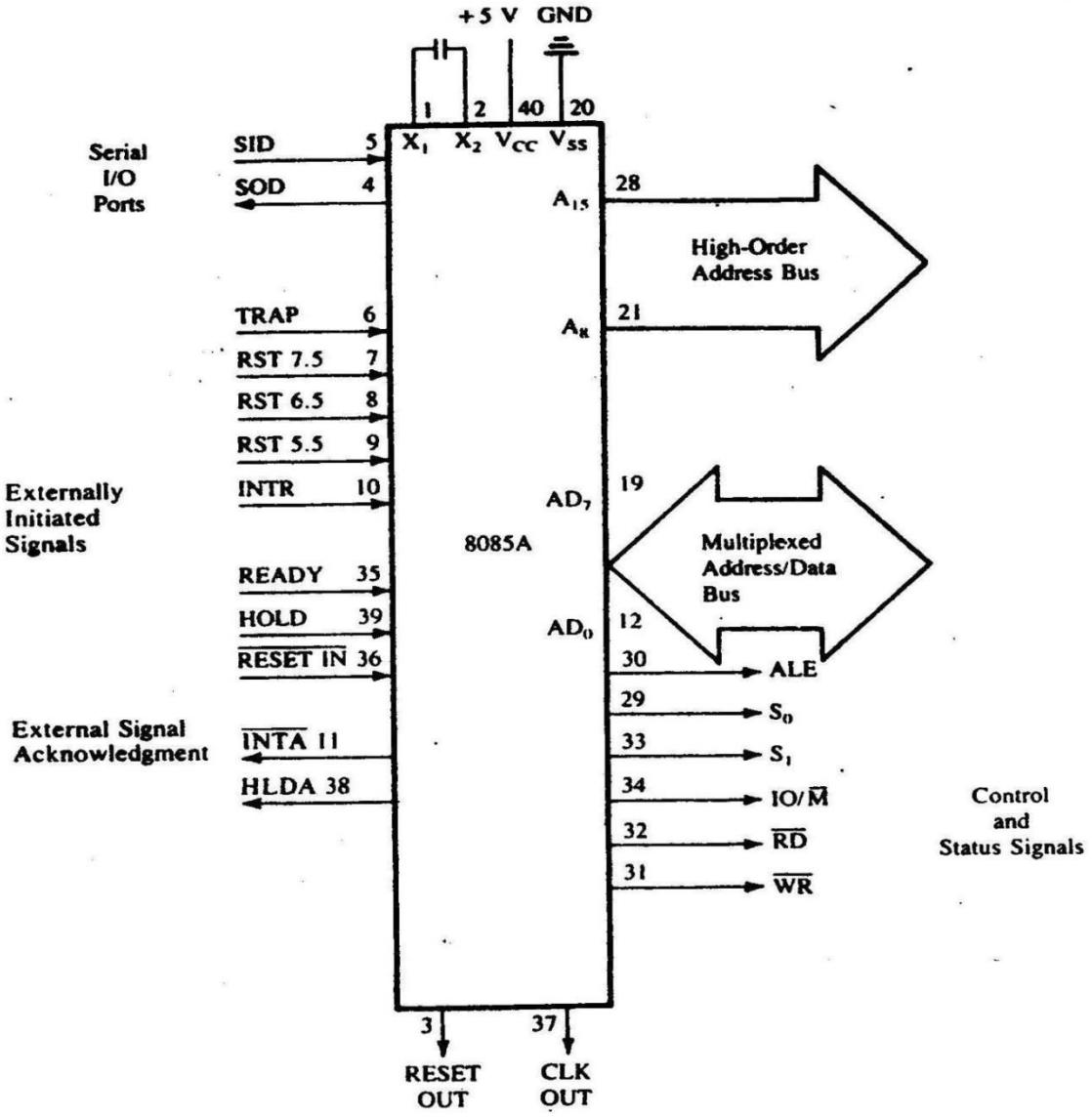


FIGURE 3.1
The 8085 Microprocessor Pinout and Signals

NOTE: The 8085A is commonly known as the 8085.
SOURCE (Pinout): Intel Corporation, *Embedded Microprocessors* (Santa Clara, Calif.: Author, 1994), pp. 1-11.

Figure 3.1 shows the logic pinout of the 8085 microprocessor. All the signal can be classified into six groups:

1) Address bus.
2) Data bus.
3) Control and status signals.
4) Power supply and frequency signals.
5) Externally initiated signals.
6) Serial I/O ports.

ADDRESS BUS

- A_{15} - A_8 are unidirectional and high order address bus.

MULTIPLEXED ADDRESS/DATA BUS

- AD_7 - AD_0 are bidirectional and serve a dual purpose. During instruction fetch these are used as address lines and during operand fetch these are used as data lines.

CONTROL AND STATUS SIGNALS

Control and status signals indicate the nature of the operation.

- Control Signals: $\overline{RD}$ and $\overline{WR}$.
- Status Signals: IO/$\overline{M}$, S_1 , and S_0.
- Special Signal: ALE. Indicate the beginning of the operation.
- $\overline{RD}$: Low for read operation(active low).
- $\overline{WR}$: Low for write operation (active low).
- IO/$\overline{M}$: High for I/O operation (active high) and low for memory operation (active low).
- S_1 , and S_0 : Similar to IO/M and rarely used in small system.

ALE (Address Latch Enable)

- This is a positive going pulse and generated every time 8085 begins an operation; it indicates that bits on AD_7 - AD_0 are address bits. This signal are used to latch the low-order address bus an generate a separate set of eight address lines; A_7 - A_0

EXTERNALLY INITIATED SIGNALS INCLUDING INTERRUPT

TABLE 3.2
8085 Interrupts and Externally Initiated Signals

- INTR (Input)
- $\overline{\text{INTA}}$ (Output)
- RST 7.5 (Inputs)
- RST 6.5
- RST 5.5
- TRAP (Input)
- HOLD (Input)
- HLDA (Output)
- READY (Input)

3.12 Microprocessor Communication and Bus Timing

Example: The instruction code 01001111 (4FH-MOV C,A) is stored in memory location 2005H. Illustrate the data flow and list the sequence of events when the instruction code is fetched by the MPU.

Solution: To fetch the byte, the MPU performs the following steps:

Step 1: The program counter places the 16-bit memory address on the address bus (Figure 3.2).

Figure 3.3 shows that at T_1 the high-order address (20H) is placed on A_{15} - A_8 and the low-order address (05H) is placed on AD_7 - AD_0 , ALE goes high, $IO/\overline{M}$ goes low.

Step 2: The control unit sends the control signal $\overline{RD}$ to enable the memory chip (Figure 3.2).

Step 3: The byte from the memory location is placed on the data bus.

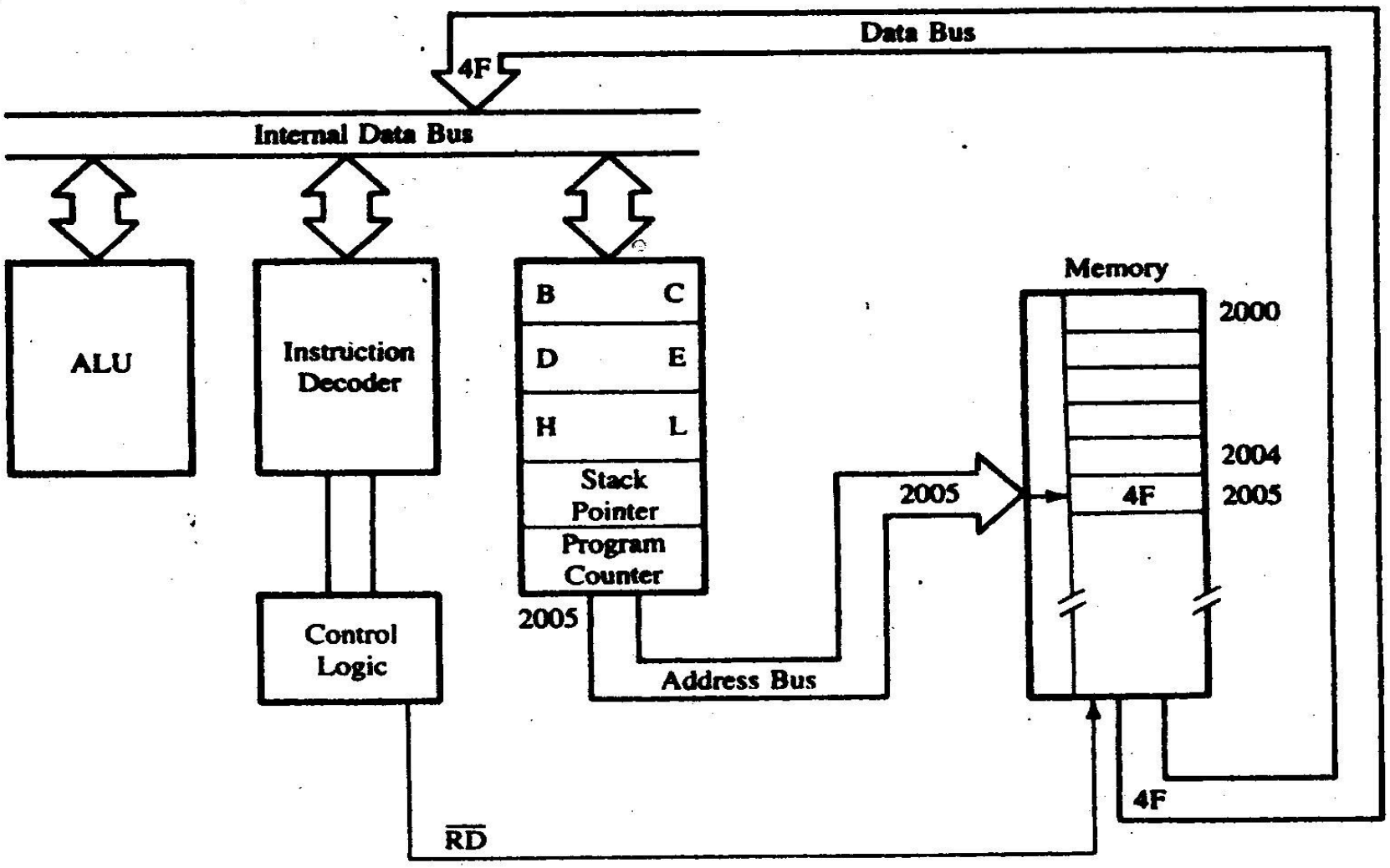


FIGURE 3.2
Data Flow from Memory to the MPU

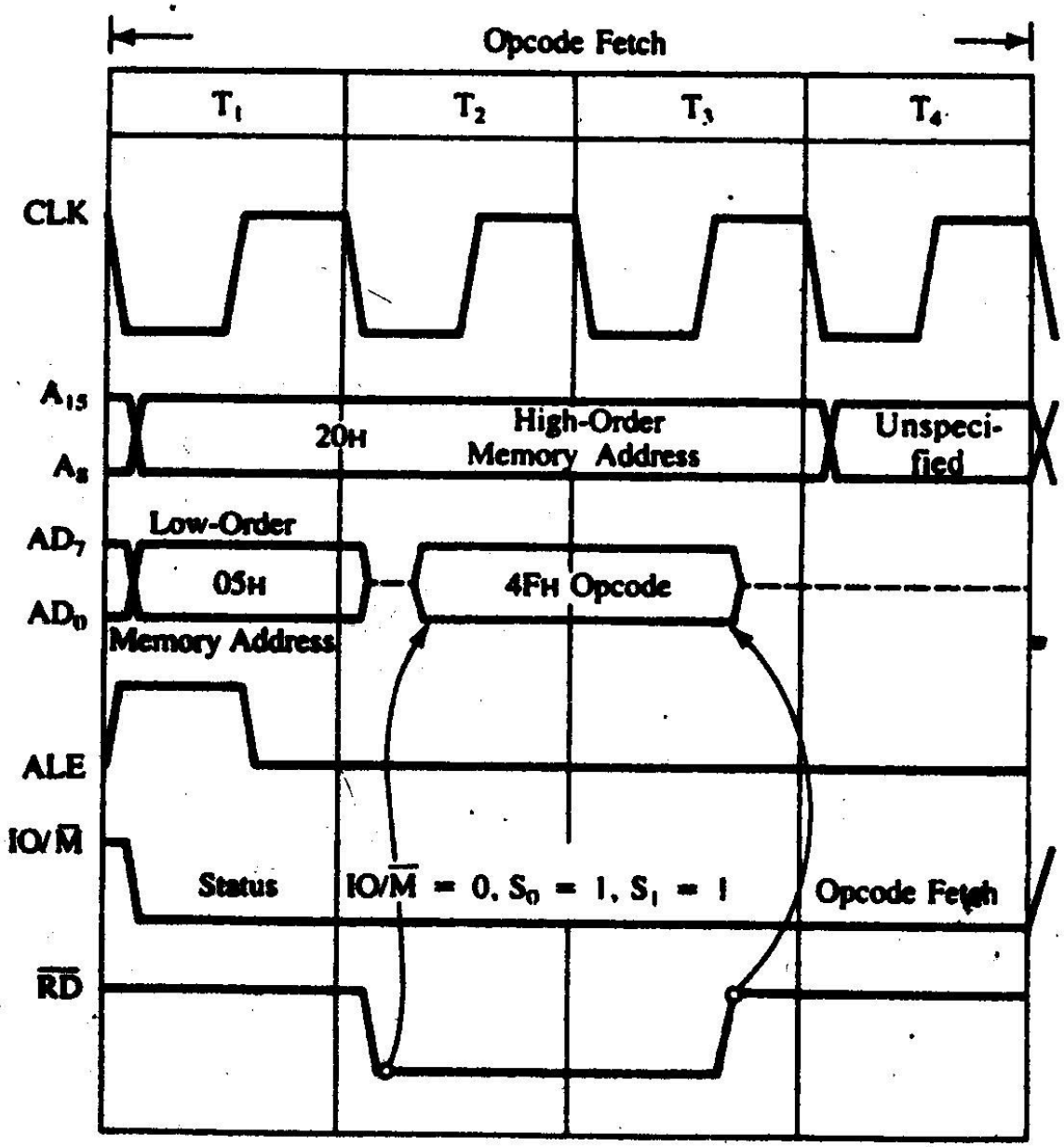


FIGURE 3.3
Timing: Transfer of Byte from Memory to MPU

The $\overline{RD}$ signal causes 4FH to be placed on bus AD_7 - AD_0 (shown by arrow).

Step 4: The byte is placed in the instruction decoder of the microprocessor, and the task is carried out according to the instruction.

3.13 Demultiplexing the Bus AD_7-AD_0

Figure 3.3 shows that the address on the high-order bus (20H) remains on the bus for three clock periods (T_1 to T_3). However, the low-order address (05H) is lost after the first clock period. The address needs to be latched for identifying the memory address. Otherwise, the address 2005H will change to 204FH after the first clock period.

Figure 3.4 shows that the uses of a latch (74LS373) and the ALE signal demultiplexes the low-order bus.

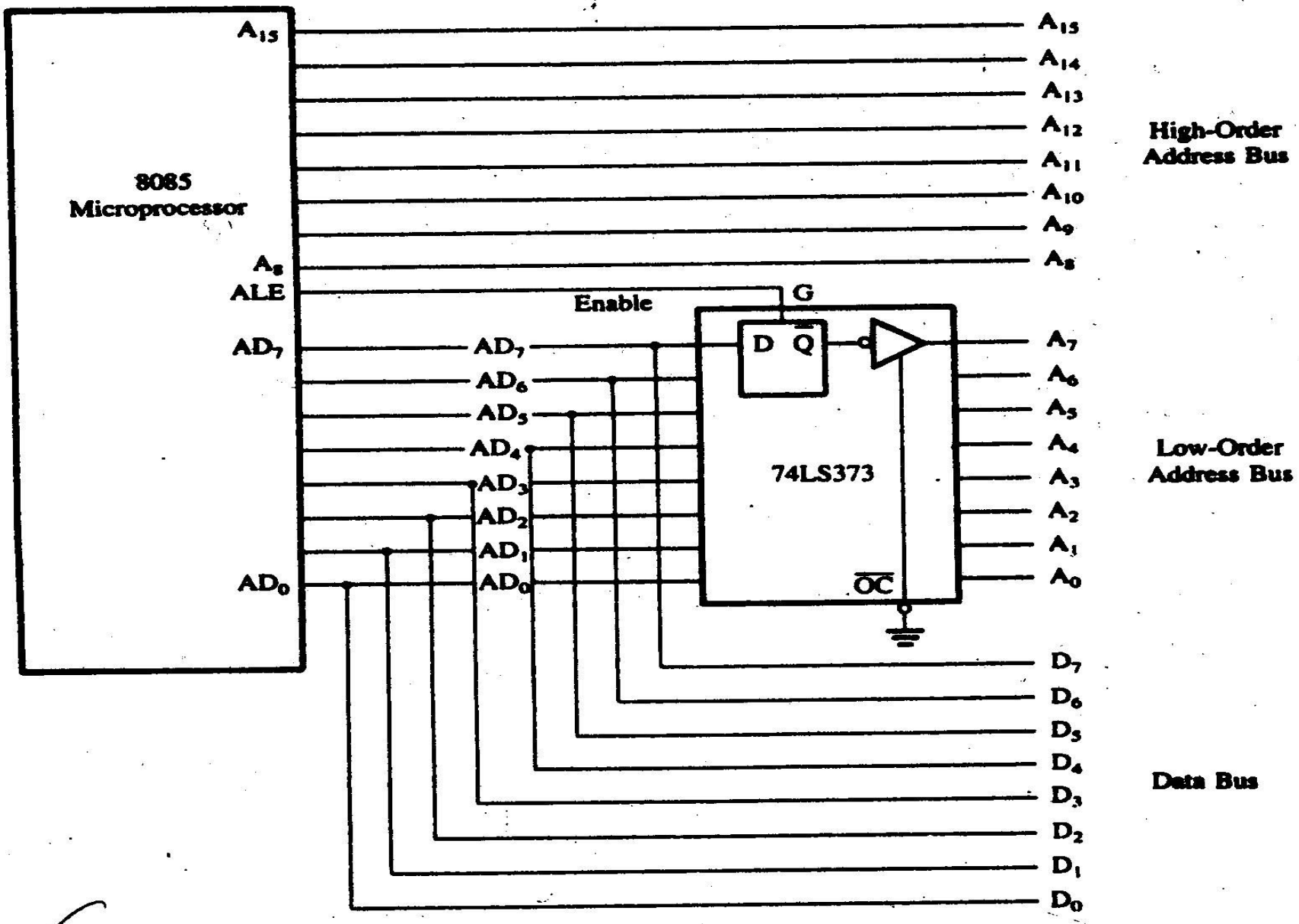


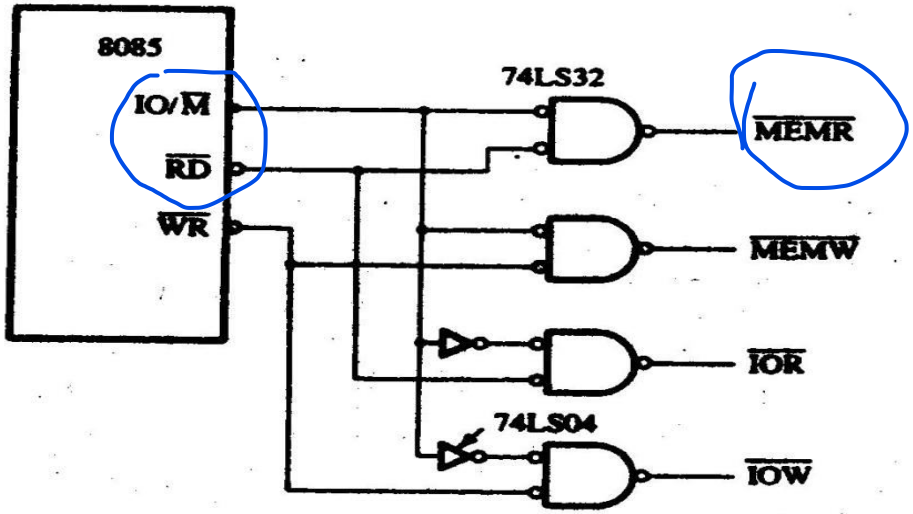
FIGURE 3.4
Schematic of Latching Low-Order Address Bus

Figure 3.3 shows that when the ALE is high (at T_1), the latch is transparent; this means the output changes according to the input data (05H).
When the ALE goes low, the data 05H is latched until the ALE becomes high again.

3.14 Generating Control Signals

Figure 3.5 shows that four control signals are generated by combining $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$.

FIGURE 3.5
Schematic to Generate Read/Write Control Signals for Memory and I/O



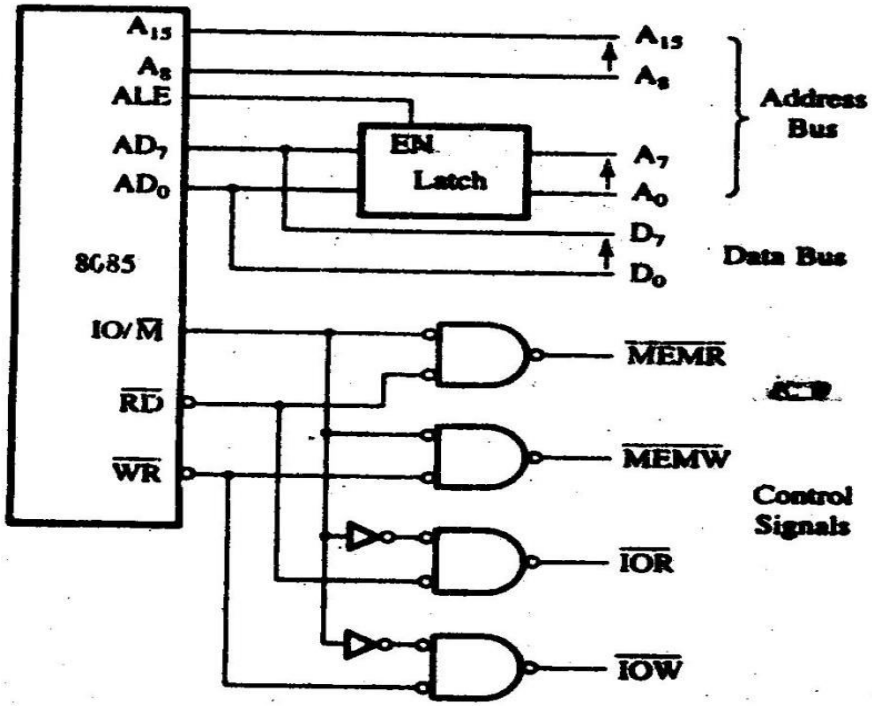
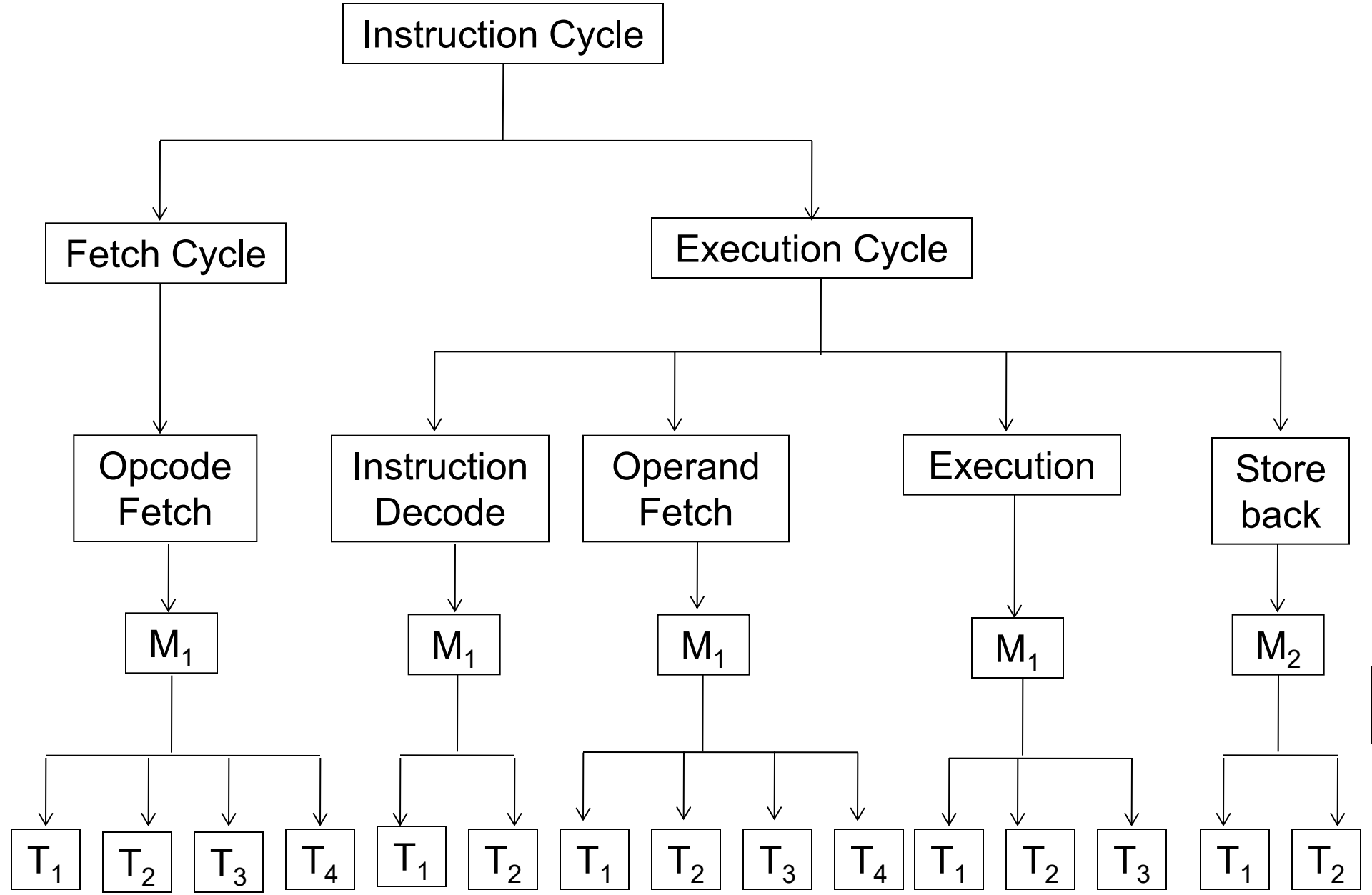


FIGURE 3.6
8085 Demultiplexed Address and Data Bus with Control Signals

3.21 The 8085 Machine Cycles and Bus Timing

To execute an instruction, 8085 needs to complete an instruction cycle. An instruction cycle is consisted of one or more machine cycles. A machine cycle is again consisted of two or more clock periods (T-states).

- Instruction cycle = Fetch cycle + Execution cycle
- Fetch cycle = Opcode fetch (from memory)
- Execution cycle = Opcode decode (in CPU) + Operand fetch [if necessary] (from memory) + Execution (in CPU) + Store back [optional] (to memory)


Instruction Cycle
Fetch Cycle
Execution Cycle
Opcode Fetch
Instruction Decode
Operand Fetch
Execution
Store back
M1
M1
M1
M1
M2
T1
T2
T3
T4
T1
T2
T1
T2
T3
T4
T1
T2
T3
T1
T2

3.22 Opcode Fetch Machine Cycle

To execute any instruction, 8085 at first fetches the opcode of the instruction and it requires a single machine cycle. In Figure 3.3 we have seen how the opcode 4FH (MOV C,A) is fetched from memory location 2005H.

3.23 Memory Read Machine Cycle (Operands-Data/Address)

In Figure 3.3 the instruction MOV C,A is a 1-byte instruction and only the opcode is fetched from memory, no operand (data or address) is read from memory. For an instruction which is more than 1-byte a further memory read operation is needed for operand(s) [data or address].

Example: The machine codes-00111110 (3EH-MVI A) and 00110010 (32H) – are stored in memory locations: 2000H and 2001H.

Memory Location	Machine Code	Hex	Instruction
2000H	00111110	3EH	MVI A,32H
2001H	00110010	32H	

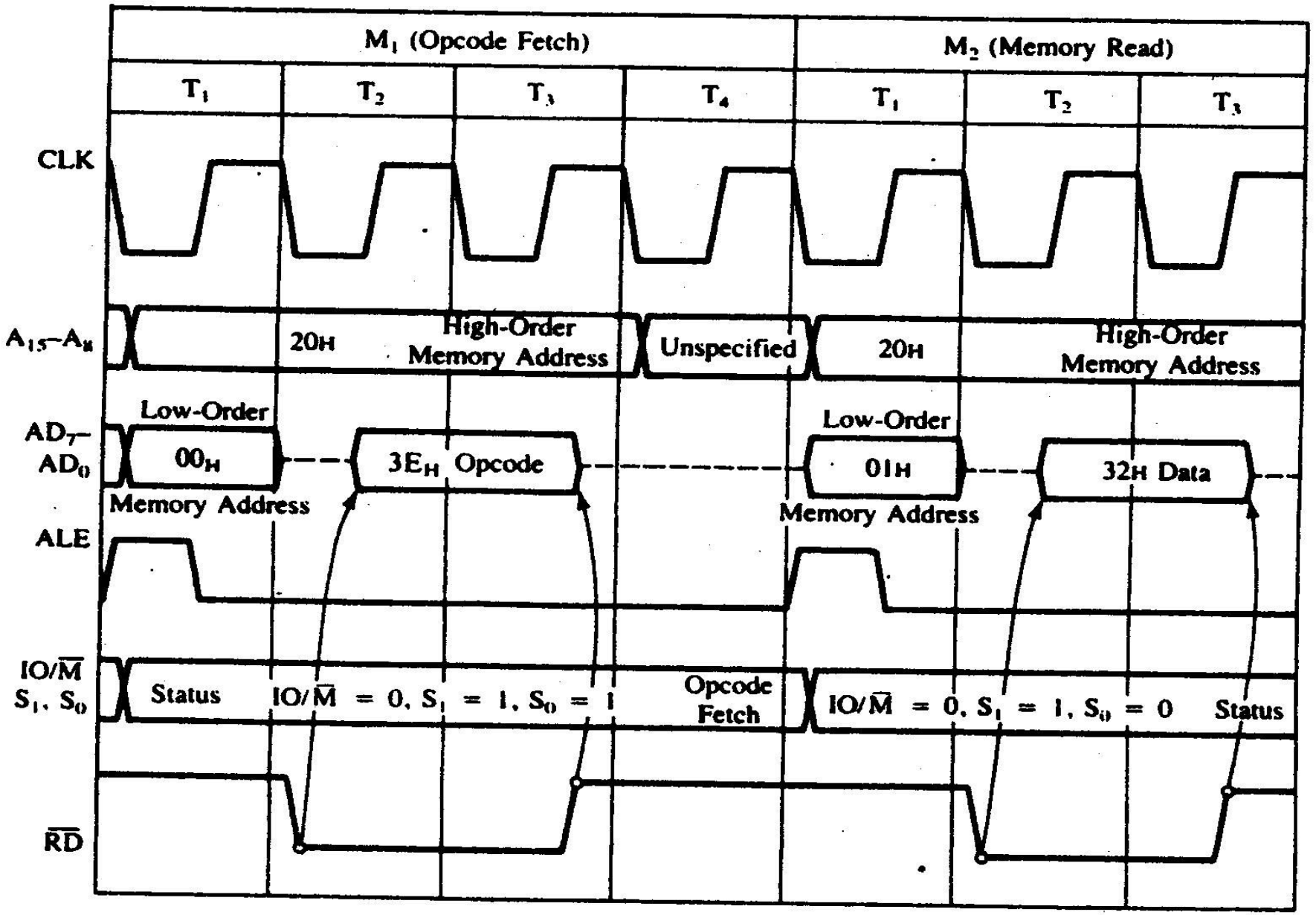
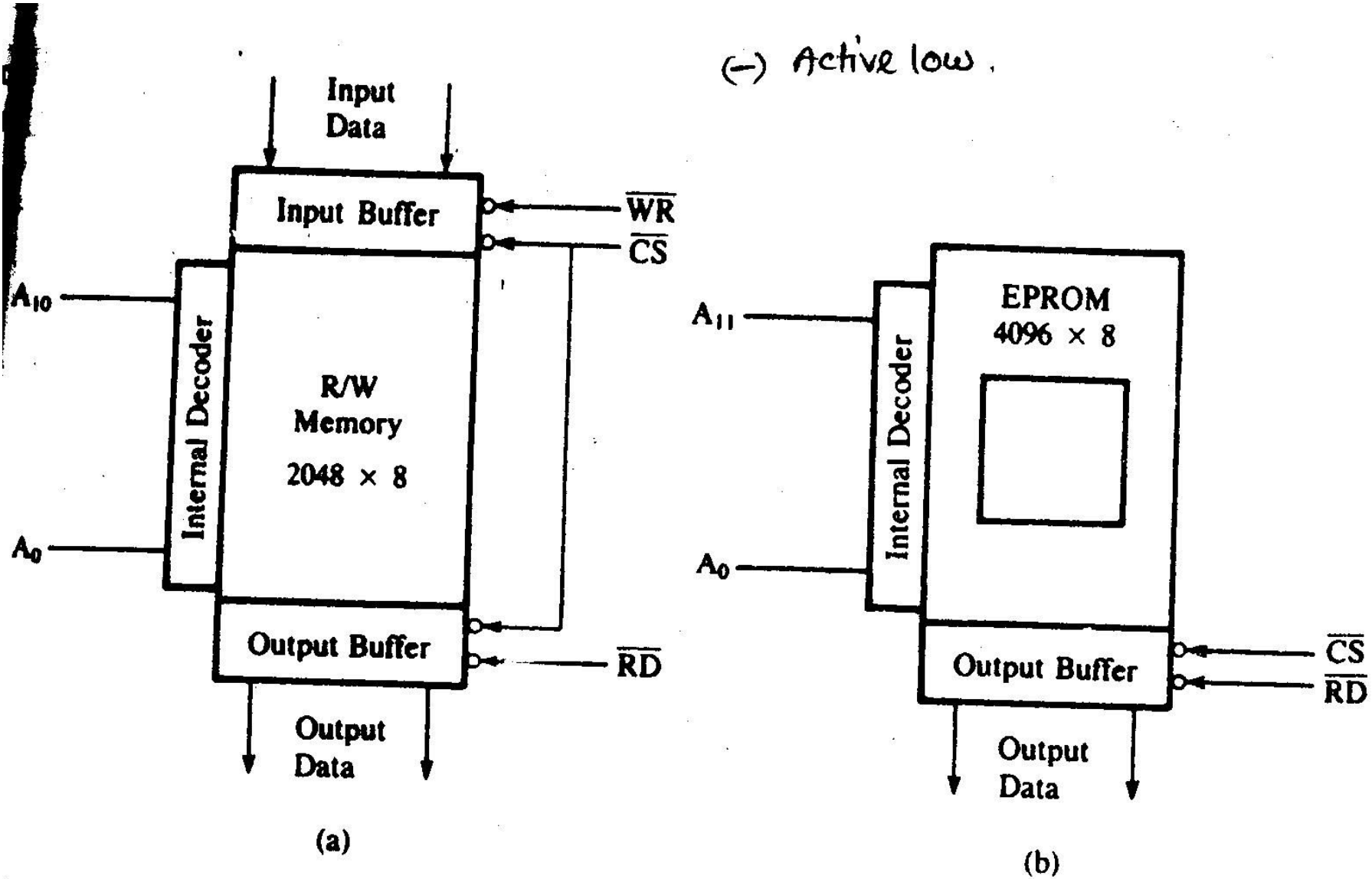


FIGURE 3.10
8085 Timing for Execution of the Instruction MVI A,32H

3.3 MEMORY INTERFACING

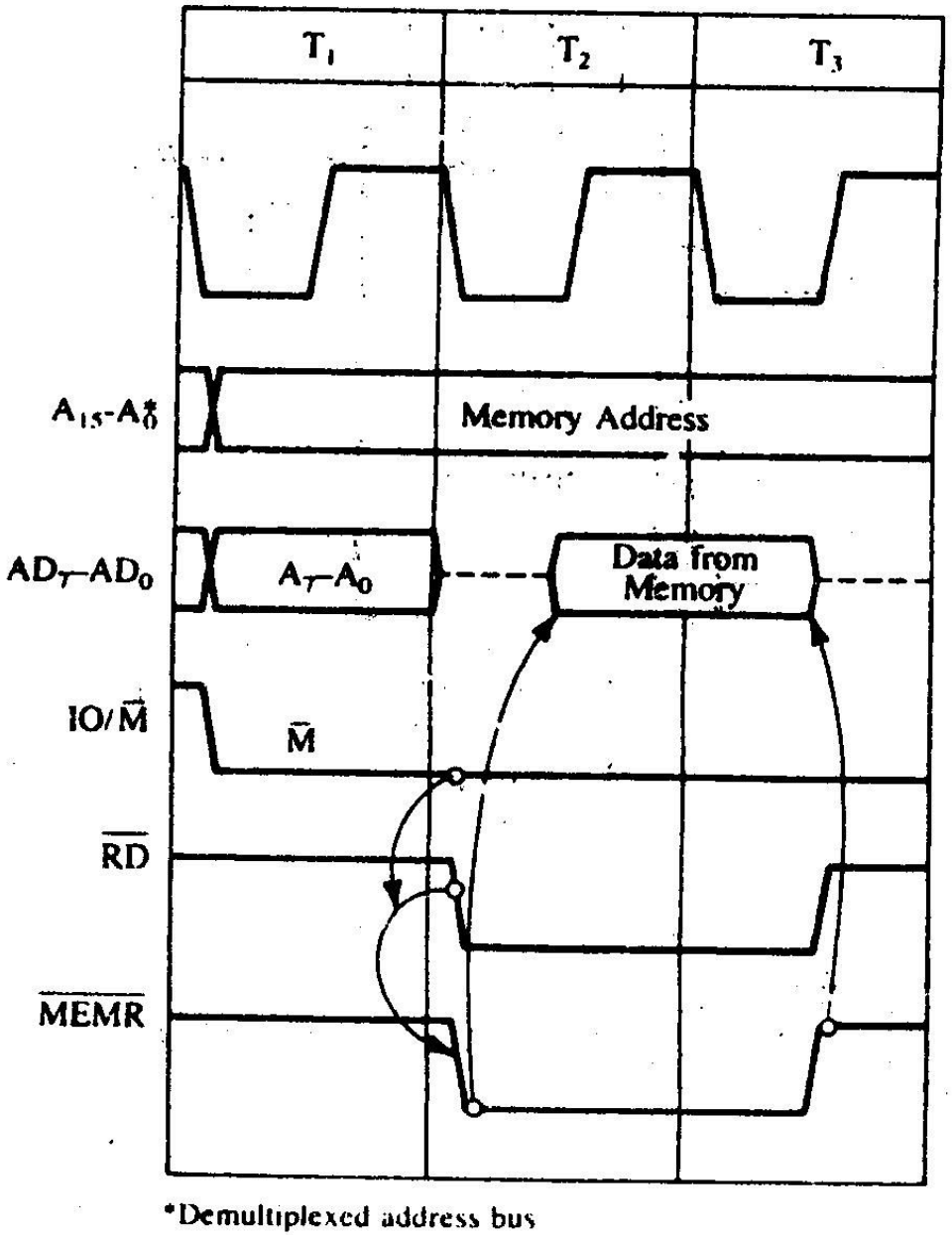
(-) Active low.



IGURE 3.11

ypical Memory Chips: R/W Static Memory (a) and EPROM (b)

FIGURE 3.12
Timing of the Memory Read Cycle



*Demultiplexed address bus

FIGURE 3.13
Timing of the Memory Write Cycle