Chapter-8

Counter and Time Delays

8.1 COUNTER AND TIME DELAYS

Counters are used primarily to keep track of events; time delays are important in setting up reasonably accurate timing between two events.

COUNTER

A counter is designed simply by loading an appropriate number into one of the registers and using INR (for up-counter) or DCR (for down-counter) instructions. A loop is established to update the count.

TIME DELAY

The procedure used to design a specific delay is similar to that used to set up a counter. A register is loaded with a number, depending on the time delay required, and then the register is decremented until it reaches zero.

8.11 Time Delay Using One Register

Label	Opcode	Operand	T-states
	MVI	C,FFH	7
LOOP:	DCR	C	4
	JNZ	LOOP	10/7

An 8085–based microcomputer with 2 MHz clock frequency will execute the instruction MVI in 3.5 μs as follows:

Clock frequency of the system f = 2 MHz
Clock period $T = 1/f = 1/2 \times 10^{-6} = 0.5\ \mu s$
Time to execute MVI = 7 T-states x 0.5
= 3.5 μs

The time delay in the loop T_L with 2 MHz clock frequency is calculated as

$$T_L = (T \times \text{Loop T-states} \times N_{10})$$

Where T_L = Time delay in the loop
T = System clock period
N_{10} = Decimal equivalent of the count loaded in the delay register

$$T_L = (0.5 \times 10^{-6} \times 14 \times 255)$$
$$= 1785\ \mu s$$
$$\approx 1.8\ ms$$

The T-states for JNZ instruction are 10/7. So the adjusted loop delay is

$$T_{LA} = T_L - (3 \text{ T-states} \times \text{Clock period})$$
$$= 1785\ \mu s - 1.5\ \mu s = 1783.5\ \mu s$$

Therefore, the total delay is

Total Delay = Time to execute instructions outside loop + Time to execute loop instructions

$$T_D = T_O + T_{LA}$$
$$= (7 \times 0.5\ \mu s) + 1783.5\ \mu s = 1787\ \mu s$$
$$\approx 1.8\ ms$$

The difference between the loop delay T_L and these calculations is only 2 μs and can be ignored in most cases.

8.12 Time Delay Using a Register Pair

Here the counter value can be a 16-bit number and maximum of FFFFH.

Label	Opcode	Operand	T-states
	LXI	B,2384H	10
LOOP:	DCX	B	6
	MOV	A,C	4
	ORA	B	4
	JNZ	LOOP	10/7

TIME DELAY

The loop includes 24 clock periods for execution. The decimal equivalent of counter value is

$$2384H = 9092_{10}$$

If the clock period of the system = 0.5 μs, the delay in the loop T_L is

$$\begin{aligned} T_L &= (T \times \text{Loop T-states} \times N_{10}) \\ &= (0.5 \times 24 \times 9092_{10}) \\ &\approx 109 \text{ ms (without adjusting for the last cycle)} \end{aligned}$$

Total Delay T_D = 109 ms + T_O
≈ 109 ms (the instruction LXI adds only 5 µs)

8.13 Time Delay Using a Loop within a Loop Technique

Label	Opcode	Operand	T-states
	MVI	B,38H	7
LOOP2:	MVI	C,FFH	7
LOOP1:	DCR	C	4
	JNZ	LOOP1	10/7
	DCR	B	4
	JNZ	LOOP2	10/7

DELAY CALCULATIONS

The delay in LOOP1 is T_{L1} = 1783.5 µs. The counter value of LOOP2 is 56_{10} (38H). Delay for the LOOP2 is calculated as follows:

$$T_{L2} = 56\,(T_{L1} + 21 \text{ T-states} \times 0.5\ \mu s)$$
$$= 56\,(1783.5\ \mu s + 10.5\ \mu s)$$
$$= 100.46 \text{ ms}$$

8.3 ILLUSTRATIVE PROGRAM: ZERO-TO-NINE (MODULO TEN) COUNTER

PROBLEM STATEMENT

Write a program to count from 0 to 9 with a one-second delay between each count. At the count of 9, the counter should reset itself to 0 and repeat the sequence continuously. Assume the clock frequency of the microprocessor is 1 MHz.

Delay Calculations

Loop Delay T_L = 24 T-states x T x Count

1 second = $24 \times 1.0 \times 10^{-6}$ x Count

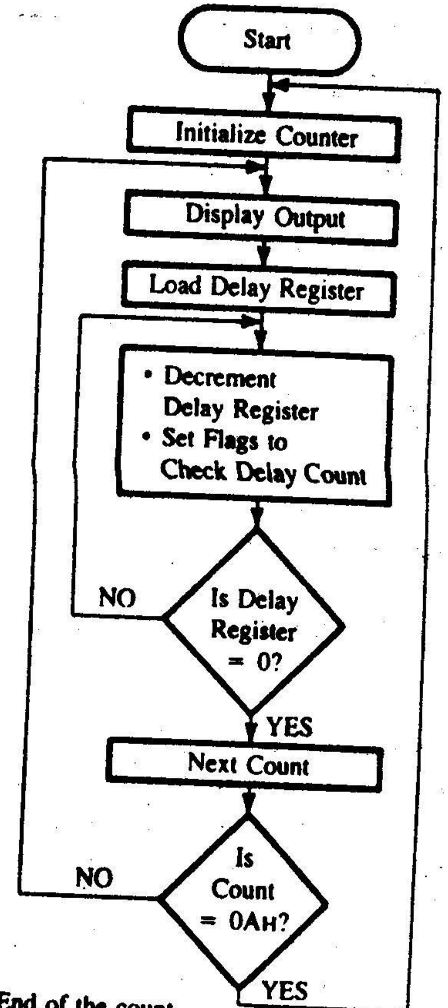
Count = $1/(24 \times 10^{-6})$

= 41666_{10}

= A2C2H

... displayed at the end of the

Memory Address HI-LO XX00	Hex Code	Label	Mnemonics	T	Comments
01	06	START:	MVI B,00H		
02	00				
03	D3	DSPLAY:	OUT PORT#	10	T_O
04	PORT#				
05	21		LXI H,16-Bit	10	
06	LO*				
07	HI				
08	2B	LOOP:	DCX H	6	T_L: 24 T-states
09	7D		MOV A,L	4	
0A	B4		ORA H	4	
0B	C2		JNZ LOOP	10/7	
0C	08				
0D	XX†				
0E	04		INR B	4	T_O
0F	78		MOV A,B	4	
10	FE		CPI 0AH	7	
11	0A				
12	C2		JNZ DSPLAY	10/7	
13	03				
14	XX†				
15	CA		JZ START		;End of the count, start again
16	00				
17	XX				



*Enter 16-bit delay count in place of LO and HI, appropriate to the clock period in your system.
†Enter high-order address (page number) of your R/W memory.

FIGURE 8.7
Program and Flowchart for a Zero-to-Nine Counter