

Chapter-13

Interfacing Data Converters

13.1 DIGITAL-TO-ANALOG (D/A) CONVERTERS

Digital-to-Analog converters can be classified in three categories:

- ☐ current output: provides current as output signal.
- ☐ voltage output: internally converts current signal into voltage signal.
- ☐ multiplying type: output current or voltage is product of input current or voltage.

Voltage output is slower than current output because of the delay in converting the current signal into voltage signal. However, in many applications, it is necessary to convert current into voltage by using an external operational amplifier.

13.1.1 Basic Concepts

Figure 13.1(a) shows a block diagram of a 3-bit D/A converter. If the input ranges from 0 to 1 V, it can be divided into eight equal parts ($1/8$ V); each successive is $1/8$ V higher than the previous combination, as shown in Figure 13.1(b).

The following points can be summarized from the graph:

1. If a converter has n input lines, it can have 2^n input combinations.
2. If the full-scale analog voltage is 1 V, the smallest unit or the LSB (001_2) is equivalent to $1/2^n$ of 1 V. This is defined as resolution.
3. The MSB represents half of the full-scale value. In this example, the MSB (100_2) = $1/2$ V.
4. For the maximum input signal (111_2), the output signal is equal to the value of the full scale input signal minus the value of the 1 LSB input signal. In this example, the maximum input signal (111_2) represents $7/8$ V.

Example 13.1: Calculate the values of the LSB, MSB, and full-scale output for an 8-bit DAC for the 0 to 10 V range.

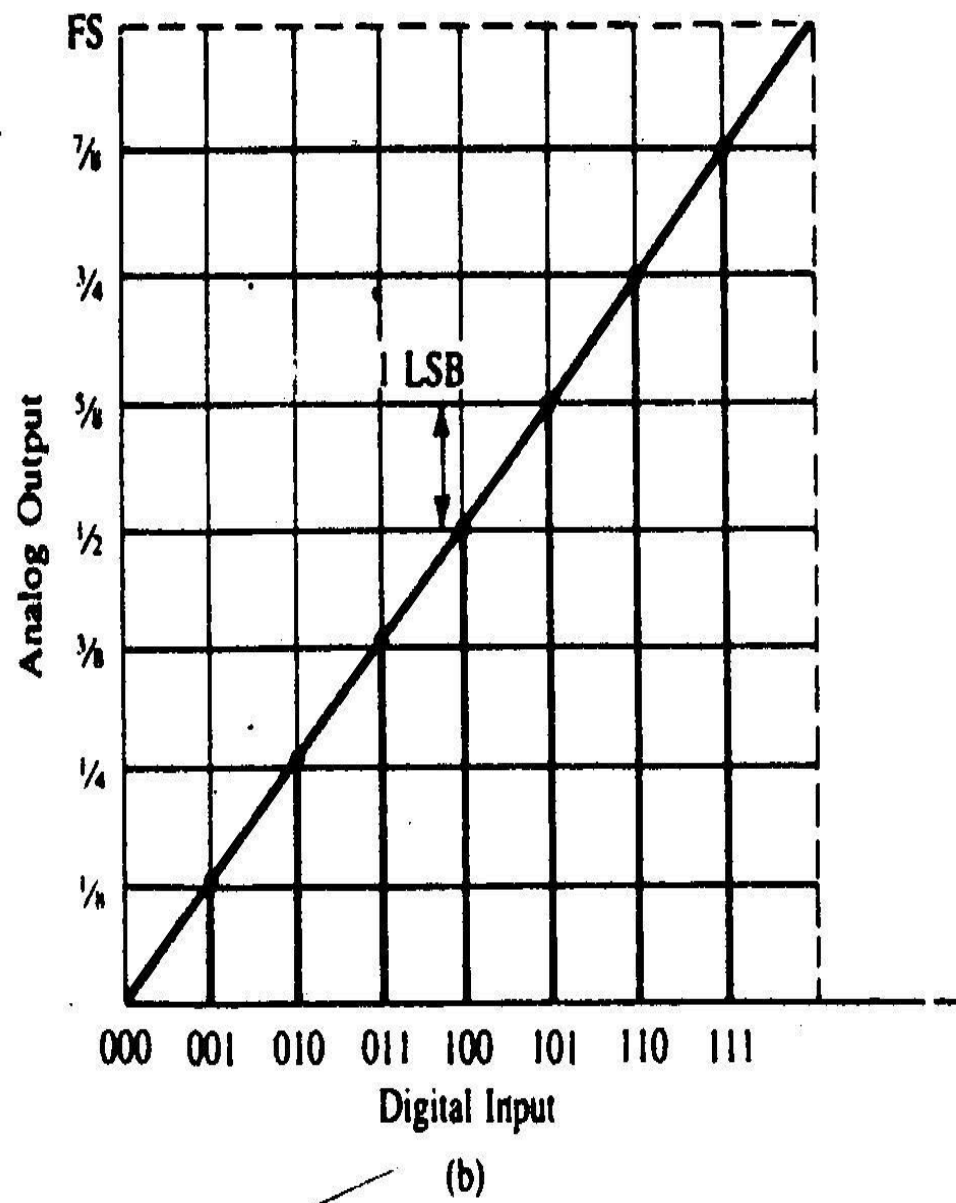
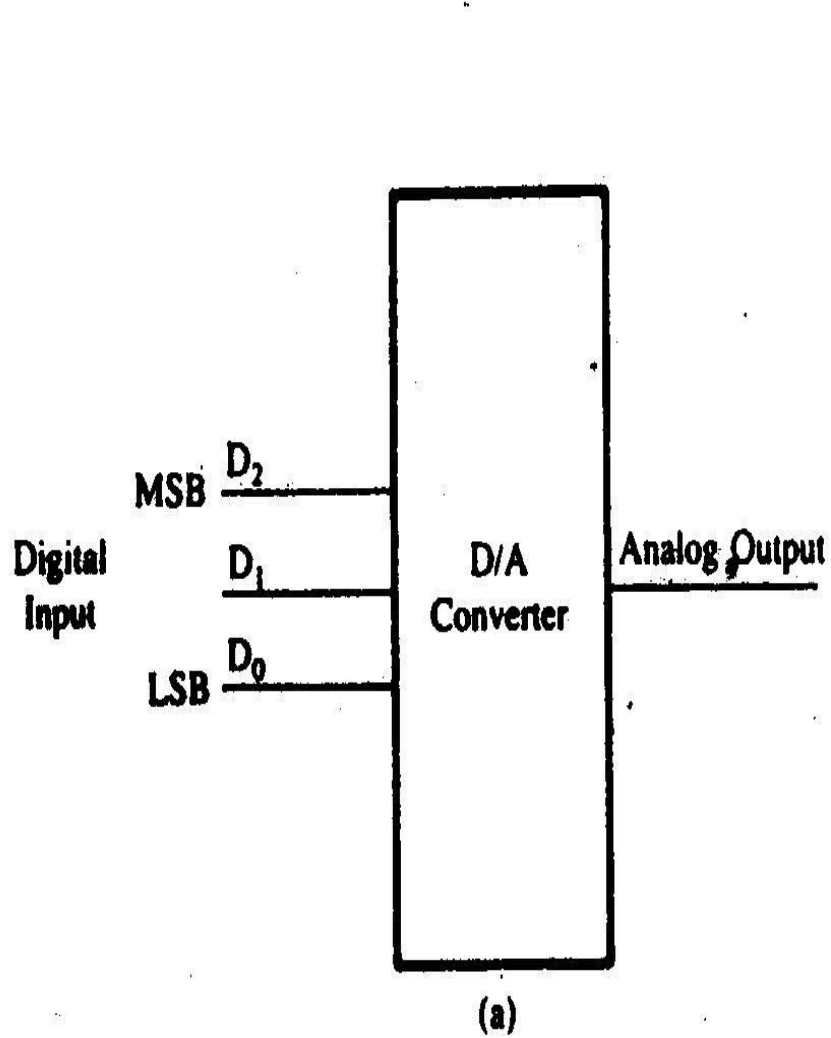


FIGURE 13.1

A 3-Bit D/A Converter: Block Diagram (a) and Digital Input vs. Analog Output (b)

Solution:

1. $\text{LSB} = 1/2^8 = 1/256$

For 10 V, $\text{LSB} = 10 \text{ V}/256 = 39 \text{ mV}$

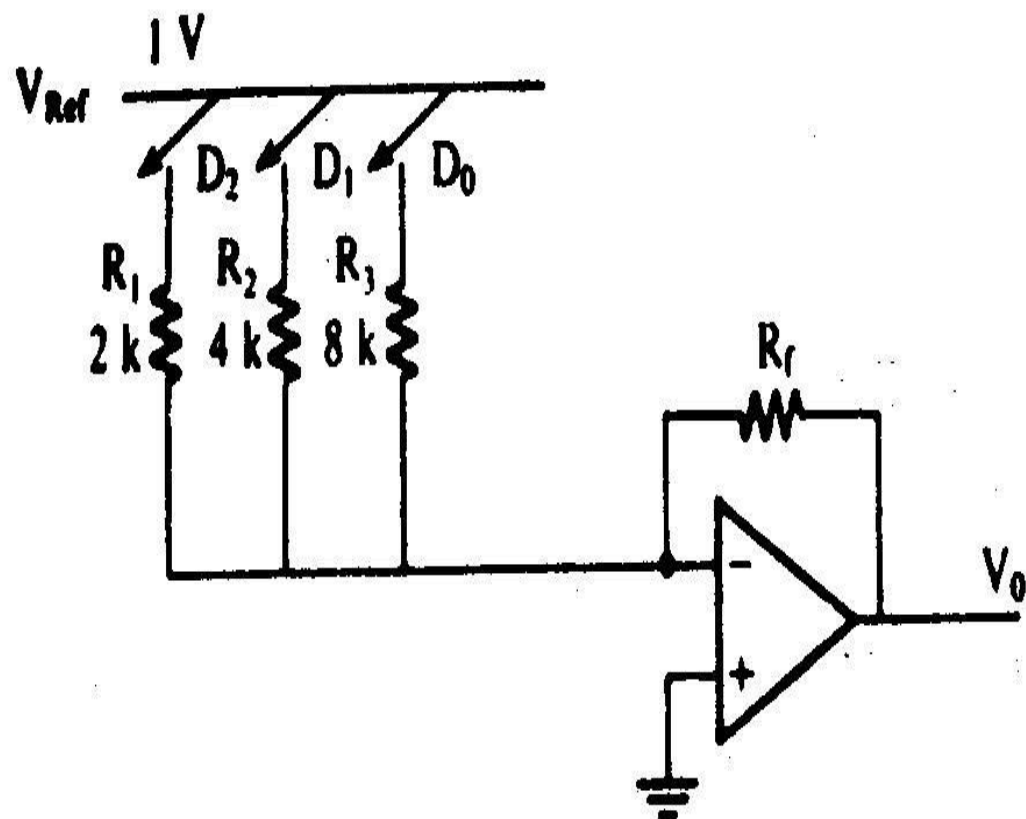
2. $\text{MSB} = 1/2 \text{ full scale} = 5\text{V}$

3. Full-Scale Output = (Full-Scale Value – 1 LSB)
= $10\text{V} - 0.039 \text{ V}$
= 9.961 V

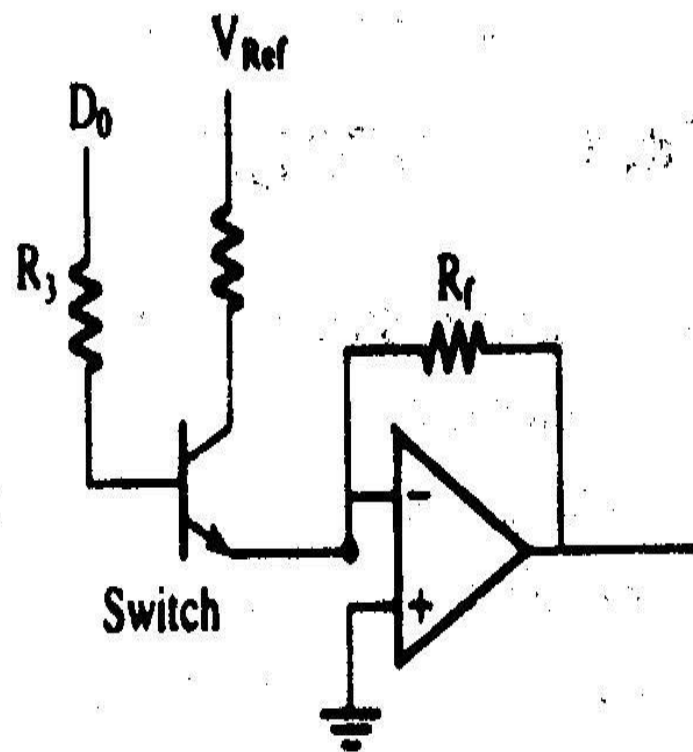
13.1.2 D/A Converter Circuits

The input resistors R_1 , R_2 , and R_3 are selected in binary weighted proportion; each has double the value of the previous resistor. If all three inputs are 1 V, the total output current is

$$\begin{aligned} I_o = I_T &= I_1 + I_2 + I_3 \\ &= V_{in}/R_1 + V_{in}/R_2 + V_{in}/R_3 \\ &= V_{in}/1\text{k}(1/2 + 1/4 + 1/8) \\ &= 0.875 \text{ mA} \end{aligned}$$



(a)



(b)

FIGURE 13.3

Simulated D/A Converter (a) and Transistor Switch to Turn On/Off Bit D_0 (b)

The voltage output is

$$\begin{aligned}V_o &= -R_f I_T \\&= -(1 \text{ k}) (0.875 \text{ mA}) \\&= -7/8\end{aligned}$$

This example shows that for the input = 111_2 , the output is equal to either 7/8 mA or 7/8 V, representing the D/A conversion process.

Now the output current I_o can be generalized for any number of bits as

$$I_o = V_{\text{Ref}} / R (A_1/2 + A_2/4 + \dots + A_n/2^n)$$

The following points can be inferred from the above example:

1. A D/A converter circuit requires three elements: resistor network with appropriate weighting, switches, and a reference source.
2. The output can be a current signal or converted into a voltage signal using an operational amplifier.
3. The time required for conversion, called settling time, is dependent on the response of the switches and output amplifier (for a voltage output DAC).

13.1.3 Illustration: Interfacing an 8-Bit D/A Converter

PROBLEM STATEMENT

1. Design an output port with the address FFH to interface the 1408 D/A converter that is calibrated for a 0 to 10 V range; refer to Figure 13.5(a).
2. Write a program to generate a continuous ramp waveform.
3. Explain the operation of the 1408 in Figure 13.5(b) , which is calibrated for a bipolar range $\pm 5V$. Calculate the output V_O if the input is 10000000_2 .

HARDWARE DESCRIPTION

The total reference current source is determined by the resistor R_{14} and the voltage V_{Ref} . The resistor R_{15} is generally equal to R_{14} to match the input impedance of the reference source. The output I_O is calculated as follows:

$$I_O = V_{Ref} / R_{14} (A_1/2 + A_2/4 + A_3/8 + A_4/16 + A_5/32 + A_6/64 + A_7/128 + A_8/256)$$

Where inputs A_1 through $A_8 = 0$ or 1 .

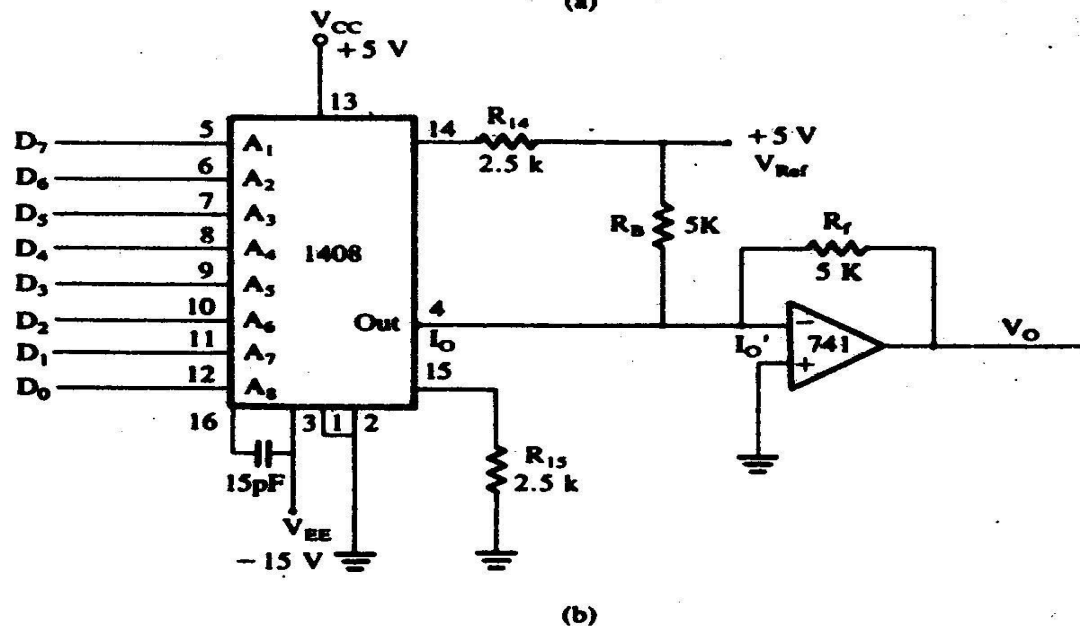
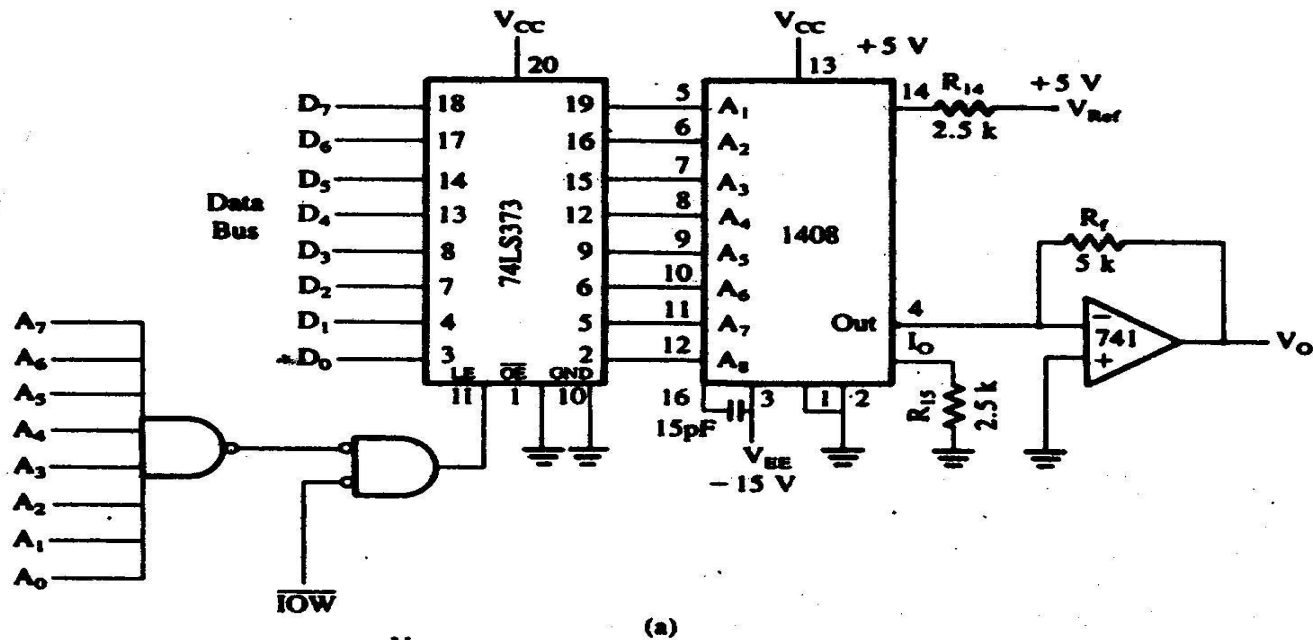


FIGURE 13.5

Interfacing the 1408 D/A Converter: Voltage Output in Unipolar Range (a) and in Bipolar Range (b)

This formula is an application of the generalized formula for the current I_o . For full scale input (D_7 through $D_0 = 1$).

$$\begin{aligned} I_o &= 5 \text{ V} / 2.5 \text{ k} (1/2 + 1/4 + 1/8 + 1/16 + 1/32 + 1/64 + 1/128 + 1/256) \\ &= 2 \text{ mA} (255/256) \\ &= 1.992 \text{ mA}. \end{aligned}$$

The output is 1 LSB less than full-scale reference source of 2 mA. The output voltage V_o for the full-scale input is

$$\begin{aligned} &= 2 \text{ mA} (255/256) \times 5 \text{ k} \\ &= 9.961 \text{ V} \end{aligned}$$

PROGRAM

To generate a continuous waveform, the instructions are as follows:

	MVI A, 00H	; First input 00H for DAC
DTOA:	OUT FFH	; Output to DAC
	MVI B, COUNT	; COUNT for delay
DELAY:	DCR B	
	JNZ DELAY	
	INR A	; Next input for DAC
	JMP DTOA	

Program Description:

The program outputs 00H to FFH as the digital inputs for DAC. The analog output of the DAC starts at 0 V and increases up to 10 V (approximately) as a ramp. When the accumulator contents go to 0, the next cycle begins; thus the ramp signal is generated continuously and that can be displayed on oscilloscope.

The delay in the program is necessary for two reasons:

1. The time needed for a microprocessor to execute an output loop is likely to be less than the settling time of the DAC.
2. The slope of the ramp can be varied by changing the delay.

OPERATING THE D/A CONVERTER IN A BIPOLAR RANGE

The 1408 in Figure 13.5(b) is calibrated for the range from -5 V to +5 V by adding the resistor R_B (5.0 k) between the reference voltage V_{Ref} and the output pin. The resistor R_B supplies 1 mA (V_{Ref}/R_B) current to the opposite direction of the current generated by the input signal. Therefore, the output current for the bipolar operation I_o is

$$\begin{aligned} I_o' &= I_o - V_{Ref}/R_B \\ &= V_{Ref}/R_{14} (A_1/2 + A_2/4 + A_3/8 + A_4/16 + A_5/32 + A_6/64 + A_7/128 + A_8/256) - V_{Ref}/R_B \end{aligned}$$

When the input signal is equal to zero, the output V_o is

$$\begin{aligned} V_o &= I_o' R_f \\ &= (I_o - V_{Ref}/R_B) R_f \\ &= (0 - 5 \text{ V}/5\text{k}) (5\text{k}) && (I_o = 0 \text{ for input} = 0) \\ &= -5\text{V} \end{aligned}$$

When the input = 1000 0000, the output V_o is

$$\begin{aligned} V_o &= (I_o - V_{\text{Ref}}/R_B) R_f \\ &= (V_{\text{Ref}}/R_{14} \times A_1/2 - V_{\text{Ref}}/R_B) R_f & (A_2 - A_8 = 0) \\ &= (5 \text{ V}/2.5 \text{ k} \times 1/2 - 5 \text{ V}/5 \text{ k}) 5 \text{ k} \\ &= (1 \text{ mA} - 1 \text{ mA}) 5 \text{ k} \\ &= 0 \end{aligned}$$

13.2 ANALOG-TO-DIGITAL CONVERTERS

The A/D conversion is a quantization process whereby an analog signal is represented by equivalent binary states; this is opposite to the D/A conversion process. Analog-to-Digital converters can be classified in two general groups based on the conversion technique:

- ❑ Successive-approximation A/D converter: used in instrumentation.
- ❑ Integration-type A/D converter: used in digital meters, monitoring systems.

13.2.1 Basic Concepts

Figure 13.8(a) shows a block diagram of a 3-bit A/D converter. Figure 13.8(b) shows the graph of the analog input voltage (0 to 1 V) and the corresponding digital output signal. The resolution of the converter is $1/8$ V.

13.2.1 Successive-Approximation A/D Converter

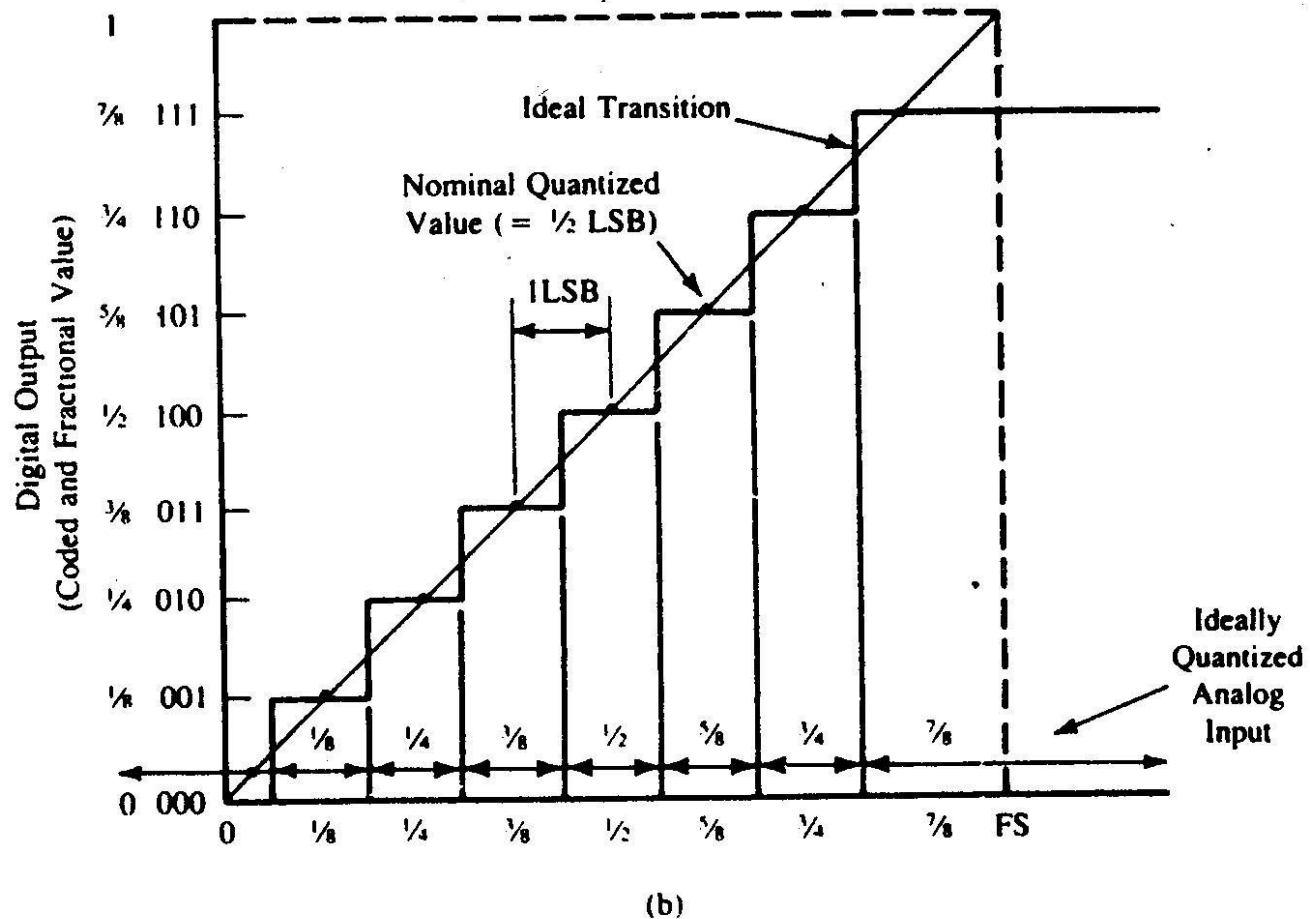
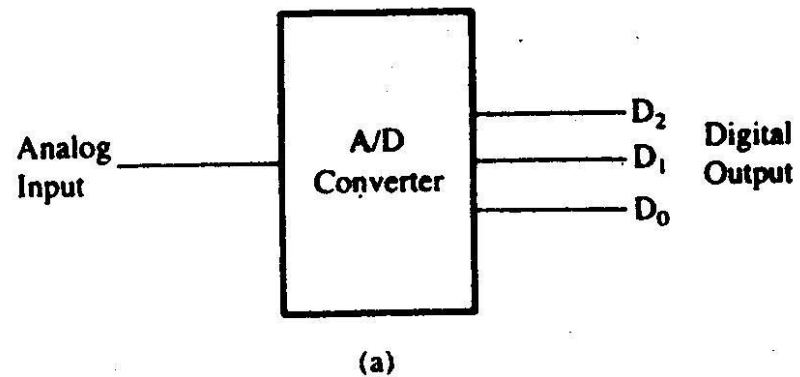
Figure 13.9(a) shows the block diagram of a successive approximation A/D converter includes three major elements: the D/A converter, the successive approximation register (SAR), and the comparator. The conversion technique involves the output of the D/A converter V_o with the analog input signal V_{in} . The digital input to the DAC is generated using the successive-approximation method (explain below). When the DAC output matches the analog signal, the input to the DAC is equivalent digital signal.

In the case of a 4-bit A/D converter, bit D_3 is turned on first and the output of the DAC is compared with an analog signal. If the comparator changes the state, indicating that the output generated by D_3 is larger than the analog signal, bit D_3 is turned off in the SAR and bit D_2 is turned on. The process continues until the input reaches bit D_0 .

FIGURE 13.8

**A 3-Bit A/D Converter: Block
Diagram (a) and Analog Input vs.
Digital Output (b)**

SOURCE: Analog Devices, Inc., *Integrated
Circuit Converters, Data Acquisition Systems,
and Analog Signal Conditioning Components*
(Norwood, Mass.: Author, 1979), pp. 1-18.



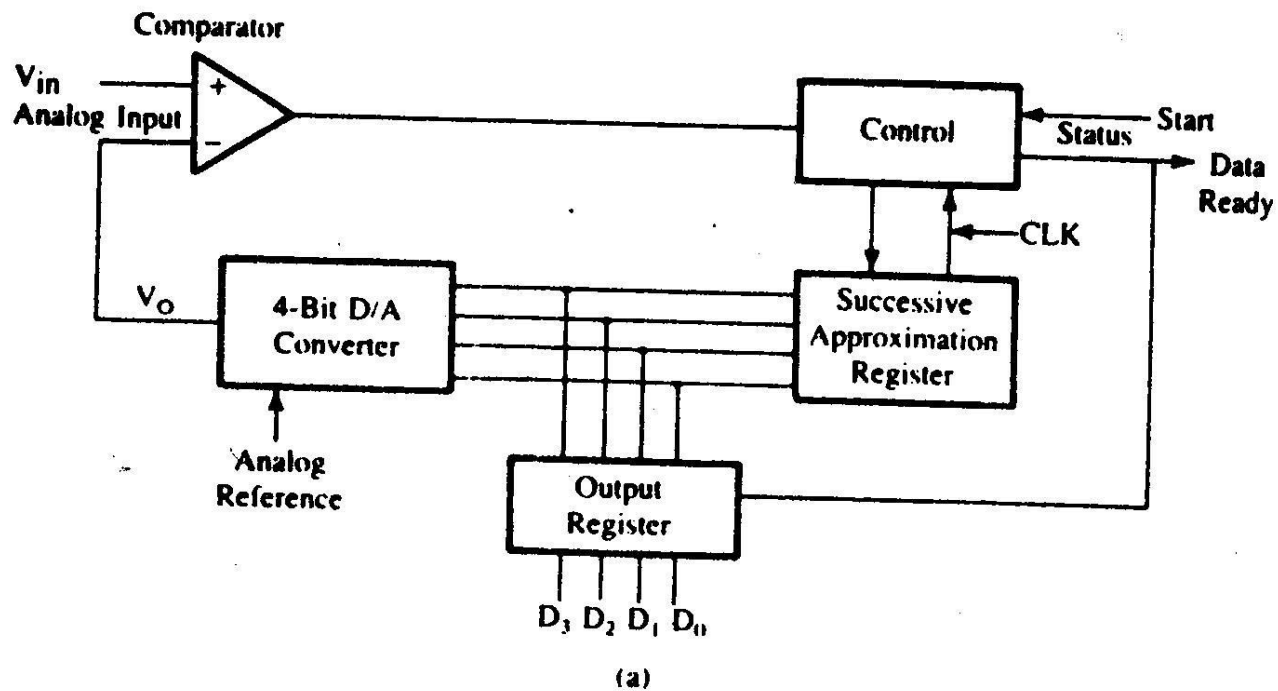


FIGURE 13.9
 Successive-Approximation A/D
 Converter: Block Diagram (a) and
 Conversion Process for a 4-Bit
 Converter (b)

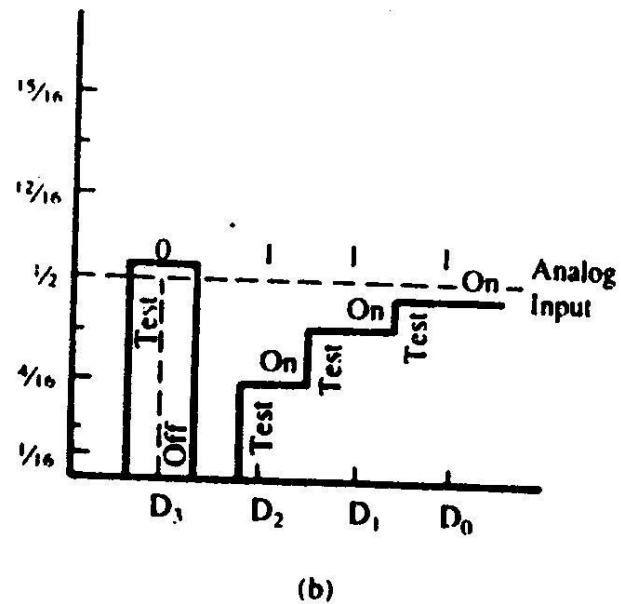


Figure 13.9(b) illustrates a 4-bit conversion process. When bit D_3 is turned on, the output exceeds the analog signal and therefore, D_3 is turned off. When the next three successive bits are turned on, the output becomes approximately equal to the analog signal.

13.2.1 Interfacing 8-Bit A/D Converters

INTERFACING AN 8-Bit A/D CONVERTER USING STATUS CHECK

Figure 13.11 shows a schematic of interfacing a typical A/D converter using status check.

PROGRAM

```
TEST: OUT 82H
      IN 80H
      RAR
      JC TEST
      IN 81H
      RET
```

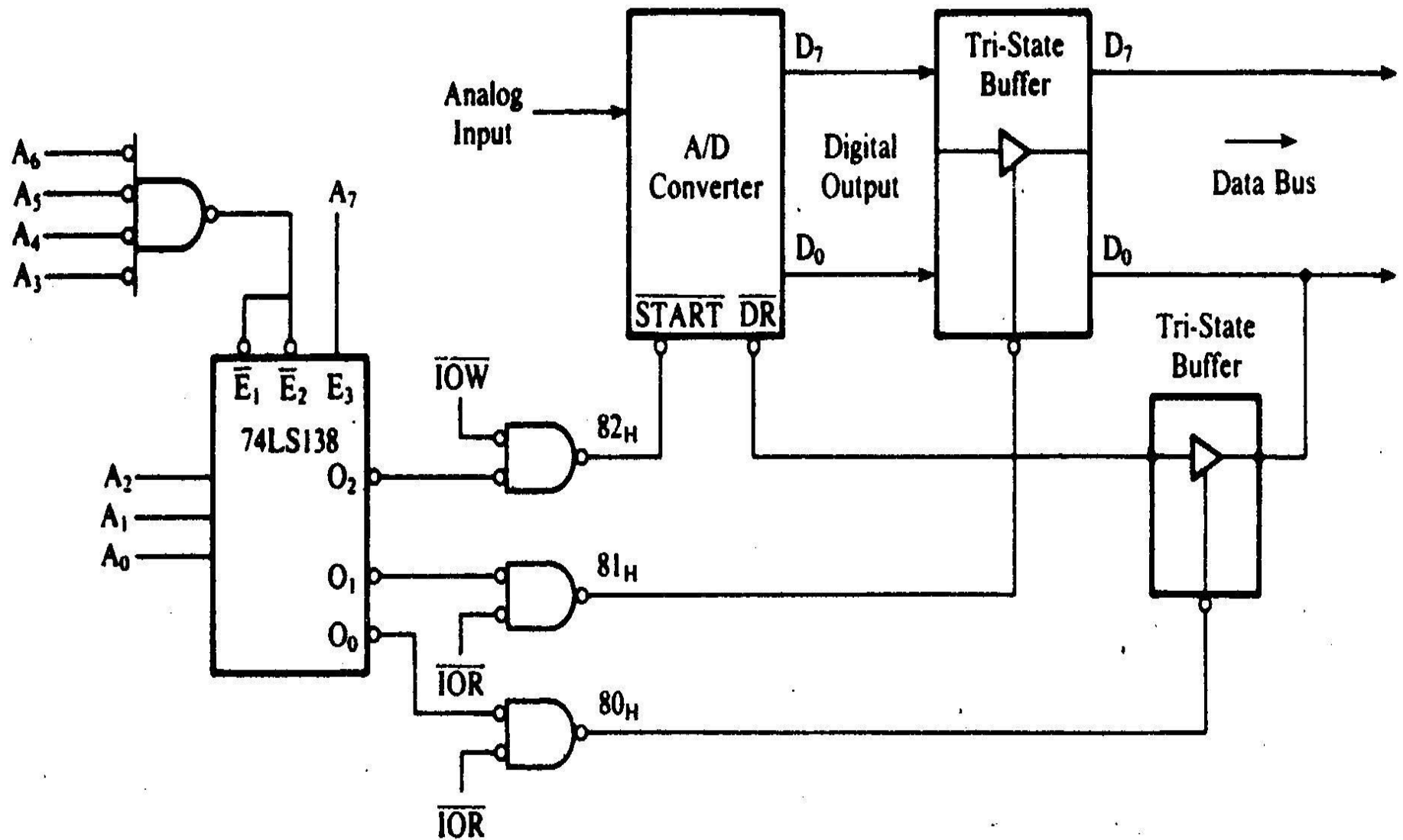



FIGURE 13.11

Interfacing an A/D Converter Using the Status Check