Git repository link: https://github.com/jeniffer83/ECE6780_Lab2

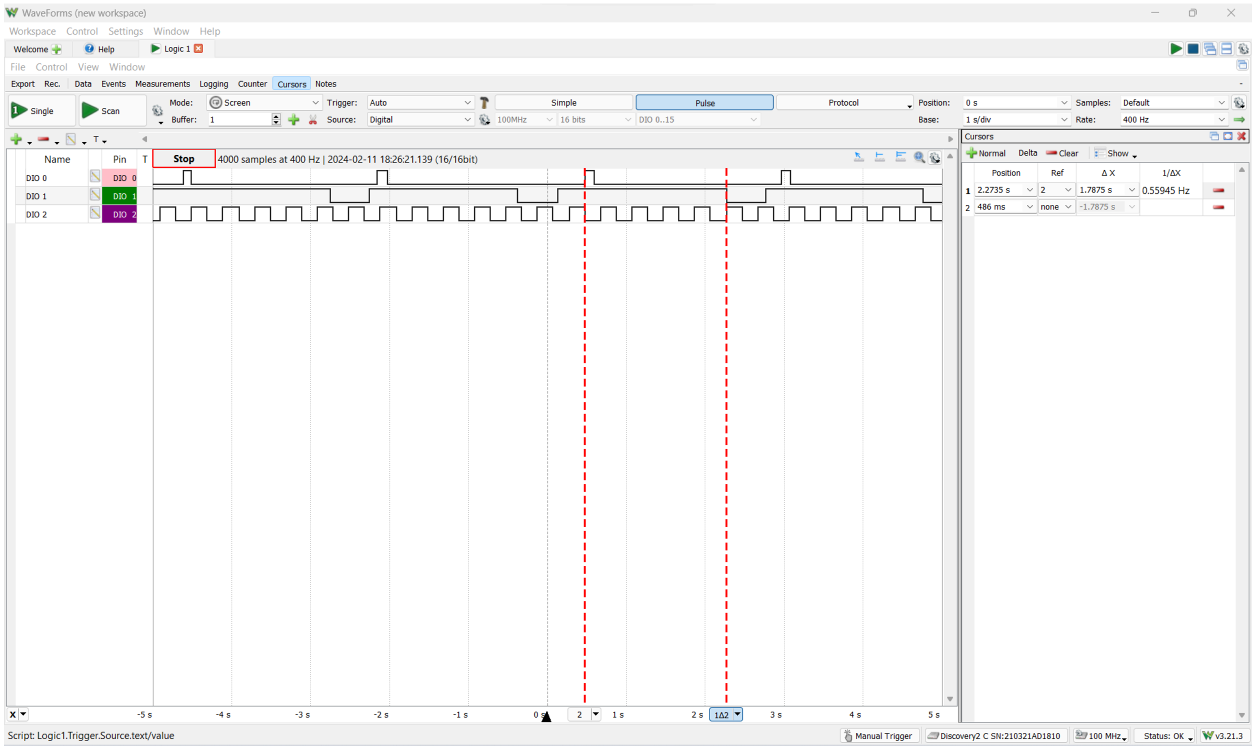
Postlab 02 Questions

1. **Why can't you use both pins PA0 and PC0 for external interrupts at the same time?**
   When working with external interrupts on the STM32FO family, it's essential to remember that you cannot use pins PA0 and PC0 simultaneously. This is due to a limitation in the SYSCFG pin multiplexers that route external pins to the EXTI lines. Only one pin from a group (e.g., PA0, PB0,… PF0) can be connected to a single EXTI line at any given time. Therefore, planning carefully to avoid conflicts when using multiple external interrupts is crucial.

2. **What software priority level gives the highest priority? What level gives the lowest?**
   In the NVIC for STM32FO the highest level is 0, and the lowest level is 3.

3. **How many bits does the NVIC have reserved in its priority (IPR) registers for each interrupt (including non-implemented bits)? Which bits in the group are implemented?**
   The NVIC in the STM32F0 has priority (IPR) registers that configure the priorities for each interrupt. Each IPR register contains four 8-bit regions, but only the upper two bits from these regions are implemented, giving four possible configurable priority levels (0-3). This means two bits are reserved for each interrupt priority, but only these two bits are implemented to set the priority level.

4. **What was the latency between pushing the Discovery board button and the LED change (interrupt handler start) that you measured with the logic analyzer? Make sure to include a screenshot in the post-lab submission.**


WaveForms (new workspace)
Workspace Control Settings Window Help
Welcome Help Logic 1
File Control View Window
Export Rec. Data Events Measurements Logging Counter Cursors Notes
Single Scan
Stop
DIO 0
DIO 1
DIO 2
-5 s -4 s -3 s -2 s -1 s 0 s 1 s 2 s 3 s 4 s 5 s
Manual Trigger
Status: OK
v3.21.3

Mode: Screen
Buffer: 1
Trigger: Auto
Source: Digital
100MHz 16 bits DIO 0..15
Position: 0 s
Base: 1 s/div
Samples: Default
Rate: 400 Hz

4000 samples at 400 Hz | 2024-02-11 18:26:21.139 (16/16bit)

Name	Pin
DIO 0	DIO 0
DIO 1	DIO 1
DIO 2	DIO 2

Cursors

	Position	Ref	Δ X	1/ΔX
1	2.2735 s	2	1.7875 s	0.55945 Hz
2	486 ms	none	-1.7875 s	

Script: Logic1.Trigger.Source.text/value

Discovery2 C SN:210321AD1810 100 MHz

The latency between pushing the Discovery board button and the LED change (interrupt start) that I measured with the logic analyzer is approximately 1.7875 s.

Note that DIO 0 is the PA0 (Discovery board button which is the blue button), DIO 1 is the PC6, and DIO 2 is the PC7.

5. **Why do you need to clear status flag bits in peripherals when servicing their interrupts?**
   Clearing the status flag is necessary to acknowledge that the interrupt condition has been met, thus preventing the interrupt from triggering repeatedly. If the corresponding status bit is not cleared manually, the handler will continuously execute because the peripheral will show the interrupt condition is being met.