Design Project #4

ELECENG 2EI4- Electronic Devices and Circuits

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Part 1

a) **Circuit Schematic:**

In order to implement the CMOS logic, there are Key Principles to Note down:
Each input controls a pair of MOSFETS , one NMOS and one PMOS
The PUN and PDN are dual networks
Therefore, only one of the networks can be achieved at a time
CMOS logic is a negative logic

From there, to design the XOR, I then wrote out the XOR function in terms of AND and OR operations.

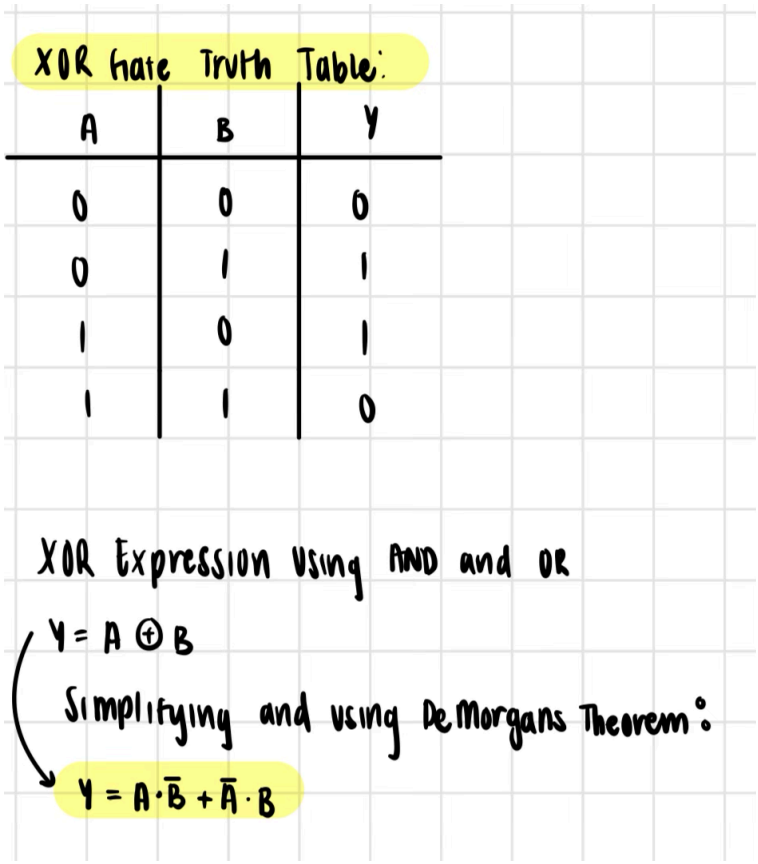

Figure 1: XOR Truth Table and Equation

Therefore, within this design, the completed circuit has a total of 12 MOSFETs. In this 12 MOSFEt design there are two networks, the PDN and the PUN. The Pull-Down Network (PDN) is composed of 4 N-MOS transistors, and the Pull-Up Network (PUN) consists of 4 P-MOS transistors. To handle the complemented inputs A and B, 4 additional transistors are needed, including 2 N-MOS and 2 P-MOS transistors, to create 2 CMOS inverters. As shown below, there is a CMOS inverter and CMOS XOR gate used to obtain this schematic/ design.

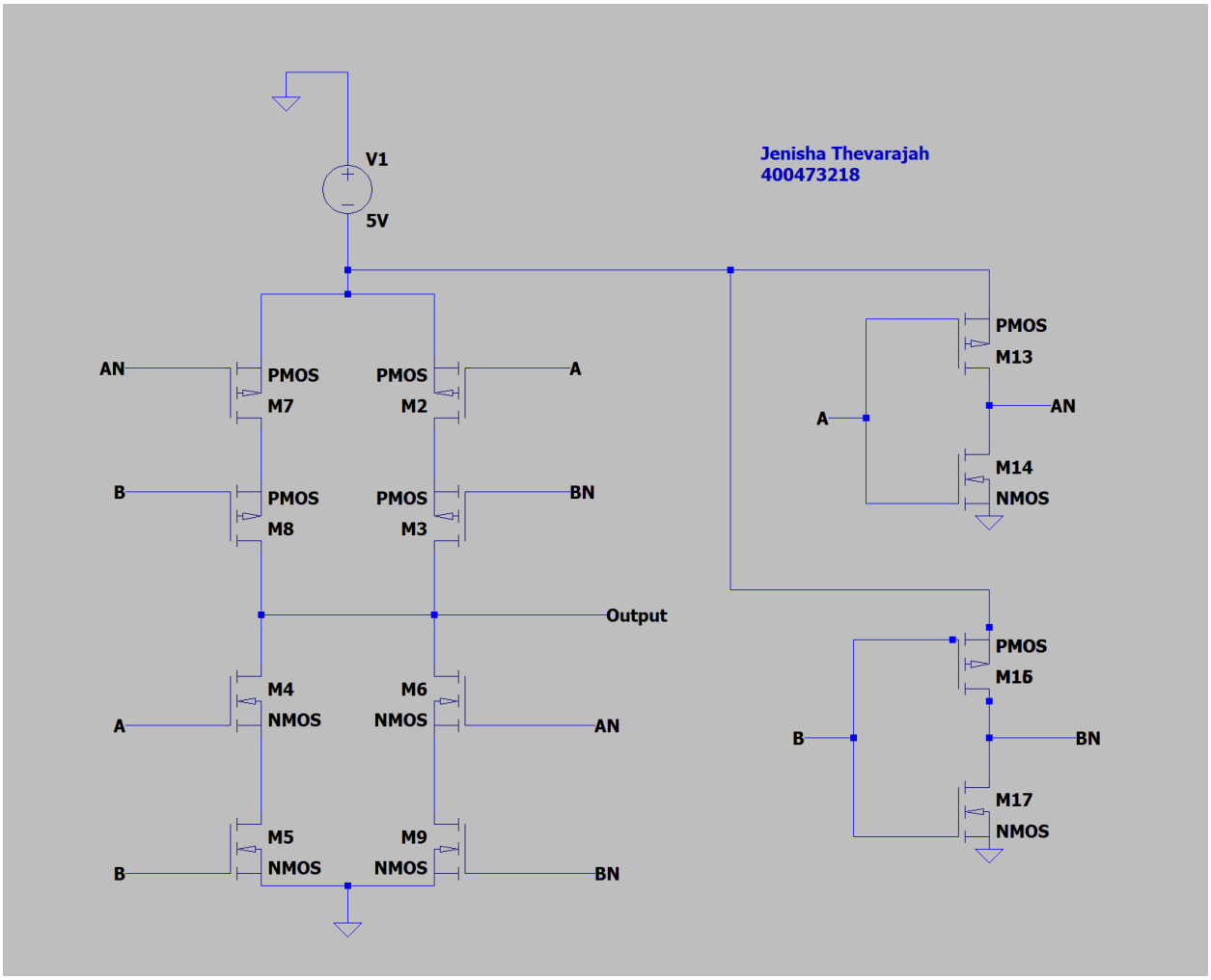

Figure 2: Circuit Schematic on LTSpice

b) Ideal Sizing:

Within the design schematic for this XOR circuit, the optimal size between the PMOS and the NMOS transistors has a 1:1 ratio because it is reflecting the balanced presence of both PMOS and NMOS within the circuit. This is because it must have an ideal delay because of the CMOS circuit. This balance is important because it ensures that all transistors have the same resistance levels in both their on and off states, which makes it easier for them to act as switches. As a result, this configuration makes it possible to create a truth table that illustrates how the XOR gate behaves with various input combinations. In particular, this design uses an equal number of six PMOS and six NMOS transistors.

c) Implementation of Ideal Sizing:

My hardware design can attain the ideal transistor proportions by employing the MC14007UB, facilitating the incorporation of 12 transistors, split equally with 6 NMOS and 6 PMOS components.

The circuit layout (Figure 2), it is observed that both the pull-up and pull-down networks consist of two transistors each. This arrangement allows us to calculate their total resistances, which should be similar for optimal circuit function. To minimize delays when the circuit switches between states, a balanced design with equal pull-up and pull-down resistance is preferred. Since the size of the transistor directly affects resistance (smaller transistors have higher resistance), the sizing of the PMOS and NMOS transistors needs careful consideration. This specific design seems to deviate slightly from this ideal 1:1 resistance ratio which is also shown through a calculation within Figure 3.

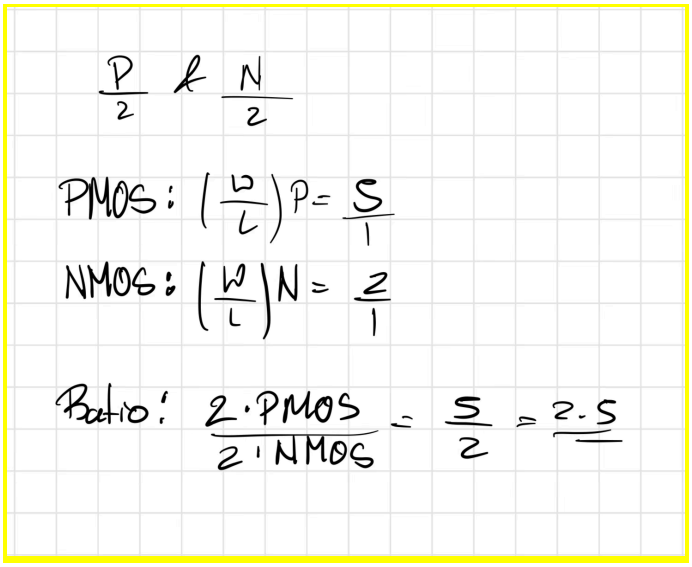

Figure 3: Ideal Sizing of the NMOS and PMOS

PART 2:

a) **Functional Testing:**

As shown within the graph of the logic testing from the AD2 it shows that DIO 2 (which is the 3rd function) serves as an output while the DIO 0 and DIO 1 functions are shown to be the input. As shown below as well is the circuit created and implemented to obtain these results. This graph clearly shows how it illustrates the XOR truth table as shown below in my annotated picture. As shown in my illustration, when my output is high DIO 0 and DIO 1 are low and high respectively.

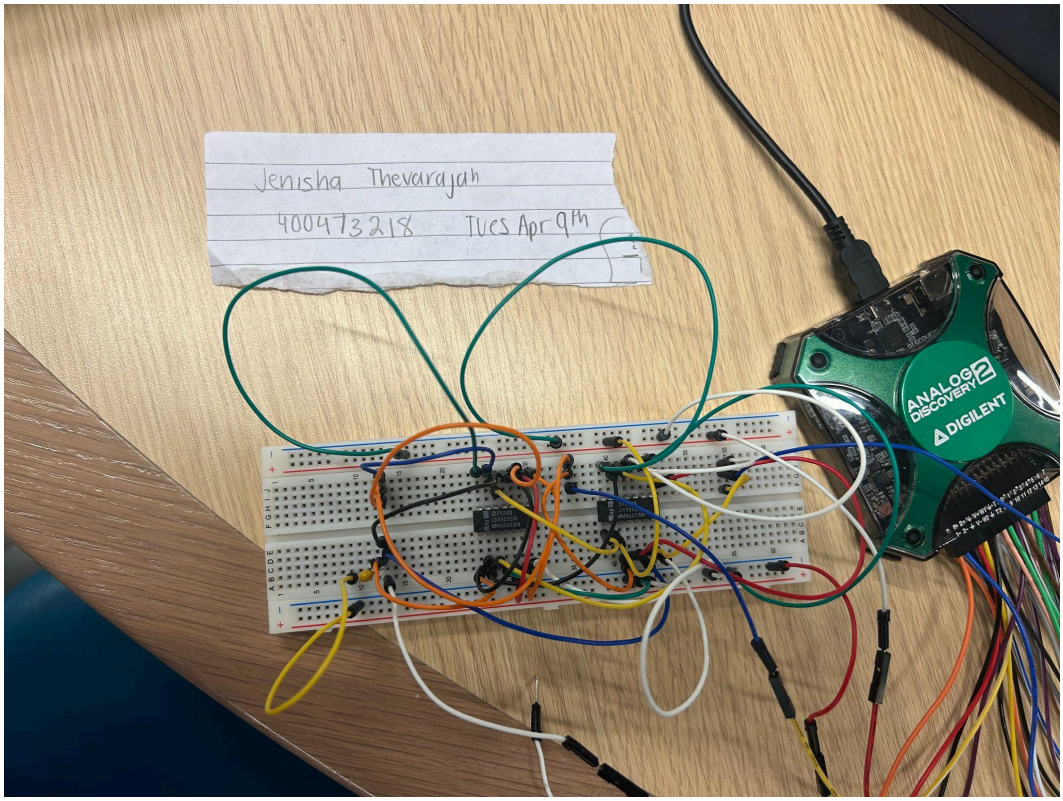

Figure 4: Physical circuit from design schematic.

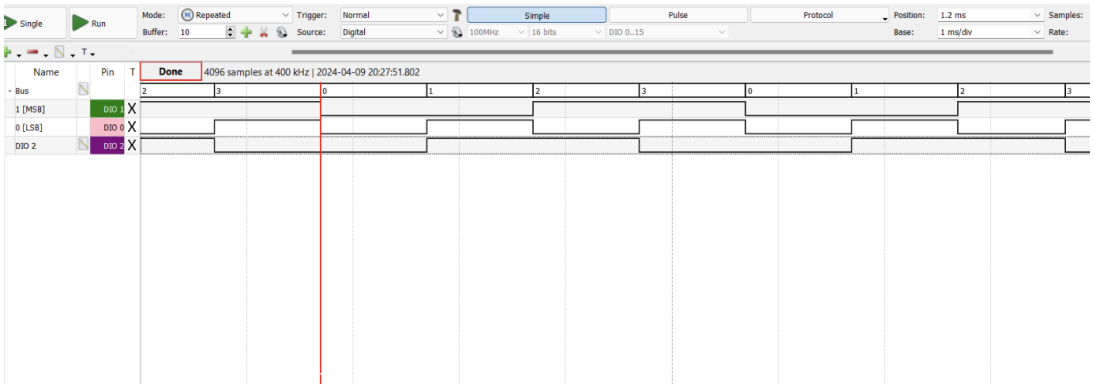

Figure 5: Functional Testing of input DIO 0 and DIO 1 and output DIO 2

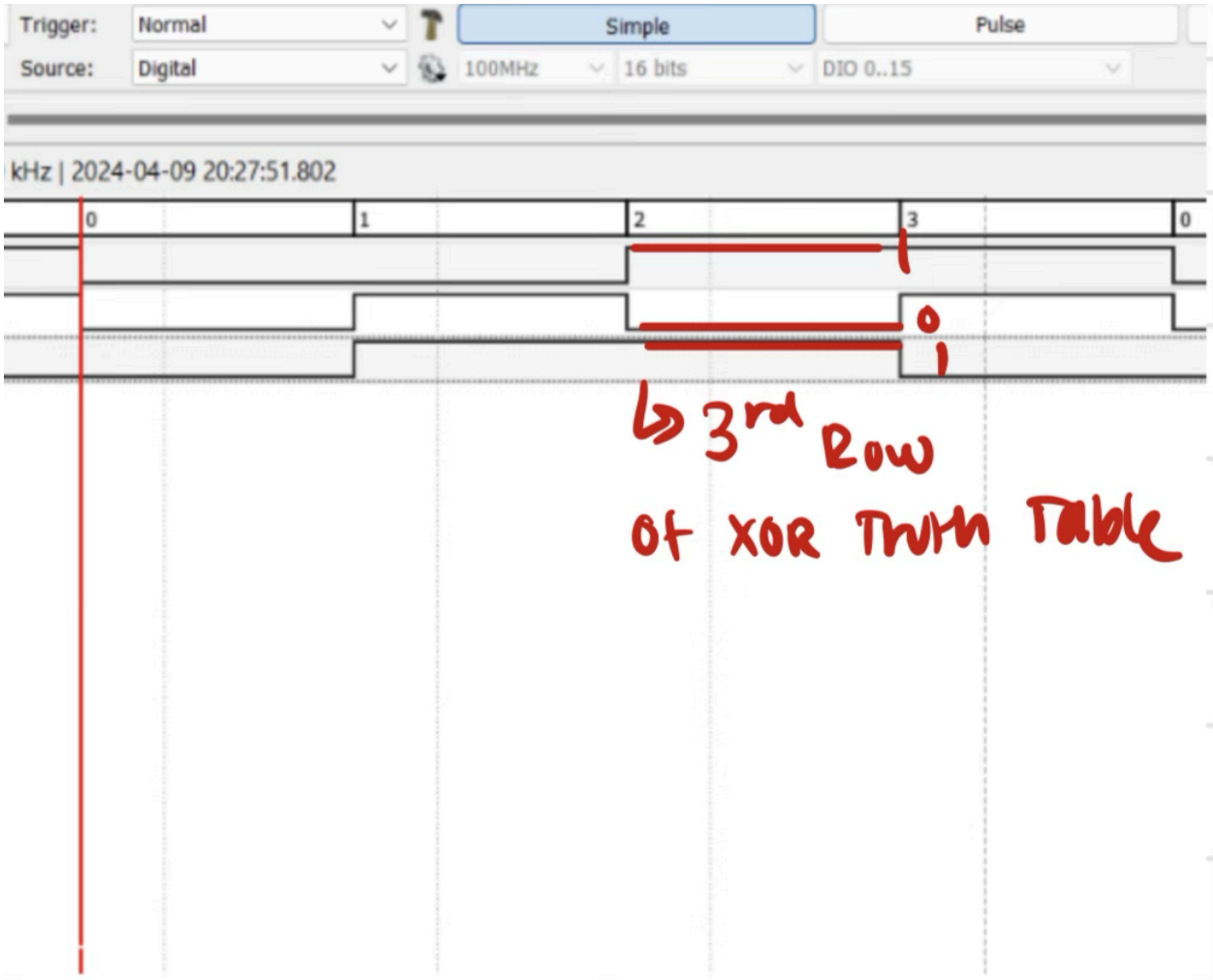

Figure 6: Annotation of Functional Testing of XOR Gate

b) Static Level Testing:

To analyze the circuit's static behavior, we applied a constant high voltage (+5V) to one input while varying the other with a square wave (0V to 5V). We then swapped the input configuration to see if the response changed. As shown in Figure 12, a constant high voltage on input A resulted in measured values of V = 2.5V and V1 = 2.72mV.
Then, I had to put the input B as high, the measured voltages were V = 3.977V and V1 = 11.23mV as shown within the AD2 graph below.
As we can see, there is a difference within the high voltage which answers the question of whether or not VH and VL change
Several factors might account for the observed variation in the high output voltage (V). Issues such as improper wiring or increased internal resistance along one of the input paths could be contributing factors. Additionally, a disparity in the impedance levels of the voltage sources attached to the inputs might result in a significant voltage drop, thereby reducing the V level for one input relative to the other.

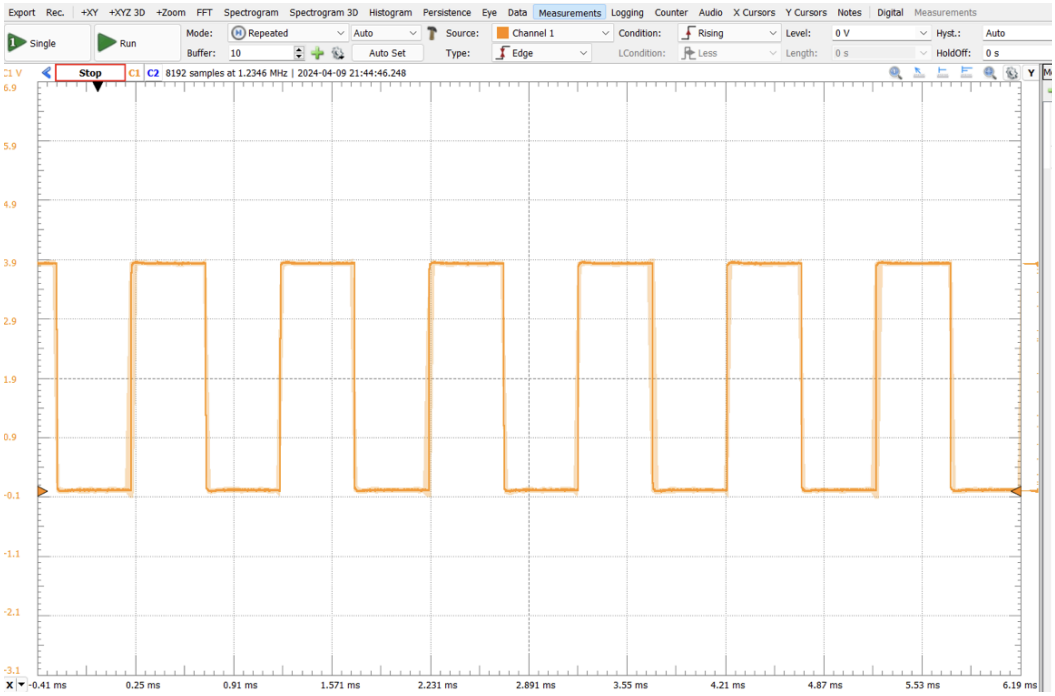

Figure 6: Physical AD2 when behavior of a logic function

PART 3:

a) **Timing Analysis:**

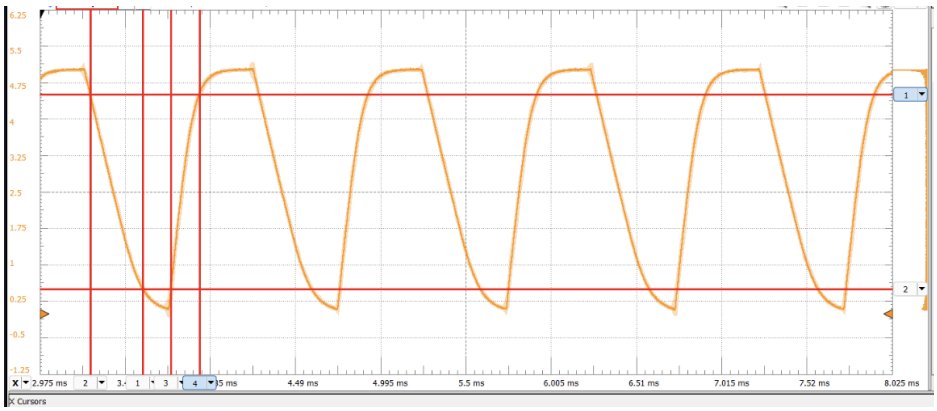

Figure 7: Time analysis

To determine the rise and fall times of the output waveform, proceed as follows: Set one input to a logic-1 state, equivalent to +5V, and configure the second input as a square wave oscillating between 0V and 5V. At the output, connect a 100 nF capacitor to simulate a load. From this AD2 graph, we can see that the phase of the analysis, input B was maintained at a steady 5V DC, while input A received a square wave signal, marked by an amplitude of 2.5V, an offset of 2.5V, and set to a frequency of 500mHz.

The examination of the graph revealed that the rise time was 147.3 ms and the fall time was 325.5 ms(This was determined from the 4 graph cursors). To calculate the high-to-low propagation delay, the approach involved comparing the 50% point of the input pulse's low-to-high transition to the 50% point of the output's high-to-low transition.

This calculation produced a high-to-low propagation delay (pHL) of 325.5 ms. Following a similar method, the low-to-high propagation delay for the opposite transition was determined to be tpLH = 147.3 ms. Employing the formula to calculate the average propagation delay, tp = (pHL + tpLH) / 2, yielded a total propagation delay of 236.25 ms.

<u>Calculation:</u>

Formula:
Tp = (TPHL + TPLH)/2
Tp= (325.5+147.3)/2
Tp = 236.25 ms

Bonus:

Circuit Schematic: