

Design Project #5- Bonus

ELECENG 2EI4- Electronic Devices and Circuits

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PART 1:

a) Summary:

A 3-bit DAC transforms a binary signal made up of three bits into an analog signal. With each bit taking a value of either 0 or 1, there are eight possible combinations from 000 to 111. These converters are utilized in a range of applications including audio equipment, voltage regulation, and measuring instruments, becoming indispensable components within broader electronic systems. Their function of converting digital information into analog form allows for the meticulous management and tuning of analog signals.

i) Circuit Diagram:

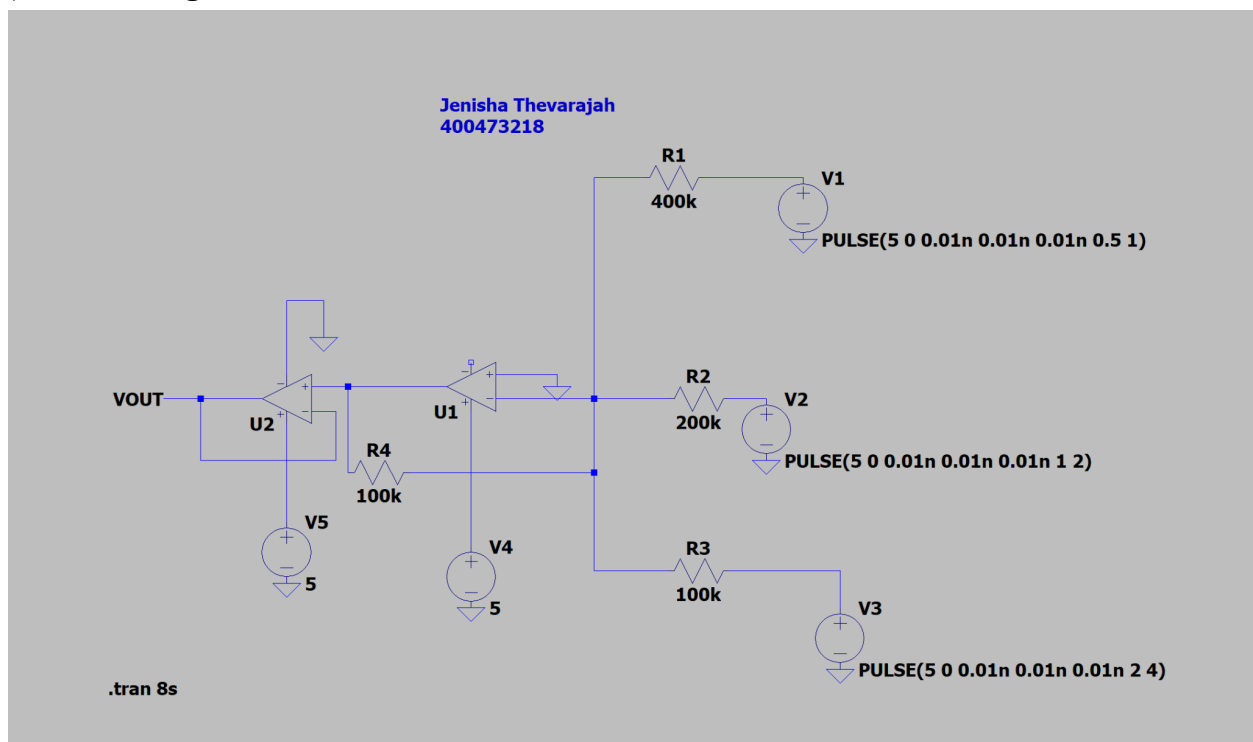


Figure 1: Circuit Design Schematic

ii) Description of how the circuit works

3-bit DAC employing a summing operational amplifier (op-amp) for combining and amplifying three input voltages. This circuit integrates three input resistors, each linked to an input voltage, and a resistor attached to the op-amp's output. This design schematic was inspired from figure 3 as shown below. The input voltages, with each being proportionally weighted according to the resistance values assigned to them. The op-amp then boosts this cumulative voltage and routes it back to its input, establishing a feedback loop.

Switching to a configuration using two op-amps, the circuit could be adapted to enhance performance or functionality. For example, the first op-amp could serve as a precision summing amplifier, accurately combining the input voltages. The second op-amp is then utilized to further amplify the summed signal or to apply additional processing such as filtering or level adjustment. This dual op-amp setup allows for more flexibility in designing the circuit's characteristics, such as adjusting gain stages independently or implementing more complex signal processing tasks, potentially leading to improved accuracy or signal quality in the DAC's output. The final output voltage from the op-amp mirrors the aggregate of the input voltages.

iii) Any calculations that are required as part of the design

Output Voltage Calculations:

$$V_{out} = -R \left(\frac{V_2}{R} + \frac{V_1}{2R} + \frac{V_0}{4R} \right)$$

$$V_{out} = -\frac{1}{4} (4V_2 + 2V_1 + V_0)$$

Figure 2: Calculations needed for this design

iv) Reference for the circuit (i.e. where did you find this design)

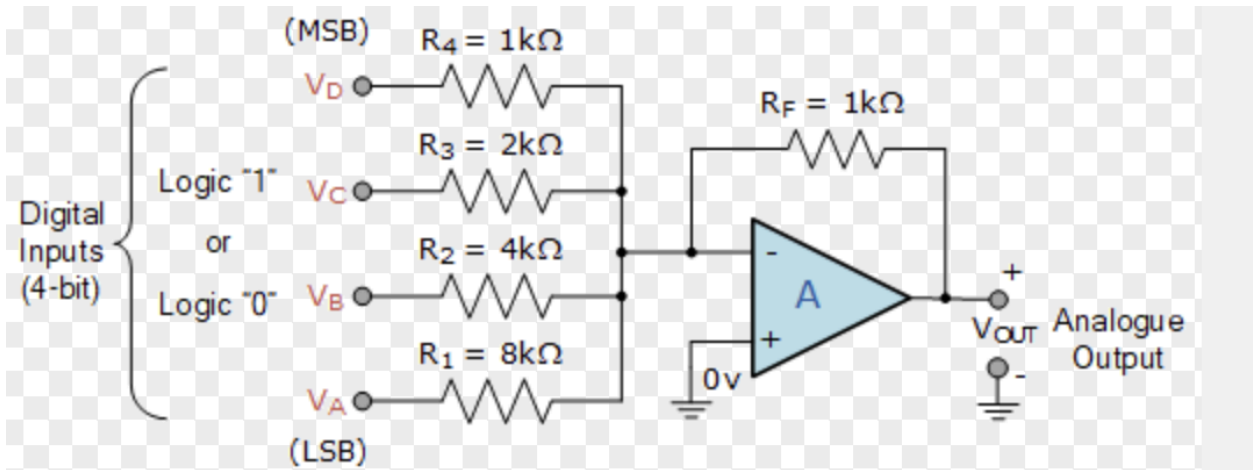


Figure 3: Reference Picture

PART 2:

a) Measurement and analysis:

i) Actual Circuit:

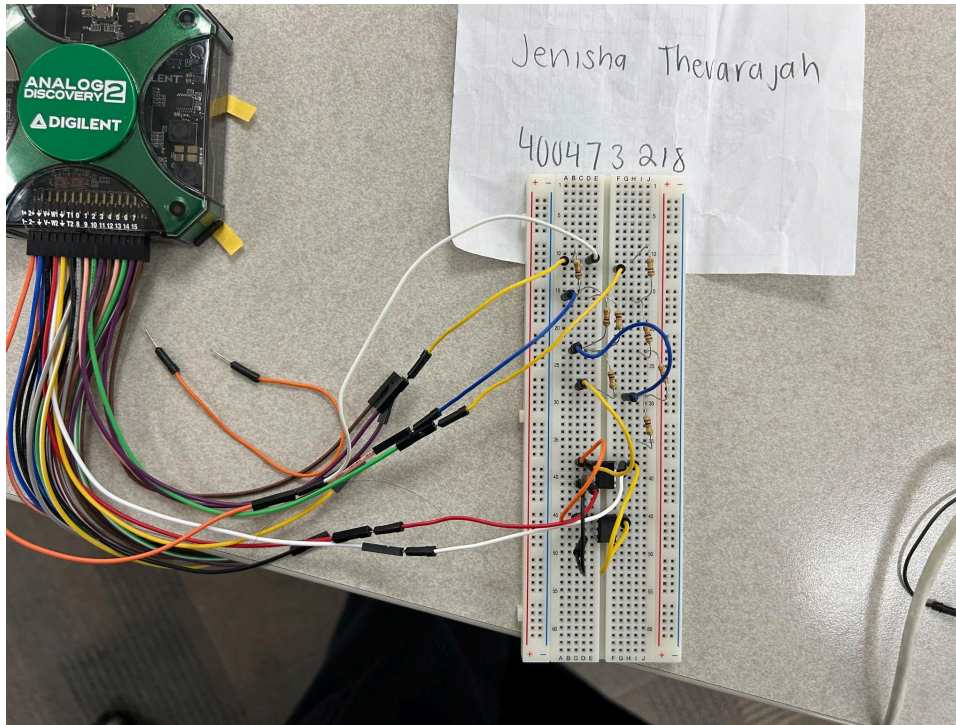


Figure 4: Physical AD2 circuit of Schematic Design

ii) Generation of the digital inputs

In order to get this AD2 waveform simulation, I had to use the digital IO pins in order to create pulses as the input signal, where each pulse corresponded to one of the three digital inputs. This was because there are not enough wavegens from the ad2 to allow this. In order for these pulses to work, different combinations of high and low states within the logic analyzer had to be implemented.

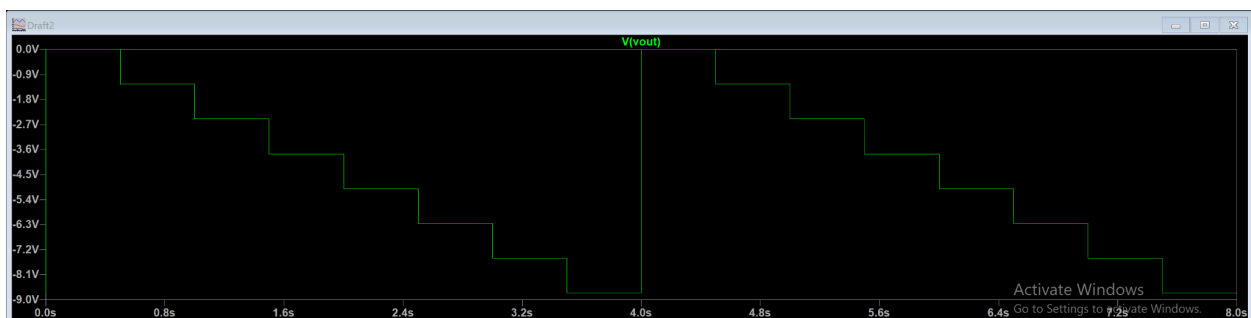
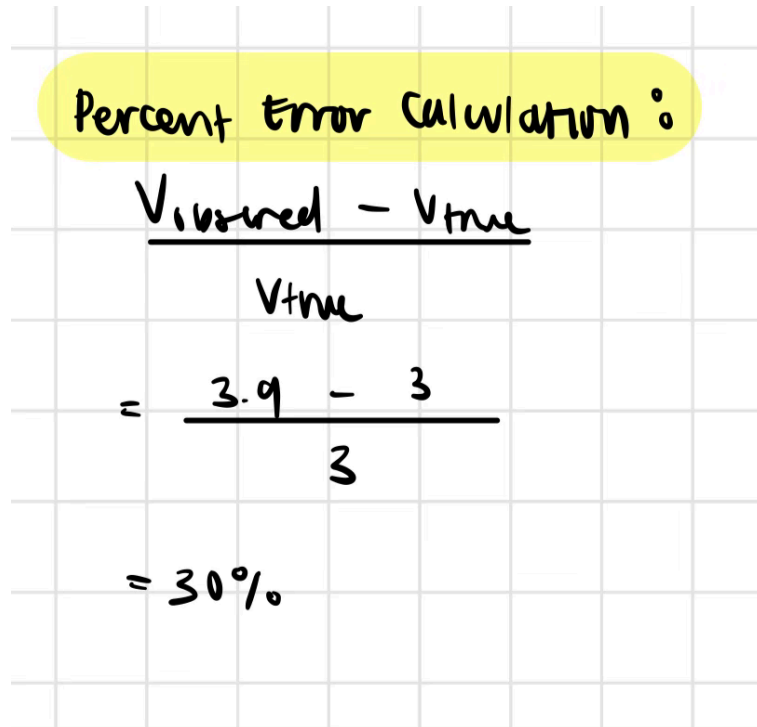


Figure 5: Simulation of Schematic Design

iv) Gain error:

A discrepancy was observed between the gain as calculated by the AD2 and the gain predicted by the circuit schematic during simulation.

The measured gain turned out to be -3.9, however the actual value for the gain is -3, giving a percent error calculator of 30%



The image shows a handwritten calculation on a grid background. At the top, the text "Percent Error Calculation %" is written in black ink and highlighted with a yellow rounded rectangle. Below this, the formula for percent error is written:
$$\frac{V_{\text{observed}} - V_{\text{true}}}{V_{\text{true}}}$$
 The next line shows the substitution of values:
$$= \frac{3.9 - 3}{3}$$
 The final result is shown on the next line:
$$= 30\%$$

Figure 6: Percent Error Calculations

v) Measure the maximum differential non-linearity.:

Maximum Differential Non-linearity Calculations:

Anticipated:

$$\frac{[1(1+1) - 1(1)]}{1}$$
$$< 1$$

Theoretical from graph

$$\frac{[0.9(1+1) - 0.9(1)]}{1}$$
$$= 1$$

↳ 10% Error

Figure 7: MDI Calculations

vi) Offset Error

The discrepancy in Maximum Differential Non-Linearity (DNL) reflects the difference between the actual DNL measurement and the expected or accurate value, attributed to various measurement uncertainties such as noise, or inaccuracies. In addition, with the AD2, there may have been errors that led to these discrepancies.

The offset error was determined to be nonexistent. Calculating the offset error in an electronic circuit involves subtracting the actual voltage output from the desired voltage output, and dividing this variance by the circuit's maximum voltage range. This calculation expresses the offset error as a proportion of the full-scale voltage range.

PART 3:

a) Discussion:

In the realm of digital-to-analog conversion, various errors such as quantization, linearity, and thermal drift challenge the fidelity of the analog output. The choice between DAC architectures—like the high-accuracy Sigma-Delta versus the simpler R-2R Ladder—balances factors like resolution, speed, and power consumption. To illustrate, we'll simulate quantization error, a fundamental discrepancy that arises when the infinite nuances of an analog signal are approximated by a DAC's finite set of output levels. This simulation will provide a visual understanding of how such errors impact signal integrity.