

## **Design Project #2**

ELECENG 2EI4- Electronic Devices and Circuits

Jenisha Thevarajah - C01- 400473218

**Test Plan:**

- a) When the switch is closed, a fundamental property asserts that V1 is equal to V2, ensuring seamless connectivity within the circuit. This aligns with the ideal switch having zero ON resistance ( $R_{on}$ ), signifying minimal resistance when the switch is in the ON state. Alternatively, when the switch is open, it functions as an open circuit, preventing the flow of current. This behavior corresponds to the ideal switch having infinite OFF resistance ( $R_{off}$ ), symbolizing an impassable barrier to current in the OFF state. Third, the ideal switch exhibits bidirectional operation, accommodating the flow of current in both directions. Lastly, it has a range of unlimited voltages for V1 and V2, providing adaptability to a variety of voltage conditions within the circuit
- b) To gauge the real-world performance of switches, we look at several key metrics. The on-resistance ( $R_{on}$ ) reveals imperfections if any resistance is detected when the switch is on. Off-resistance ( $R_{off}$ ) indicates the switch's effectiveness when off, with high resistance being ideal. Leakage current ( $I_{off}$ ) when the switch is off and voltage drop ( $V_{switch}$ ) when it's on are also crucial, as they signal non-ideal behavior. Additionally, ensuring the switch operates within a specific voltage range ( $V_{min} < V1, V2 < V_{max}$ ) and maintains consistent  $R_{on}$  regardless of voltage variations is important for assessing its reliability. Quick switching times ( $t_{switch}$ ) further indicate a switch's efficiency. These factors together help determine a switch's suitability for real-life applications, focusing on efficiency and reliability.
- c) **Test plan: For each non-ideality specified above, describe the experiment that you will use to determine the quantitative performance of your design.**

**Switch 1:****i) Values set for Vcontrol, Vsupply and and V1:**

When switch is CLOSED:

Vsupply: 5V

V1: 5V

Vcontrol: 0V

**ii) Values that you will measure:**

We are finding the voltage at V2

Ideally,  $V1 = V2$

**Values set for Vcontrol, Vsupply and V1:**

When switch is OPEN:

Vsupply: 5V

V1: 5V

Vcontrol: 5V

**ii) Values that you will measure:**

We are finding the voltage at V2

Ideally,  $I_1 = I_2 = 0$

**iii) Calculations**

**CALCULATIONS:**

$$V_{ON} = (V_1 - V_2)$$

$$V_{OFF} = V_2$$

$$I_{Leakage} = V_{OFF} / R_L$$

$$I = V_{ON} / R_L$$

Figure 1: Calculations for switch 1

**Switch 2:**

**i) Values set:**

Vcontrol: 0V

Vsupply: 5V

V1: 5V

**Ideally,  $V_1 = V_a$**

**ii) Values that you will measure:**

We are finding the voltage at V1

i) Values set:

Vcontrol: 5V

Vsupply: 5V

V1: 5V

Ideally,  $V_1 = V_b$

ii) Values that you will measure:

We are finding the voltage at V1

iii) Calculations

CALCULATIONS:

$$V_{ON} = (V_1 - V_2)$$

$$V_{OFF} = V_2$$

$$I_{Leakage} = V_{OFF} / R_L$$

$$I = V_{ON} / R_L$$

Figure 2: Calculations for switch 1

## Switch type 1:

### i) Circuit Schematic

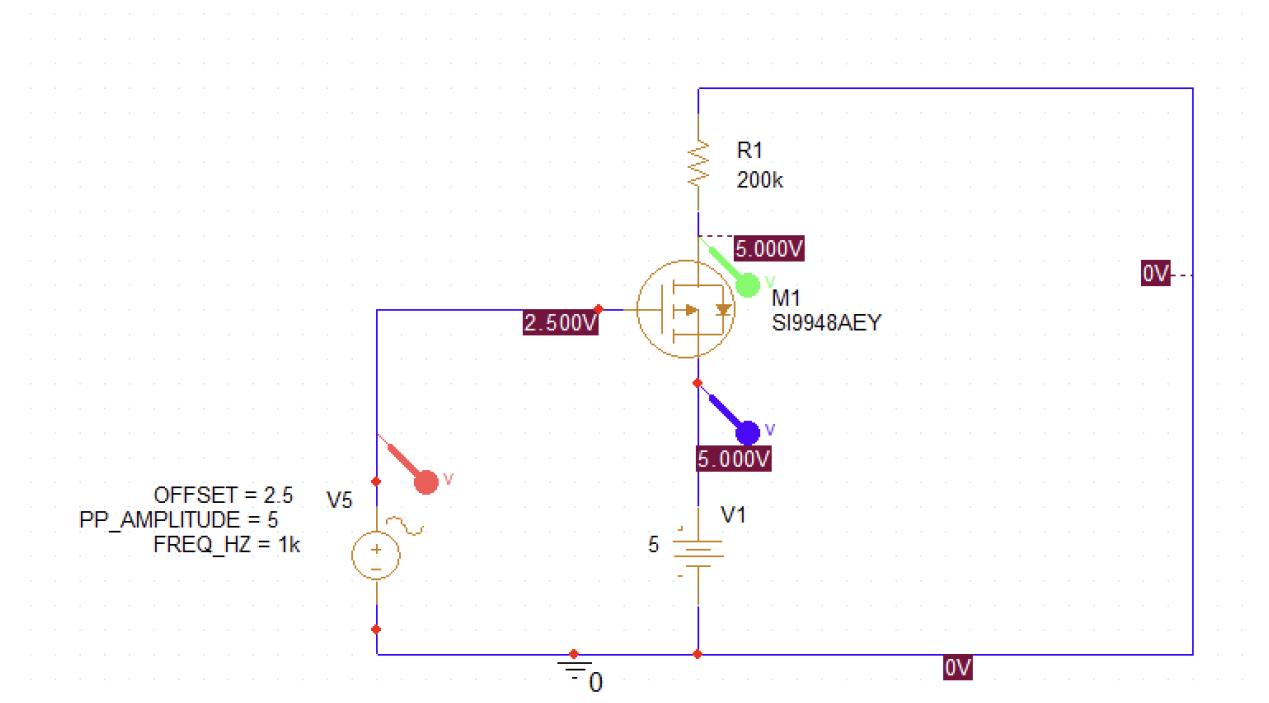


Figure 3: PSpice Circuit Schematic for Switch 1 Design

### Netlist:

```
1: * source 2EI4_PROJECT2
2: V_V1          N00193 0 5
3: R_R1          0 N00395 200k TC=0,0
4: X_M1          N00395 N00104 N00193 SI9948AEY
5: V_V5          N00104 0 DC 0Vdc AC 0Vac
6: +SIN 2.5 {.5*5} 1k 0 0 0
```

Figure 4: NetList for PSpice Switch I

## ii) Measurements:

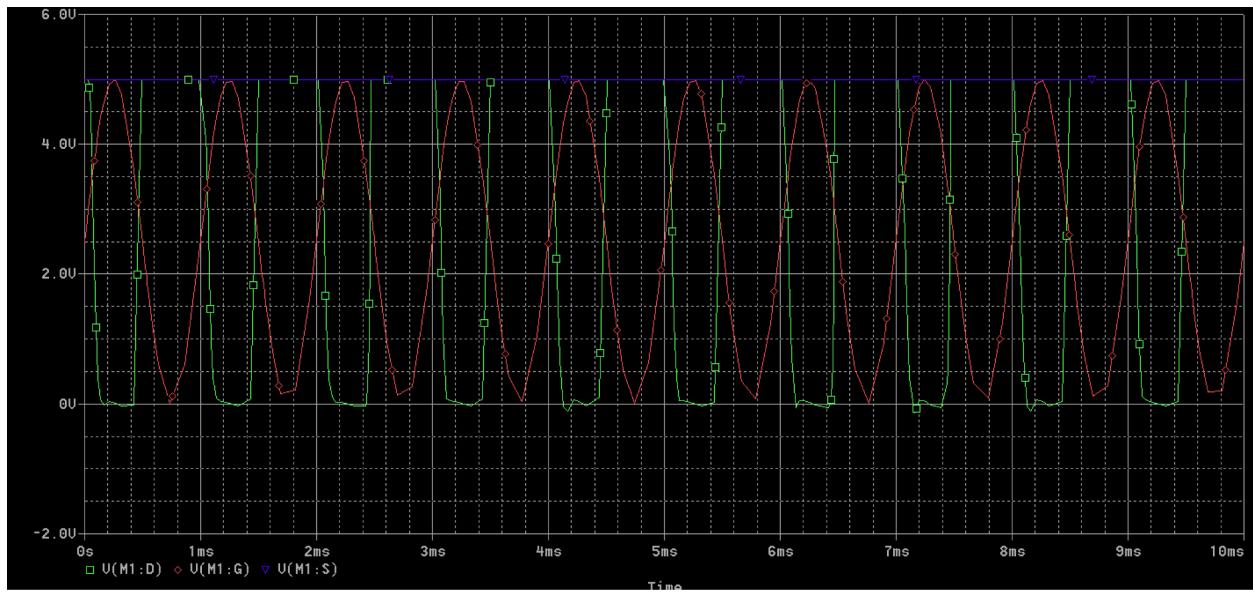


Figure 5: PSpice Simulation for Switch 1

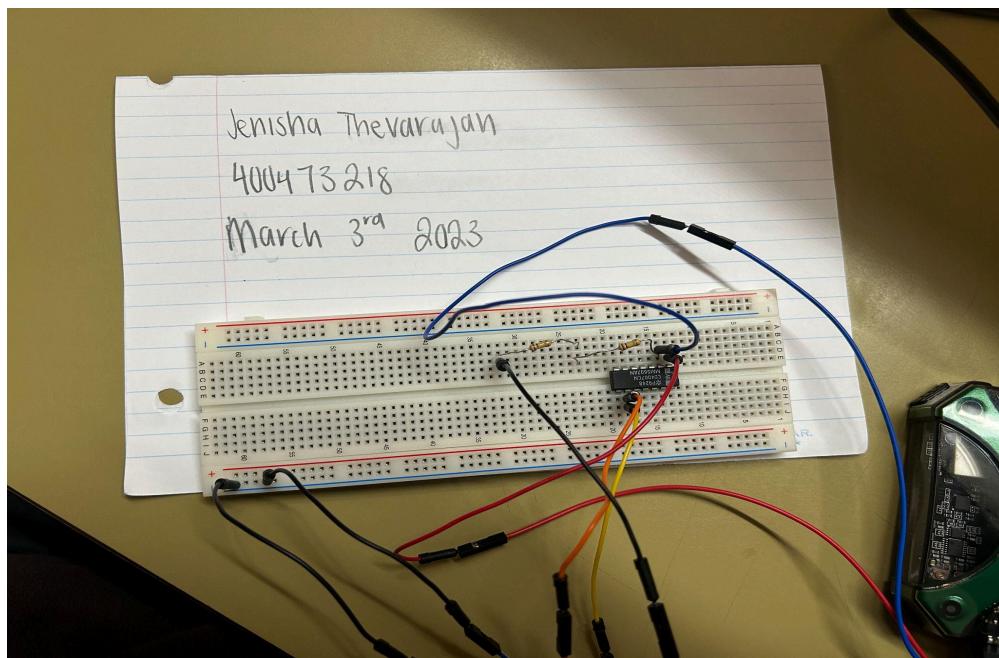


Figure 6: AD2 Circuit design for switch 1 with 200k resistor

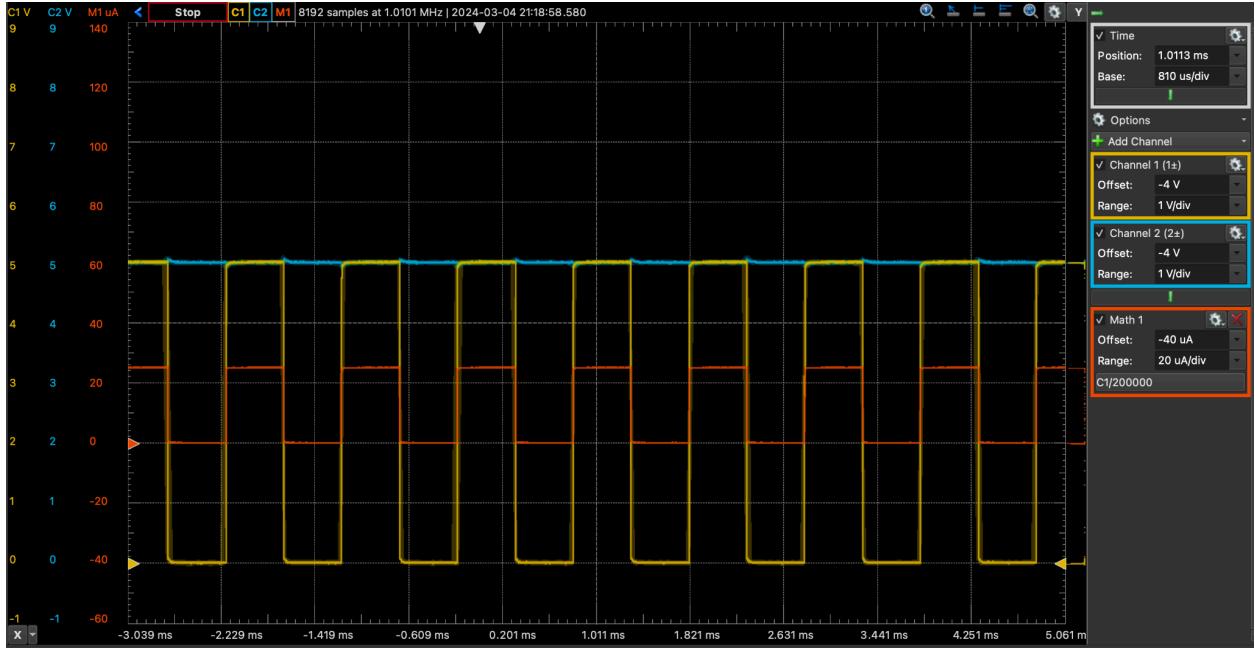


Figure 7: AD2 Waveform generator for Switch 1

### iii) Theoretical explanation:

After reviewing my theoretical calculations and numerical data, I observed that in the simulation graph, the value precisely reached 5V. I opted for a PMOS enhancement MOSFET since I was unable to use the CD4007 MOSFET. This limitation prevented me from measuring the voltage accurately as planned. However, the voltage readings obtained with the enhancement PMOS are closely aligned with the AD2 values.

When the switch is closed, ideally, V1 should be equal to V2; the AD2 waveform in *Figure 7* accurately displays that when the switch was closed. Within *Figure 7*, Channel 2 represented the V1 as shown in the PSpice schematic in *Figure 3*. V1 will be consistently at 5V and V2 will vary between 5V (if Vcontrol = 0V), and V2 will be 0V (if Vcontrol = 5V).

When the switch is closed:

$$V_{ON} = (V_1 - V_2) \quad V_{OFF} = V_2 = 5V$$

$$V_{ON} = (5 - 5)$$

$$V_{ON} = 0V$$

$$I = V_{ON} / 200K$$

$$I = 0A$$

Figure 8: Calculations when the switch is closed.

If the V control = 5V then the switch is open and ideally the current should be 0. No current leakage was seen within the AD2 graph, therefore, my leakage current is calculated to be 0 as shown below:

When switch is opened:

$$V_1 = 5V, V_2 = 0V$$

$$V_{OFF} = V_2 = 0V$$

$$I_2 = V_2 / R$$

$$I_2 = 0 / 200K$$

$$I_2 = 0A$$

$$I_{leakage} = V_{OFF} / R$$

$$= 0 / 200K$$

$$= 0A$$

Figure 9: Calculations when the switch is open.

#### **iv) Design Tradeoffs**

When deciding on the design, I had to think about a few key things, like how much voltage the device can take. This is to prevent any damages to the components and to ensure efficiency within the AD2. It can only handle from 0V to 5V; anything more could damage components used such as the CN4007 MOSFET. I realized it was important to use high resistance to avoid big voltage drops that make things inefficient, so I chose a 200k resistance. This approach also explains why the current measured is so low. I didn't use the exact MOSFET for the pspice simulation, so some of the measurements might not be spot-on, but in the end, the results from the wavegen and the pspice simulation were pretty similar. Maintaining a straightforward design was crucial because a complex schematic can lead to difficulties, yet an overly simplistic design might compromise the circuit's functionality and potentially cause it to malfunction. Lastly, I had to take into consideration the cost. Cost plays a significant role in the design process, we hope for components that are affordable yet perform efficiently. However, lower-cost designs might not work or perform as well compared to higher-cost alternatives.

## Switch Type 2:

### i) Circuit Schematic

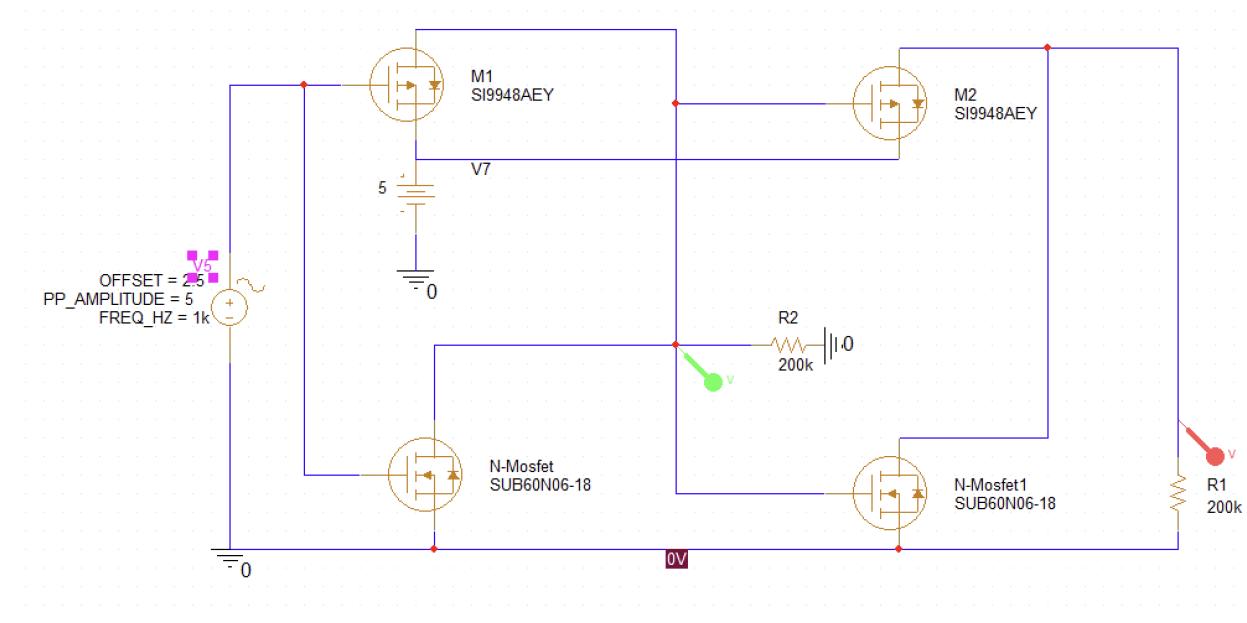


Figure 10: PSPice Circuit Schematic for Switch 2 Design

### Netlist:

```

1: * source SWITCH2
2: V_VControl      N16229 0 DC 0Vdc AC 0Vac
3: +SIN 2.5 {.5*5} 1k 0 0 0
4: X_P-Mosfet1     N16250 N16229 N16191 SI9948AEY
5: X_P-Mosfet2     N16267 N16250 N16191 SI9948AEY
6: X_N-Mosfet1     N16250 N16229 0 SUB60N06-18
7: X_N-Mosfet2     N16267 N16250 0 SUB60N06-18
8: V_Vsupply       N16191 0 5
9: R_R1            0 N16267 200k TC=0,0
10: R_R2           N16250 0 200k TC=0,0
11:

```

Figure 11: NetList for PSPice Switch 1

## ii) Measurements:

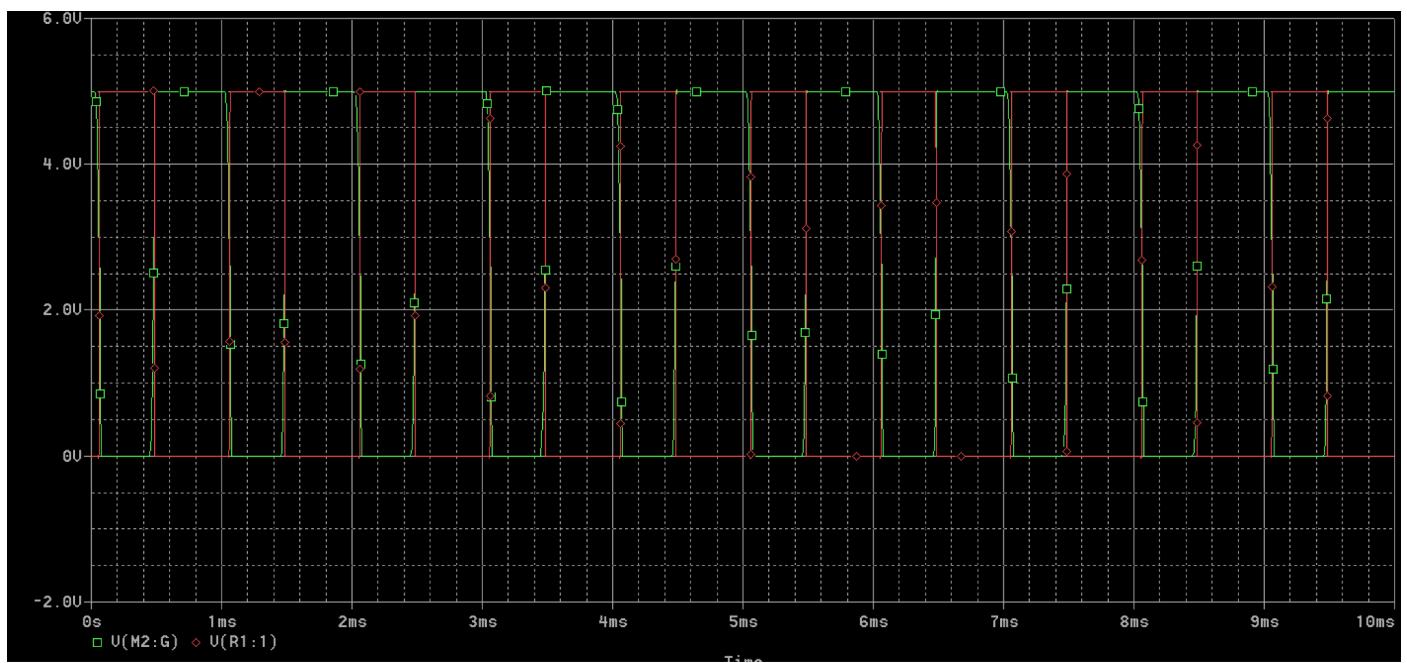


Figure 12: PSpice Simulation for Switch 2

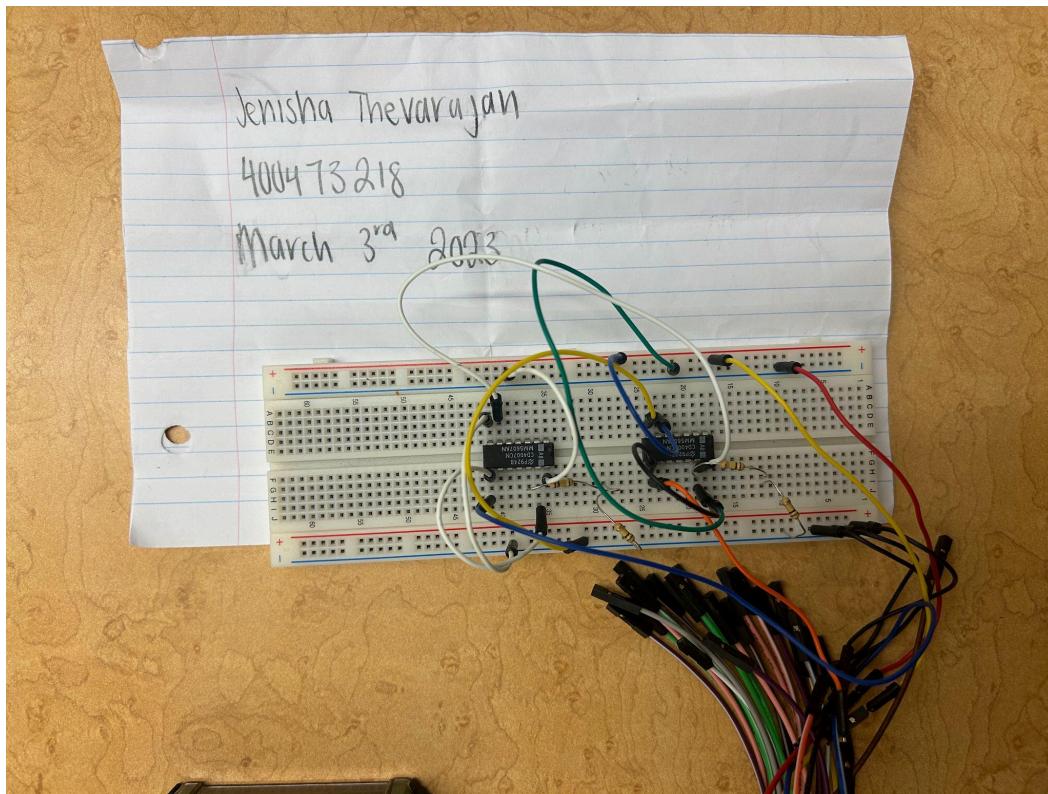


Figure 13: AD2 Circuit design for switch 2 with 2, 200k resistor

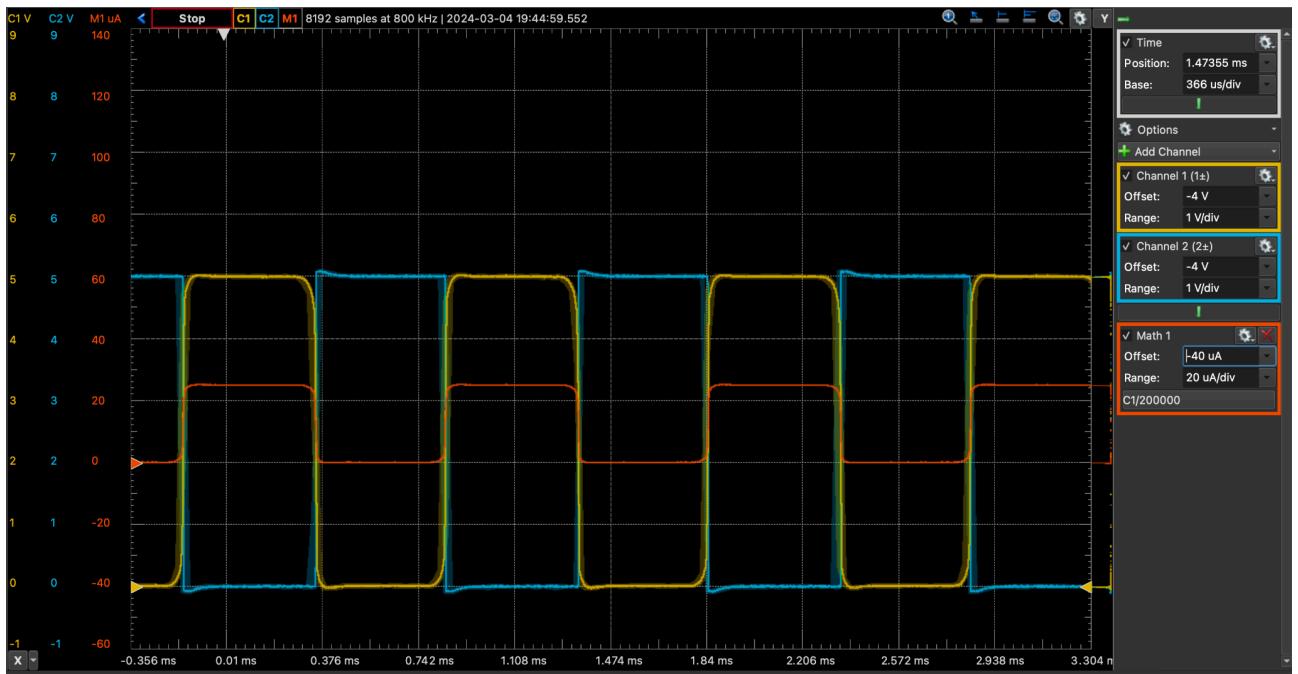


Figure 14: AD2 Waveform generator for Switch 2

### iii. Theoretical explanation

As mentioned earlier with circuit 1, I couldn't utilize the CN4007 MOSFET, so I opted for an enhancement NMOS and PMOS in the schematic design instead. Once more, the schematic and the AD2 graphs align closely, demonstrating similar outputs.

When the control voltage is 0V,  $V_1$  equals  $V_a$ , as shown in the AD2 wavegen's results, showing a value near 5V. When the control voltage is 5V,  $V_1$  equals  $V_b$ , as indicated by the wavegen's results, showing a value near 5V. However, the AD2 graph displayed some current leakage, as detailed in the calculations presented in *Figure 14*, because of the discrepancy in the  $V_a$  and  $V_b$  displayed in the wavegen. The power loss within the circuit is not zero, which can be attributed to the leakage current flowing through the MOSFET.

When  $V_{control} = 0$ :

$$V_I = V_A$$

$$V_I = 5V$$

$$V_A = 4.95$$

$$V_{ON} = V_I - V_A$$

$$V_{ON} = 5 - 4.95$$

$$V_{ON} = 0.02$$

When  $V_{control} = 5V$

$$V_I = V_B$$

$$V_I = 5V$$

$$V_B = 4.975$$

$$V_{ON} = V_I - V_B$$

$$V_{ON} = 5 - 4.975$$

$$V_{ON} = 0.025$$

$$\begin{aligned} I_{leakage} &= V_{ON} / R_L \\ &= 0.02 / 200 \\ &= \underline{\underline{0.014A}} \end{aligned}$$

$$\begin{aligned} I_{leakage} &= V_{ON} / R_L \\ &= 0.025 / 200 \\ &= \underline{\underline{0.0125 A}} \end{aligned}$$

Figure 15: Calculations for Switch 2

#### **iv. Design Tradeoffs:**

Even though the design is simple to construct, damage may result from exceeding its voltage and current thresholds. It's important to take into account the relationship between resistance and threshold voltage in order to maintain accuracy and no damage done to the circuit. Lower resistance at the threshold voltage leads to increased efficiency and reduced power consumption. That is why I opted to use a 2, 200k resistor. As mentioned previously, the MOSFET I used for the pspice simulation wasn't the exact model, which means some of the measurements could be slightly off. However, ultimately, the outcomes from both the wavegen and the pspice simulation turned out to be quite comparable. In this design, a PMOSFET and an NMOSFET voltage inverter are connected, and the characteristics of the PMOS influence both switches. The voltage inverter (the two mosfets) create complexity within this switch 2 design. The MOSFET's capacity to handle low voltage and current levels places restrictions on the design's usefulness and how efficiently it will work. Finally, as previously discussed regarding the trade-offs for switch 1, cost is a crucial factor in the design process. We aim for components that are both cost-effective and efficient.